

# NTMD3P03, NVMD3P03

## MOSFET – Power, Dual, P-Channel, SOIC-8 -3.05 A, -30 V



ON Semiconductor®

<http://onsemi.com>

### Features

- High Efficiency Components in a Dual SOIC-8 Package
- High Density Power MOSFET with Low  $R_{DS(on)}$
- Miniature SOIC-8 Surface Mount Package – Saves Board Space
- Diode Exhibits High Speed with Soft Recovery
- $I_{DSS}$  Specified at Elevated Temperature
- Avalanche Energy Specified
- Mounting Information for the SOIC-8 Package is Provided
- AEC-Q101 Qualified – NVMD3P03R2G
- These Devices are Pb-Free and are RoHS Compliant

### Applications

- DC-DC Converters
- Low Voltage Motor Control
- Power Management in Portable and Battery-Powered Products, i.e.:  
Computers, Printers, PCMCIA Cards, Cellular & Cordless Telephones

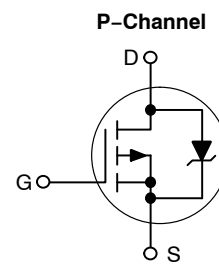
### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	-30	V
Gate-to-Source Voltage – Continuous	$V_{GS}$	$\pm 20$	V
Thermal Resistance – Junction-to-Ambient (Note 1)	$R_{\theta JA}$	171	$^\circ\text{C}/\text{W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	0.73	W
Continuous Drain Current @ $25^\circ\text{C}$	$I_D$	-2.34	A
Continuous Drain Current @ $70^\circ\text{C}$	$I_D$	-1.87	A
Pulsed Drain Current (Note 4)	$I_{DM}$	-8.0	A
Thermal Resistance – Junction-to-Ambient (Note 2)	$R_{\theta JA}$	100	$^\circ\text{C}/\text{W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	1.25	W
Continuous Drain Current @ $25^\circ\text{C}$	$I_D$	-3.05	A
Continuous Drain Current @ $70^\circ\text{C}$	$I_D$	-2.44	A
Pulsed Drain Current (Note 4)	$I_{DM}$	-12	A
Thermal Resistance – Junction-to-Ambient (Note 3)	$R_{\theta JA}$	62.5	$^\circ\text{C}/\text{W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	2.0	W
Continuous Drain Current @ $25^\circ\text{C}$	$I_D$	-3.86	A
Continuous Drain Current @ $70^\circ\text{C}$	$I_D$	-3.1	A
Pulsed Drain Current (Note 4)	$I_{DM}$	-15	A
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ( $V_{DD} = -30$ Vdc, $V_{GS} = -4.5$ Vdc, Peak $I_L$ $= -7.5$ Apk, $L = 5$ mH, $R_G = 25$ $\Omega$ )	$E_{AS}$	140	mJ
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	$T_L$	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Minimum FR-4 or G-10 PCB,  $t =$  Steady State.
2. Mounted onto a 2" square FR-4 Board (1 in sq, 2 oz Cu 0.06" thick single sided),  $t =$  steady state.

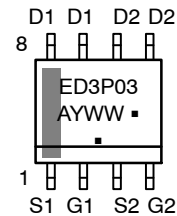
$V_{DSS}$	$R_{DS(on)}$ Typ	$I_D$ Max
-30 V	85 m $\Omega$ @ -10 V	-3.05 A



### MARKING DIAGRAM\* AND PIN ASSIGNMENT



SOIC-8  
SUFFIX NB  
CASE 751  
STYLE 11



ED3P03= Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

Device	Package	Shipping†
NTMD3P03R2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel
NVMD3P03R2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

## NTMD3P03, NVMD3P03

3. Mounted onto a 2" square FR-4 Board (1 in sq, 2 oz Cu 0.06" thick single sided),  $t \leq 10$  seconds.
4. Pulse Test: Pulse Width = 300  $\mu$ s, Duty Cycle = 2%.

# NTMD3P03, NVMD3P03

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted) (Note 5)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Drain-to-Source Breakdown Voltage ( $V_{GS} = 0\text{ Vdc}$ , $I_D = -250\ \mu\text{Adc}$ ) Temperature Coefficient (Positive)	$V_{(BR)DSS}$	-30 -	- -30	- -	Vdc mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current ( $V_{DS} = -24\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ , $T_J = 25^\circ\text{C}$ ) ( $V_{DS} = -24\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ , $T_J = 125^\circ\text{C}$ ) ( $V_{DS} = -30\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ , $T_J = 25^\circ\text{C}$ )	$I_{DSS}$	- - -	- - -	-1.0 -20 -2.0	$\mu\text{Adc}$
Gate-Body Leakage Current ( $V_{GS} = -20\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	-	-	-100	nAdc
Gate-Body Leakage Current ( $V_{GS} = +20\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	-	-	100	nAdc

## ON CHARACTERISTICS

Gate Threshold Voltage ( $V_{DS} = V_{GS}$ , $I_D = -250\ \mu\text{Adc}$ ) Temperature Coefficient (Negative)	$V_{GS(th)}$	-1.0 -	-1.7 3.6	-2.5 -	Vdc
Static Drain-to-Source On-State Resistance ( $V_{GS} = -10\text{ Vdc}$ , $I_D = -3.05\text{ Adc}$ ) ( $V_{GS} = -4.5\text{ Vdc}$ , $I_D = -1.5\text{ Adc}$ )	$R_{DS(on)}$	- -	0.063 0.090	0.085 0.125	$\Omega$
Forward Transconductance ( $V_{DS} = -15\text{ Vdc}$ , $I_D = -3.05\text{ Adc}$ )	$g_{FS}$	-	5.0	-	Mhos

## DYNAMIC CHARACTERISTICS

Input Capacitance	$(V_{DS} = -24\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ , $f = 1.0\text{ MHz}$ )	$C_{iss}$	-	520	750	pF
Output Capacitance		$C_{oss}$	-	170	325	
Reverse Transfer Capacitance		$C_{rss}$	-	70	135	

## SWITCHING CHARACTERISTICS (Notes 6 and 7)

Turn-On Delay Time	$(V_{DD} = -24\text{ Vdc}$ , $I_D = -3.05\text{ Adc}$ , $V_{GS} = -10\text{ Vdc}$ , $R_G = 6.0\ \Omega$ )	$t_{d(on)}$	-	12	22	ns
Rise Time		$t_r$	-	16	30	
Turn-Off Delay Time		$t_{d(off)}$	-	45	80	
Fall Time		$t_f$	-	45	80	
Turn-On Delay Time	$(V_{DD} = -24\text{ Vdc}$ , $I_D = -1.5\text{ Adc}$ , $V_{GS} = -4.5\text{ Vdc}$ , $R_G = 6.0\ \Omega$ )	$t_{d(on)}$	-	16	-	ns
Rise Time		$t_r$	-	42	-	
Turn-Off Delay Time		$t_{d(off)}$	-	32	-	
Fall Time		$t_f$	-	35	-	
Total Gate Charge	$(V_{DS} = -24\text{ Vdc}$ , $V_{GS} = -10\text{ Vdc}$ , $I_D = -3.05\text{ Adc}$ )	$Q_{tot}$	-	16	25	nC
Gate-Source Charge		$Q_{gs}$	-	2.0	-	
Gate-Drain Charge		$Q_{gd}$	-	4.5	-	

## BODY-DRAIN DIODE RATINGS (Note 6)

Diode Forward On-Voltage	$(I_S = -3.05\text{ Adc}$ , $V_{GS} = 0\text{ V}$ ) $(I_S = -3.05\text{ Adc}$ , $V_{GS} = 0\text{ V}$ , $T_J = 125^\circ\text{C}$ )	$V_{SD}$	- -	-0.96 -0.78	-1.25 -	Vdc
Reverse Recovery Time	$(I_S = -3.05\text{ Adc}$ , $V_{GS} = 0\text{ Vdc}$ , $di_S/dt = 100\text{ A}/\mu\text{s}$ )	$t_{rr}$	-	34	-	ns
		$t_a$	-	18	-	
		$t_b$	-	16	-	
Reverse Recovery Stored Charge		$Q_{RR}$	-	0.03	-	$\mu\text{C}$

5. Handling precautions to protect against electrostatic discharge is mandatory.
6. Indicates Pulse Test: Pulse Width = 300  $\mu\text{s}$  max, Duty Cycle = 2%.
7. Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

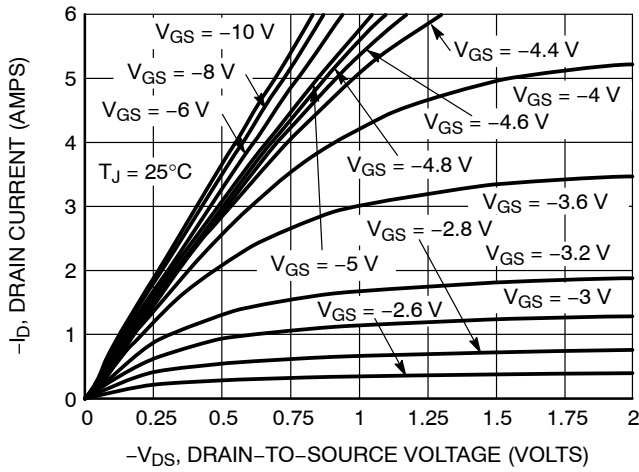


Figure 1. On-Region Characteristics

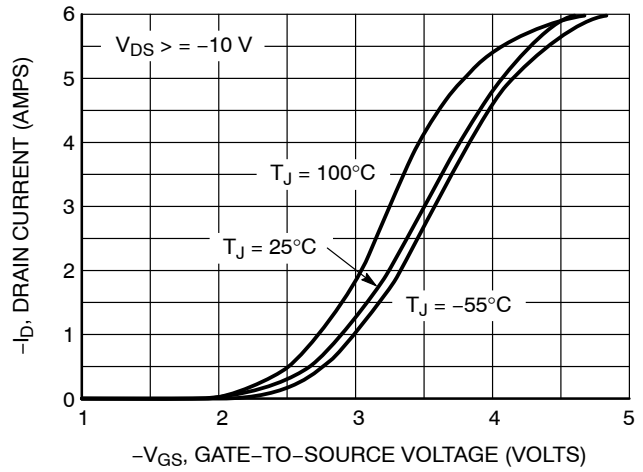


Figure 2. Transfer Characteristics

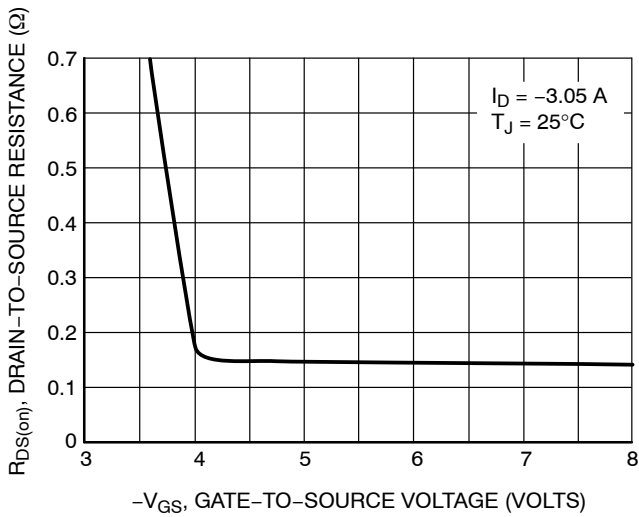


Figure 3. On-Resistance vs. Gate-to-Source Voltage

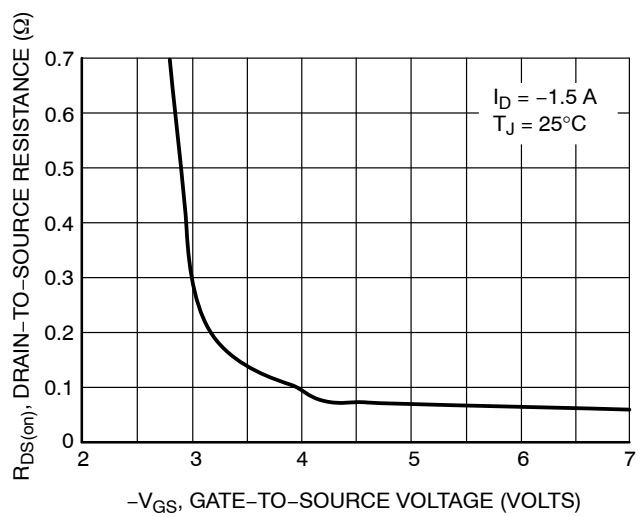


Figure 4. On-Resistance vs. Gate-to-Source Voltage

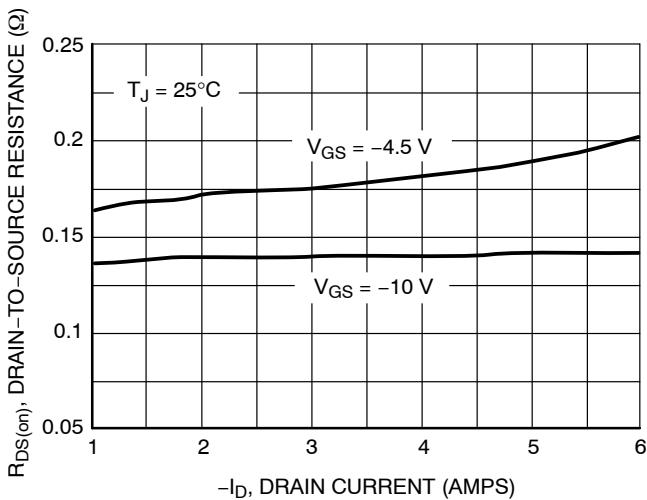


Figure 5. On-Resistance vs. Drain Current and Gate Voltage

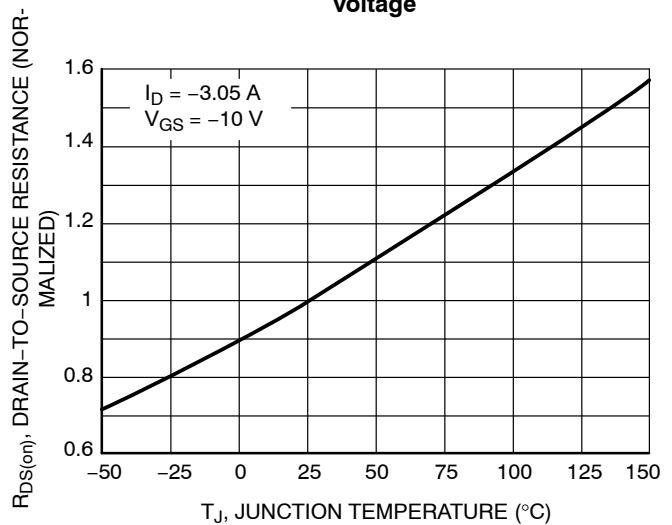
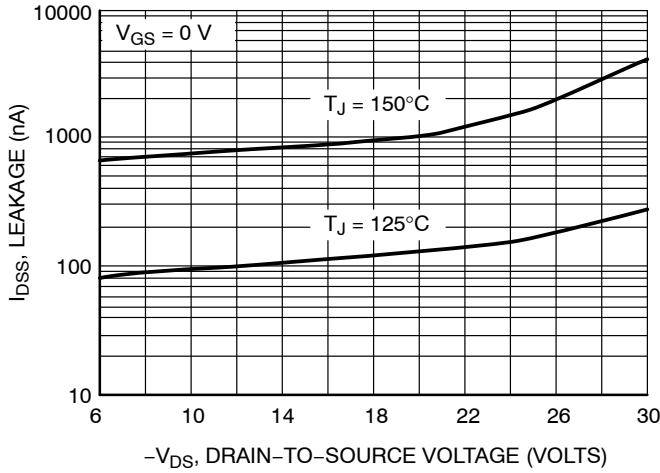
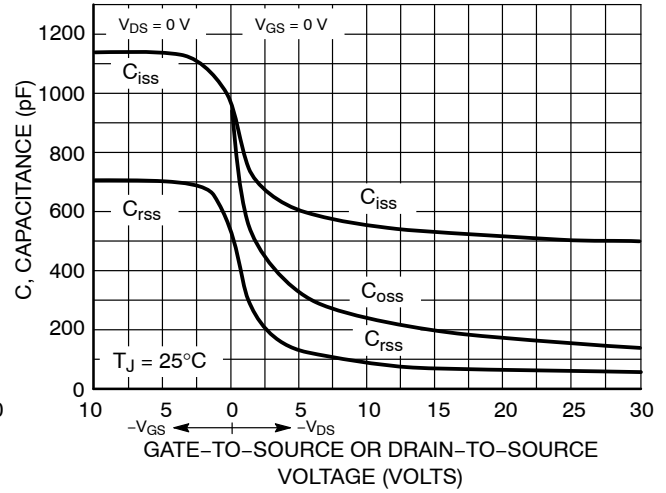


Figure 6. On Resistance Variation with Temperature

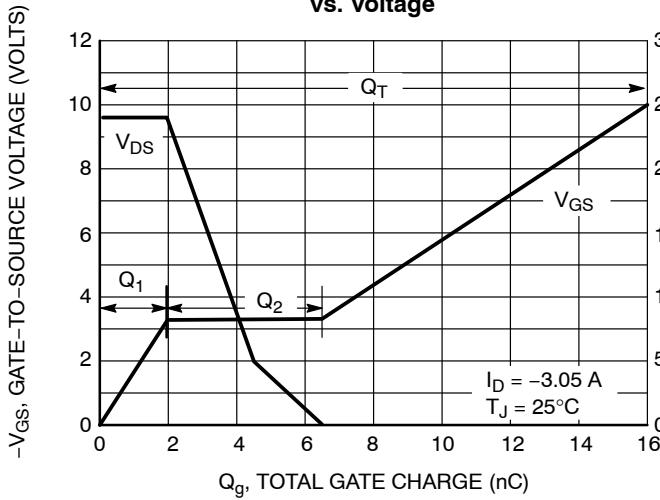
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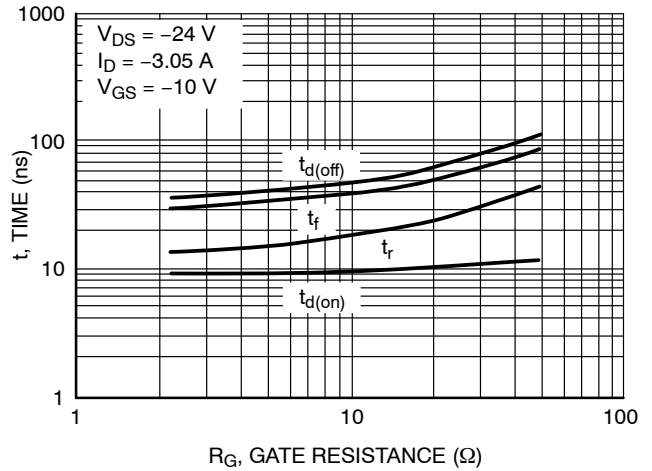
**Figure 7. Drain-to-Source Leakage Current vs. Voltage**



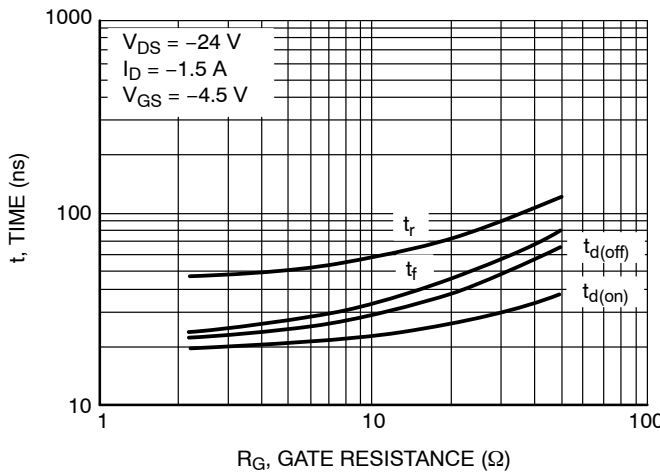
**Figure 8. Capacitance Variation**



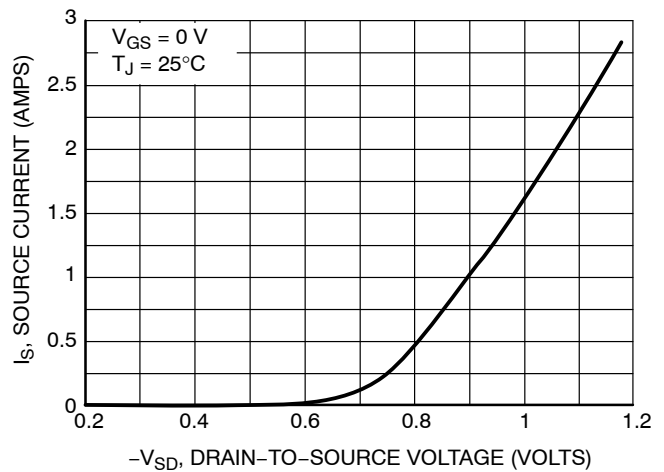
**Figure 9. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge**



**Figure 10. Resistive Switching Time Variation vs. Gate Resistance**

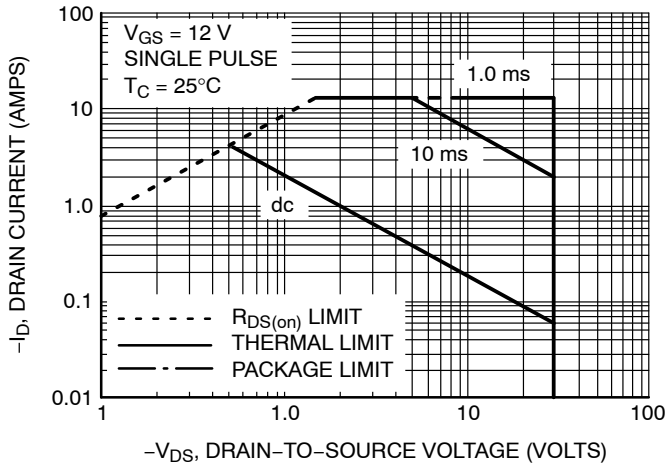


**Figure 11. Resistive Switching Time Variation vs. Gate Resistance**

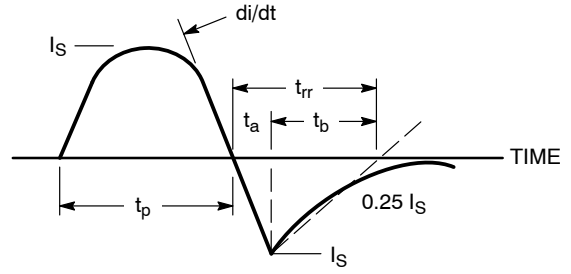


**Figure 12. Diode Forward Voltage vs. Current**

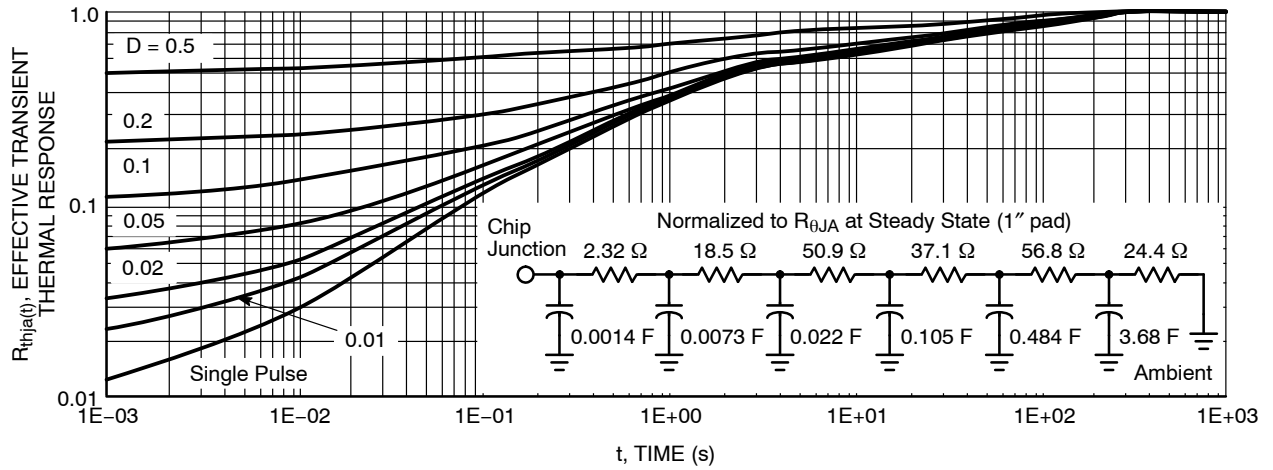
# NTMD3P03, NVMD3P03



**Figure 13. Maximum Rated Forward Biased Safe Operating Area**



**Figure 14. Diode Reverse Recovery Waveform**



**Figure 15. FET Thermal Response**

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

## GENERIC MARKING DIAGRAM\*



SCALE 6:1 ( $\frac{\text{mm}}{\text{inches}}$ )



XXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## STYLES ON PAGE 2

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DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2

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**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

- |   |  |  |  |
|---|--|--|--|
| <p>STYLE 1:<br/>         PIN 1. EMITTER<br/>         2. COLLECTOR<br/>         3. COLLECTOR<br/>         4. EMITTER<br/>         5. EMITTER<br/>         6. BASE<br/>         7. BASE<br/>         8. EMITTER</p>   | <p>STYLE 2:<br/>         PIN 1. COLLECTOR, DIE, #1<br/>         2. COLLECTOR, #1<br/>         3. COLLECTOR, #2<br/>         4. COLLECTOR, #2<br/>         5. BASE, #2<br/>         6. EMITTER, #2<br/>         7. BASE, #1<br/>         8. EMITTER, #1</p>               | <p>STYLE 3:<br/>         PIN 1. DRAIN, DIE #1<br/>         2. DRAIN, #1<br/>         3. DRAIN, #2<br/>         4. DRAIN, #2<br/>         5. GATE, #2<br/>         6. SOURCE, #2<br/>         7. GATE, #1<br/>         8. SOURCE, #1</p>                            | <p>STYLE 4:<br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. ANODE<br/>         4. ANODE<br/>         5. ANODE<br/>         6. ANODE<br/>         7. ANODE<br/>         8. COMMON CATHODE</p>   |
| <p>STYLE 5:<br/>         PIN 1. DRAIN<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. DRAIN<br/>         5. GATE<br/>         6. GATE<br/>         7. SOURCE<br/>         8. SOURCE</p>   | <p>STYLE 6:<br/>         PIN 1. SOURCE<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. SOURCE<br/>         5. SOURCE<br/>         6. GATE<br/>         7. GATE<br/>         8. SOURCE</p>  | <p>STYLE 7:<br/>         PIN 1. INPUT<br/>         2. EXTERNAL BYPASS<br/>         3. THIRD STAGE SOURCE<br/>         4. GROUND<br/>         5. DRAIN<br/>         6. GATE 3<br/>         7. SECOND STAGE Vd<br/>         8. FIRST STAGE Vd</p>                    | <p>STYLE 8:<br/>         PIN 1. COLLECTOR, DIE #1<br/>         2. BASE, #1<br/>         3. BASE, #2<br/>         4. COLLECTOR, #2<br/>         5. COLLECTOR, #2<br/>         6. EMITTER, #2<br/>         7. EMITTER, #1<br/>         8. COLLECTOR, #1</p>                              |
| <p>STYLE 9:<br/>         PIN 1. EMITTER, COMMON<br/>         2. COLLECTOR, DIE #1<br/>         3. COLLECTOR, DIE #2<br/>         4. EMITTER, COMMON<br/>         5. EMITTER, COMMON<br/>         6. BASE, DIE #2<br/>         7. BASE, DIE #1<br/>         8. EMITTER, COMMON</p> | <p>STYLE 10:<br/>         PIN 1. GROUND<br/>         2. BIAS 1<br/>         3. OUTPUT<br/>         4. GROUND<br/>         5. GROUND<br/>         6. BIAS 2<br/>         7. INPUT<br/>         8. GROUND</p>  | <p>STYLE 11:<br/>         PIN 1. SOURCE 1<br/>         2. GATE 1<br/>         3. SOURCE 2<br/>         4. GATE 2<br/>         5. DRAIN 2<br/>         6. DRAIN 2<br/>         7. DRAIN 1<br/>         8. DRAIN 1</p>   | <p>STYLE 12:<br/>         PIN 1. SOURCE<br/>         2. SOURCE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>   |
| <p>STYLE 13:<br/>         PIN 1. N.C.<br/>         2. SOURCE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>  | <p>STYLE 14:<br/>         PIN 1. N-SOURCE<br/>         2. N-GATE<br/>         3. P-SOURCE<br/>         4. P-GATE<br/>         5. P-DRAIN<br/>         6. P-DRAIN<br/>         7. N-DRAIN<br/>         8. N-DRAIN</p>   | <p>STYLE 15:<br/>         PIN 1. ANODE 1<br/>         2. ANODE 1<br/>         3. ANODE 1<br/>         4. ANODE 1<br/>         5. CATHODE, COMMON<br/>         6. CATHODE, COMMON<br/>         7. CATHODE, COMMON<br/>         8. CATHODE, COMMON</p>               | <p>STYLE 16:<br/>         PIN 1. EMITTER, DIE #1<br/>         2. BASE, DIE #1<br/>         3. EMITTER, DIE #2<br/>         4. BASE, DIE #2<br/>         5. COLLECTOR, DIE #2<br/>         6. COLLECTOR, DIE #2<br/>         7. COLLECTOR, DIE #1<br/>         8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17:<br/>         PIN 1. VCC<br/>         2. V2OUT<br/>         3. V1OUT<br/>         4. TXE<br/>         5. RXE<br/>         6. VEE<br/>         7. GND<br/>         8. ACC</p>  | <p>STYLE 18:<br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. CATHODE<br/>         8. CATHODE</p>   | <p>STYLE 19:<br/>         PIN 1. SOURCE 1<br/>         2. GATE 1<br/>         3. SOURCE 2<br/>         4. GATE 2<br/>         5. DRAIN 2<br/>         6. MIRROR 2<br/>         7. DRAIN 1<br/>         8. MIRROR 1</p>   | <p>STYLE 20:<br/>         PIN 1. SOURCE (N)<br/>         2. GATE (N)<br/>         3. SOURCE (P)<br/>         4. GATE (P)<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>   |
| <p>STYLE 21:<br/>         PIN 1. CATHODE 1<br/>         2. CATHODE 2<br/>         3. CATHODE 3<br/>         4. CATHODE 4<br/>         5. CATHODE 5<br/>         6. COMMON ANODE<br/>         7. COMMON ANODE<br/>         8. CATHODE 6</p>  | <p>STYLE 22:<br/>         PIN 1. I/O LINE 1<br/>         2. COMMON CATHODE/VCC<br/>         3. COMMON CATHODE/VCC<br/>         4. I/O LINE 3<br/>         5. COMMON ANODE/GND<br/>         6. I/O LINE 4<br/>         7. I/O LINE 5<br/>         8. COMMON ANODE/GND</p> | <p>STYLE 23:<br/>         PIN 1. LINE 1 IN<br/>         2. COMMON ANODE/GND<br/>         3. COMMON ANODE/GND<br/>         4. LINE 2 IN<br/>         5. LINE 2 OUT<br/>         6. COMMON ANODE/GND<br/>         7. COMMON ANODE/GND<br/>         8. LINE 1 OUT</p> | <p>STYLE 24:<br/>         PIN 1. BASE<br/>         2. EMITTER<br/>         3. COLLECTOR/ANODE<br/>         4. COLLECTOR/ANODE<br/>         5. CATHODE<br/>         6. CATHODE<br/>         7. COLLECTOR/ANODE<br/>         8. COLLECTOR/ANODE</p>                                      |
| <p>STYLE 25:<br/>         PIN 1. VIN<br/>         2. N/C<br/>         3. REXT<br/>         4. GND<br/>         5. IOUT<br/>         6. IOUT<br/>         7. IOUT<br/>         8. IOUT</p>   | <p>STYLE 26:<br/>         PIN 1. GND<br/>         2. dv/dt<br/>         3. ENABLE<br/>         4. ILIMIT<br/>         5. SOURCE<br/>         6. SOURCE<br/>         7. SOURCE<br/>         8. VCC</p>  | <p>STYLE 27:<br/>         PIN 1. ILIMIT<br/>         2. OVLO<br/>         3. UVLO<br/>         4. INPUT+<br/>         5. SOURCE<br/>         6. SOURCE<br/>         7. SOURCE<br/>         8. DRAIN</p>  | <p>STYLE 28:<br/>         PIN 1. SW_TO_GND<br/>         2. DASIC_OFF<br/>         3. DASIC_SW_DET<br/>         4. GND<br/>         5. V_MON<br/>         6. VBULK<br/>         7. VBULK<br/>         8. VIN</p>  |
| <p>STYLE 29:<br/>         PIN 1. BASE, DIE #1<br/>         2. EMITTER, #1<br/>         3. BASE, #2<br/>         4. EMITTER, #2<br/>         5. COLLECTOR, #2<br/>         6. COLLECTOR, #2<br/>         7. COLLECTOR, #1<br/>         8. COLLECTOR, #1</p>                        | <p>STYLE 30:<br/>         PIN 1. DRAIN 1<br/>         2. DRAIN 1<br/>         3. GATE 2<br/>         4. SOURCE 2<br/>         5. SOURCE 1/DRAIN 2<br/>         6. SOURCE 1/DRAIN 2<br/>         7. SOURCE 1/DRAIN 2<br/>         8. GATE 1</p>                           |  |  |

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