LMK05028EVM

User's Guide

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Introduction

Overview

The LMK05028EVM is an evaluation module for the LMK05028 Network Clock Generator and Synchronizer. The EVM can be used for device evaluation, compliance testing, and system prototyping.

The LMK05028 integrates two Digital PLLs (DPLLs) with programmable bandwidth for input wander and jitter attenuation. The EVM includes SMA connectors for clock inputs, oscillator inputs, and clock outputs to interface the device with 50-Ω test equipment. The onboard XO and TCXO options allow the LMK05028 to be evaluated in free-running, locked, or holdover mode of operation. The EVM can be configured through the onboard USB microcontroller (MCU) interface using a PC with TI's TICS Pro software graphical user interface (GUI). TICS Pro can be used to program the LMK05028 registers and store the settings in the on-chip EEPROM, enabling custom clock configuration upon power up.

Trademarks

Features

- LMK05028:
  - Dual DPLLs with programmable jitter-attenuation bandwidths
  - Dual Analog PLLs (APLLs) for flexible low-jitter clock generation
  - 4 clock inputs supporting hitless switching and holdover
  - 8 differential or 16 LVCMOS output clocks or combination of both
  - On-chip EEPROM for custom start-up clocks
- SMA ports for clock input, oscillator inputs, and clock outputs
- Onboard oscillator options: 48-MHz XO, LMK61E2 (I2C-programmable), 10-MHz TCXO
- USB MCU interface for I2C/SPI and GPIO pin control using TICS Pro GUI
- Status LEDs for power supplies and device status indicators

What's Included

- LMK05028EVM
- Mini-USB cable

What's Needed

- Windows PC - TICS Pro GUI
- Test Equipment
  - DC power supply (5V, 1A)
  - Real-time oscilloscope
  - Phase noise analyzer
  - Precision frequency counter
  - Signal generator / reference clock

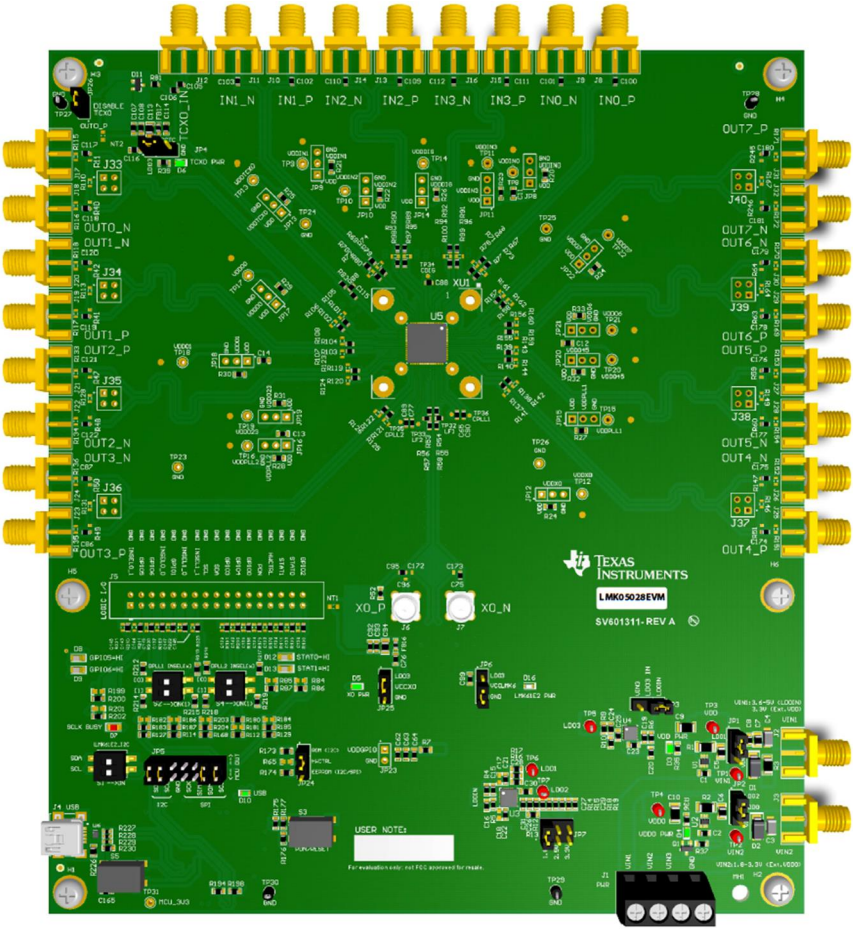

Figure 1. LMK05028EVM

LMK05028EVM User's Guide

1 EVM Quick Start

This quick start guide can be followed to evaluate the LMK05028 (DUT) with the default EVM and device configurations, which are summarized in Section 1.1.

1. Verify the EVM jumper defaults:
   a. JP1, JP2, JP7: Tie pins 1-2 (routes regulated power to DUT).
   b. JP3, JP4, JP25: Tie pins 1-2 (routes regulated power to XO and TCXO).
   c. JP5: Tie pins 1-2, 3-4, 11-12, and 13-14 (routes MCU I2C lines to DUT).
   d. JP6: Tie pins 2-3 (disconnects power to LMK61E2).
   e. JP24: Tie pins 2-3 (selects EEPROM+I2C start-up mode).
   f. S1: Both OFF (disconnects LMK61E2 from I2C bus)
2. Connect 5-V supply and ground from external DC power supply (1-A limit) to VIN1 and GND pins of header J1.
3. Toggle switch S3 (PDN/RESET) to initialize the DUT registers from on-chip EEPROM.
4. Verify LEDs D12/D13 are ON (DPLL1/2 not locked) and D8/D9 are ON (DPLL1/2 holdover active).
   1. With no valid clock input, the clock outputs will free-run and track the frequency stability of the TCXO (Y2).
5. To lock the DPLLs, connect an external 25-MHz single-ended clock input to any IN[0:3] SMA port.
   a. When a valid clock input is detected, observe LEDs D12/D13 are OFF (DPLL1/2 locked) and D8/D9 are OFF (DPLL1/2 holdover not active).
   b. The output clocks should track the frequency accuracy of the clock input.
6. Observe any clock outputs on the OUT[0:7] SMA ports. For best results:
   a. A balun is recommended to interface differential outputs to single-ended RF test equipment, such as a phase noise analyzer.
   b. Terminate active output SMA ports with 50-Ω loads to minimize noise, or disable unused outputs through register programming.
7. To program the LMK05028 through the USB interface, connect the USB cable from connector J4 to the PC and configure the device through the TICS Pro GUI.
   a. See Appendix A for TICS Pro software installation and usage.

TICS Pro uses the "USB2ANY" API software driver to control the USB MCU interfaces (I2C/SPI, Logic pins) on the EVM. TICS Pro can be used to write or read the device registers and program the device EEPROM for a different start-up configuration.

1.1 Default EVM Configuration

- Power Supplies:
  - VIN1: 5 V (Main supply to onboard LDO regulators)
  - LMK05028 VDD: 3.3 V from LDO1 regulator
  - LMK05028 VDDO: 1.8 V from LDO2 regulator
  - XO and TCXO: 3.3 V from LDO3 regulator

- LMK05028 (U5):
  - Clock Inputs:
    - IN[0:3]: DC-coupled from SMA connectors
  - Clock Outputs:
    - OUT[0:6]: AC-coupled to SMA connectors
    - OUT7: DC-coupled to SMA connectors
- Oscillators onboard:
  - TCXO (Y2): 10.000000 MHz, 3.3 V, LVCMOS, ±4.6-ppm stability
  - XO (Y1), Default: 48.0048 MHz, 3.3 V, LVCMOS, low-jitter, ±25-ppm stability
  - XO (Y2), Alternate: LMK61E2, 10–1000 MHz (I2C-programmable), 3.3 V, Differential, low-jitter, ±50-ppm stability

NOTE: The EEPROM image of the LMK05028 was custom-programmed to demonstrate the default configuration in Table 1, which is different from generic factory-programmed devices.

Table 1. Default Configuration - EEPROM Start-Up Modes

DEVICE START-UP MODE	EEPROM + I2C MODE (HW_SW_CTRL = 0)	EEPROM + SPI MODE (HW_SW_CTRL = FLOAT)
HW_SW_CTRL (JP24) Jumper Setting	Tie Pins 2-3	Open
MCU I2C/SPI (JP5) Jumper Settings	Tie Pins 1-2, 3-4, 11-12, 13-14 (Routes MCU I2C to DUT)	Tie Pins 1-2, 3-4, 7-8, 9-10 (Routes MCU SPI to DUT)
XO Input	48.0048-MHz Differential or Single-Ended	
TCXO Input	10-MHz Single-Ended	
IN[0:3] Clock Inputs	25-MHz Differential or Single-Ended Input on-chip termination disabled	
DPLL1 Clock Input Assignment	IN0, IN1, IN2, IN3 (highest to lowest priority order)	
DPLL2 Clock Input Assignment	IN0, IN1, IN2, IN3 (highest to lowest priority order)	
DPLL1 Clock Input Selection	Auto Non-Revertive	
DPLL2 Clock Input Selection	Auto Non-Revertive	
VCO1 Frequency	5000 MHz	
VCO2 Frequency	5529.6 MHz	
OUT[0:3] Output Frequency	122.88-MHz AC-LVPECL (VCO2 domain)	
OUT[4:7] Output Frequency	156.25-MHz AC-LVPECL (VCO1 domain)	
DPLL1 Loop Mode	3 Loop: REF-DPLL, TCXO-DPLL, APLL	
DPLL2 Loop Mode	3 Loop: REF-DPLL, TCXO-DPLL, APLL	
DPLL1 Loop Bandwidth	10 Hz	
DPLL2 Loop Bandwidth	10 Hz	
DPLL1 TCXO Loop Bandwidth	600 Hz	
DPLL2 TCXO Loop Bandwidth	600 Hz	
IN[0:3] Frequency Detect Thresholds	Valid < 55 ppm, Invalid > 60 ppm (1)	
GPIO5 Output	DPLL1 Holdover Active (active high)	
GPIO6 Output	DPLL2 Holdover Active (active high)	
STATUS0 Output	DPLL1 Loss of Lock (active high)	
STATUS1 Output	DPLL2 Loss of Lock (active high)	

(1) Clock input frequency thresholds (ppm) are relative to the frequency accuracy of the TCXO input, as configured.

2 Device Under Test

The evaluation module is shipped with the LMK05028 DUT (U5) soldered-down. The pin 1 position of the 64-pin QFN package is indicated by a dot symbol in top silkscreen. Alternatively, U5 can be unmounted and a test socket (XU1) can be populated. See the Bill of Materials for the socket part number. TI recommends populating the socket with the hinge on the left hand side (towards OUT[0:3] ports) and the latch on the right hand side.

2.1 Device Start-Up Modes

The LMK05028 can start-up in one of three modes depending on the 3-level input level sampled on the HW_SW_CTRL pin upon power-on reset (POR). The start-up modes are listed in Table 2 and determine the following:

1. The memory bank (EEPROM or ROM) used to initialize the registers upon start-up.
2. The serial interface (I2C or SPI) used for register access.
3. The logic pin definitions.

The I2C or SPI interface allows for register access to configure the device after start-up and monitor its status. The register map configurations are the same for I2C and SPI.

See Section 3.2 for detailed descriptions of the logic pins for each start-up mode.

Table 2. Device Start-Up Modes

HW_SW_CTRL (JP24) INPUT LEVEL(1)	START-UP MODE (2)(3)	MODE DESCRIPTION
0	EEPROM + I2C	Registers are initialized from EEPROM, and I2C interface is enabled. Logic pins: • SDA, SCL: I2C Data, I2C Clock • GPIO0: Output Sync (active low) • GPIO[2:1]: I2C Address LSB Select (00, 01, 10, 11b) • GPIO[4:3]: DPLL1 DCO FDEC/FINC (active high) • GPIO[6:5]: DPLL2 DCO FDEC/FINC (active high), or Status Outputs
Float	EEPROM + SPI	Registers are initialized from EEPROM, and SPI interface is enabled. Logic pins: • SDA, SCL: SPI Data In (SDI), SPI Clock • GPIO1: SPI Chip Select (SCS) • GPIO2: SPI Data Out (SDO) • GPIO[0, 3-6]: Same as for HW_SW_CTRL = 0
1	ROM + I2C	Registers are initialized from the ROM page selected by GPIO pins, and I2C interface is enabled. Logic pins: • SDA, SCL: I2C Data, I2C Clock • GPIO[3:0]: ROM Page Select (0000 to 1111b) • GPIO[6:5]: Status Outputs • GPIO4: Not used

(1) HW_SW_CTRL pin (3-level input) has a weak internal bias to about 0.9 V (Float state). When HW_SW_CTRL = Float, STATUS[1:0] pins must not be pulled high or low externally during POR to ensure proper start-up into EEPROM+SPI Mode.
(2) EEPROM Mode is also called *Soft Pin Mode*. EEPROM settings are software programmable in NVM through registers (in-system or factory programmable).
(3) ROM Mode is also called *Hard Pin Mode*. ROM settings are fixed in hardware memory map (factory-set by metal mask).

In typical applications, EEPROM Mode is only recommended if one custom start-up configuration is needed from a single Orderable Part Number (OPN), or if auto start-up operation from EEPROM is not required because a system host (for example, MCU, FPGA) would be able to program the registers through I2C or SPI after power up. ROM Mode is a reserved mode for customers that require multiple custom start-up configurations supported by a single OPN.

NOTE: Please contact TI Field Sales or email appscts@list.ti.com to inquire about a custom OPN with factory-programmed EEPROM or ROM configurations.

3 EVM Configuration

The LMK05028 is a highly configurable clock chip with multiple power domains, PLL domains, and clock input and output domains. To support a wide range of LMK05028 use cases, the EVM was designed with more flexibility and functionality than needed to implement the chip in a customer system application.

This section describes the power, logic, and clock input and output interfaces on the EVM, as well as how to connect, set up, and operate the EVM.

An overview of some key components are shown in Table 3, Figure 2, and Figure 3.

Table 3. List of Key Components

ITEM NO.	REF DES	DESCRIPTION / LABEL
1	U5	LMK05028 DUT
2	VIN1 (terminal) **or** J2 (SMA)	Main Supply Input (5 V using Default configuration)
3	Y4 **or** J6/J7	Y4 (bottom side): 48.0048-MHz XO (Default), or J6/J7: SMA ports for external XO_P/N input (requires BOM change)
4	Y2 **or** J12	Y2 (bottom side): 10-MHz TCXO (Default), or J12: SMA port for external TCXO input
5	U7	LMK61E2 (bottom side)
6	J8/J9 to J15/J16 (excluding J12)	SMA ports for DPLL Ref. Clock Inputs (IN0_P/N to IN3_P/N)
7	J17/J18 to J31/J32	SMA ports for Clock Outputs (OUT0_P/N to OUT7_P/N)
8	S3	Toggle switch for DUT power-down reset (PDN) pin
9	S2/S4	DIP switches for DPLL 1/2 input select pins
10	D8, D9	Status LEDs for DUT GPIO[5:6] pins
11	D12, D13	Status LEDs for DUT STATUS[0:1] pins
12	JP5	2x7 Header for I2C/SPI Jumpers (MCU-DUT)
13	J4	USB port for MCU

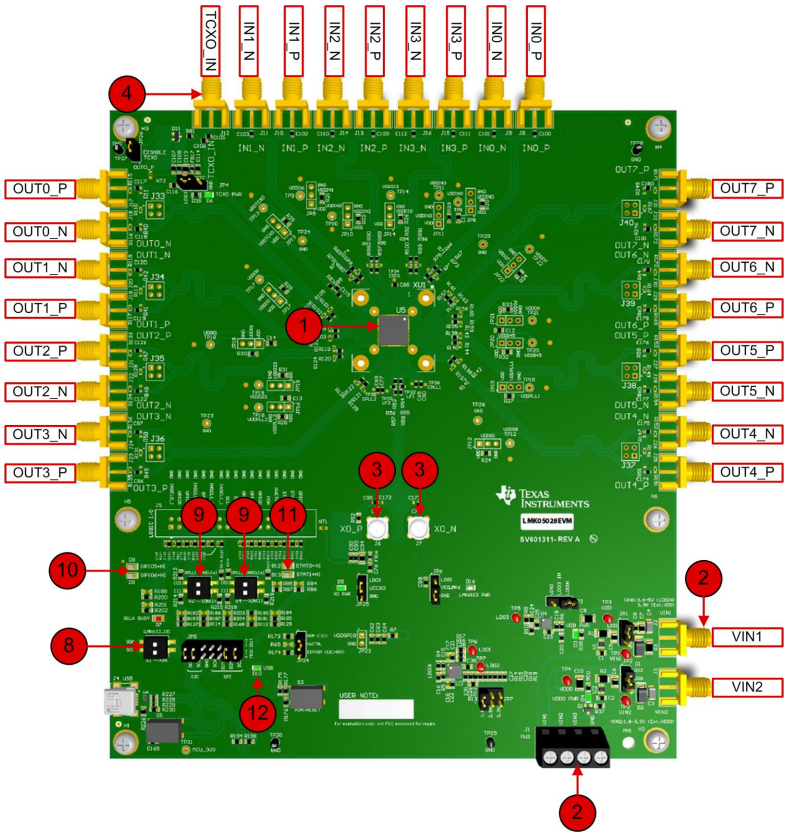

Figure 2. Key Components - EVM Top Side

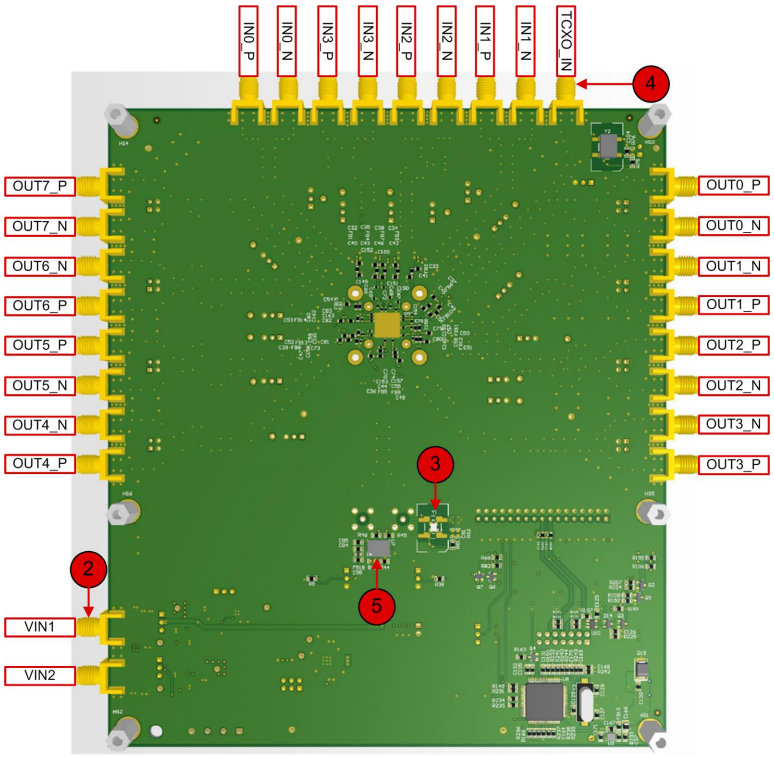

Figure 3. Key Components - EVM Bottom Side

3.1 Power Supply

The LMK05028 has 9 core VDD supply pins that operate from 3.3 V ± 5% and 6 output VDDO supply pins that operate from 1.8 V, 2.5 V, or 3.3 V ± 5%.

J1 is the main power terminal to connect power and ground to an external 1-A power supply. Power SMA port VIN1 (J2) provides an alternative connector style to apply power through coax cable.

On the EVM, the default power configuration uses the onboard LDO regulators to power all VDD and VDDO pins from an external 5-V supply input VIN1 to J1 (or J2). A Dual LDO regulator (U3) is used to power the VDD and VDDO rails of the DUT and its peripheral circuitry. A separate LDO regulator (U4), also supplied from VIN1, is used to power the onboard XO and TCXO circuits.

NOTE: Not every power connection is used nor required to operate the EVM. Other power configurations are possible. See Figure 10 and Figure 11 for the power schematics.

Figure 4 shows the default power jumper locations and settings.

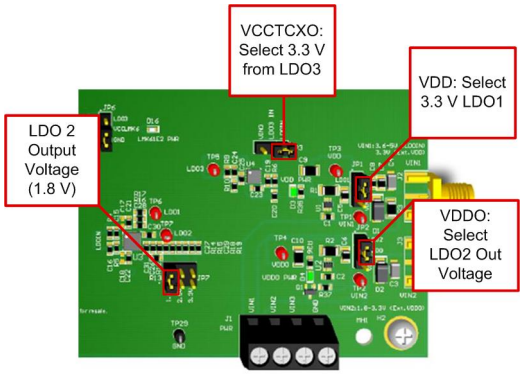

Figure 4. Default Power Jumper Configuration

Table 4 shows the suggested power configurations for the DUT.

Table 4. Suggested DUT Power Configurations

CONNECTION	NAME	ONBOARD LDO REGULATORS (DEFAULT)	DIRECT EXTERNAL SUPPLIES
		VDD = 3.3 V VDDO = 1.8 / 2.5 / 3.3 V	VDD = 3.3 V VDDO = 1.8 / 2.5 / 3.3 V
J1 (1)	PWR	Pin 1 (VIN1): Connect to external 5-V supply Pin 2 (VIN2): N/A Pin 3 (VIN3): N/A Pin 4 (GND): Connect to supply ground	Pin 1 (VIN1): Connect to external 3.3-V supply Pin 2 (VIN2): Connect to external 1.8-V, 2.5-V, or 3.3-V supply Pin 3 (VIN3): N/A Pin 4 (GND): Connect to supply ground
JP1	VDD	Tie pins 1-2: Selects 3.3 V from LDO1 to VDD Plane	Tie pins 2-3: Selects ext. 3.3V supply from VIN1 to VDD Plane
JP2	VDDO	Tie pins 1-2: Selects LDO2 output to VDDO Plane	Tie pins 2-3: Selects ext. supply from VIN2 to VDDO Plane
JP7	VOUT2	Tie pins 1-2: LDO2 out = 1.8 V (default) Tie pins 3-4: LDO2 out = 2.5 V Tie pins 5-6: LDO2 out = 3.3 V	N/A

(1) SMA ports J2 or J3 can be used to power VIN1 or VIN2 respectively via coaxial cable, instead of using bare wires to J1.

Table 5 shows the suggested power configurations for the onboard XO and TCXO circuits.

Table 5. Suggested XO and TCXO Power Configurations

CONNECTION	NAME	ONBOARD LDO REGULATORS (DEFAULT)	DIRECT EXTERNAL SUPPLIES
		LDO3 = 3.3 V	VCCXO = 3.3 V VCCTC = 3.3 V
J1	PWR	Pin 1 (VIN1): Connect to external 5-V supply Pin 2 (VIN2): N/A Pin 3 (VIN3): N/A Pin 4 (GND): Connect to supply ground	N/A
JP3	LDO3 IN	Tie pins 1-2: Selects 5 V from VIN1 to LDO3 IN	N/A
JP25	VCCXO	Tie pins 1-2: Select 3.3 V from LDO3	Pin 1 (LDO3): Open Pin 2 (VCCTC): Connect to external 3.3-V supply Pin 3 (GND): Connect to external supply ground
JP27	VCCTC	Tie pins 1-2: Select 3.3 V from LDO3	Pin 1 (LDO3): Open Pin 2 (VCCXO): Connect to external 3.3-V supply Pin 3 (GND): Connect to external supply ground
JP29	VCCLMK6	Tie pins 1-2: Selects 3.3 V from LDO3	Pin 1 (LDO3): Open Pin 2 (VCCLMK6): Connect to external 3.3-V supply Pin 3 (GND): Connect to external supply ground

NOTE: Disconnect the power / signal paths from any XO or TCXO circuit not used for a given configuration to avoid unwanted spurious noise on the board.

3.2 Logic Inputs and Outputs

The logic I/O pins of the DUT support different functions depending on the device start-up mode chosen by the HW_SW_CTRL input level upon POR. Moreover, GPIO[5:6] and STATUS[0:1] pins are programmable.

The default logic input pin states are determined by onboard pullup or pulldown resistors, but some inputs pin can be driven high or low state by MCU output or DIP switch control. The onboard MCU can be driven from a PC running TICS Pro to set the DUT logic input states, as well as program the device registers through I2C or SPI.

Refer to the following tables for logic pin descriptions according to each device start-up mode:

1. **EEPROM + I2C Mode (HW_SW_CTRL = 0)** – see Table 6
2. **EEPROM + SPI Mode (HW_SW_CTRL = Float)** – see Table 7
3. **ROM + I2C Mode (HW_SW_CTRL = 1)** – see Table 8

Logic pins not listed in Table 7 or Table 8 are the same as described in Table 6.

Table 6. Logic Pin Descriptions - EEPROM + I2C Mode (HW_SW_CTRL = 0)

<table>
<tr><th>PIN NAME
(TYPE)</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td rowspan="4">PDN
(2-level input)</td><td colspan="2">Chip Power-down (active low)
When PDN rises to 1, the digital control block triggers the internal POR sequence, initializes all registers and logic pins for the start-up mode selected by the HW_SW_CTRL input level, restores all internal circuits including the serial interface to their initial state, and begins normal operation.
This pin is high by default through an external pullup resistor, but can be pulled down through switch S3.</td></tr>
<tr><td>PDN STATE</td><td>CHIP STATE</td></tr>
<tr><td>0
(S3 pushed)</td><td>Power-down reset state
(Serial interface disabled)</td></tr>
<tr><td>1
(default)</td><td>Normal operation</td></tr>
<tr><td>SDA
(open drain)</td><td colspan="2">I2C Data
The I2C interface between the DUT and MCU connect through two jumpers on JP5.
Tie JP5 pins 1-2 (SDA) and pins 3-4 (SCL) to connect the MCU and DUT to allow register programming through I2C. Remove jumpers from JP5 pins 7-8 and pins 9-10, so the MCU SPI SCL and SDI pins are not connected simultaneously.
Also, it is possible to program an off-board LMK05028 DUT by removing the I2C jumpers from JP5, and connecting the MCU side (JP5 pins 1, 3, and 5) to the SDA, SCL, and GND lines of the DUT on the target board. The MCU side of J5 has external I2C pullup resistors to 3.3 V.</td></tr>
<tr><td>SCL
(open drain)</td><td colspan="2">I2C Clock
See SDA pin description above. Red LED (D7) will turn ON during I2C activity.</td></tr>
<tr><td rowspan="4">GPIO0
(2-level input)</td><td colspan="2">Output SYNC (active low)
GPIO0 can be used to mute the output clocks and trigger output divider synchronization if synchronization is enabled by registers. Alternatively, SYNC can also be triggered via register programming without using this pin.
This pin is pulled high by default through an external pullup resistor, but the pin can also be driven high through MCU control.</td></tr>
<tr><td>GPIO0 STATE</td><td>OUTPUT SYNC STATE</td></tr>
<tr><td>0</td><td>SYNC asserted: Outputs muted, output dividers held in reset.</td></tr>
<tr><td>1 (default)</td><td>SYNC deasserted: Normal output operation.</td></tr>
</table>

Table 6. Logic Pin Descriptions - EEPROM + I2C Mode (HW_SW_CTRL = 0) (continued)

PIN NAME (TYPE)	DESCRIPTION	
GPIO[2:1] (2-level inputs)	**I2C Slave Address LSB Select** GPIO[2:1] is sampled on POR to configure the lower 2 bits of the 7-bit slave address (excluding W/R bit). The upper 5 bits of the slave address are initialized from EEPROM (SLAVEADR[7:3] = 11000b). These pins are both pulled low by default through external pulldown resistors, but external pullup resistor options are also available to select a different slave address on start-up.	
	GPIO[2:1] STATE	**7-BIT SLAVE ADDRESS**
	00b (default)	1100000b / 0x60h
	01b	1100001b / 0x61h
	10b	1100010b / 0x62h
	11b	1100011b / 0x63h
GPIO[4:3] (2-level inputs)	**DPLL1 DCO Mode Frequency Decrement/Increment** When DPLL1 is configured for DCO Mode, a logic high input on GPIO3 or GPIO4 can accordingly increment or decrement the DCO numerator by the programmable frequency deviation (FDEV) step size to adjust its frequency. These pins are pulled low by default via external pulldown resistors, and can be pulsed high through MCU control using TICS Pro. Alternatively, FINC1/FDEC1 can be triggered through register programming without using these pins.	
	GPIO[3:4] STATE	**DPLL1 DCO NUMERATOR**
	0 (default)	Not updated
	1	Incremented (GPIO3) or Decremented (GPIO4)
GPIO[6:5] (2-level inputs)	**DPLL2 DCO Mode Frequency Decrement/Increment** When DPLL2 is configured for DCO Mode, a logic high input on GPIO5 or GPIO6 can accordingly increment or decrement the DCO numerator by the programmable frequency deviation (FDEV) step size to adjust its frequency. These pins are pulled low by default through external pulldown resistors, and can be pulsed high through MCU control using TICS Pro. Alternatively, FINC2/FDEC2 can be triggered through register programming without using these pins. If DPLL2 DCO mode control via pins in not used, GPIO[5:6] pins could be each programmed as additional status outputs, if needed. As status outputs, the GPIO[5:6] pins are individually programmable and support NMOS open-drain (requires external pullup resistor) or 3.3-V LVCMOS driver type.	
	GPIO[5:6] STATE	**DPLL2 DCO FREQUENCY CONTROL**
	0 (default)	Not updated
	1	Incremented (GPIO5) or Decremented (GPIO6)
INSEL0_[1:0] (2-level inputs)	**DPLL1 Ref. Input Selection** INSEL0_[1:0] pins select the DPLL1 reference input when Manual Input Select Mode and HW Pin Control (via INSEL pins) are selected by register configuration. These pins are ignored when Auto Input Select Mode or SW Register Control is selected. These pins are pulled low by default through external pulldown resistors, but either pin can be pulled high through a stronger pullup resistor when switch S2 (SPST-2) is set to ON.	
	INSEL0_[1:0] (S2) STATE	**DPLL1 REF INPUT**
	00b	IN0
	01b	IN1
	10b	IN2
	11b	IN3

Table 6. Logic Pin Descriptions - EEPROM + I2C Mode (HW_SW_CTRL = 0) (continued)

PIN NAME (TYPE)	DESCRIPTION	
INSEL1_[1:0] (2-level inputs)	**DPLL2 Ref. Input Selection** INSEL1_[1:0] pins select the DPLL2 reference input when Manual Input Select Mode and HW Pin Control (via INSEL pins) are selected by register configuration. These pins are ignored when Auto Input Select Mode or SW Register Control is selected. These pins are pulled low by default through external pulldown resistors, but either pin can be pulled high through a stronger pullup resistor when switch S4 (SPST-2) is set to ON.	
	INSEL1_[1:0] (S4) STATE	**DPLL2 REF INPUT**
	00b	IN0
	01b	IN1
	10b	IN2
	11b	IN3
STATUS[1:0] (logic outputs)	**Status Outputs** STATUS[1:0] pins are individually programmable status outputs that support NMOS open-drain (requires external pullup resistor) or 3.3-V LVCMOS driver type.	

Table 7. Logic Pin Descriptions - EEPROM + SPI Mode (HW_SW_CTRL = Float) (1) (2)

PIN NAME (TYPE)	DESCRIPTION
SDA (2-level input)	**SPI Data In (SDI / SIMO)** The SPI interface between the DUT and MCU can be connected using four jumpers on JP5. Tie JP5 pins 7-8 (SCL), pins 9-10 (SCL), pins 11-12 (SDO), and pins 13-14 (SCS) to connect the MCU and DUT to allow register programming through SPI. Remove jumpers from JP5 pins 1-2 and pins 3-4, so the MCU I2C pins are not connected simultaneously. Also, it is possible to program an off-board LMK05028 DUT by removing the SPI jumpers from JP5, and connecting the MCU side (JP5 pins 5, 7, 9, 11, and 13) to the GND, SCL, SDI, SDO, and SCS lines of the DUT on the target board.
SCL (2-level input)	**SPI Clock (SCK)** See SDA pin description above. Red LED (D7) will turn ON during SPI activity.
GPIO1 (2-level input)	**SPI Chip Select (SCS)** See SDA pin description above.
GPIO2 (2-level input)	**SPI Data Out (SDO / SOMI)** See SDA pin description above.
STATUS[1:0] (logic outputs)	**Status Outputs** During POR, the HW_SW_CTRL and STATUS[1:0] pin input levels are all sampled with during POR to determine the device start-up mode. If HW_SW_CTRL is float (or about 0.9V) and either STATUS pin is externally pulled high or low, the device will start up into a special test mode not intended for customer use. Therefore, both STATUS pins must be allowed to float to about 0.9 V (through internal or external bias) during POR to ensure proper start-up into EEPROM+SPI Mode. STATUS[1:0] pins are individually programmable status outputs that support NMOS open-drain or 3.3-V LVCMOS driver type. However, 3.3-V LVCMOS driver type is recommended since external pullup resistors are to be avoided on the STATUS pins when using EEPROM+SPI Mode.

(1) Logic pins not listed in Table 7 are the same as described in Table 6.

(2) When HW_SW_CTRL = Float, STATUS[1:0] pins must not be pulled high or low externally during POR to ensure proper start-up into EEPROM+SPI Mode.

Table 8. Logic Pin Descriptions - ROM + I2C Mode (HW_SW_CTRL = 1)[1]

PIN NAME (TYPE)	DESCRIPTION	
GPIO[3:0] (2-level inputs)	**ROM Page Selection** GPIO[3:0] pins are sampled on POR to select the ROM page settings used to initialize the registers. These pins are pulled low by default through external pulldown resistors, but external pullup resistor options are available to select a different ROM page on start-up.	
	GPIO[3:0] STATES	**ROM PAGE SELECT**
	0000b (default)	ROM Page 0
	0001b	ROM Page 1
	0010b	ROM Page 2
	...	...
	1101b	ROM Page 13
	1110b	ROM Page 14
	1111b	ROM Page 15
GPIO4	**Not used.**	
GPIO[6:5] (logic outputs)	**Status Outputs** GPIO[6:5] pins are individually programmable status outputs that can support NMOS open-drain (required external pullup resistor) or 3.3-V LVCMOS driver type.	

(1) Logic pins not listed in Table 8 are the same as described in Table 6.

3.3 TCXO Input

The LMK05028 has a TCXO input (TCXO_IN pin) to accept a system reference clock for any DPLL/DCO mode that uses the TCXO-DPLL loop. This input can be driven by a low-frequency TCXO or OCXO that conforms to the frequency accuracy and holdover stability requirements required by the application. The TCXO input frequency will depend on the LMK05028 frequency plan configuration, but 10 MHz and 12.8 MHz are common.

Y2 is populated on the bottom side with a 10-MHz, 3.3-V, LVCMOS TCXO (Y2) to drive the TCXO input of the chip through a voltage divider. The TCXO input path is terminated by 50 Ω and AC-coupled to the TCXO_IN pin of the chip, which has internal input biasing. If a different TCXO frequency or model must be evaluated, Y2 has multiple 4-pad SMD footprints overlaid to populate another TCXO/OCXO (3.2x2.5, 5x7, or 9x14-mm size) after the pre-installed TCXO is carefully unmounted. The EVM has copper cutout areas in the PCB layers below footprint Y2 to isolate the TCXO from PCB thermal gradients, which may help maintain better frequency stability.

Alternatively, the TCXO input can be driven from an external single-ended clock source (1.3-Vpp maximum swing) through the SMA input port, J12.

The onboard TCXO should be powered off through the JP4 (tie pins 2-3) when using the external SMA input path or when the TCXO input not used in the device configuration. Because the external SMA input path and Y2's output pin are both connected the same path through C105 and C106, D11 (Schottky type) and R81 are intended to protect Y2 by limiting the voltage at its output (pin 3) when the SMA input path is driven externally while the Y2 is powered off.

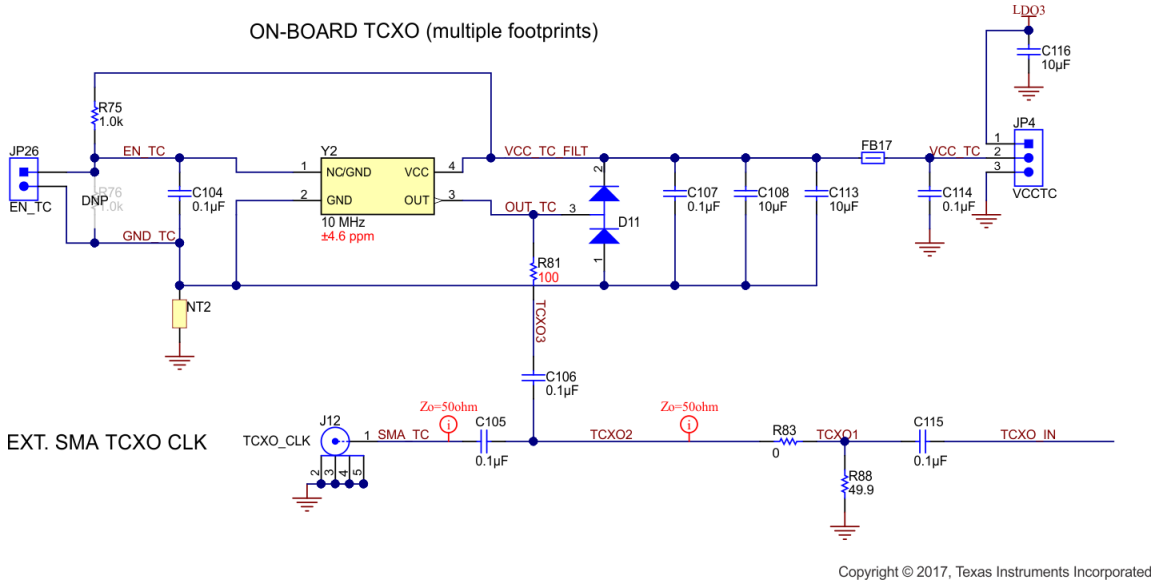

Figure 5. TCXO Input Interface - 10-MHz TCXO (Y2) and SMA Port

3.4 XO Input

The LMK05028 has an XO input (XO_P/N pins) to accept a reference clock for the Fractional-N APLLs. The optimal XO frequency depends on the LMK05028 frequency plan configuration. Typically, it should be between 48 to 54 MHz and have a non-integer frequency relationship with the target VCO frequencies so the APLLs operate in Fractional mode. The XO input of the LMK05028 has programmable on-chip input termination and biasing options to support any clock interface type.

For flexibility, the EVM provides the following options to drive the XO input (use one at a time).

By default, the EVM is populated with a 48.0048-MHz, 3.3-V LVCMOS, low-jitter oscillator (Y1) to drive the XO_P input of the DUT with onboard termination and AC coupling. See Figure 6. Y1 can be used to demonstrate various frequency plan configurations. If a different XO frequency or model must be evaluated, Y1 has multiple 4-pad SMD footprints overlaid to populate another XO (2.5x2.0, 3.2x2.5, 5x7, or 9x14-mm size) after the pre-installed XO is carefully unmounted.

An alternative option is to use the other onboard LMK61E2 differential oscillator (U7). See Figure 7. U7 can be programmed through I2C to any supported XO frequency. The outputs of U7 can be routed to the XO_P/N input of the DUT with minimal PCB rework by placing 0.1-µF capacitors on C172 and C173, and opening C75, C95, and C96 (note: C172 shares a pad with C95 and C96, and C173 shares a pad with C75). U7 can be powered by 3.3 V from LDO3 by JP6 (tie pins 1-2). After both S1 switches are set to the ON position, U7 will share the same I2C bus as the DUT, and U7 (slave address 0x58) can be programmed using the LMK61E2 device profile in TICS Pro.

The last option is to drive the XO input from an external clock through SMA input ports, J6/J7. This path can be connected to the XO_P/N input pins by placing 0.1-µF capacitors on C75 and C96, and opening C95, C172, and C173. Y1 and U7 should be powered down when using the external XO input path.

NOTE: Disconnect the power / signal paths from any XO circuit not used for a given configuration to avoid unwanted spurious noise on the board. Y1 can be powered down by JP25 (Tie pins 2-3). U7 can be powered down by JP6 (Tie pins 2-3).

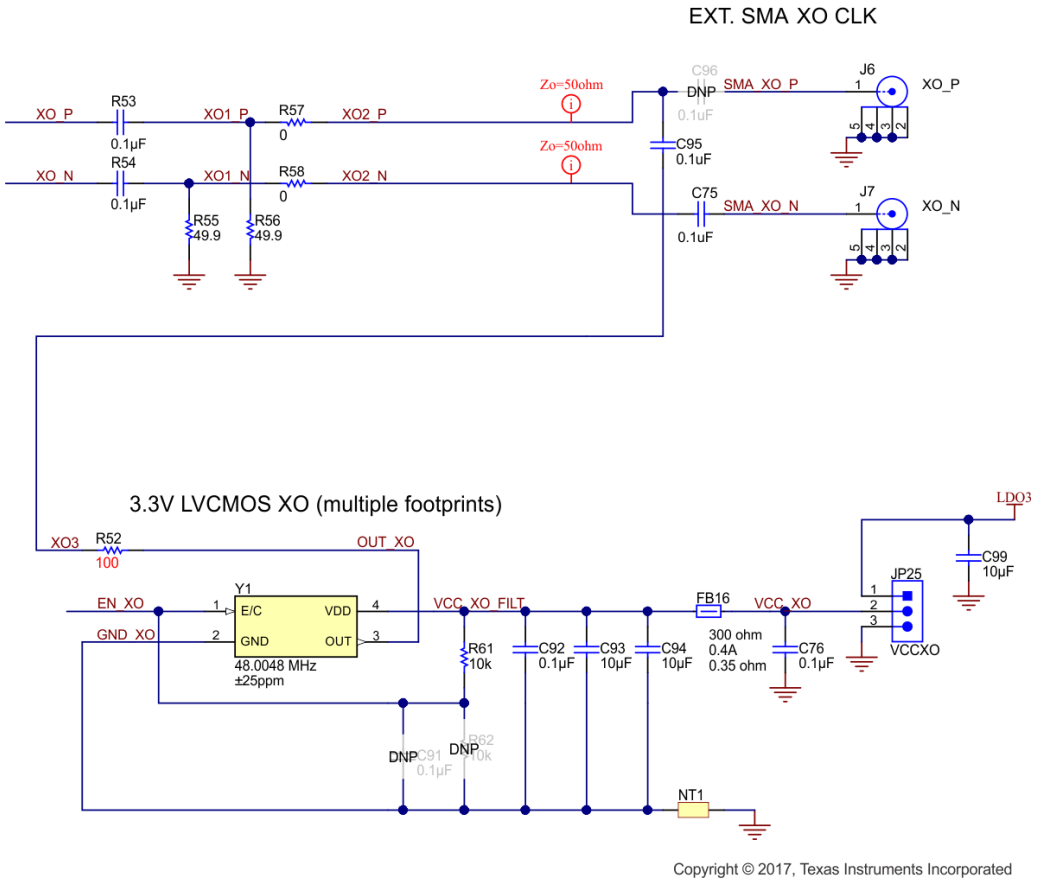

Figure 6. XO Input Interface (1 of 2) - 48.0048-MHz Oscillator and SMA Ports

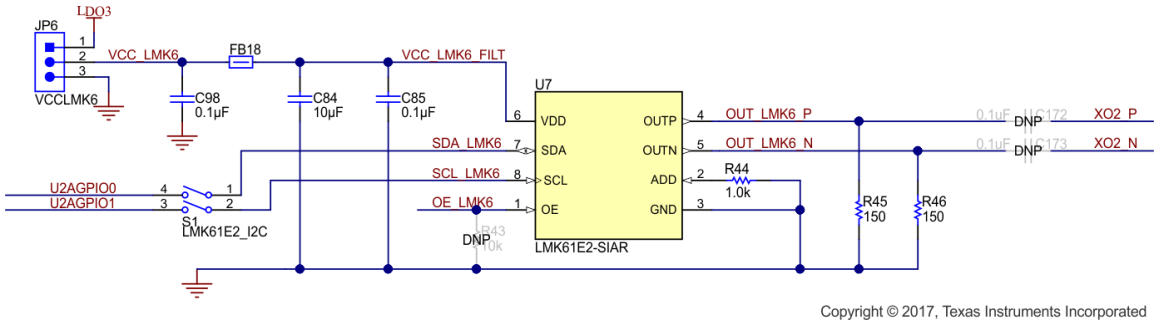

Figure 7. XO Input Interface (2 of 2) - LMK61E2 Oscillator

3.5 Reference Clock Inputs

The LMK05028 has 4 reference clock input pairs (IN[0:3]_P/N) that can be assigned to either DPLL or both DPLL domains with programmable reference input priority and automatic or manual input selection modes. The inputs have programmable input type, termination, and biasing options to support any clock interface type.

External LVCMOS or Differential reference clock inputs can be applied to the SMA ports, labeled IN0_P/N to IN3_P/N. All SMA inputs are routed through 50-Ω single-ended traces and DC-coupled to the INx_P/N pins of the DUT.

LVCMOS clock inputs can be driven to INx_P with INx_N pulled down. LVCMOS input type is recommended for clock input frequencies of 1 MHz or lower. LVCMOS clock inputs should conform to the voltage levels and minimum slew rate specifications in the data sheet for proper amplitude detection.

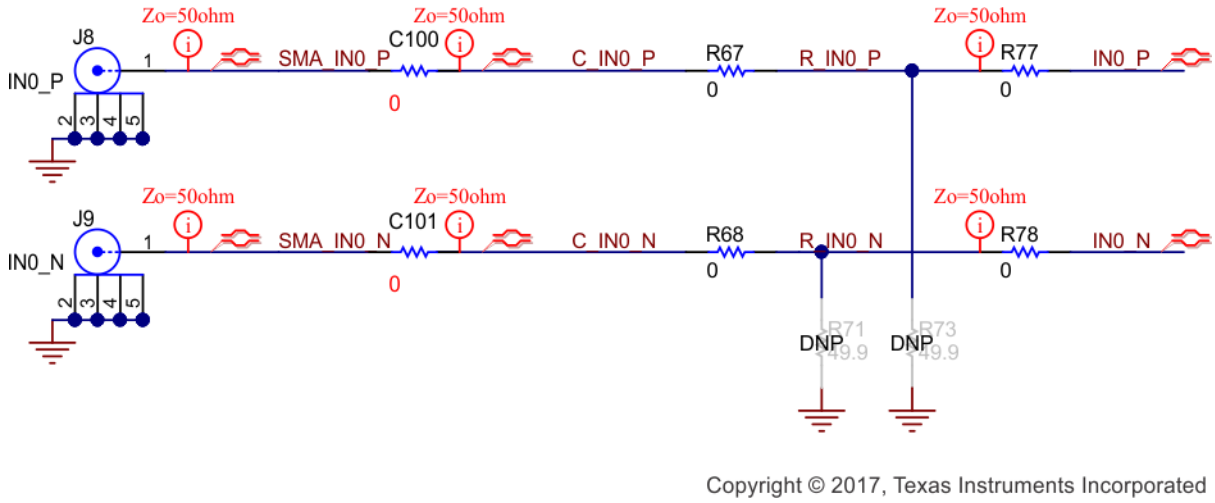

Figure 8. Clock Input Interface - IN0 (similar for IN1-IN3)

3.6 Clock Outputs

The LMK05028 has 8 clock output pairs (OUT[0:7]_P/N) that can be sourced from either DPLL1 or DPLL2 domain. On OUT0 and OUT1, it is also possible to output a buffered copy of the TCXO, XO, DPLL1 REF, or DPLL2 REF inputs.

Output clocks are routed through 50-Ω single-ended traces and AC-coupled to the SMA ports labeled OUT[0:6]_P/N. OUT7_P/N is also routed through 50-Ω single-ended traces, but is DC-coupled to the SMA port to allow for evaluation of low frequency outputs (for example, 1 PPS or 1 Hz), as well as LVCMOS or HCSL output clocks. Each output pair supports AC-LVDS/CML/LVPECL, HCSL, and 1.8-V/2.5-V LVCMOS driver types. HCSL driver has programmable on-chip termination or can used external termination. Each LVCMOS driver has internal 50-Ω output impedance and supports 2 output clocks (per P/N pair) with independently programmable polarity and tri-state options.

Each output channel has its own VDDO output supply pin that operates from 1.8 V, 2.5 V, or 3.3 V, and its own internal LDO regulator to provide excellent output phase noise and high power-supply noise rejection.

Note that LVCMOS output high level (VOH) cannot reach VDDO when VDDO = 3.3 V because the LDO regulator has a dropout voltage that reduces the internal supply voltage to the LVCMOS driver. For VDDO = 1.8 V or 2.5 V, the LVCMOS driver is powered directly from VDDO (channel LDO is bypassed) which allows full rail-to-rail output swing.

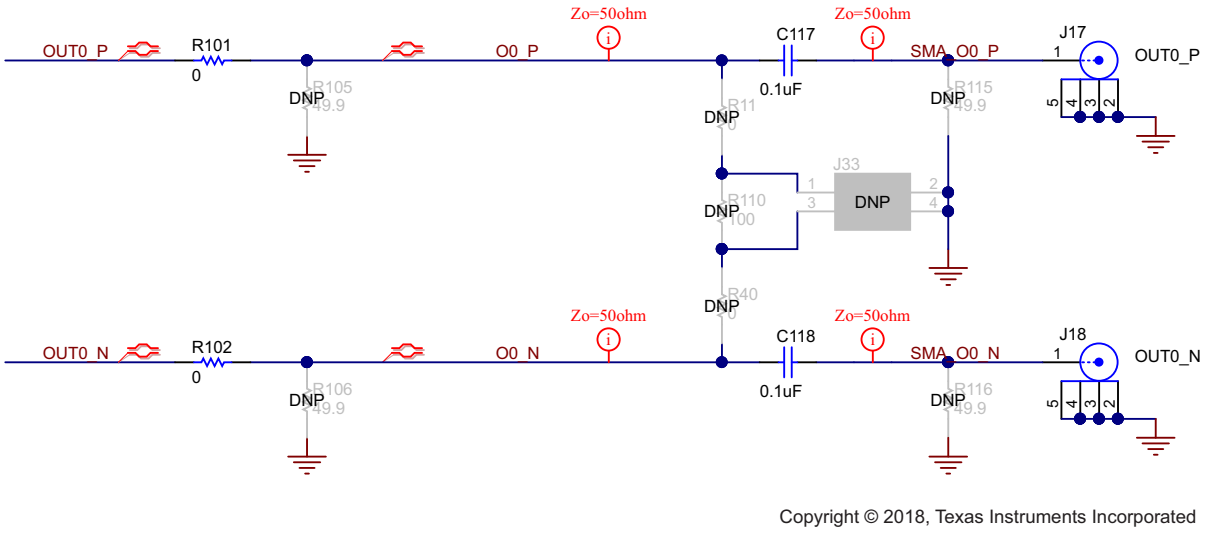

Figure 9. Clock Output Interface - OUT0 (similar for OUT1-OUT7)

3.7 Status Outputs and LEDs

Status outputs pins can be enabled on GPIO5, GPIO6, STATUS0, and STATUS1. The status output signal, output type (3.3-V LVCMOS or NMOS open-drain), and output polarity are register programmable. The output states for these pins (and other logic pins) can be probed at location J5.

GPIO5, GPIO6, STATUS0, and STATUS1 outputs drive the orange LEDs D8, D9, D12, and D13, respectively, for visual indication. The LED will turn ON when the status output is logic 1 (active high).

4 EVM Schematics

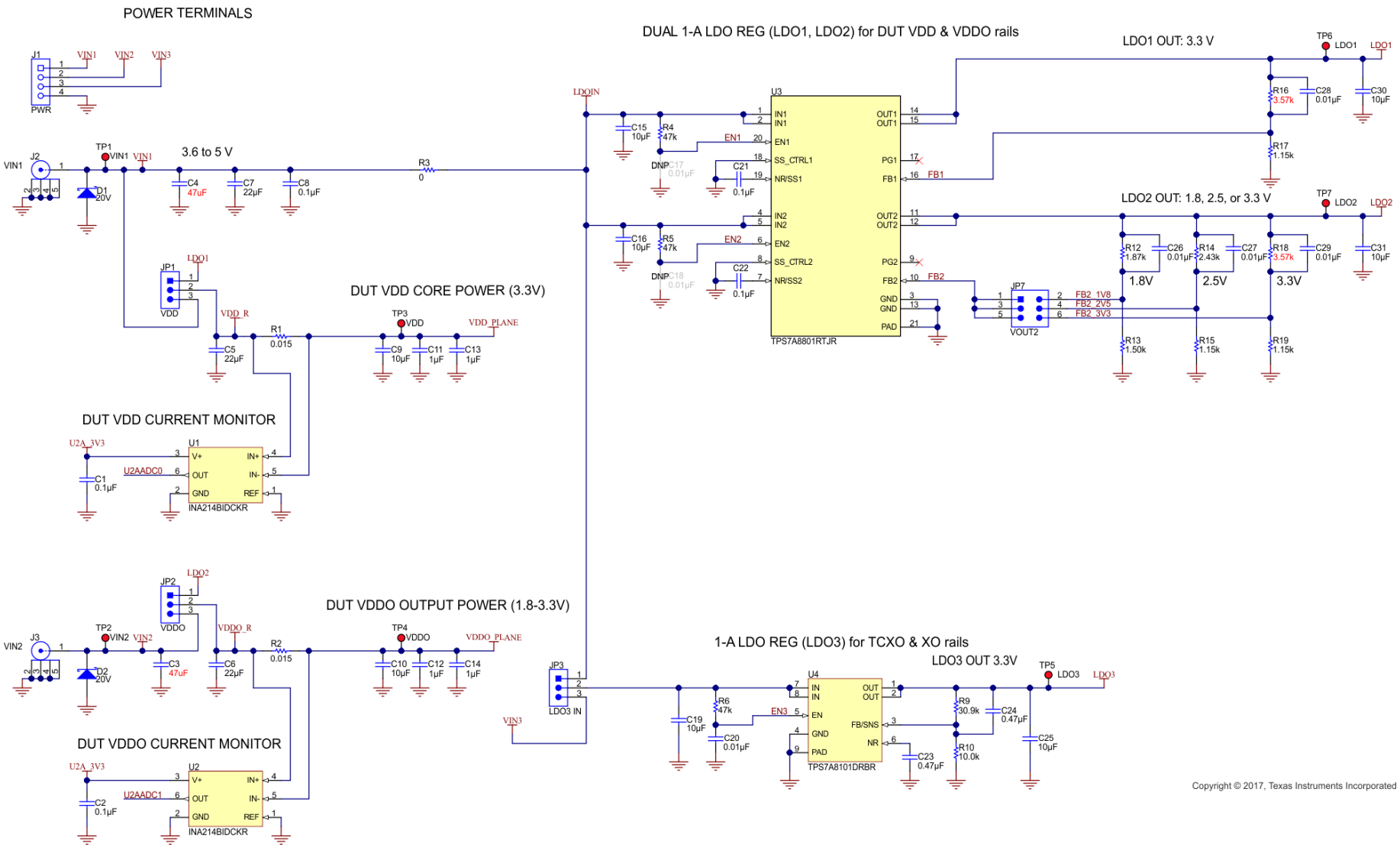

Figure 10. Schematic 1 - Power Supplies

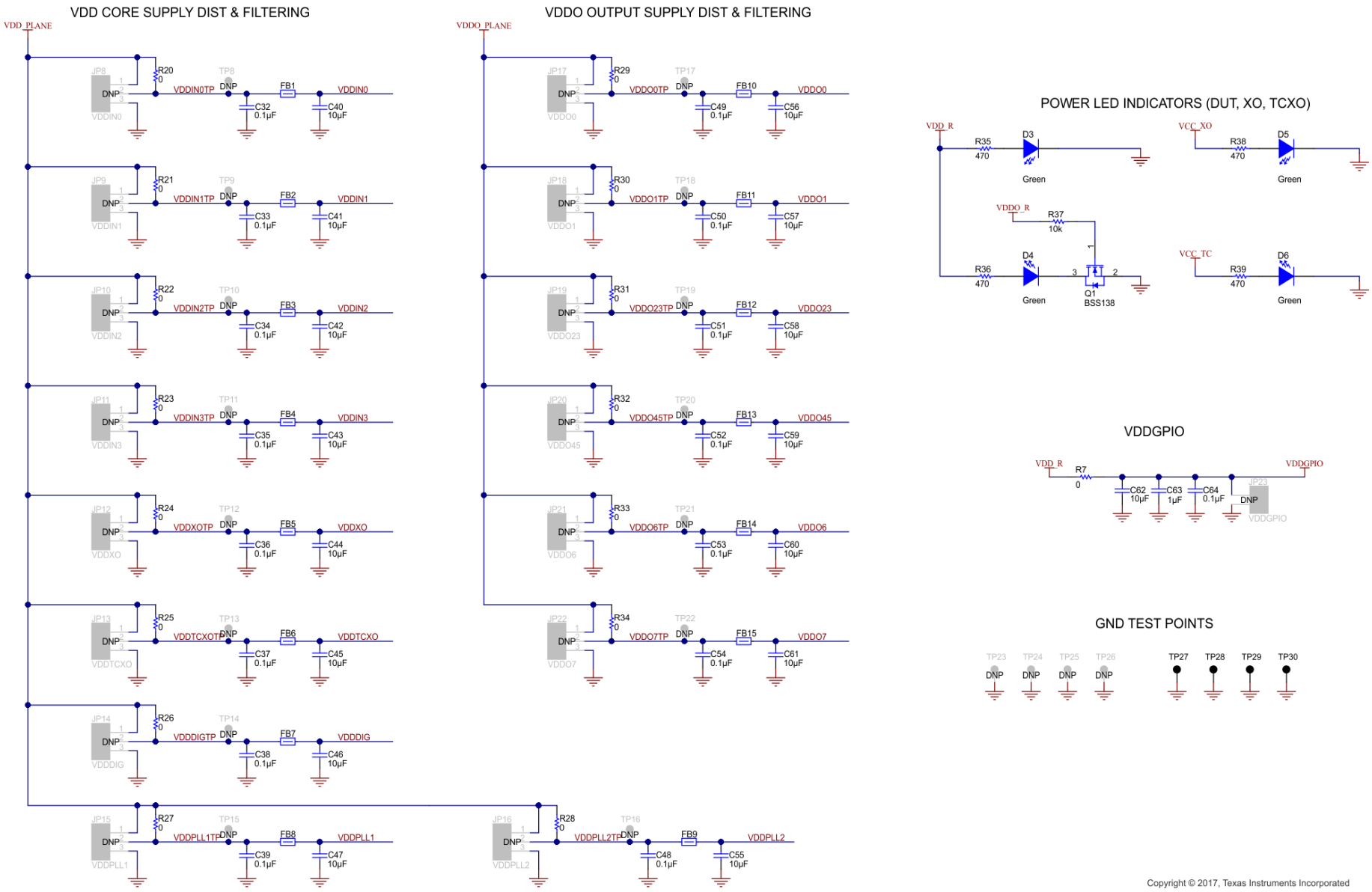

Figure 11. Schematic 2 - Power Distribution

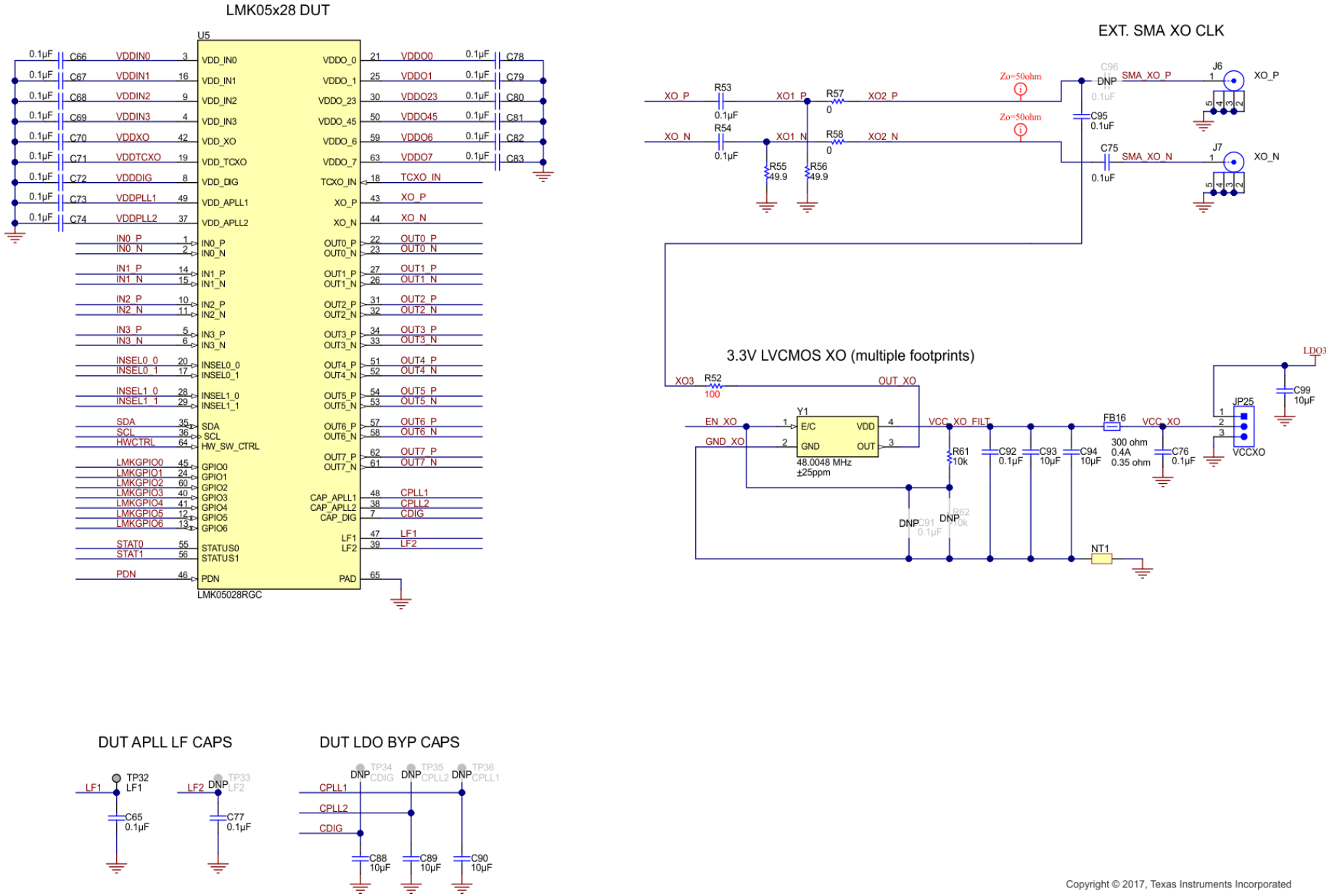

Figure 12. Schematic 3 - LMK05028 and XO Input Interfaces

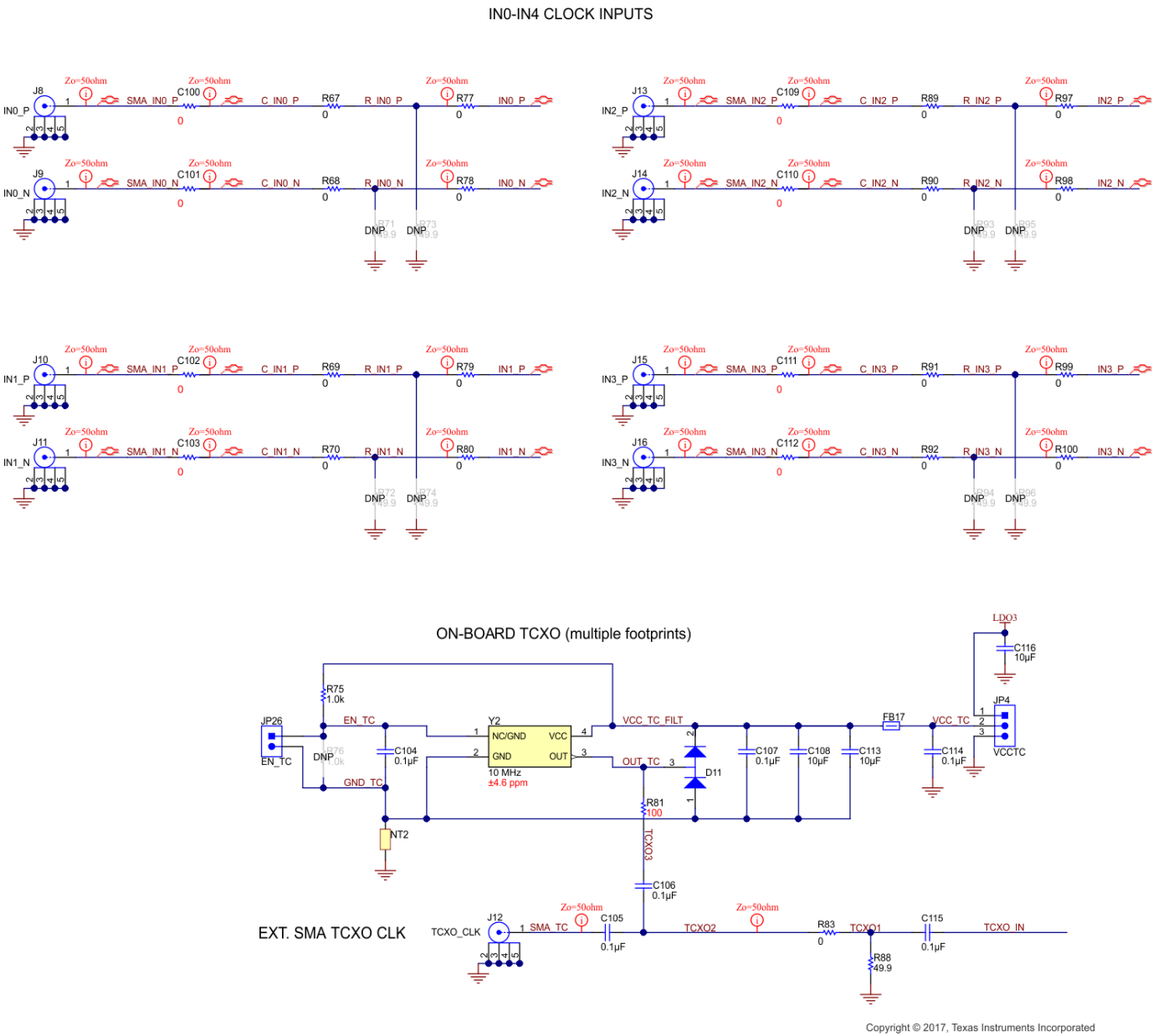

Figure 13. Schematic 4 - Clock Input and TCXO Input Interfaces

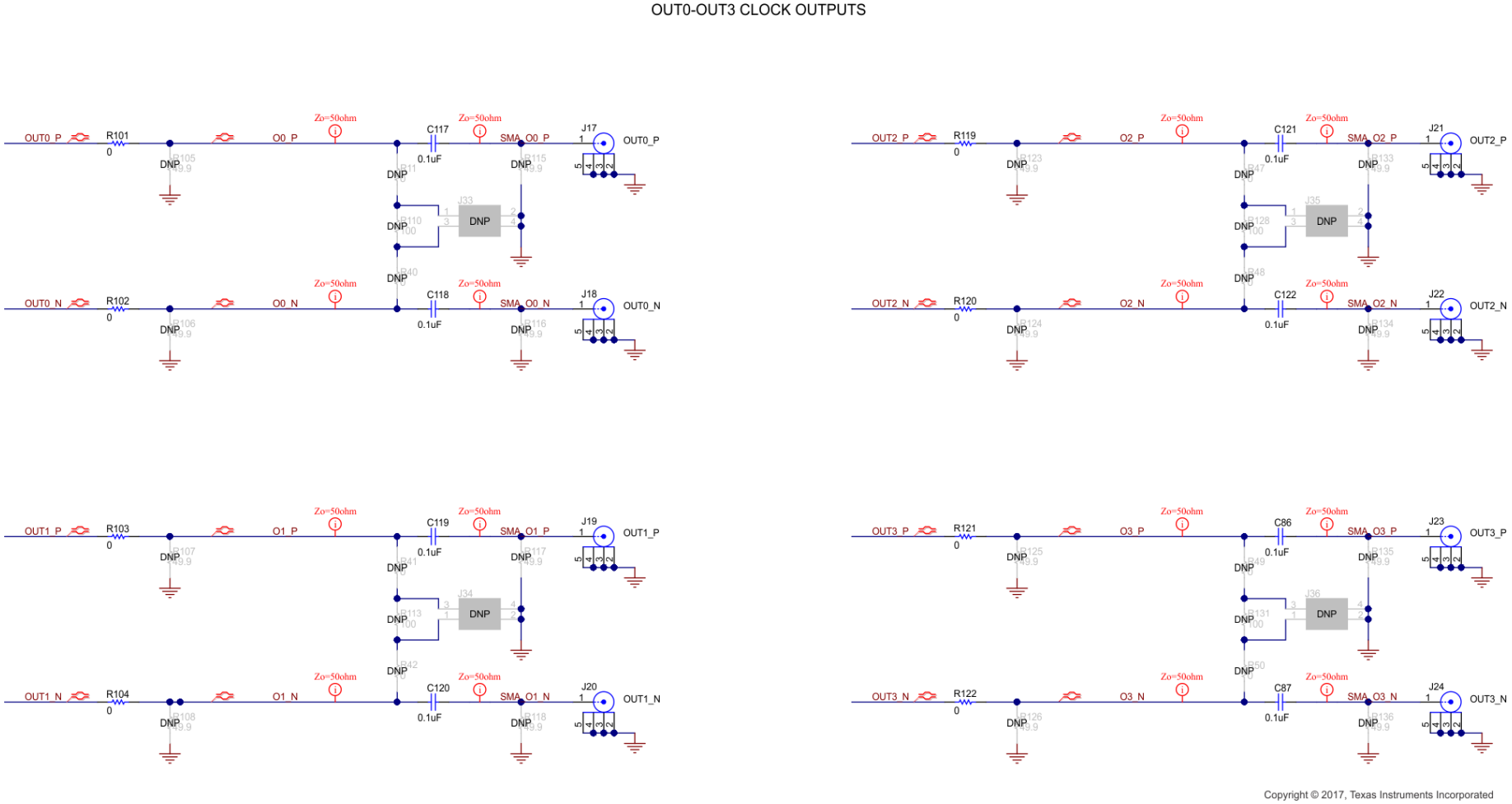

Figure 14. Schematic 5 - Clock Output Interfaces (OUT0 to OUT3)

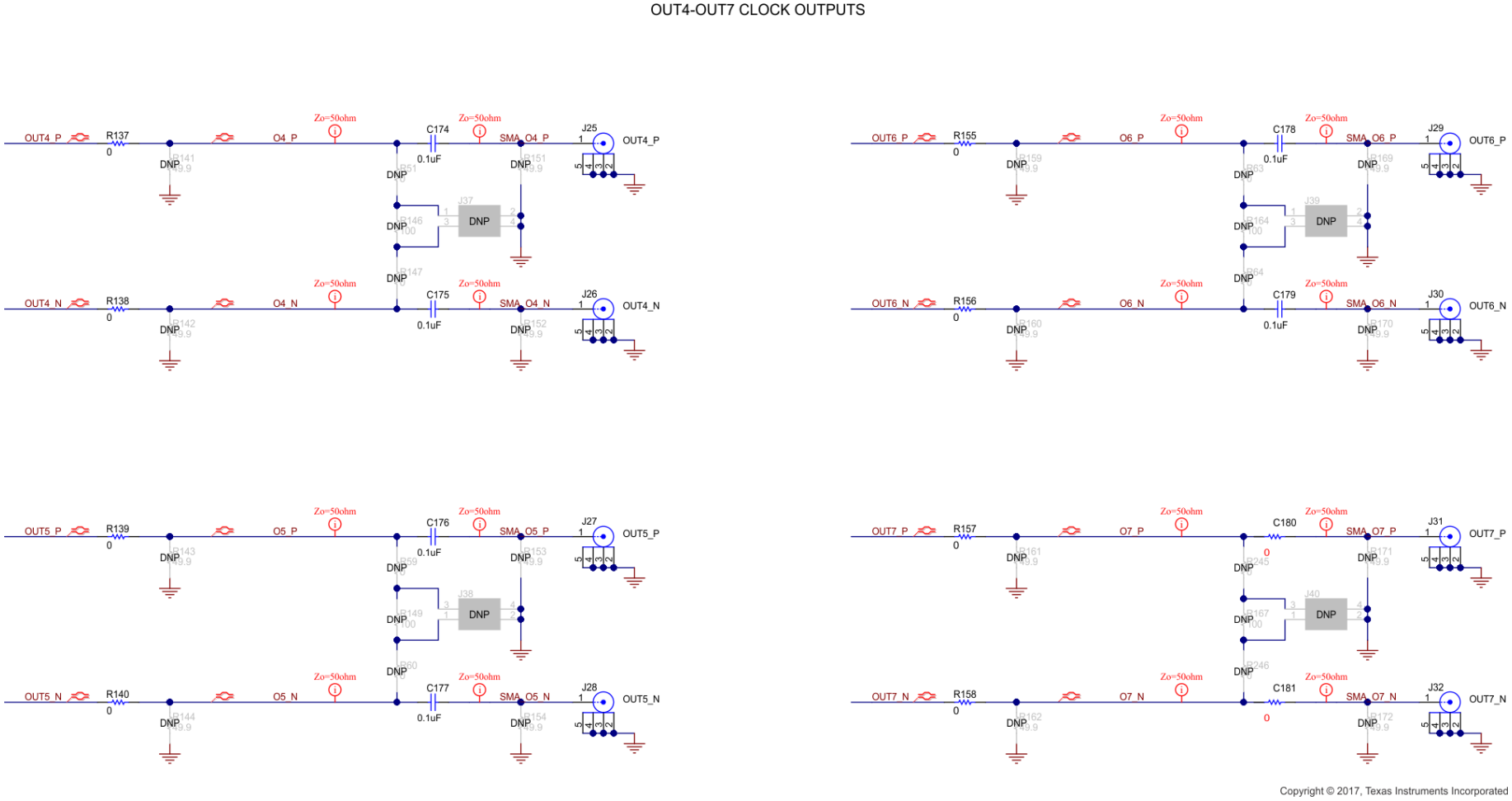

Figure 15. Schematic 6 - Clock Outputs (OUT4 to OUT7)

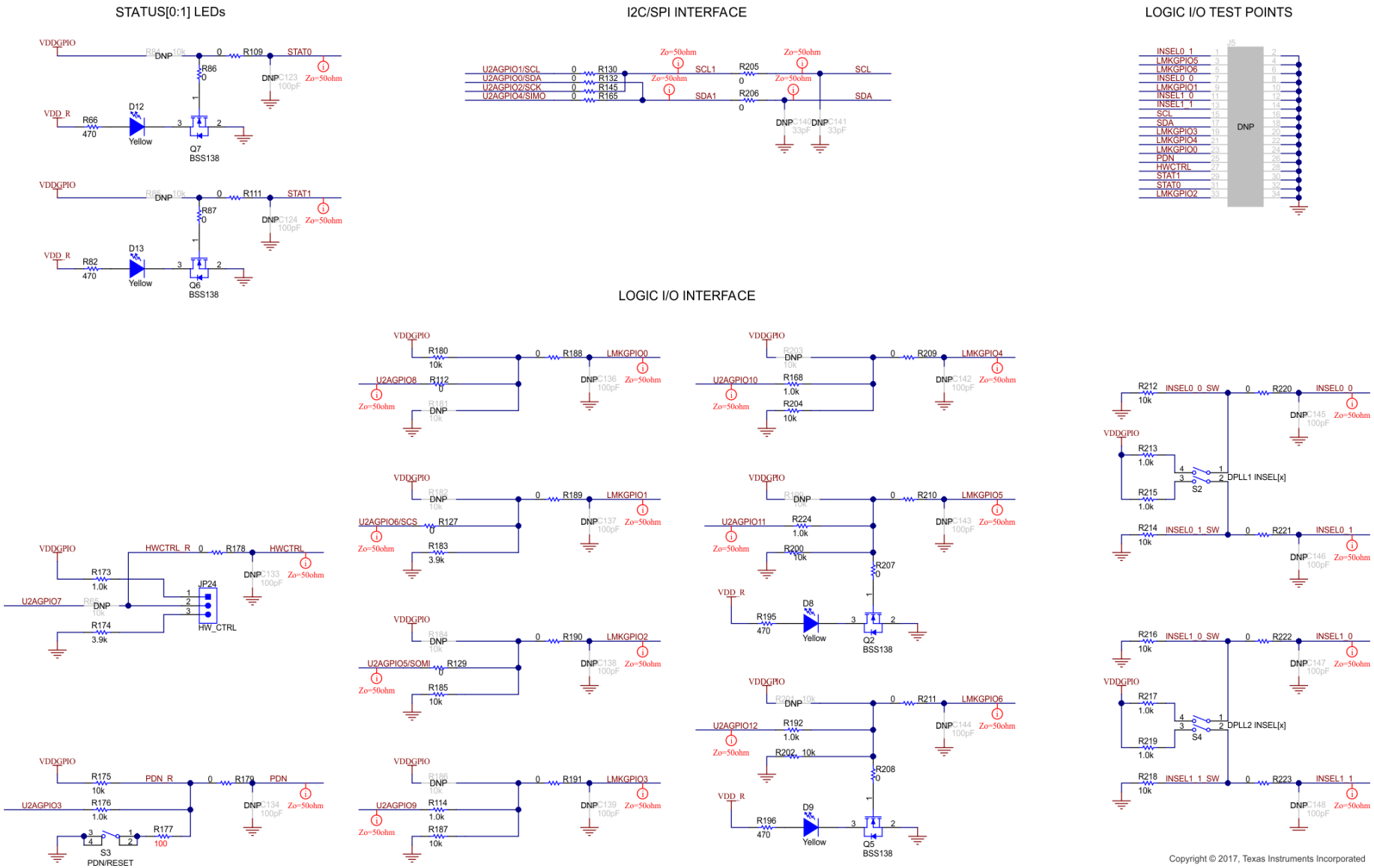

Figure 16. Schematic 7 - Logic I/O Interfaces

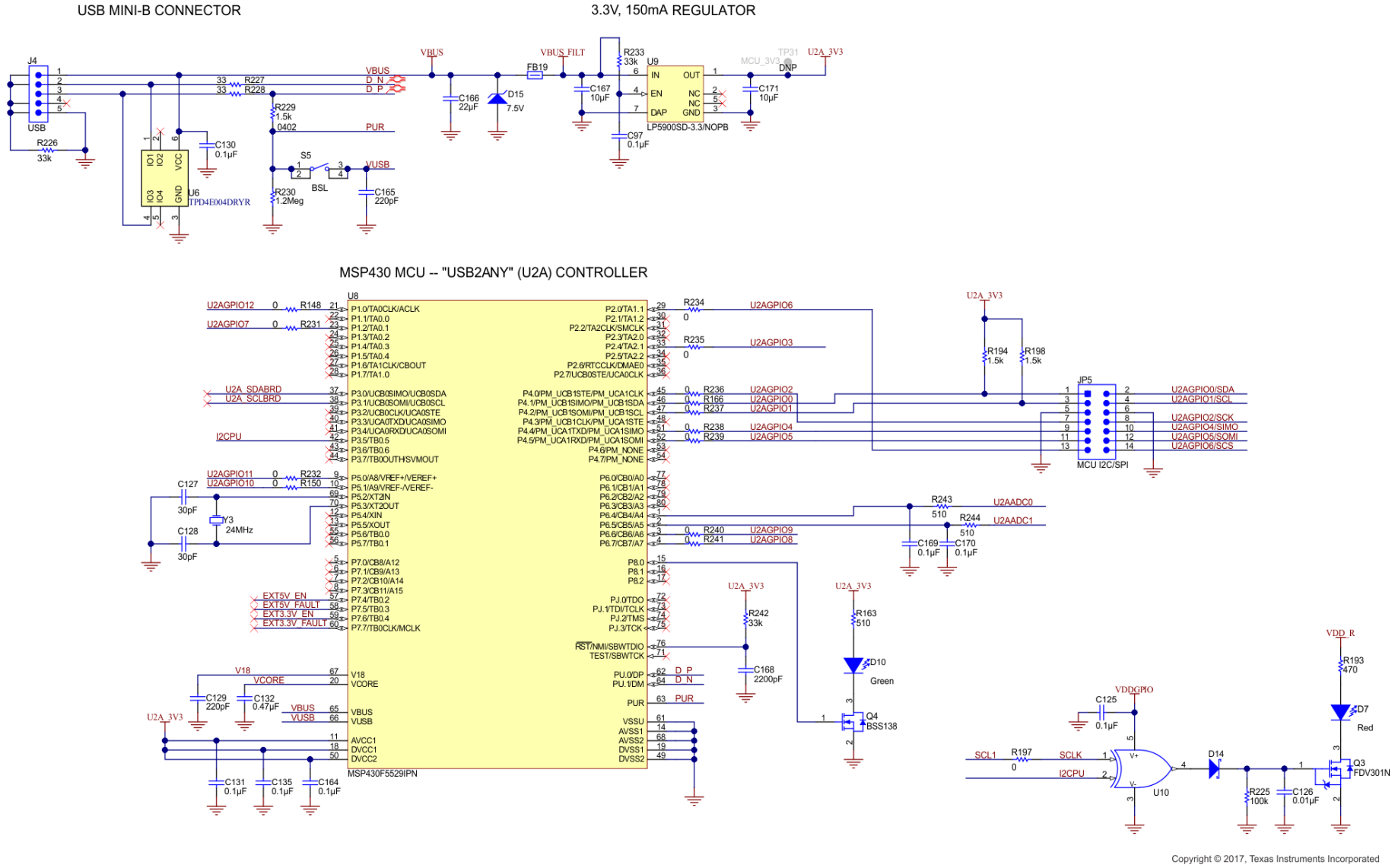

Figure 17. Schematic 8 - USB MCU and I2C/SPI Jumper Block

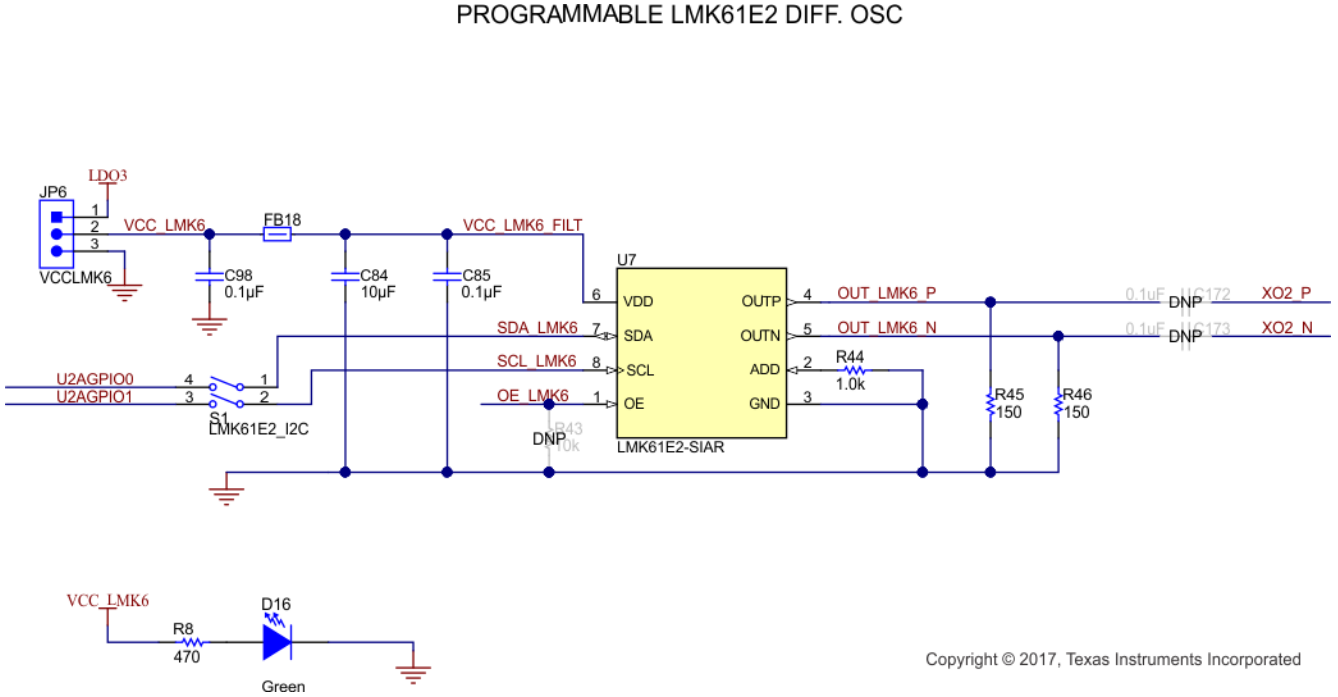

Figure 18. Schematic 9 - LMK61E2 Oscillator

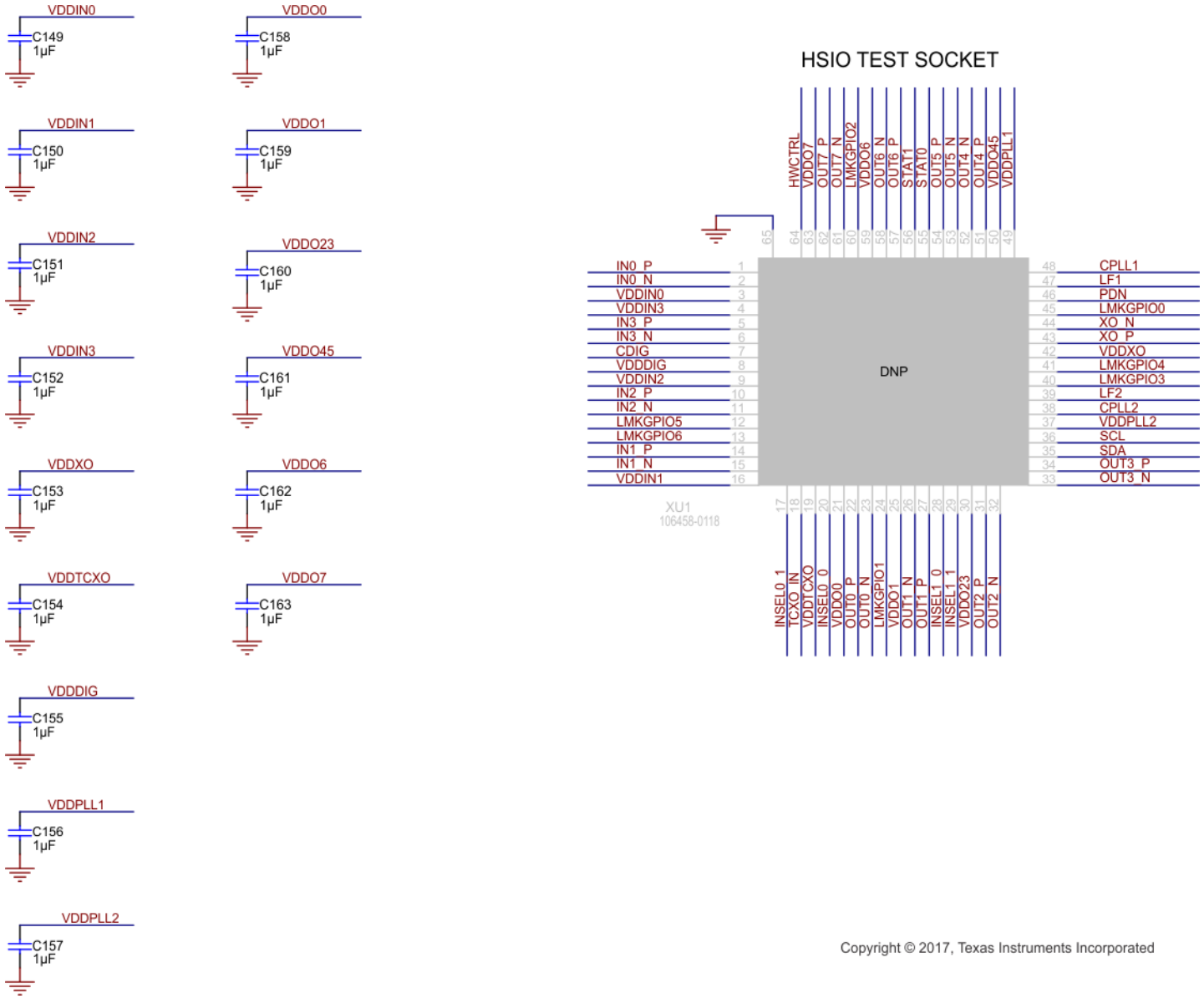

Figure 19. Schematic 10 - DUT Test Socket

5 EVM Layouts

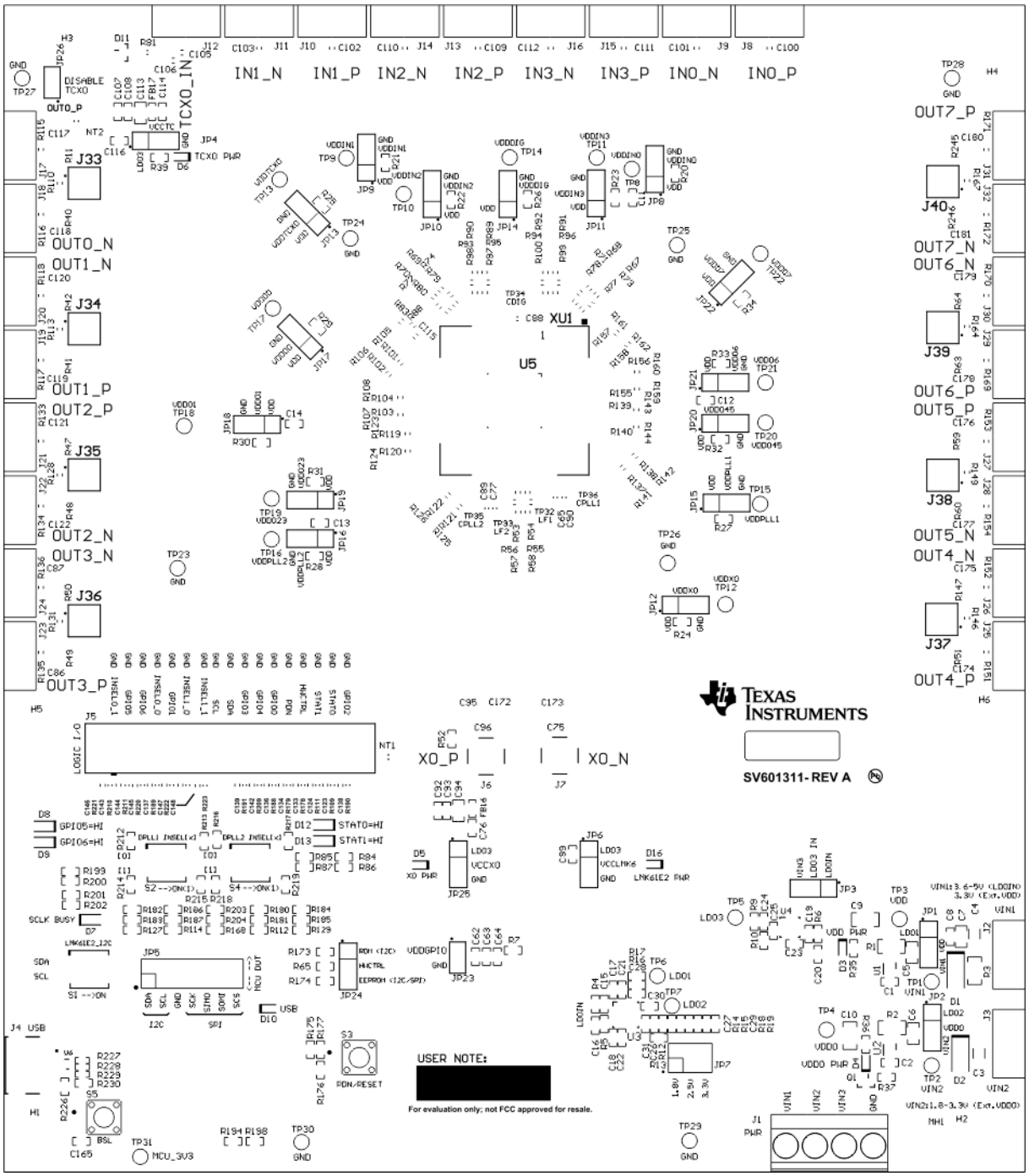

Figure 20. Top Overlay

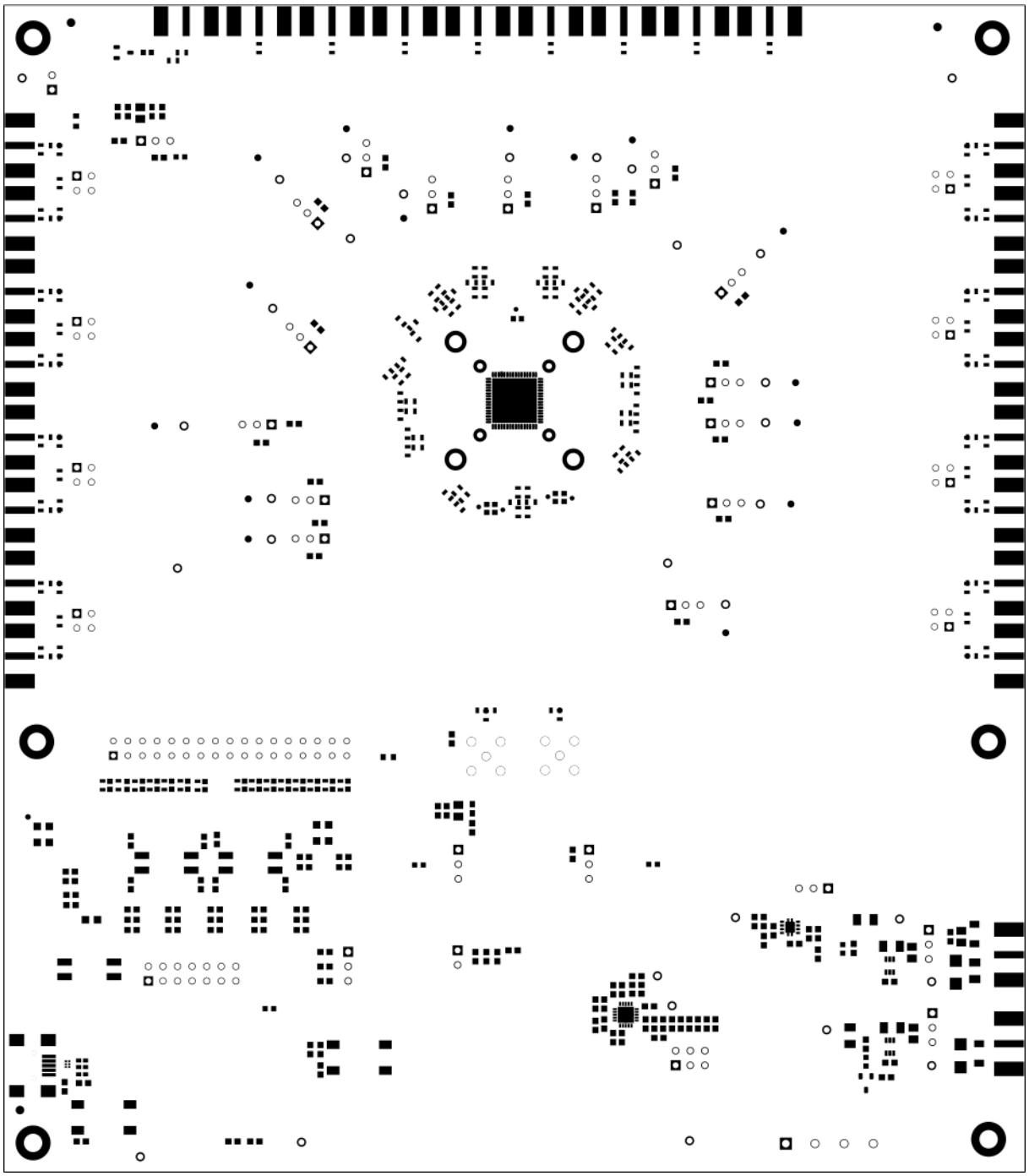

Figure 21. Top Solder Mask

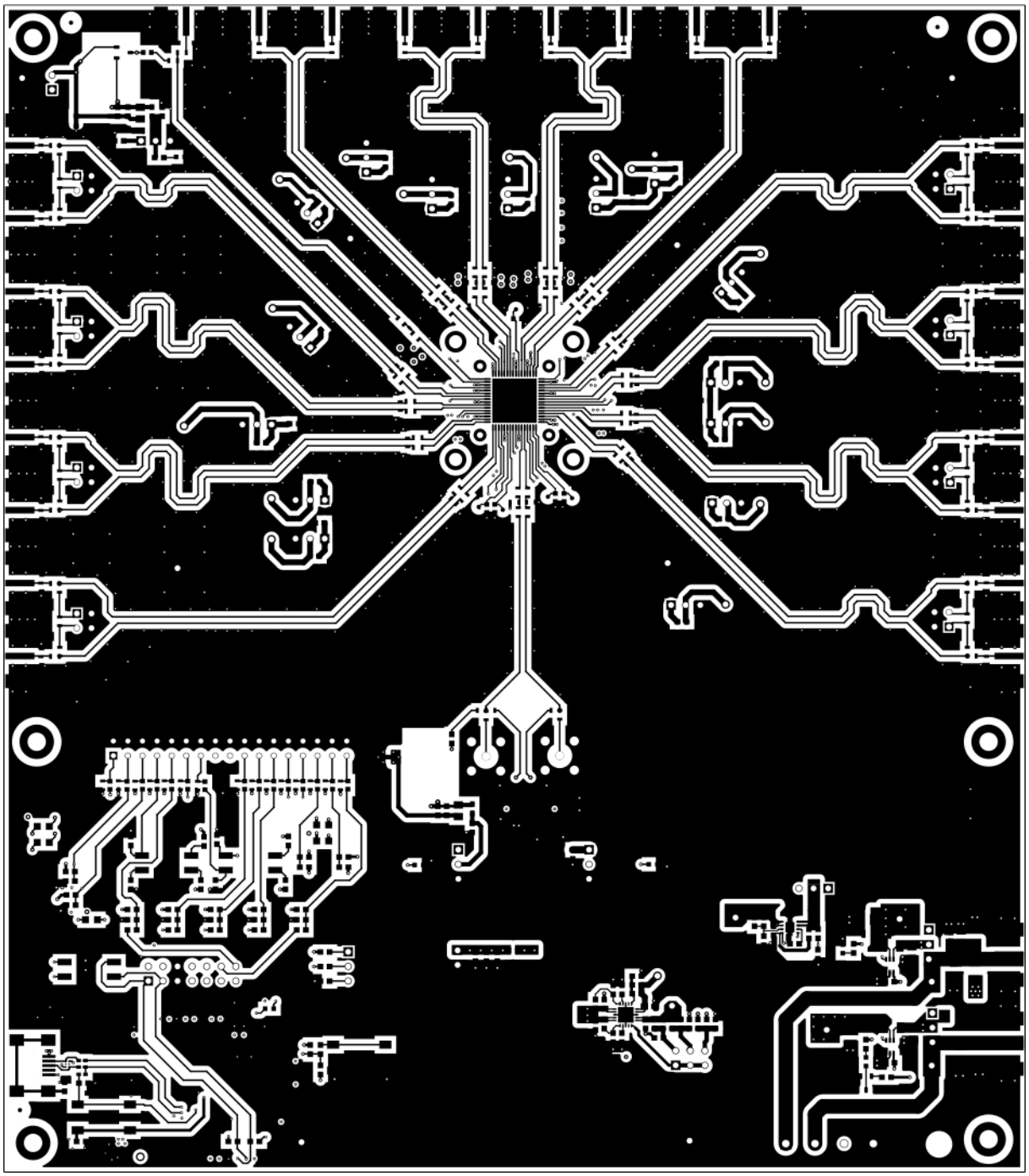

Figure 22. Layer 1 (Top Side) - Clock I/Os, Logic, and Power Routing, Ground Fill

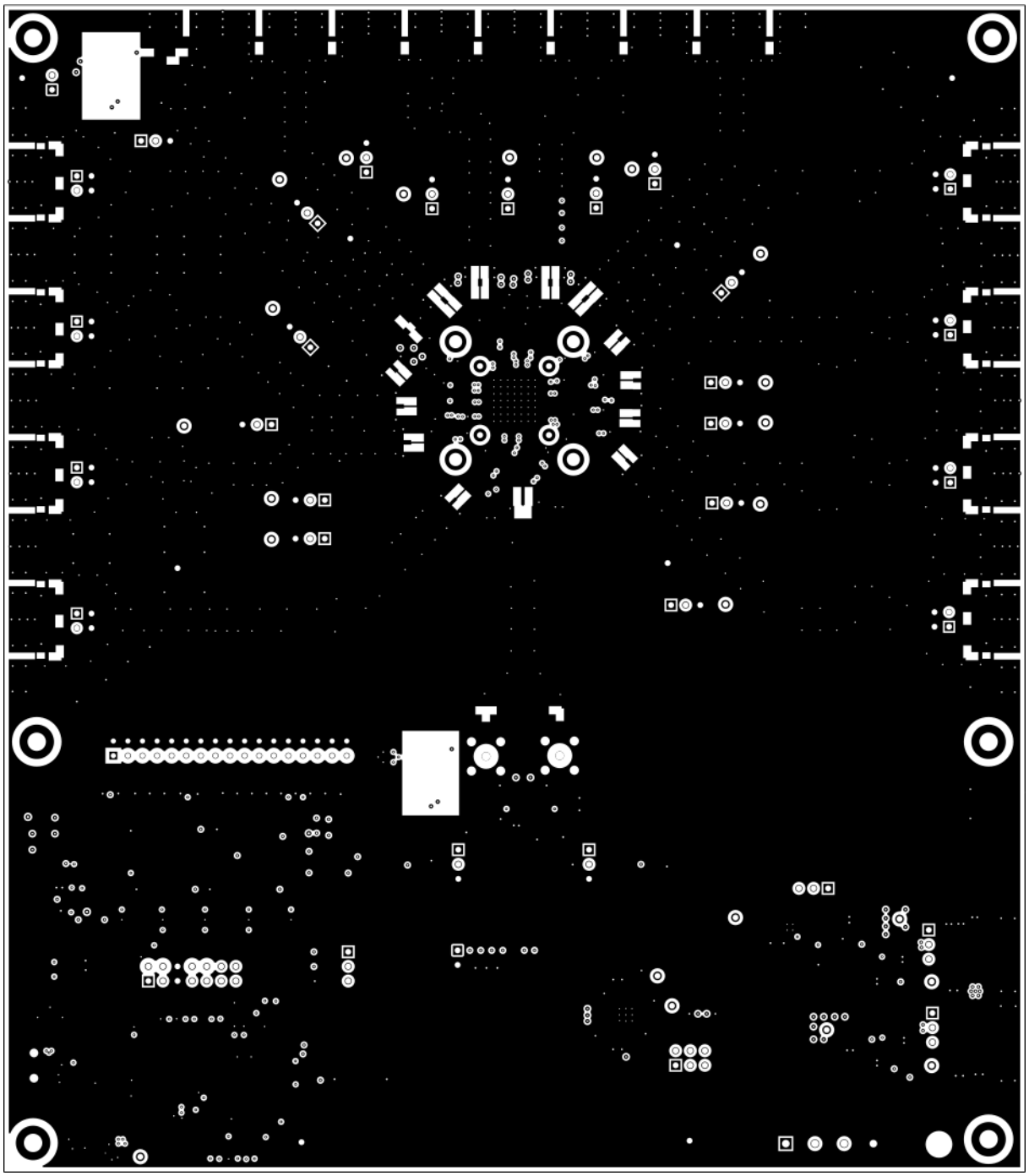

Figure 23. Layer 2 - Ground Plane

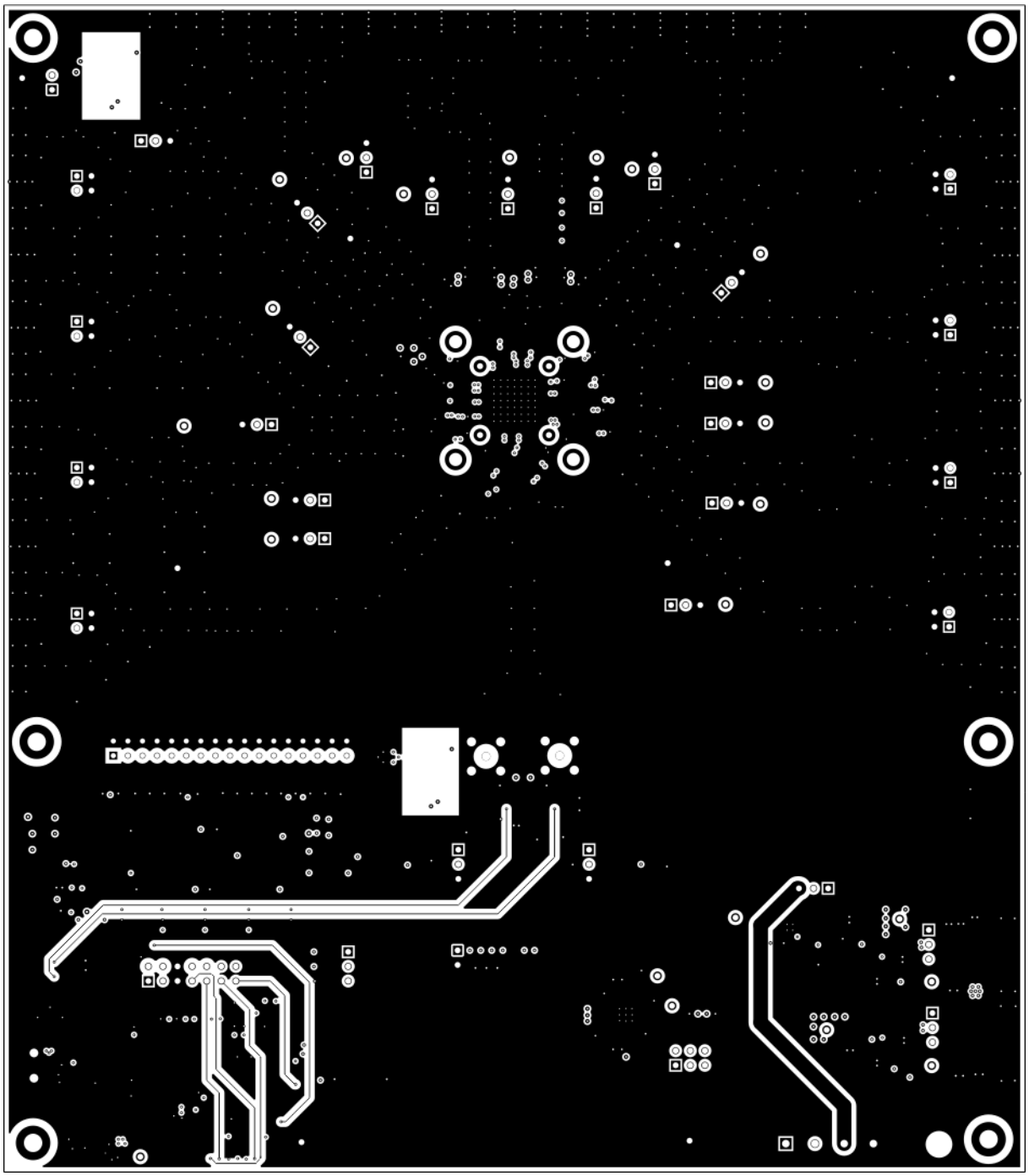

Figure 24. Layer 3 - Logic Routing, Ground Fill

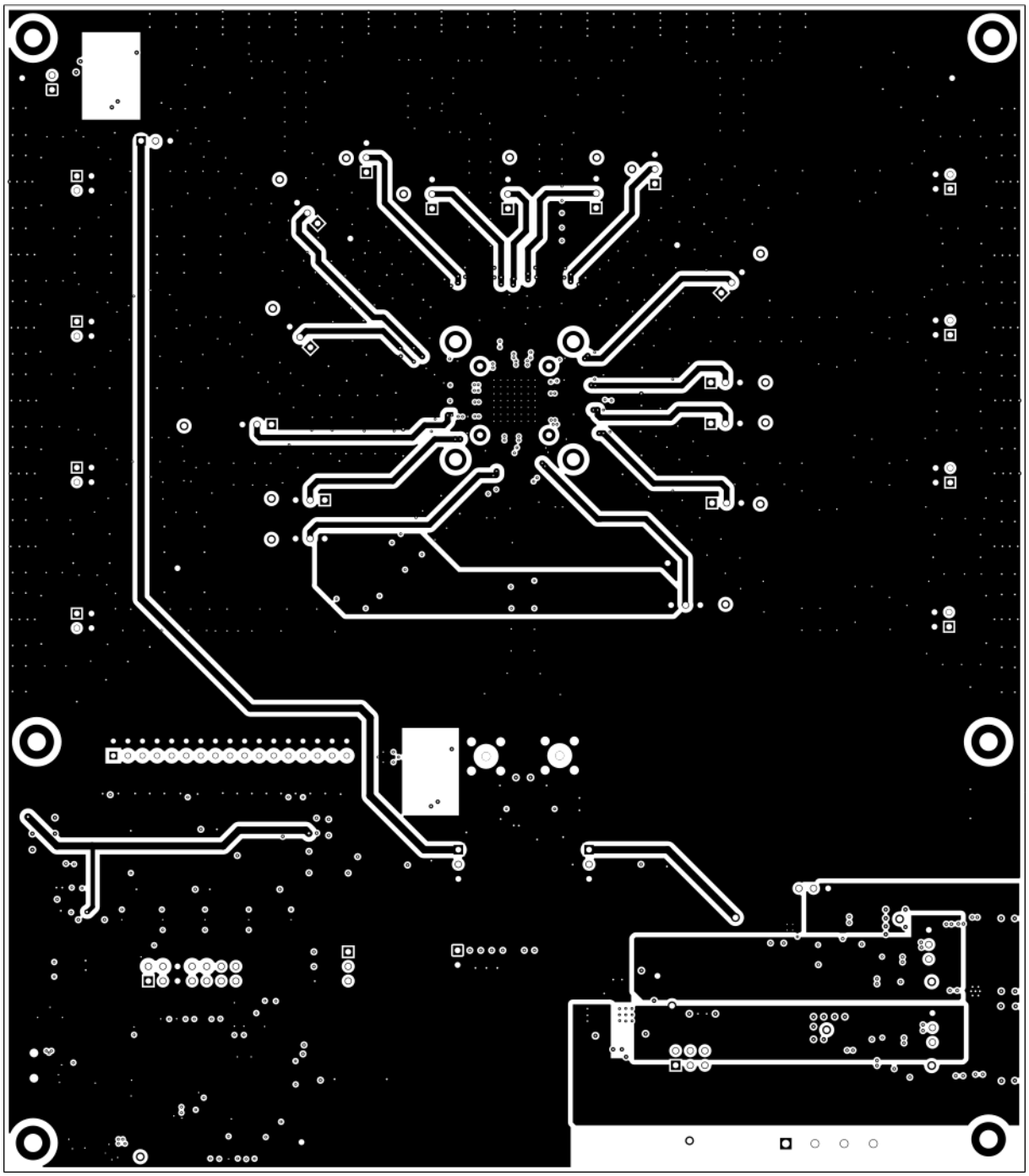

Figure 25. Layer 4 - Power Routing, Ground Fill

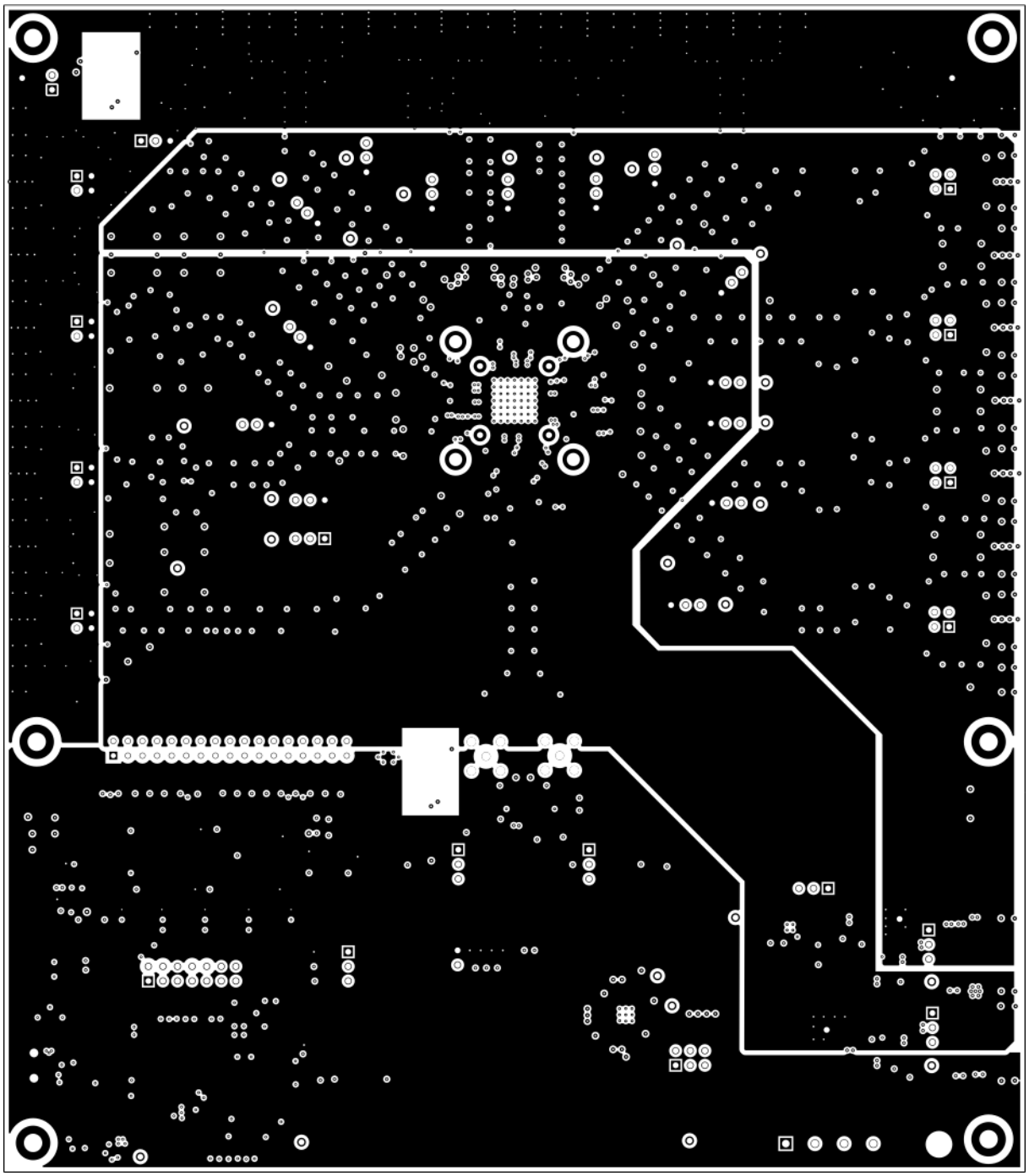

Figure 26. Layer 5 - Power and Ground Planes

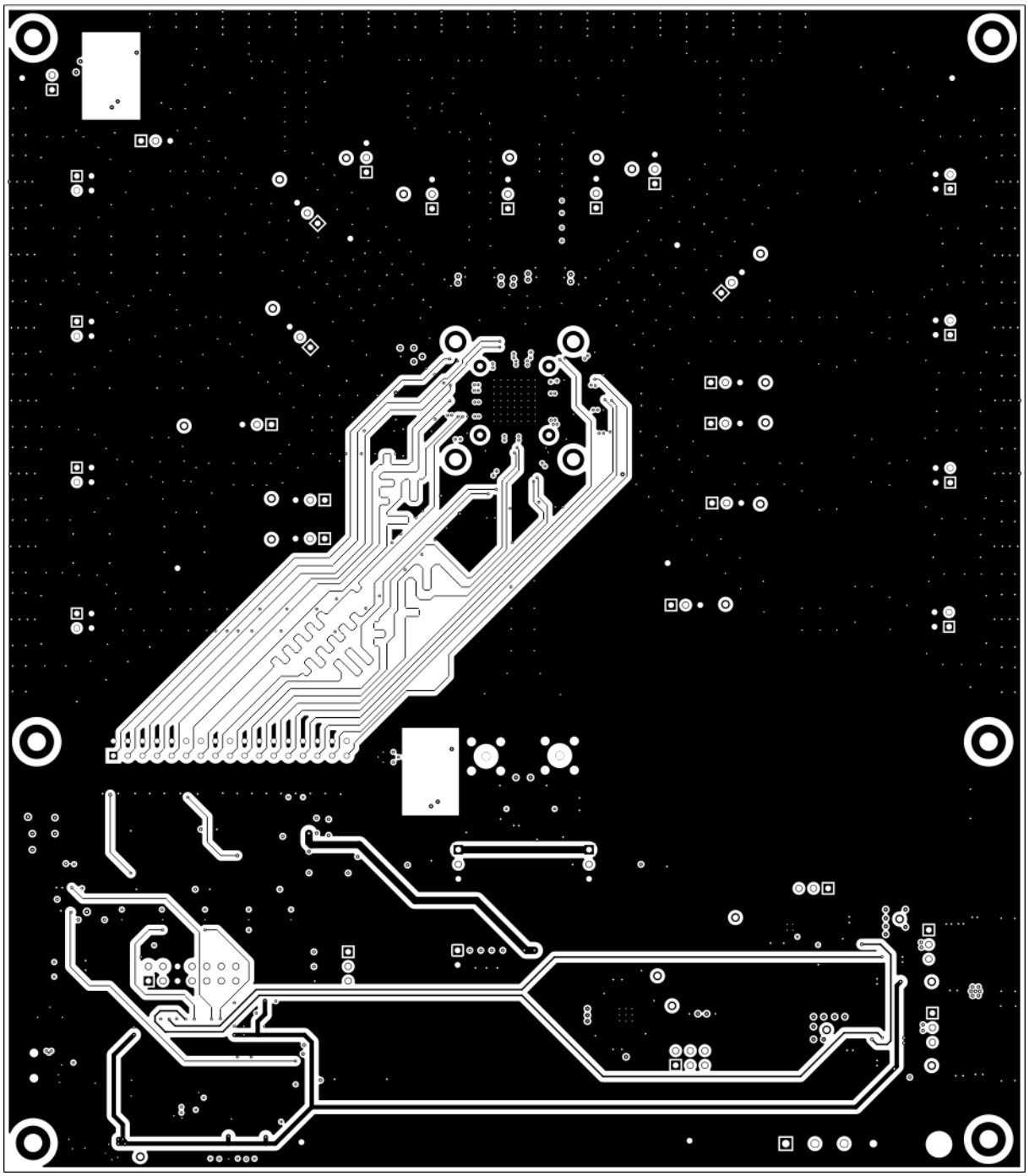

Figure 27. Layer 6 - Logic Routing, Ground Fill

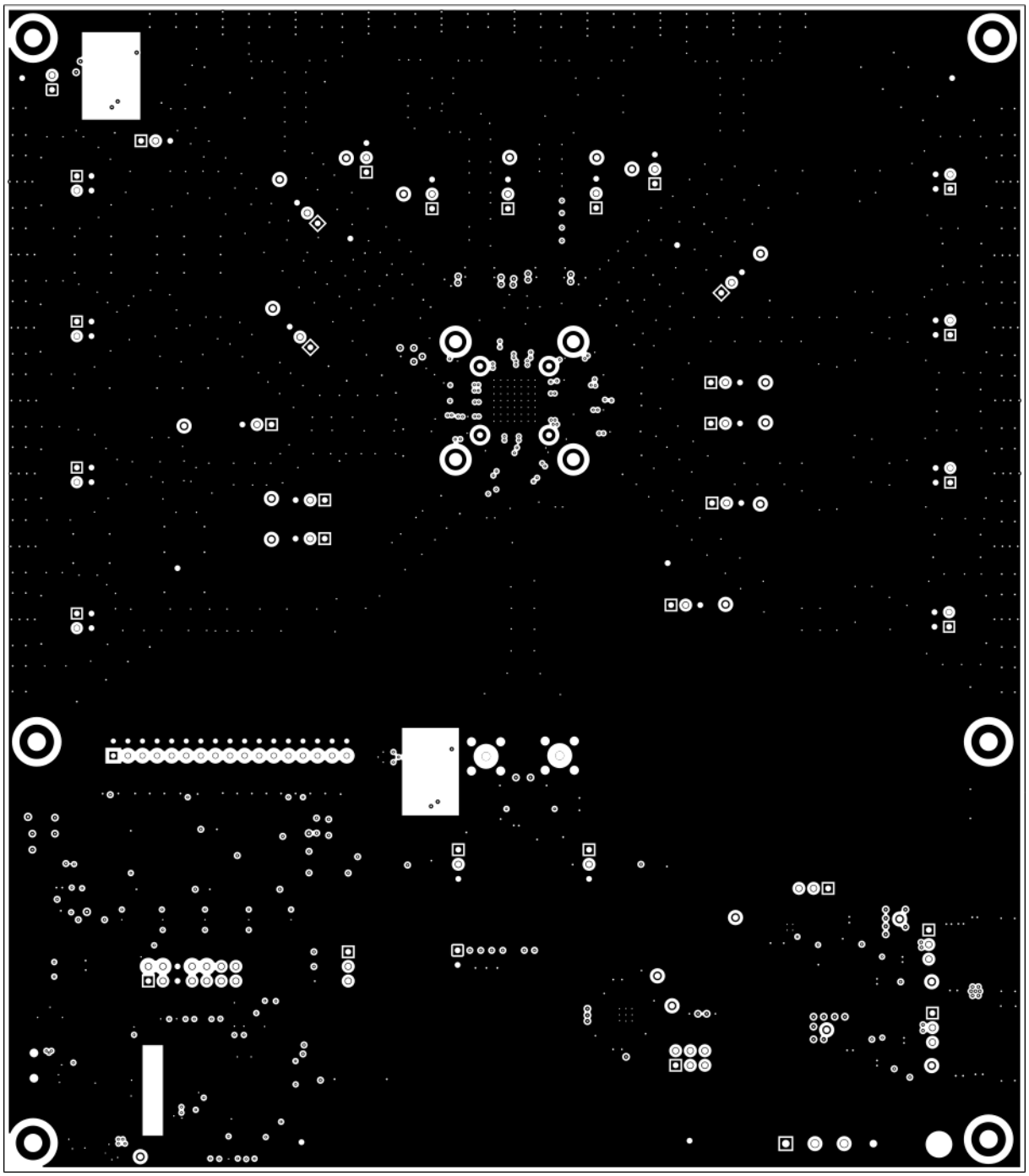

Figure 28. Layer 7 - Ground Plane

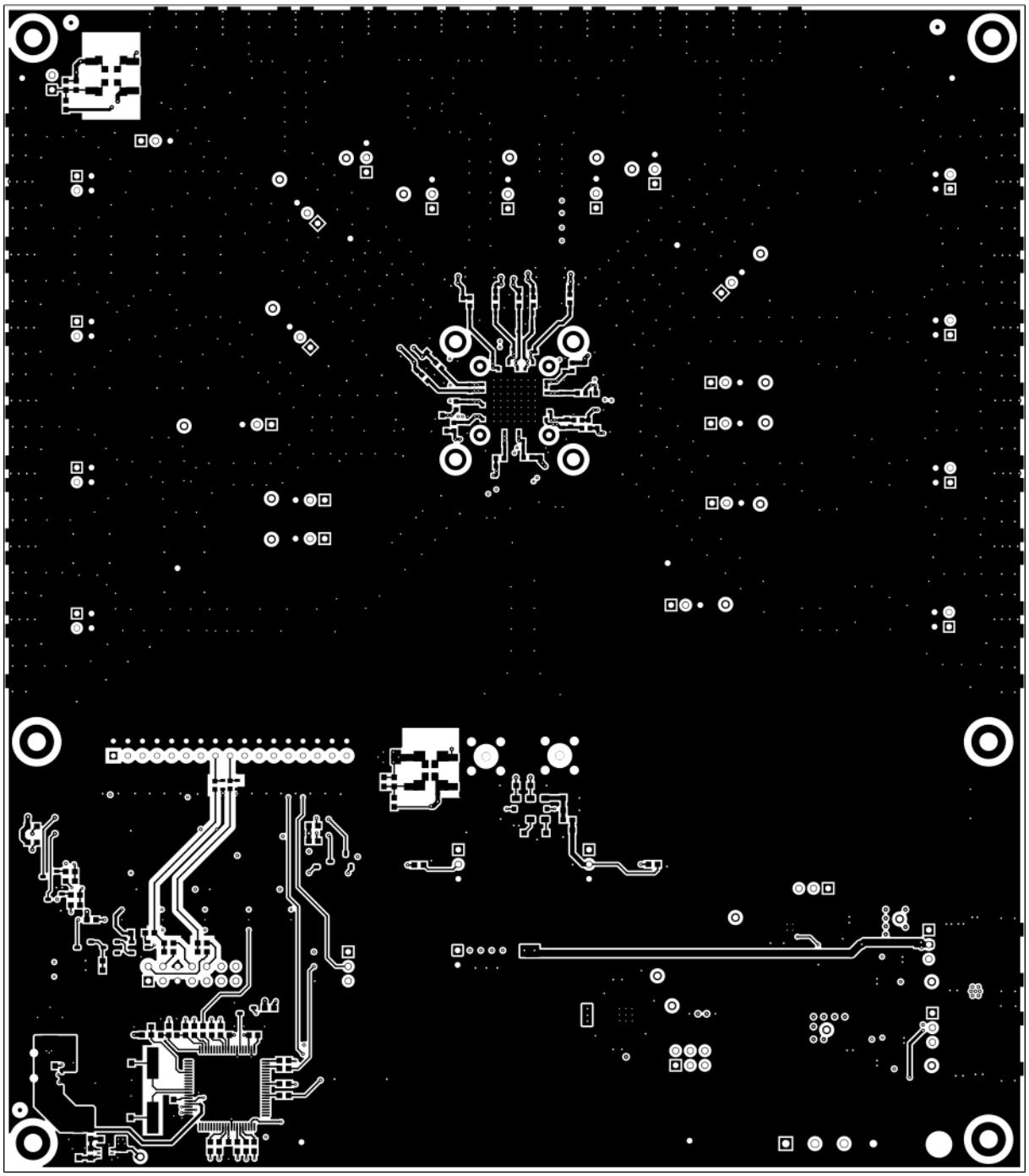

Figure 29. Layer 8 (Bottom Side, View From Top) - Logic and Power Routing, Ground Fill

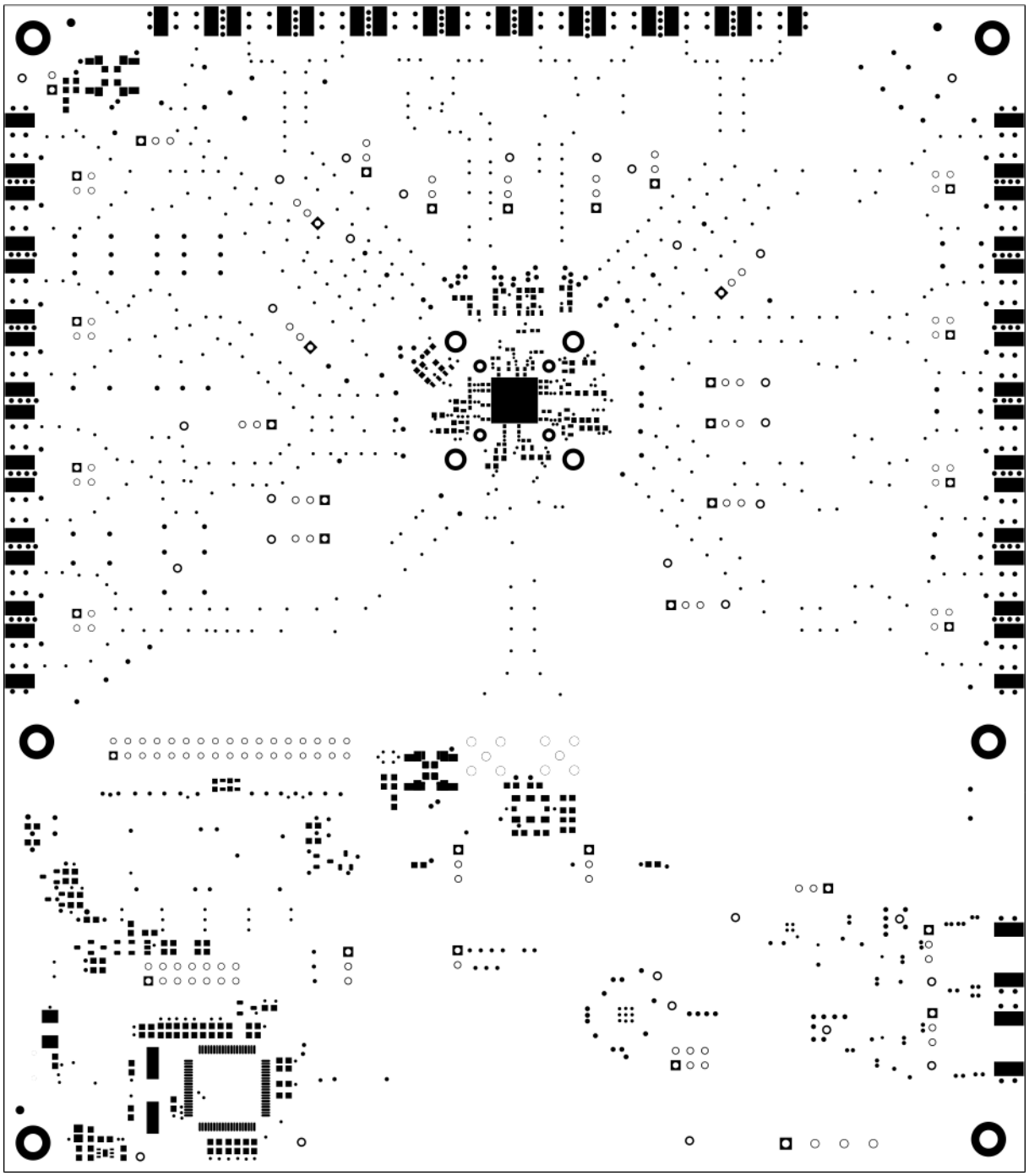

Figure 30. Bottom Solder Mask

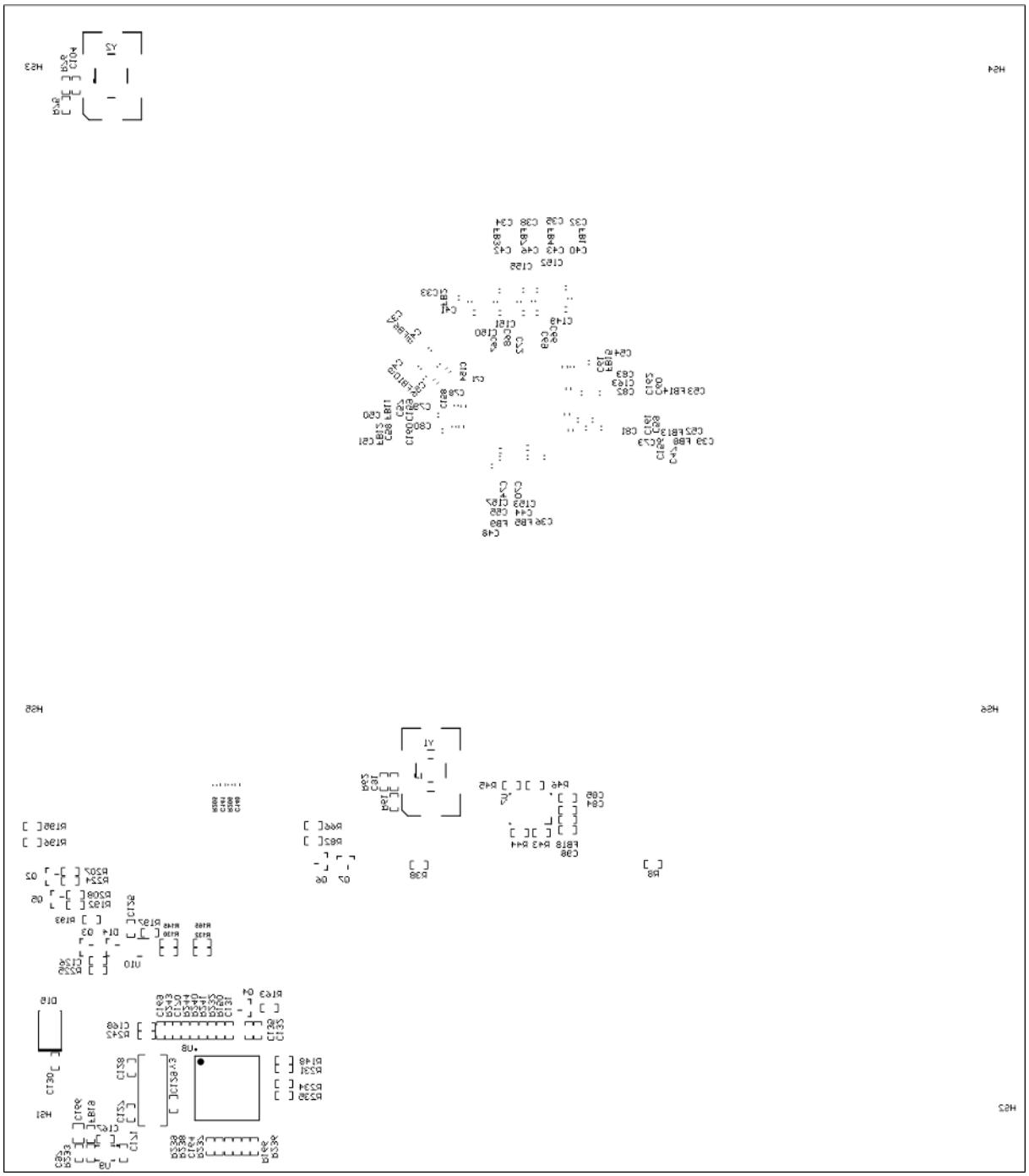

Figure 31. Bottom Overlay

6 EVM Bill of Materials

Table 9 lists the bill of materials.

Table 9. Bill of Materials

REF DES	DESCRIPTION	MFR	PART NUMBER	QTY
!PCB1	Printed Circuit Board	Any	SV601311	1
C1, C2, C8, C97, C125, C130, C131, C135, C164, C169, C170	CAP, CERM, 0.1uF, 16 V, + /- 5%, X7R, 0603	Kemet	C0603C104 J4RACTU	11
C3, C4	CAP, CERM, 47 uF, 10 V, + /- 10%, X5R, AEC-Q200 Grade 1, 1206	MuRata	GRT31CR61A476KE13 L	2
C5, C6, C7	CAP, CERM, 22 µF, 10 V, + /- 20%, X5R, 0805	Taiyo Yuden	LMK212BJ226MG-T	3
C9, C10	CAP, CERM, 10 µF, 10 V, + /- 20%, X7R, 1206	TDK	C3216X7R1A106M160AC	2
C11, C12, C13, C14, C63	CAP, CERM, 1uF, 10 V, + /- 10%, X5R, 0603	Kemet	C0603C105K8PACTU	5
C15, C16, C19, C25, C30, C31, C40, C41, C42, C43, C44, C45, C46, C47, C55, C56, C57, C58, C59, C60, C61, C62, C84, C88, C89, C90, C93, C99, C108, C116	CAP, CERM, 10 µF, 10 V, + /- 20%, X5R, 0603	TDK	C1608X5R1A106M080AC	30
C20, C26, C27, C28, C29	CAP, CERM, 0.01 µF, 50 V, + /- 5%, X7R, 0603	Kemet	C0603C103 J5RACTU	5
C21, C22, C32, C33, C34, C35, C36, C37, C38, C39, C48, C49, C50, C51, C52, C53, C54, C64, C65, C77, R53, R54	CAP, CERM, 0.1 µF, 25 V, + /- 5%, X7R, 0603	Kemet	C0603C104 J3RACTU	22
C23, C24	CAP, CERM, 0.47 µF, 10 V, + /- 10%, X7R, 0603	Kemet	C0603C474K8RACTU	2
C66, C67, C68, C69, C70, C71, C72, C73, C74, C78, C79, C80, C81, C82, C83	CAP, CERM, 0.1 µF, 10 V, + /- 10%, X5R, 0402	TDK	C1005X5R1A104K050BA	15
C75	CAP, CERM, 0.1 uF, 25 V, + /- 5%, X7R, 0603 S	Kemet	C0603C104 J3RACTU	1
C76, C85, C92, C98, C104, C105, C106, C107, C114, C115	CAP, CERM, 0.1uF, 25 V, + /- 5%, X7R, 0603	Kemet	C0603C104 J3RACTU	10
C86, C87, C95, C117, C118, C119, C120, C121, C122, C174, C175, C176, C177, C178, C179	CAP, CERM, 0.1 uF, 25 V, + /- 5%, X7R, 0603	Kemet	C0603C104 J3RACTU	15
C94, C113	CAP, CERM, 10 µF, 10 V, + /- 10%, X5R, 0805	Taiyo Yuden	LMK212BJ106KG-T	2
C100, C101, C102, C103, C109, C110, C111, C112, R7, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R86, R87, R101, R102, R103, R104, R109, R111, R112, R119, R120, R121, R122, R127, R129, R130, R132, R137, R138, R139, R140, R145, R155, R156, R157, R158, R165, R178, R179, R188, R189, R190, R191, R197, R205, R206, R207, R208, R209, R210, R211, R220, R221, R222, R223	RES, 0, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06030000Z0EA	69

Table 9. Bill of Materials (continued)

REF DES	DESCRIPTION	MFR	PART NUMBER	QTY
C126	CAP, CERM, 0.01 µF, 50 V, + /- 5%, X7R, 0603	Kemet	C0603C103 J5RACTU	1
C127, C128	CAP, CERM, 30 pF, 100 V, + /-5%, C0 G/NP0, 0603	MuRata	GRM1885C2A300 JA01D	2
C129, C165	CAP, CERM, 220 pF, 50 V, + /-1%, C0 G/NP0, 0603	AVX	06035A221FAT2A	2
C132	CAP, CERM, 0.47uF, 10 V, + /-10%, X7R, 0603	MuRata	GRM188R71A474KA61D	1
C149, C150, C151, C152, C153, C154, C155, C156, C157, C158, C159, C160, C161, C162, C163	CAP, CERM, 1 µF, 10 V, + /-10%, X5R, 0402	MuRata	GRM155R61A105KE15D	15
C166	CAP, CERM, 22uF, 10 V, + /-20%, X5R, 0805	Taiyo Yuden	LMK212BJ226MG-T	1
C167, C171	CAP, CERM, 10 µF, 10 V, + /-20%, X5R, 0603	TDK	C1608X5R1A106M080AC	2
C168	CAP, CERM, 2200 pF, 50 V, + /-10%, X7R, 0603	Kemet	C0603C222K5RACTU	1
C180, C181	RES, 0, 5%, 0.1 W, 0603 S	Vishay-Dale	CRCW06030000Z0EA	2
D1, D2	Diode, Schottky, 20 V, 2A, SMA	Diodes Inc.	B220A-13-F	2
D3, D4, D5, D6, D10, D16	LED, Green, SMD	Lite-On	LTST-C190 GKT	6
D7	LED, Red, SMD	Lite-On	LTST-C170KRKT	1
D8, D9, D12, D13	LED, Yellow , SMD	Lite-On	LTST-C170KSKT	4
D11	Diode, Switching, 100 V, 0.2 A, SOT-23	ON Semiconductor	MMBD7000 LT1 G	1
D14	Diode, Schottky, 30 V, 0.2 A, SOT-23	Diodes Inc.	BAT54-7-F	1
D15	Diode, Zener, 7.5 V, 550 mW, SMB	ON Semiconductor	1 SMB5922BT3 G	1
FB1, FB2, FB3, FB4, FB5, FB6, FB7, FB8, FB9, FB10, FB11, FB12, FB13, FB14, FB15	Ferrite Bead, 220 ohm @ 100 MHz, 2.5 A, 0603	MuRata	BLM18 SG221 TN1D	15
FB16, FB17, FB18	Ferrite Bead, 300 ohm @ 100 MHz, 0.4 A, 1.6x0.8x0.95 mm	Laird-Signal Integrity Products	LI0603D301R-10	3
FB19	Ferrite Bead, 60 ohm @ 100 MHz, 3.5 A, 0603	TDK	MPZ1608 S600ATAH0	1
H1, H2, H3, H4, H5, H6	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	B&F Fastener Supply	NY PMS 440 0025 PH	6
HS1, HS2, HS3, HS4, HS5, HS6	Standoff, Hex, 0.5"L #4-40 Nylon	Keystone	1902C	6
J1	Terminal Block, 4x1, 5.08 mm, TH	Molex	39544-3004	1
J2, J3, J8, J9, J10, J11, J12, J13, J14, J15, J16, J17, J18, J19, J20, J21, J22, J23, J24, J25, J26, J27, J28, J29, J30, J31, J32	Connector, End launch SMA, 50 ohm, SMT	Emerson Network Power	142-0701-851	27
J4	Connector, Receptacle, Mini-USB Type B, R/A, Top Mount SMT	TE Connectivity	1734035-2	1
J6, J7	SMA Straight PCB Socket Die Cast, 50 Ohm, TH	TE Connectivity	5-1814832-1	2
JP1, JP2, JP3, JP4, JP6, JP24, JP25	Header, 100 mil, 3x1, Gold, TH	Samtec	TSW-103-07-G-S	7

Table 9. Bill of Materials (continued)

REF DES	DESCRIPTION	MFR	PART NUMBER	QTY
JP5	Header, 100 mil, 7x2, Tin, TH	Sullins Connector Solutions	PEC07DAAN	1
JP7	Header, 100 mil, 3x2, Gold, TH	Samtec	TSW-103-07-G-D	1
JP26	Header, 100 mil, 2x1, Gold, TH	Samtec	TSW-102-07-G-S	1
LBL1	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10, 000 per roll	Brady	THT-14-423-10	1
Q1, Q2, Q4, Q5, Q6, Q7	MOSFET, N-CH, 50 V, 0.22A, SOT-23	Fairchild Semiconductor	BSS138	6
Q3	MOSFET, N-CH, 25 V, 0.22 A, SOT-23	Fairchild Semiconductor	FDV301 N	1
R1, R2	RES, 0.015, 1%, 0.5 W, 1206	Stackpole Electronics Inc	CSR1206FK15 L0	2
R3	RES, 0, 5%, 0.25 W, 1206	Vishay-Dale	CRCW12060000Z0EA	1
R4, R5, R6	RES, 47 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW060347K0 JNEA	3
R8, R35, R36, R38, R39, R66, R82, R193, R195, R196	RES, 470, 5%, 0.1 W, 0603	Vishay-Dale	CRCW0603470RJNEA	10
R9	RES, 30.9 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060330K9FKEA	1
R10	RES, 10.0 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060310K0FKEA	1
R12	RES, 1.87 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06031K87FKEA	1
R13	RES, 1.50 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06031K50FKEA	1
R14	RES, 2.43 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06032K43FKEA	1
R15, R17, R19	RES, 1.15 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06031K15FKEA	3
R37, R61, R175, R180, R185, R187, R200, R202, R204, R212, R214, R216, R218	RES, 10 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW060310K0 JNEA	13
R44, R75, R114, R168, R173, R176, R192, R213, R215, R217, R219, R224	RES, 1.0 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06031K00 JNEA	12
R45, R46	RES, 150, 5%, 0.1 W, 0603	Vishay-Dale	CRCW0603150RJNEA	2
R52, R81, R177	RES, 100, 5%, 0.25 W, AEC-Q200 Grade 0, 0603	Rohm	ESR03EZPJ101	3
R55, R56, R88	RES, 49.9, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060349R9FKEA	3
R57, R58, R67, R68, R69, R70, R77, R78, R79, R80, R83, R89, R90, R91, R92, R97, R98, R99, R100, R148, R150, R166, R231, R232, R234, R235, R236, R237, R238, R239, R240, R241	RES, 0 ohm, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06030000Z0EA	32
R163, R243, R244	RES, 510, 5%, 0.1 W, 0603	Vishay-Dale	CRCW0603510RJNEA	3
R174, R183	RES, 3.9 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06033K90 JNEA	2
R194, R198	RES, 1.5 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06031K50 JNEA	2
R225	RES, 100 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW0603100KJNEA	1
R226, R233, R242	RES, 33k ohm, 5%, 0.1 W, 0603	Vishay-Dale	CRCW060333K0 JNEA	3
R227, R228	RES, 33 ohm, 5%, 0.063 W, 0402	Vishay-Dale	CRCW040233R0 JNED	2
R229	RES, 1.5k ohm, 5%, 0.063 W, 0402	Vishay-Dale	CRCW04021K50 JNED	1
R230	RES, 1.2Meg ohm, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06031M20 JNEA	1

Table 9. Bill of Materials (continued)

REF DES	DESCRIPTION	MFR	PART NUMBER	QTY
S1, S2, S4	Switch, SPST, Slide, Off-On, 2 Pos, 0.1A, 20 V, SMD	CTS Electrocomponents	219-2MST	3
S3, S5	Switch, Tactile, SPST-NO, 0.05A, 12 V, SMT	TE Connectivity	FSM4 JSMA	2
SH1, SH2, SH3, SH4, SH5, SH6, SH7, SH8, SH9, SH10, SH11, SH12, SH13	Shunt, 100 mil, Gold plated, Black	3M	969102-0000-DA	13
TP1, TP2, TP3, TP4, TP5, TP6, TP7	Test Point, Miniature, Red, TH	Keystone	5000	7
TP27, TP28, TP29, TP30	Test Point, Miniature, Black, TH	Keystone	5001	4
U1, U2	Voltage Output, High or Low-side Measurement, Bi-Directional Zerø-Drift Series Current-Shunt Monitor, DCK0006A	Texas Instruments	INA214BIDCKR	2
U3	Dual, 1-A, Low Noise (3.8-uVRMS), LDO Voltage Regulator, RTJ0020D (WQFN-20)	Texas Instruments	TPS7A8801RTJR	1
U4	Low-Noise, Wide-Bandwidth, High PSRR, Low-Dropout 1-A Linear Regulator, DRB0008A	Texas Instruments	TPS7A8101DRBR	1
U5	Network Clock Generator/Synchronizer, RGC0064 J (VQFN-64)	Texas Instruments	LMK05028RGC	1
U6	ESD-Protection Array for High-Speed Data Interfaces, 4 Channels, -40 to + 85 degC, 6-pin SON (DRY), Green (RoHS and no Sb/Br)	Texas Instruments	TPD4E004DRYR	1
U7	Ultra-Low Jitter Programmable Oscillator with Internal EEPROM, SIA0008B (QFM-8)	Texas Instruments	LMK61E2-SIAR	1
U8	Mixed Signal MicroController, PN0080A	Texas Instruments	MSP430F5529IPN	1
U9	Ultra Low Noise, 150 mA Linear Regulator for RF/Analog Circuits Requires No Bypass Capacitor, 6-pin LLP, Pb-Free	National Semiconductor	LP5900 SD-3.3/NOPB	1
U10	Single 2-Input Exclusive-OR Gate, DBV0005A (SOT-5)	Texas Instruments	SN74 LVC1 G86DBVR	1
Y1	OSC, 48.004800 MHz, 3.3 V, SMD	TXC Corporation	8 W48070002	1
Y2	TCXO, 3.3 V, 10 MHz, ±4.6 ppm, SMD	TXC Corporation	7 N10070005	1
Y3	Crystal, 24.000 MHz, 20 pF, SMD	ECS Inc.	ECS-240-20-5PX-TR	1
C17, C18	CAP, CERM, 0.01 µF, 50 V, + /- 5%, X7R, 0603	Kemet	C0603C103 J5RACTU	0
C91	CAP, CERM, 0.1uF, 25 V, + /- 5%, X7R, 0603	Kemet	C0603C104 J3RACTU	0
C96, C172, C173	CAP, CERM, 0.1 uF, 25 V, + /- 5%, X7R, 0603	Kemet	C0603C104 J3RACTU	0
C123, C124, C133, C134, C136, C137, C138, C139, C142, C143, C144, C145, C146, C147, C148	CAP, CERM, 100 pF, 50 V, + /- 5%, C0 G/NP0, 0603	AVX	06035A101 JAT2A	0

Table 9. Bill of Materials (continued)

REF DES	DESCRIPTION	MFR	PART NUMBER	QTY
C140, C141	CAP, CERM, 33 pF, 100 V, +/- 5%, C0 G/NP0, 0603	AVX	06031A330 JAT2A	0
FID1, FID2, FID3, FID4, FID5, FID6	Fiducial mark. There is nothing to buy or mount.	N/A	N/A	0
J5	Header (shrouded), 2.54 mm, 17x2, Gold, TH	3M	N2534-6002-RB	0
J33, J34, J35, J36, J37, J38, J39, J40	Header, 100 mil, 2x2, Tin, TH	Sullins Connector Solutions	PEC02DAAN	0
JP8, JP9, JP10, JP11, JP12, JP13, JP14, JP15, JP16, JP17, JP18, JP19, JP20, JP21, JP22	Header, 100 mil, 3x1, Gold, TH	Samtec	TSW-103-07-G-S	0
JP23	Header, 100 mil, 2x1, Gold, TH	Samtec	TSW-102-07-G-S	0
R11, R40, R41, R42, R47, R48, R49, R50, R51, R59, R60, R63, R64, R147, R245, R246	RES, 0, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06030000Z0EA	0
R43, R62, R65, R84, R85, R181, R182, R184, R186, R199, R201, R203	RES, 10 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW060310K0 JNEA	0
R71, R72, R73, R74, R93, R94, R95, R96, R105, R106, R107, R108, R115, R116, R117, R118, R123, R124, R125, R126, R133, R134, R135, R136, R141, R142, R143, R144, R151, R152, R153, R154, R159, R160, R161, R162, R169, R170, R171, R172	RES, 49.9, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060349R9FKEA	0
R76	RES, 1.0 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06031K00 JNEA	0
R110, R113, R128, R131, R146, R149, R164, R167	RES, 100, 5%, 0.1 W, 0603	Vishay-Dale	CRCW0603100RJNEA	0
TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP31	Test Point, Miniature, Red, TH	Keystone	5000	0
TP23, TP24, TP25, TP26	Test Point, Miniature, Black, TH	Keystone	5001	0
XU1	Socket, SQA64A, hinged	HSIO Technologies	106458-0118	0

Software

A.1 Software Installation (One-Time)

1. Download and Install TICS Pro software GUI v1.6.7 (or later).
2. Download and Install MATLAB Runtime v9.0 (2015b, 64-bit).
   a. Download the installer here
   b. This is required to run the compiled Matlab script bundled with the device profile.
3. Re-boot PC for proper installation of MATLAB Runtime.
4. Obtain the LMK05028 device profile: LMK05x28-ENGINEERING.zip (no need to un-zip this file).
5. Launch TICS Pro.
6. Import the device profile: Click Select Device > Import User Device, select: LMK05X28-ENGINEERING.zip from Step 3.

NOTE: Please contact TI Field Sales or email appscts@list.ti.com to obtain the pre-release software files for the LMK05028 specifically, including TICS Pro v1.6.7 (adds support for SPI protocol) and the latest device profile.

A.2 TICS Pro Usage for LMK05028

1. Launch TICS Pro.
2. Connect the PC to the EVM with the USB cable.
3. On the EVM, confirm switches S1A and S1B are OFF, so only LMK05028 is found when the I2C bus is scanned.
4. If needed, select the LMK05028 profile: Click Select Device > User Devices > LMK05x28-ENGINEERING.zip
5. Click USB communication > Interface.
   a. Under Interface, tick USB2ANY.
   b. Select Protocol: I2C or SPI_CLKLOW.
   c. Follow the Change Device Mode & Protocol dialog:
      i. On the EVM, set JP5 / JP24 jumpers accordingly for I2C or SPI Mode.
      ii. Click Yes to confirm change, or No to cancel.
   d. Press Close to apply the Mode & Protocol changes.
6. Follow the dialogs:
   a. Scan I2C Bus (I2C only) – Yes to confirm, No to skip.
      - LMK05028 should be found at 0x60.
      - If the scan found at device at 0x58, it is probably U7 (LMK61E2); in this case, re-start from Step 3 to find the LMK05028.
      - Alternatively, in the Communication setup window (Step 5), manually enter the I2C address as 0x60 and click Set I2C address.
   b. Write All Registers – Yes to confirm, No to skip.
7. In the GUI Main Page, follow the step-by-step procedure to enter the clock design parameters, run the script to generate the register settings, and program the device registers and EEPROM.

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

3 *Regulatory Notices:*

   3.1 *United States*

      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
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なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

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