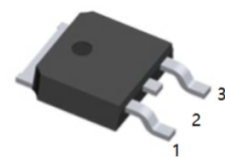


Description

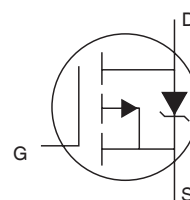
Features of this design are a 150°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in a wide variety of other applications.

Features

- V_{DS} (V) = -60V
- I_D = -42A (V_{GS} = -10V)
- $R_{DS(ON)}$ < 20m Ω (V_{GS} = -10V)
- Advanced Process Technology
- Ultra Low On-Resistance
- 150°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to T_{jmax}
- Some Parameters Are Different from IRF4905S



1.G 2.D 3.S
TO-252(DPAK) top view



Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	-70	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	-44	
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V (Package Limited)	-42	
I_{DM}	Pulsed Drain Current ¹ .	-280	
P_D @ $T_C = 25^\circ\text{C}$	Power Dissipation	170	W
	Linear Derating Factor	1.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ² .	140	mJ
E_{AS} (Tested)	Single Pulse Avalanche Energy Tested Value ⁶ .	790	
I_{AR}	Avalanche Current ¹ .	See Fig.12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche Energy ⁵ .		mJ
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting Torque, 6-32 or M3 screw ⁷ .		

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⁸ .		0.75	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount, steady state) ^{7,8} .		40	

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-55			V	$V_{GS} = 0V, I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient		-0.054		V/ $^\circ\text{C}$	Reference to 25°C , $I_D = -1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance			20	m Ω	$V_{GS} = -10V, I_D = -42A^3$
$V_{GS(th)}$	Gate Threshold Voltage	-1.1	-1.8	-2.5	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
g_{fs}	Forward Transconductance		19		S	$V_{DS} = -25V, I_D = -42A$
I_{DSS}	Drain-to-Source Leakage Current			-25	μA	$V_{DS} = -55V, V_{GS} = 0V$
				-200		$V_{DS} = -44V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage			100	nA	$V_{GS} = -20V$
	Gate-to-Source Reverse Leakage			-100		$V_{GS} = 20V$
Q_g	Total Gate Charge		120	180	nC	$I_D = -42A$
Q_{gs}	Gate-to-Source Charge		32			$V_{DS} = -44V$
Q_{gd}	Gate-to-Drain ("Miller") Charge		53			$V_{GS} = -10V^3$
$t_{d(on)}$	Turn-On Delay Time		20		ns	$V_{DD} = -28V$
t_r	Rise Time		99			$I_D = -42A$
$t_{d(off)}$	Turn-Off Delay Time		51			$R_G = 2.6\Omega$
t_f	Fall Time		64			$V_{GS} = -10V^3$
L_S	Internal Source Inductance		7.5		nH	Between lead, and center of die contact
C_{iss}	Input Capacitance		3500		pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance		1250			$V_{DS} = -25V$
C_{rss}	Reverse Transfer Capacitance		450			$f = 1.0\text{MHz}$
C_{oss}	Output Capacitance		4620			$V_{GS} = 0V, V_{DS} = -1.0V, f = 1.0\text{MHz}$
C_{oss}	Output Capacitance		940			$V_{GS} = 0V, V_{DS} = -44V, f = 1.0\text{MHz}$
$C_{oss\text{ eff.}}$	Effective Output Capacitance		1530			$V_{GS} = 0V, V_{DS} = 0V \text{ to } -44V^4$

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)		-42		A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ¹			-280		
V_{SD}	Diode Forward Voltage			-1.3	V	$T_J = 25^\circ\text{C}, I_S = -42A, V_{GS} = 0V^3$
t_{rr}	Reverse Recovery Time		61	92	ns	$T_J = 25^\circ\text{C}, I_F = -42A, V_{DD} = -28V$
Q_{rr}	Reverse Recovery Charge		150	220	nC	$di/dt = -100A/\mu s^3$
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

1. Repetitive rating; pulse width limited by max. junction temperature.
2. Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 0.16\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = -42A$, $V_{GS} = -10V$. Part not recommended for use above this value.
3. Pulse width $\leq 1.0\text{ms}$; duty cycle $\leq 2\%$.
4. $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
5. Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
6. This value determined from sample failure population. 100% tested to this value in production.
7. This is applied to D²Pak, when mounted on 1" square PCB (FR-4 or G-10 Material).
8. R_θ is measured at T_J approximately 90°C

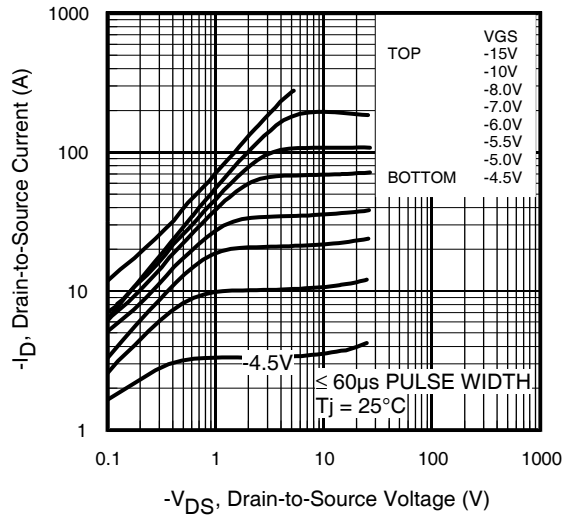


Fig 1. Typical Output Characteristics

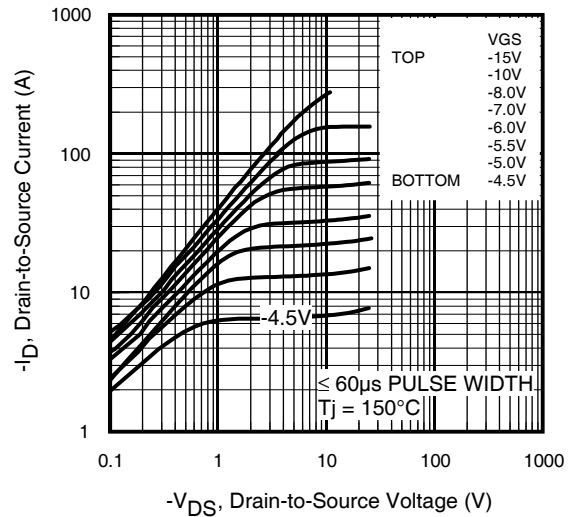


Fig 2. Typical Output Characteristics

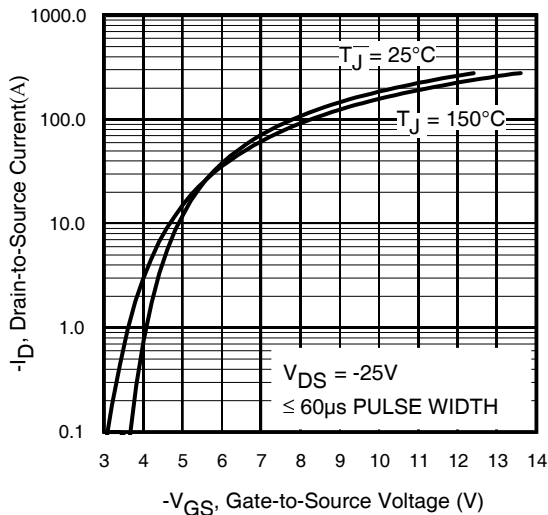


Fig 3. Typical Transfer Characteristics

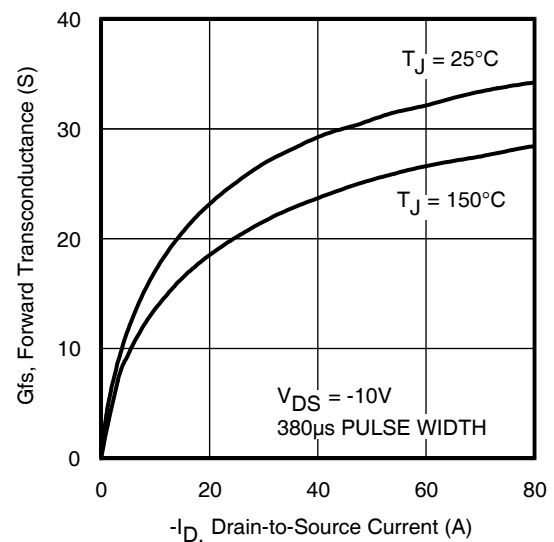


Fig 4. Typical Forward Transconductance Vs. Drain Current

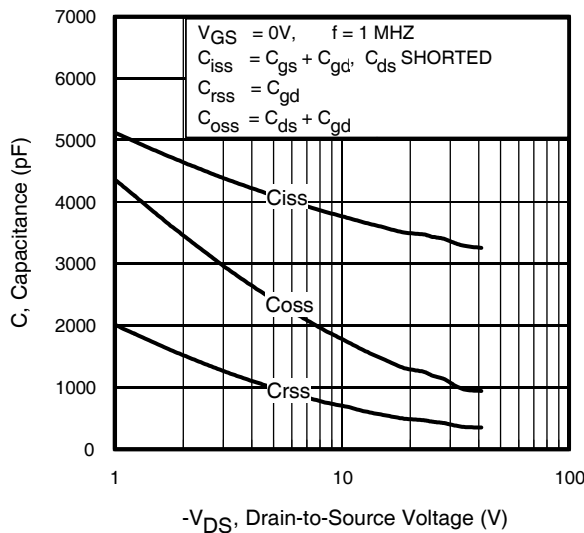


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

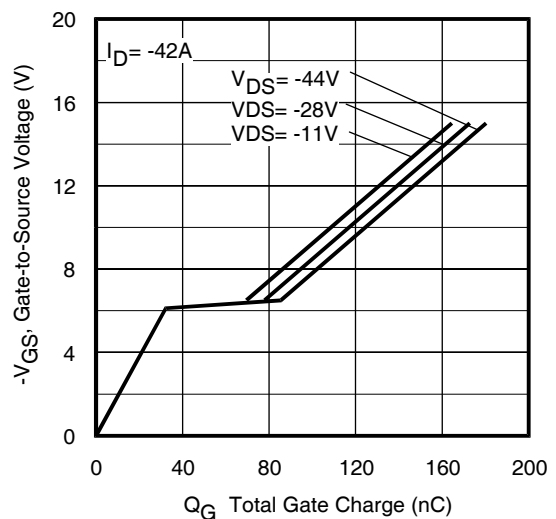


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

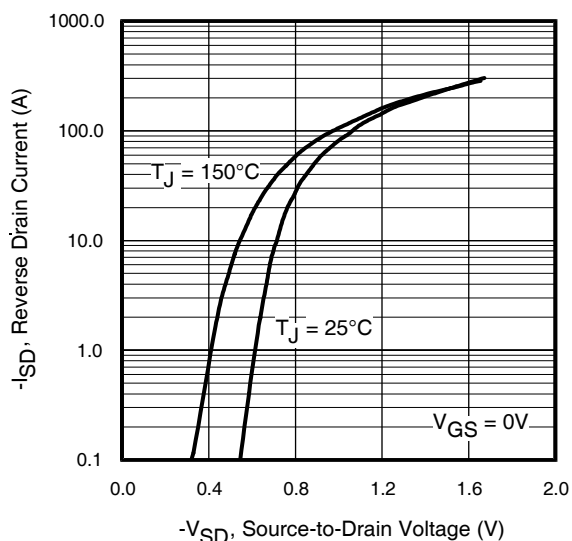


Fig 7. Typical Source-Drain Diode Forward Voltage

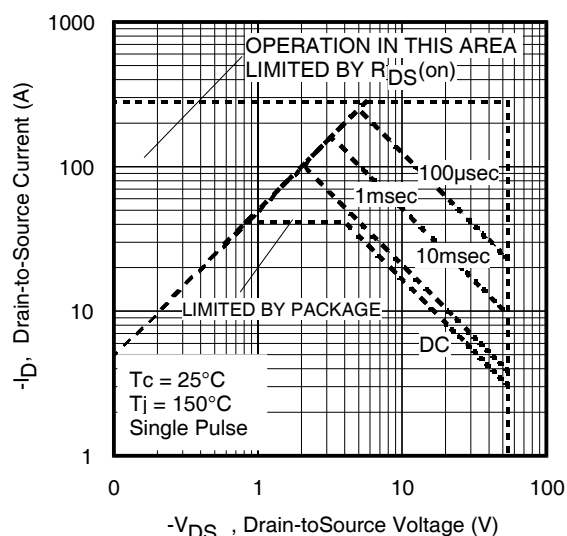


Fig 8. Maximum Safe Operating Area

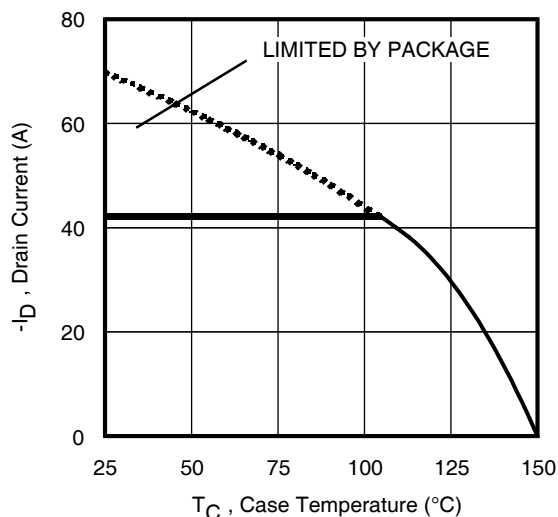


Fig 9. Maximum Drain Current Vs. Case Temperature

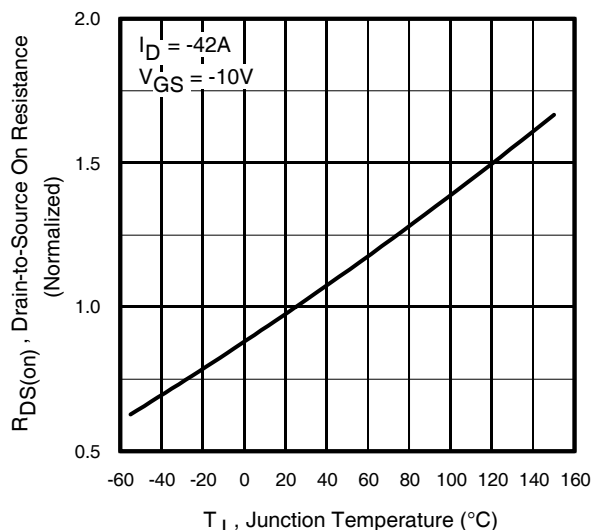


Fig 10. Normalized On-Resistance Vs. Temperature

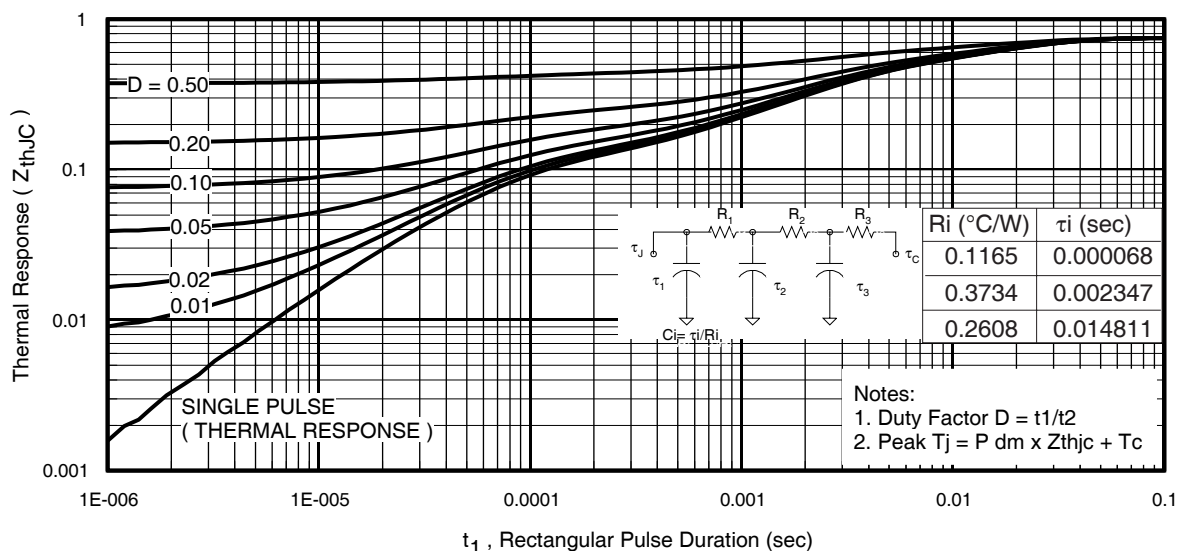


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

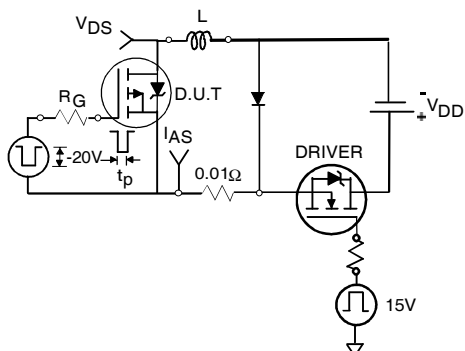


Fig 12a. Unclamped Inductive Test Circuit

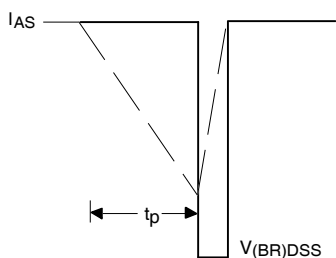


Fig 12b. Unclamped Inductive Waveforms

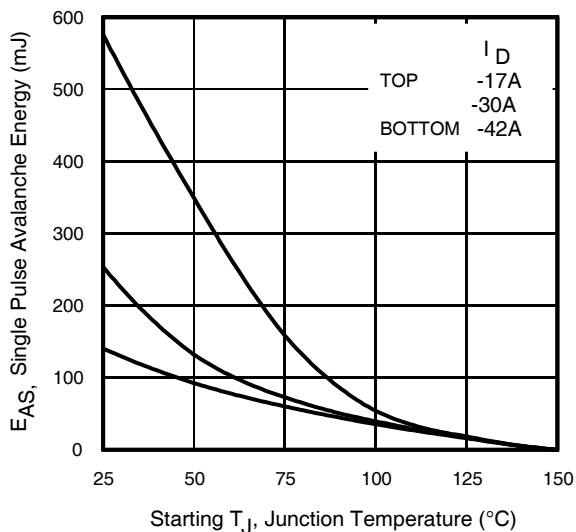


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

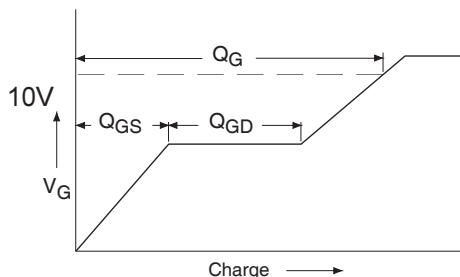


Fig 13a. Basic Gate Charge Waveform

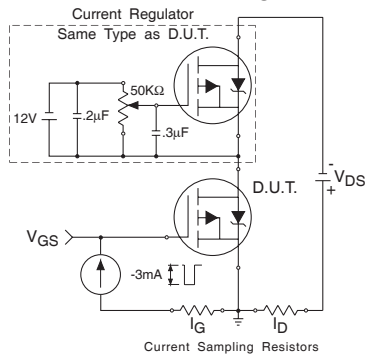


Fig 13b. Gate Charge Test Circuit

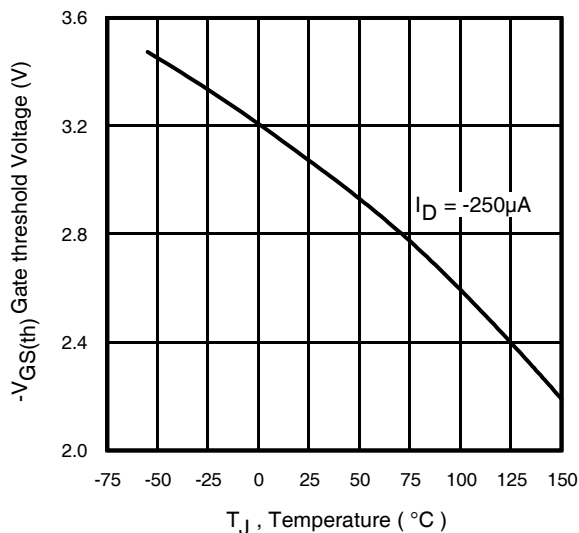


Fig 14. Threshold Voltage Vs. Temperature

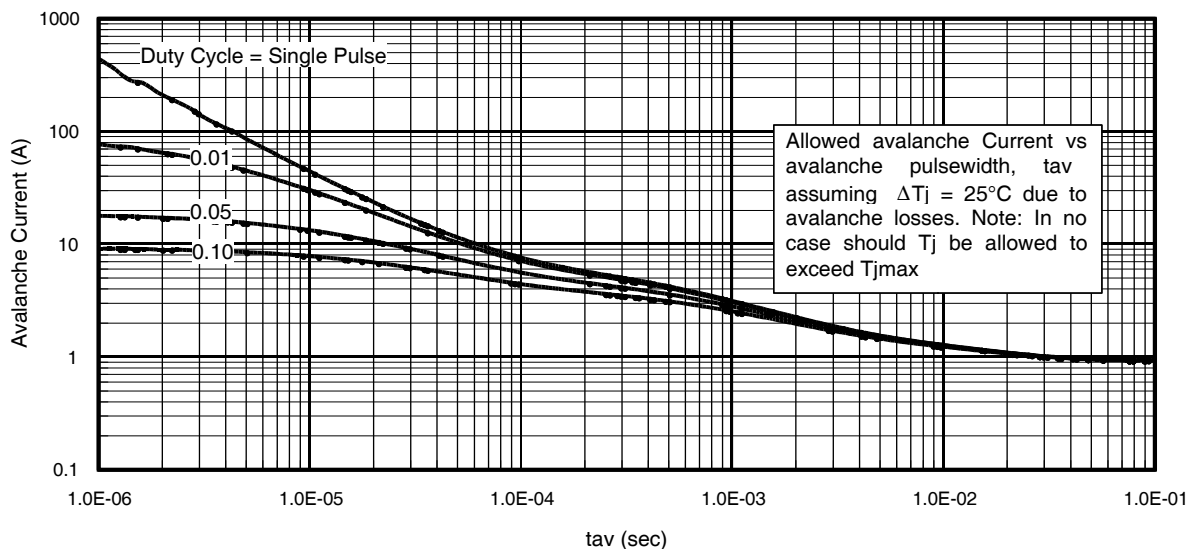


Fig 15. Typical Avalanche Current Vs. Pulsewidth

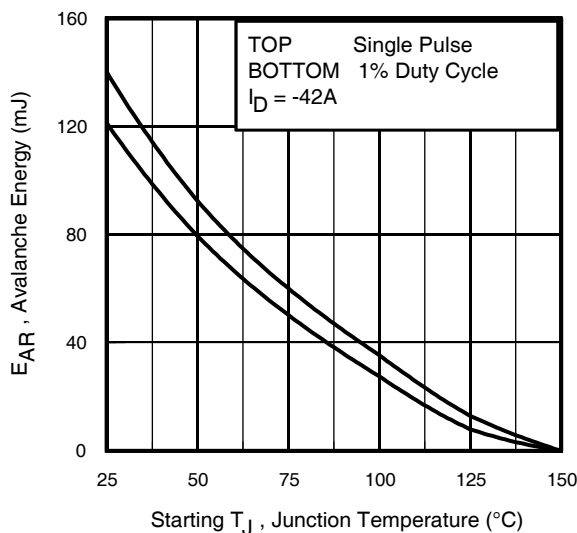


Fig 16. Maximum Avalanche Energy Vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:

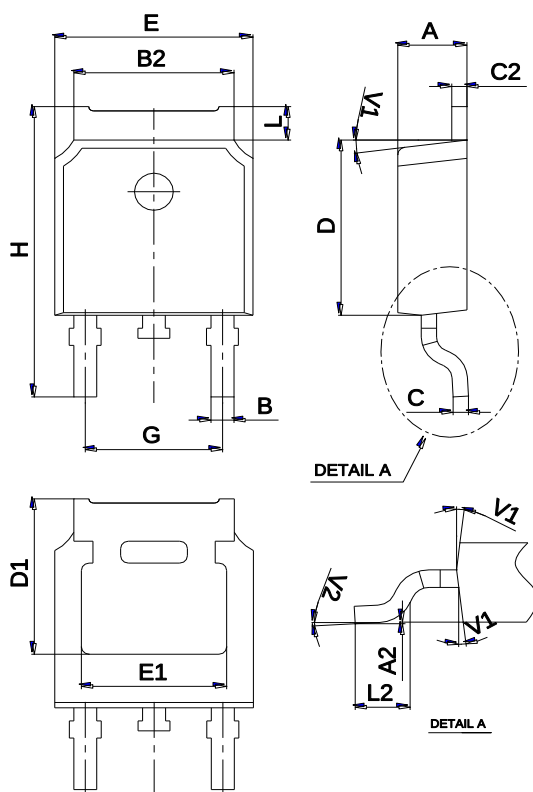
1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

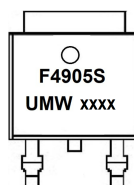
$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

Package Mechanical Data TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Marking



Ordering information

Order code	Package	Baseqty	Deliverymode
UMW IRF4905STRL	TO-252	2500	Tape and reel