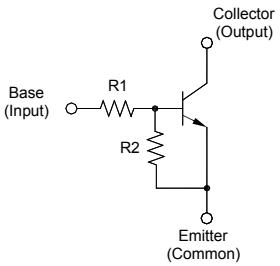
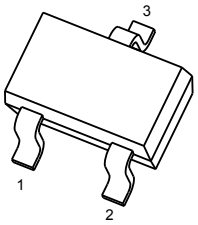
NPN Silicon Epitaxial Planar Digital Transistor

Features

- With built-in bias resistors
- Simplify circuit design
- Reduce a quantity of parts and manufacturing process

MARKING: 24





1. IN
2. GND
3. OUT

SOT-323

Absolute Maximum Ratings (T_a = 25℃)

Parameter	Symbol	Value	Unit
Collector Emitter Voltage	V_{CEO}	50	V
Input Voltage	V_I	- 10 to + 40	V
Collector Current	I_C	100	mA
Power Dissipation	P_{tot}	150	mW
Junction Temperature	T_j	150	℃
Storage Temperature Range	T_{stg}	- 55 to + 150	℃

Characteristics at T_a = 25℃

Parameter	Symbol	Min.	Typ.	Max.	Unit
DC Current Gain at V_{CE} = 5 V, I_C = 5 mA	h_{FE}	30	-	-	-
Collector Base Cutoff Current at V_{CB} = 50 V	I_{CBO}	-	-	500	nA
Emitter Base Cutoff Current at V_{EB} = 5 V	I_{EBO}	-	-	0.88	mA
Collector Emitter Saturation Voltage at I_C = 10 mA, I_B = 0.5 mA	$V_{CE(sat)}$	-	-	0.3	V
Input on Voltage at V_{CE} = 0.3 V, I_C = 10 mA	$V_{I(on)}$	-	-	3	V
Input off Voltage at V_{CE} = 5 V, I_C = 100 μA	$V_{I(off)}$	0.5	-	-	V
Transition frequency at V_{CE} = 10 V, $-I_E$ = 5 mA, f = 100 MHz	f_T	-	250	-	MHz
Input Resistance	R_1	7	10	13	KΩ
Resistance Ratio	R_2 / R_1	0.8	1	1.2	-

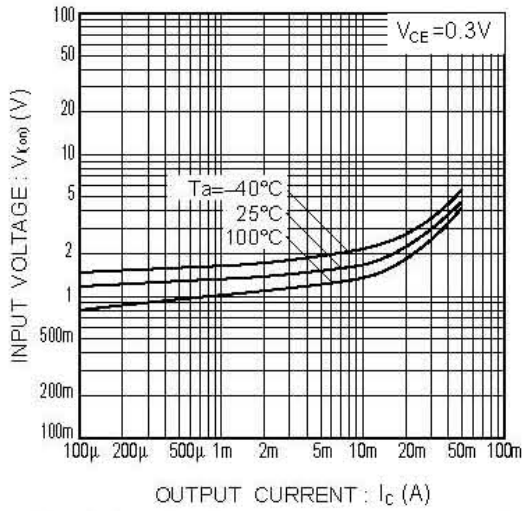


Fig.1 Input voltage vs. output current (ON characteristics)

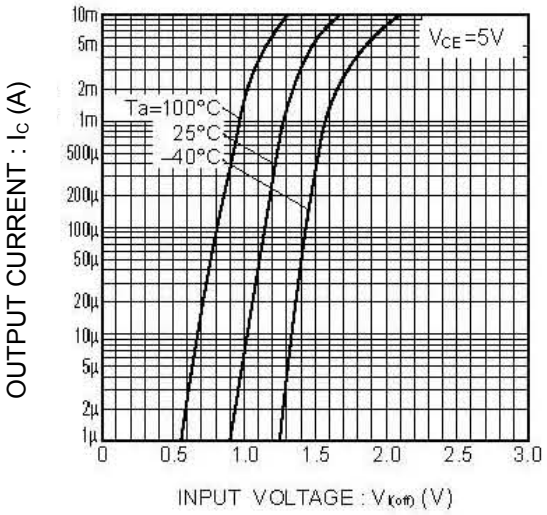


Fig.2 Output current vs. input voltage (OFF characteristics)

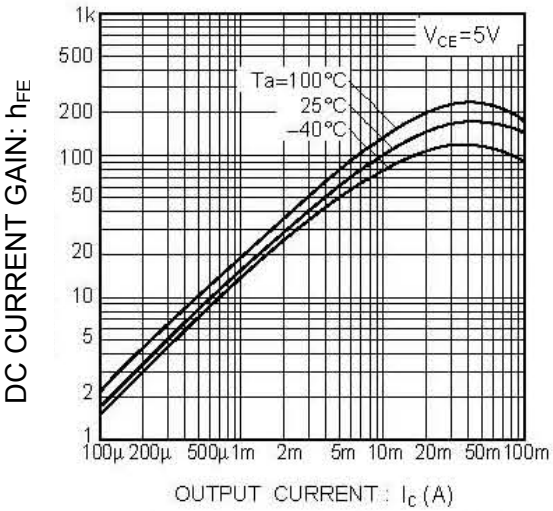


Fig.3 DC current gain vs. output current

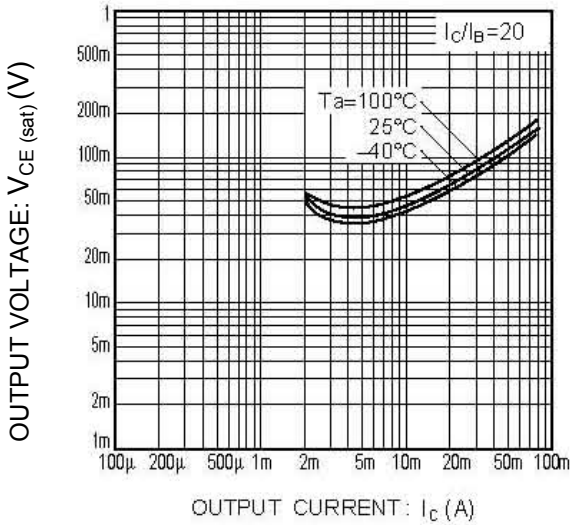
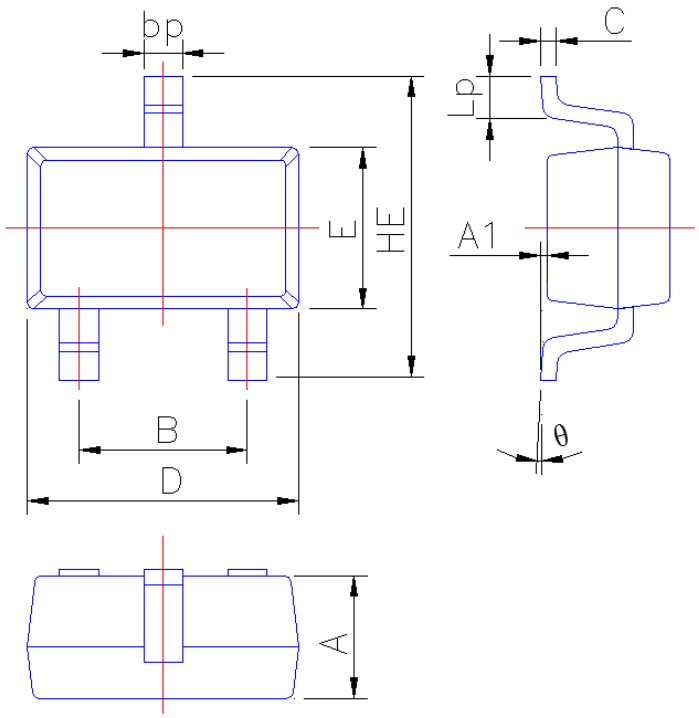


Fig.4 Output voltage vs. output current

SOT-323 Package Outline Dimensions



Symbol	Dimension in Millimeters	
	Min	Max
A	0.90	1.00
A1	0.010	0.100
B	1.20	1.40
bp	0.25	0.45
C	0.09	0.15
D	2.00	2.20
E	1.15	1.35
HE	2.15	2.55
Lp	0.25	0.46
θ	0°	6°