

RL78/G13

R01DS0131EJ0340

RENESAS MCU

Rev.3.40

May 31, 2018

True Low Power Platform (as low as 66 μ A/MHz, and 0.57 μ A for RTC + LVD), 1.6 V to 5.5 V operation, 16 to 512 Kbyte Flash, 41 DMIPS at 32 MHz, for General Purpose Applications

1. OUTLINE

1.1 Features

Ultra-low power consumption technology

- V_{DD} = single power supply voltage of 1.6 to 5.5 V
- HALT mode
- STOP mode
- SNOOZE mode

RL78 CPU core

- CISC architecture with 3-stage pipeline
- Minimum instruction execution time: Can be changed from high speed (0.03125 μ s: @ 32 MHz operation with high-speed on-chip oscillator) to ultra-low speed (30.5 μ s: @ 32.768 kHz operation with subsystem clock)
- Address space: 1 MB
- General-purpose registers: (8-bit register \times 8) \times 4 banks
- On-chip RAM: 2 to 32 KB

Code flash memory

- Code flash memory: 16 to 512 KB
- Block size: 1 KB
- Prohibition of block erase and rewriting (security function)
- On-chip debug function
- Self-programming (with boot swap function/flash shield window function)

Data Flash Memory

- Data flash memory: 4 KB to 8 KB
- Back ground operation (BGO): Instructions can be executed from the program memory while rewriting the data flash memory.
- Number of rewrites: 1,000,000 times (TYP.)
- Voltage of rewrites: V_{DD} = 1.8 to 5.5 V

High-speed on-chip oscillator

- Select from 32 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 6 MHz, 4 MHz, 3 MHz, 2 MHz, and 1 MHz
- High accuracy: \pm 1.0 % (V_{DD} = 1.8 to 5.5 V, T_A = -20 to +85°C)

Operating ambient temperature

- T_A = -40 to +85°C (A: Consumer applications, D: Industrial applications)
- T_A = -40 to +105°C (G: Industrial applications)

Power management and reset function

- On-chip power-on-reset (POR) circuit
- On-chip voltage detector (LVD) (Select interrupt and reset from 14 levels)

DMA (Direct Memory Access) controller

- 2/4 channels
- Number of clocks during transfer between 8/16-bit SFR and internal RAM: 2 clocks

Multiplier and divider/multiply-accumulator

- 16 bits \times 16 bits = 32 bits (Unsigned or signed)
- 32 bits \div 32 bits = 32 bits (Unsigned)
- 16 bits \times 16 bits + 32 bits = 32 bits (Unsigned or signed)

Serial interface

- CSI: 2 to 8 channels
- UART/UART (LIN-bus supported): 2 to 4 channels
- I²C/Simplified I²C communication: 2 to 8 channels

Timer

- 16-bit timer: 8 to 16 channels
- 12-bit interval timer: 1 channel
- Real-time clock: 1 channel (calendar for 99 years, alarm function, and clock correction function)
- Watchdog timer: 1 channel (operable with the dedicated low-speed on-chip oscillator)

A/D converter

- 8/10-bit resolution A/D converter (V_{DD} = 1.6 to 5.5 V)
- Analog input: 6 to 26 channels
- Internal reference voltage (1.45 V) and temperature sensor ^{Note 1}

I/O port

- I/O port: 16 to 120 (N-ch open drain I/O [withstand voltage of 6 V]: 0 to 4, N-ch open drain I/O [V_{DD} withstand voltage ^{Note 2}/ E_{VDD} withstand voltage ^{Note 3}]: 5 to 25)
- Can be set to N-ch open drain, TTL input buffer, and on-chip pull-up resistor
- Different potential interface: Can connect to a 1.8/2.5/3 V device
- On-chip key interrupt function
- On-chip clock output/buzzer output controller

Others

- On-chip BCD (binary-coded decimal) correction circuit

- Notes**
1. Can be selected only in HS (high-speed main) mode
 2. Products with 20 to 52 pins
 3. Products with 64 to 128 pins

Remark The functions mounted depend on the product.
See 1.6 Outline of Functions.

O ROM, RAM capacities

| Flash ROM | Data flash | RAM | RL78/G13 | | | | | |
|-----------|------------|--------------|----------|----------|----------|----------|----------|----------|
| | | | 20 pins | 24 pins | 25 pins | 30 pins | 32 pins | 36 pins |
| 128 KB | 8 KB | 12 KB | – | – | – | R5F100AG | R5F100BG | R5F100CG |
| | – | | – | – | R5F101AG | R5F101BG | R5F101CG | |
| 96 KB | 8 KB | 8 KB | – | – | – | R5F100AF | R5F100BF | R5F100CF |
| | – | | – | – | R5F101AF | R5F101BF | R5F101CF | |
| 64 KB | 4 KB | 4 KB Note | R5F1006E | R5F1007E | R5F1008E | R5F100AE | R5F100BE | R5F100CE |
| | – | | R5F1016E | R5F1017E | R5F1018E | R5F101AE | R5F101BE | R5F101CE |
| 48 KB | 4 KB | 3 KB Note | R5F1006D | R5F1007D | R5F1008D | R5F100AD | R5F100BD | R5F100CD |
| | – | | R5F1016D | R5F1017D | R5F1018D | R5F101AD | R5F101BD | R5F101CD |
| 32 KB | 4 KB | 2 KB | R5F1006C | R5F1007C | R5F1008C | R5F100AC | R5F100BC | R5F100CC |
| | – | | R5F1016C | R5F1017C | R5F1018C | R5F101AC | R5F101BC | R5F101CC |
| 16 KB | 4 KB | 2 KB | R5F1006A | R5F1007A | R5F1008A | R5F100AA | R5F100BA | R5F100CA |
| | – | | R5F1016A | R5F1017A | R5F1018A | R5F101AA | R5F101BA | R5F101CA |

| Flash ROM | Data flash | RAM | RL78/G13 | | | | | | | |
|-----------|------------|---------------|----------|----------|----------|----------|----------|----------|----------|----------|
| | | | 40 pins | 44 pins | 48 pins | 52 pins | 64 pins | 80 pins | 100 pins | 128 pins |
| 512 KB | 8 KB | 32 KB Note | – | R5F100FL | R5F100GL | R5F100JL | R5F100LL | R5F100ML | R5F100PL | R5F100SL |
| | – | | – | R5F101FL | R5F101GL | R5F101JL | R5F101LL | R5F101ML | R5F101PL | R5F101SL |
| 384 KB | 8 KB | 24 KB | – | R5F100FK | R5F100GK | R5F100JK | R5F100LK | R5F100MK | R5F100PK | R5F100SK |
| | – | | – | R5F101FK | R5F101GK | R5F101JK | R5F101LK | R5F101MK | R5F101PK | R5F101SK |
| 256 KB | 8 KB | 20 KB Note | – | R5F100FJ | R5F100GJ | R5F100JJ | R5F100LJ | R5F100MJ | R5F100PJ | R5F100SJ |
| | – | | – | R5F101FJ | R5F101GJ | R5F101JJ | R5F101LJ | R5F101MJ | R5F101PJ | R5F101SJ |
| 192 KB | 8 KB | 16 KB | R5F100EH | R5F100FH | R5F100GH | R5F100JH | R5F100LH | R5F100MH | R5F100PH | R5F100SH |
| | – | | R5F101EH | R5F101FH | R5F101GH | R5F101JH | R5F101LH | R5F101MH | R5F101PH | R5F101SH |
| 128 KB | 8 KB | 12 KB | R5F100EG | R5F100FG | R5F100GG | R5F100JG | R5F100LG | R5F100MG | R5F100PG | – |
| | – | | R5F101EG | R5F101FG | R5F101GG | R5F101JG | R5F101LG | R5F101MG | R5F101PG | – |
| 96 KB | 8 KB | 8 KB | R5F100EF | R5F100FF | R5F100GF | R5F100JF | R5F100LF | R5F100MF | R5F100PF | – |
| | – | | R5F101EF | R5F101FF | R5F101GF | R5F101JF | R5F101LF | R5F101MF | R5F101PF | – |
| 64 KB | 4 KB | 4 KB Note | R5F100EE | R5F100FE | R5F100GE | R5F100JE | R5F100LE | – | – | – |
| | – | | R5F101EE | R5F101FE | R5F101GE | R5F101JE | R5F101LE | – | – | – |
| 48 KB | 4 KB | 3 KB Note | R5F100ED | R5F100FD | R5F100GD | R5F100JD | R5F100LD | – | – | – |
| | – | | R5F101ED | R5F101FD | R5F101GD | R5F101JD | R5F101LD | – | – | – |
| 32 KB | 4 KB | 2 KB | R5F100EC | R5F100FC | R5F100GC | R5F100JC | R5F100LC | – | – | – |
| | – | | R5F101EC | R5F101FC | R5F101GC | R5F101JC | R5F101LC | – | – | – |
| 16 KB | 4 KB | 2 KB | R5F100EA | R5F100FA | R5F100GA | – | – | – | – | – |
| | – | | R5F101EA | R5F101FA | R5F101GA | – | – | – | – | – |

Note The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.

R5F100xD, R5F101xD (x = 6 to 8, A to C, E to G, J, L): Start address FF300H

R5F100xE, R5F101xE (x = 6 to 8, A to C, E to G, J, L): Start address FEF00H

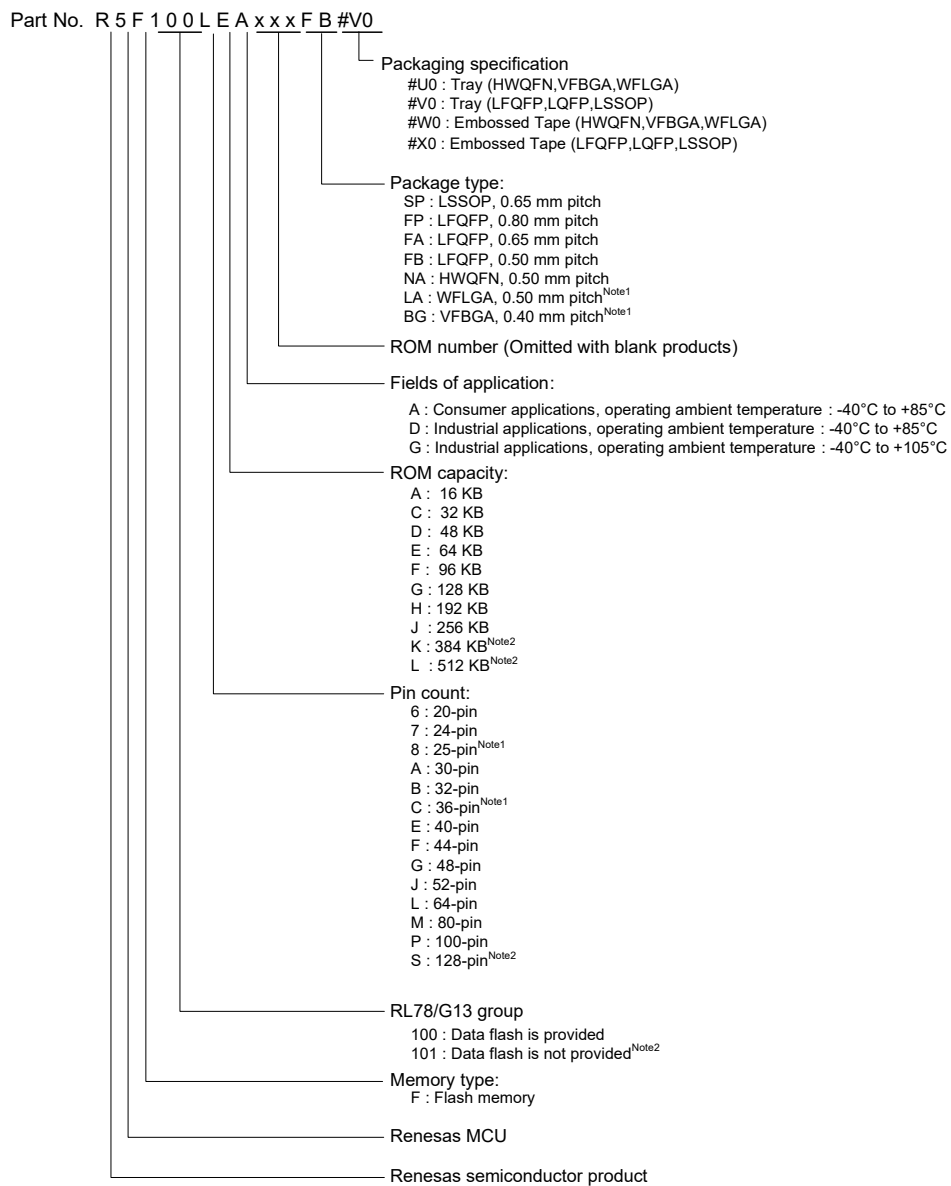
R5F100xJ, R5F101xJ (x = F, G, J, L, M, P): Start address FAF00H

R5F100xL, R5F101xL (x = F, G, J, L, M, P, S): Start address F7F00H

For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

1.2 List of Part Numbers

Figure 1-1. Part Number, Memory Size, and Package of RL78/G13



- Notes**
1. Products only for "A: Consumer applications (T_A = -40 to +85°C)", and "G: Industrial applications (T_A = -40 to +105°C)"
 2. Products only for "A: Consumer applications (T_A = -40 to +85°C)", and "D: Industrial applications (T_A = -40 to +85°C)"

Table 1-1. List of Ordering Part Numbers

(1/12)

| Pin count | Package | Data flash | Fields of Application ^{Note} | Ordering Part Number |
|-----------|--|-------------|---------------------------------------|--|
| 20 pins | 20-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch) | Mounted | A | R5F1006AASP#V0, R5F1006CASP#V0, R5F1006DASP#V0, R5F1006EASP#V0 R5F1006AASP#X0, R5F1006CASP#X0, R5F1006DASP#X0, R5F1006EASP#X0 |
| | | | D | R5F1006ADSP#V0, R5F1006CDSP#V0, R5F1006DDSP#V0, R5F1006EDSP#V0 R5F1006ADSP#X0, R5F1006CDSP#X0, R5F1006DDSP#X0, R5F1006EDSP#X0 |
| | | | G | R5F1006AGSP#V0, R5F1006CGSP#V0, R5F1006DGSP#V0, R5F1006EGSP#V0 R5F1006AGSP#X0, R5F1006CGSP#X0, R5F1006DGSP#X0, R5F1006EGSP#X0 |
| | | Not mounted | A | R5F1016AASP#V0, R5F1016CASP#V0, R5F1016DASP#V0, R5F1016EASP#V0 R5F1016AASP#X0, R5F1016CASP#X0, R5F1016DASP#X0, R5F1016EASP#X0 |
| | | | D | R5F1016ADSP#V0, R5F1016CDSP#V0, R5F1016DDSP#V0, R5F1016EDSP#V0 R5F1016ADSP#X0, R5F1016CDSP#X0, R5F1016DDSP#X0, R5F1016EDSP#X0 |
| 24 pins | 24-pin plastic HWQFN (4 × 4mm, 0.5 mm pitch) | Mounted | A | R5F1007AANA#U0, R5F1007CANA#U0, R5F1007DANA#U0, R5F1007EANA#U0 R5F1007AANA#W0, R5F1007CANA#W0, R5F1007DANA#W0, R5F1007EANA#W0 |
| | | | D | R5F1007ADNA#U0, R5F1007CDNA#U0, R5F1007DDNA#U0, R5F1007EDNA#U0 R5F1007ADNA#W0, R5F1007CDNA#W0, R5F1007DDNA#W0, R5F1007EDNA#W0 |
| | | | G | R5F1007AGNA#U0, R5F1007CGNA#U0, R5F1007DGNA#U0, R5F1007EGNA#U0 R5F1007AGNA#W0, R5F1007CGNA#W0, R5F1007DGNA#W0, R5F1007EGNA#W0 |
| | | Not mounted | A | R5F1017AANA#U0, R5F1017CANA#U0, R5F1017DANA#U0, R5F1017EANA#U0 R5F1017AANA#W0, R5F1017CANA#W0, R5F1017DANA#W0, R5F1017EANA#W0 |
| | | | D | R5F1017ADNA#U0, R5F1017CDNA#U0, R5F1017DDNA#U0, R5F1017EDNA#U0 R5F1017ADNA#W0, R5F1017CDNA#W0, R5F1017DDNA#W0, R5F1017EDNA#W0 |

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

Table 1-1. List of Ordering Part Numbers

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| Pin count | Package | Data flash | Fields of Application ^{Note} | Ordering Part Number |
|-----------|---|-------------|---------------------------------------|--|
| 25 pins | 25-pin plastic WFLGA (3 × 3 mm, 0.5 mm pitch) | Mounted | A G | R5F1008AALA#U0, R5F1008CALA#U0, R5F1008DALA#U0, R5F1008EALA#U0 R5F1008AALA#W0, R5F1008CALA#W0, R5F1008DALA#W0, R5F1008EALA#W0 R5F1008AGLA#U0, R5F1008CGLA#U0, R5F1008DGLA#U0, R5F1008EGLA#U0 R5F1008AGLA#W0, R5F1008CGLA#W0, R5F1008DGLA#W0, R5F1008EGLA#W0 |
| | | Not mounted | A | R5F1018AALA#U0, R5F1018CALA#U0, R5F1018DALA#U0, R5F1018EALA#U0 R5F1018AALA#W0, R5F1018CALA#W0, R5F1018DALA#W0, R5F1018EALA#W0 |
| 30 pins | 30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch) | Mounted | A D G | R5F100AAASP#V0, R5F100ACASP#V0, R5F100ADASP#V0, R5F100AEASP#V0, R5F100AFASP#V0, R5F100AGASP#V0 R5F100AAASP#X0, R5F100ACASP#X0, R5F100ADASP#X0, R5F100AEASP#X0, R5F100AFASP#X0, R5F100AGASP#X0 R5F100AADSP#V0, R5F100ACDSP#V0, R5F100ADDS#V0, R5F100AEDSP#V0, R5F100AFDSP#V0, R5F100AGDSP#V0 R5F100AADSP#X0, R5F100ACDSP#X0, R5F100ADDS#X0, R5F100AEDSP#X0, R5F100AFDSP#X0, R5F100AGDSP#X0 R5F100AAGSP#V0, R5F100ACGSP#V0, R5F100ADGSP#V0, R5F100AEGSP#V0, R5F100AFGSP#V0, R5F100AGGSP#V0 R5F100AAGSP#X0, R5F100ACGSP#X0, R5F100ADGSP#X0, R5F100AEGSP#X0, R5F100AFGSP#X0, R5F100AGGSP#X0 |
| | | Not mounted | A D | R5F101AAASP#V0, R5F101ACASP#V0, R5F101ADASP#V0, R5F101AEASP#V0, R5F101AFASP#V0, R5F101AGASP#V0 R5F101AAASP#X0, R5F101ACASP#X0, R5F101ADASP#X0, R5F101AEASP#X0, R5F101AFASP#X0, R5F101AGASP#X0 R5F101AADSP#V0, R5F101ACDSP#V0, R5F101ADDS#V0, R5F101AEDSP#V0, R5F101AFDSP#V0, R5F101AGDSP#V0 R5F101AADSP#X0, R5F101ACDSP#X0, R5F101ADDS#X0, R5F101AEDSP#X0, R5F101AFDSP#X0, R5F101AGDSP#X0 |
| 32 pins | 32-pin plastic HWQFN (5 × 5 mm, 0.5 mm pitch) | Mounted | A D G | R5F100BAANA#U0, R5F100BCANA#U0, R5F100BDANA#U0, R5F100BEANA#U0, R5F100BFANA#U0, R5F100BGANA#U0 R5F100BAANA#W0, R5F100BCANA#W0, R5F100BDANA#W0, R5F100BEANA#W0, R5F100BFANA#W0, R5F100BGANA#W0 R5F100BADNA#U0, R5F100BCDNA#U0, R5F100BDDNA#U0, R5F100BEDNA#U0, R5F100BFDNA#U0, R5F100BGDNA#U0 R5F100BADNA#W0, R5F100BCDNA#W0, R5F100BDDNA#W0, R5F100BEDNA#W0, R5F100BFDNA#W0, R5F100BGDNA#W0 R5F100BAGNA#U0, R5F100BCGNA#U0, R5F100BDGNA#U0, R5F100BEGNA#U0, R5F100BFGNA#U0, R5F100BGGNA#U0 R5F100BAGNA#W0, R5F100BCGNA#W0, R5F100BDGNA#W0, R5F100BEGNA#W0, R5F100BFGNA#W0, R5F100BGGNA#W0 |
| | | Not mounted | A D | R5F101BAANA#U0, R5F101BCANA#U0, R5F101BDANA#U0, R5F101BEANA#U0, R5F101BFANA#U0, R5F101BGANA#U0 R5F101BAANA#W0, R5F101BCANA#W0, R5F101BDANA#W0, R5F101BEANA#W0, R5F101BFANA#W0, R5F101BGANA#W0 R5F101BADNA#U0, R5F101BCDNA#U0, R5F101BDDNA#U0, R5F101BEDNA#U0, R5F101BFDNA#U0, R5F101BGDNA#U0 R5F101BADNA#W0, R5F101BCDNA#W0, R5F101BDDNA#W0, R5F101BEDNA#W0, R5F101BFDNA#W0, R5F101BGDNA#W0 |

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

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Table 1-1. List of Ordering Part Numbers

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| Pin count | Package | Data flash | Fields of Application ^{Note} | Ordering Part Number |
|-------------|--|--|--|--|
| 36 pins | 36-pin plastic WFLGA (4 × 4 mm, 0.5 mm pitch) | Mounted | A | R5F100CAALA#U0, R5F100CCALA#U0, R5F100CDALA#U0, R5F100CEALA#U0, R5F100CFALA#U0, R5F100CGALA#U0 R5F100CAALA#W0, R5F100CCALA#W0, R5F100CDALA#W0, R5F100CEALA#W0, R5F100CFALA#W0, R5F100CGALA#W0 R5F100CAGLA#U0, R5F100CCGLA#U0, R5F100CDGLA#U0, R5F100CEGLA#U0, R5F100CFGLA#U0, R5F100CGGLA#U0 R5F100CAGLA#W0, R5F100CCGLA#W0, R5F100CDGLA#W0, R5F100CEGLA#W0, R5F100CFGLA#W0, R5F100CGGLA#W0 |
| | | | G | |
| | A | R5F101CAALA#U0, R5F101CCALA#U0, R5F101CDALA#U0, R5F101CEALA#U0, R5F101CFALA#U0, R5F101CGALA#U0 R5F101CAALA#W0, R5F101CCALA#W0, R5F101CDALA#W0, R5F101CEALA#W0, R5F101CFALA#W0, R5F101CGALA#W0 | | |
| Not mounted | | | | |
| 40 pins | 40-pin plastic HWQFN (6 × 6 mm, 0.5 mm pitch) | Mounted | A | R5F100EAANA#U0, R5F100ECANA#U0, R5F100EDANA#U0, R5F100EEANA#U0, R5F100EFANA#U0, R5F100EGANA#U0, R5F100EHANA#U0 R5F100EAANA#W0, R5F100ECANA#W0, R5F100EDANA#W0, R5F100EEANA#W0, R5F100EFANA#W0, R5F100EGANA#W0, R5F100EHANA#W0 |
| | | | D | R5F100EADNA#U0, R5F100ECDNA#U0, R5F100EDDNA#U0, R5F100EEDNA#U0, R5F100EFDNA#U0, R5F100EGDNA#U0, R5F100EHDNA#U0 R5F100EADNA#W0, R5F100ECDNA#W0, R5F100EDDNA#W0, R5F100EEDNA#W0, R5F100EFDNA#W0, R5F100EGDNA#W0, R5F100EHDNA#W0 |
| | | G | R5F100EAGNA#U0, R5F100ECGNA#U0, R5F100EDGNA#U0, R5F100EEGNA#U0, R5F100EFGNA#U0, R5F100EGGNA#U0, R5F100EHGNA#U0 R5F100EAGNA#W0, R5F100ECGNA#W0, R5F100EDGNA#W0, R5F100EEGNA#W0, R5F100EFGNA#W0, R5F100EGGNA#W0, R5F100EHGNA#W0 | |
| | | Not mounted | A | R5F101EAANA#U0, R5F101ECANA#U0, R5F101EDANA#U0, R5F101EEANA#U0, R5F101EFANA#U0, R5F101EGANA#U0, R5F101EHANA#U0 R5F101EAANA#W0, R5F101ECANA#W0, R5F101EDANA#W0, R5F101EEANA#W0, R5F101EFANA#W0, R5F101EGANA#W0, R5F101EHANA#W0 |
| D | R5F101EADNA#U0, R5F101ECDNA#U0, R5F101EDDNA#U0, R5F101EEDNA#U0, R5F101EFDNA#U0, R5F101EGDNA#U0, R5F101EHDNA#U0 R5F101EADNA#W0, R5F101ECDNA#W0, R5F101EDDNA#W0, R5F101EEDNA#W0, R5F101EFDNA#W0, R5F101EGDNA#W0, R5F101EHDNA#W0 | | | |

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13.**

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Table 1-1. List of Ordering Part Numbers

(4/12)

| Pin count | Package | Data flash | Fields of Application ^{Note} | Ordering Part Number |
|-----------|---|-------------|---------------------------------------|--|
| 44 pins | 44-pin plastic LQFP (10 × 10 mm, 0.8 mm pitch) | Mounted | A | R5F100FAAFP#V0, R5F100FCAFP#V0, R5F100FDAFP#V0, R5F100FEAFP#V0, R5F100FFAFP#V0, R5F100FGAFP#V0, R5F100FHAFP#V0, R5F100FJAFP#V0, R5F100FKAFP#V0, R5F100FLAFP#V0 R5F100FAAFP#X0, R5F100FCAFP#X0, R5F100FDAFP#X0, R5F100FEAFP#X0, R5F100FFAFP#X0, R5F100FGAFP#X0, R5F100FHAFP#X0, R5F100FJAFP#X0, R5F100FKAFP#X0, R5F100FLAFP#X0 |
| | | | D | R5F100FADFP#V0, R5F100FCDFP#V0, R5F100FDDFP#V0, R5F100FEDFP#V0, R5F100FFDFP#V0, R5F100FGDFP#V0, R5F100FHDFP#V0, R5F100FJDFP#V0, R5F100FKDFP#V0, R5F100FLDFP#V0 R5F100FADFP#X0, R5F100FCDFP#X0, R5F100FDDFP#X0, R5F100FEDFP#X0, R5F100FFDFP#X0, R5F100FGDFP#X0, R5F100FHDFP#X0, R5F100FJDFP#X0, R5F100FKDFP#X0, R5F100FLDFP#X0 |
| | | | G | R5F100FAGFP#V0, R5F100FCGFP#V0, R5F100FDGFP#V0, R5F100FEGFP#V0, R5F100FFGFP#V0, R5F100FGGFP#V0, R5F100FHGFP#V0, R5F100JGFP#V0 R5F100FAGFP#X0, R5F100FCGFP#X0, R5F100FDGFP#X0, R5F100FEGFP#X0, R5F100FFGFP#X0, R5F100FGGFP#X0, R5F100FHGFP#X0, R5F100JGFP#X0 |
| | | Not mounted | A | R5F101FAAFP#V0, R5F101FCAFP#V0, R5F101FDAFP#V0, R5F101FEAFP#V0, R5F101FFAFP#V0, R5F101FGAFP#V0, R5F101FHAFP#V0, R5F101FJAFP#V0, R5F101FKAFP#V0, R5F101FLAFP#V0 R5F101FAAFP#X0, R5F101FCAFP#X0, R5F101FDAFP#X0, R5F101FEAFP#X0, R5F101FFAFP#X0, R5F101FGAFP#X0, R5F101FHAFP#X0, R5F101FJAFP#X0, R5F101FKAFP#X0, R5F101FLAFP#X0 |
| | | | D | R5F101FADFP#V0, R5F101FCDFP#V0, R5F101FDDFP#V0, R5F101FEDFP#V0, R5F101FFDFP#V0, R5F101FGDFP#V0, R5F101FHDFP#V0, R5F101FJDFP#V0, R5F101FKDFP#V0, R5F101FLDFP#V0 R5F101FADFP#X0, R5F101FCDFP#X0, R5F101FDDFP#X0, R5F101FEDFP#X0, R5F101FFDFP#X0, R5F101FGDFP#X0, R5F101FHDFP#X0, R5F101FJDFP#X0, R5F101FKDFP#X0, R5F101FLDFP#X0 |

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

Table 1-1. List of Ordering Part Numbers

(5/12)

| Pin count | Package | Data flash | Fields of Application ^{Note} | Ordering Part Number |
|-----------|--|-------------|---------------------------------------|--|
| 48 pins | 48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch) | Mounted | A | R5F100GAAFB#V0, R5F100GCAFB#V0, R5F100GDAFB#V0, R5F100GEAFB#V0, R5F100GFAFB#V0, R5F100GGAFB#V0, R5F100GHAFB#V0, R5F100GJAFB#V0, R5F100GKAFB#V0, R5F100GLAFB#V0 R5F100GAAFB#X0, R5F100GCAFB#X0, R5F100GDAFB#X0, R5F100GEAFB#X0, R5F100GFAFB#X0, R5F100GGAFB#X0, R5F100GHAFB#X0, R5F100GJAFB#X0, R5F100GKAFB#X0, R5F100GLAFB#X0 |
| | | | D | R5F100GADFB#V0, R5F100GCDFB#V0, R5F100GDDFB#V0, R5F100GEDFB#V0, R5F100GFDFB#V0, R5F100GGDFB#V0, R5F100GHDFB#V0, R5F100GJDFB#V0, R5F100GKDFB#V0, R5F100GLDFB#V0 R5F100GADFB#X0, R5F100GCDFB#X0, R5F100GDDFB#X0, R5F100GEDFB#X0, R5F100GFDFB#X0, R5F100GGDFB#X0, R5F100GHDFB#X0, R5F100GJDFB#X0, R5F100GKDFB#X0, R5F100GLDFB#X0 |
| | | | G | R5F100GAGFB#V0, R5F100GCGFB#V0, R5F100GDGFB#V0, R5F100GEGFB#V0, R5F100GFGFB#V0, R5F100GGGFB#V0, R5F100GHGFB#V0, R5F100GJGFB#V0 R5F100GAGFB#X0, R5F100GCGFB#X0, R5F100GDGFB#X0, R5F100GEGFB#X0, R5F100GFGFB#X0, R5F100GGGFB#X0, R5F100GHGFB#X0, R5F100GJGFB#X0 |
| | | Not mounted | A | R5F101GAAFB#V0, R5F101GCAFB#V0, R5F101GDAFB#V0, R5F101GEAFB#V0, R5F101GFAFB#V0, R5F101GGAFB#V0, R5F101GHAFB#V0, R5F101GJAFB#V0, R5F101GKAFB#V0, R5F101GLAFB#V0 R5F101GAAFB#X0, R5F101GCAFB#X0, R5F101GDAFB#X0, R5F101GEAFB#X0, R5F101GFAFB#X0, R5F101GGAFB#X0, R5F101GHAFB#X0, R5F101GJAFB#X0, R5F101GKAFB#X0, R5F101GLAFB#X0 |
| | | | D | R5F101GADFB#V0, R5F101GCDFB#V0, R5F101GDDFB#V0, R5F101GEDFB#V0, R5F101GFDFB#V0, R5F101GGDFB#V0, R5F101GHDFB#V0, R5F101GJDFB#V0, R5F101GKDFB#V0, R5F101GLDFB#V0 R5F101GADFB#X0, R5F101GCDFB#X0, R5F101GDDFB#X0, R5F101GEDFB#X0, R5F101GFDFB#X0, R5F101GGDFB#X0, R5F101GHDFB#X0, R5F101GJDFB#X0, R5F101GKDFB#X0, R5F101GLDFB#X0 |

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

Table 1-1. List of Ordering Part Numbers

(6/12)

| Pin count | Package | Data flash | Fields of Application ^{Note} | Ordering Part Number |
|-----------|--|-------------|---------------------------------------|--|
| 48 pins | 48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch) | Mounted | A | R5F100GAANA#U0, R5F100GCANA#U0, R5F100GDANA#U0, R5F100GEANA#U0, R5F100GFANA#U0, R5F100GGANA#U0, R5F100GHANA#U0, R5F100GJANA#U0, R5F100GKANA#U0, R5F100GLANA#U0 R5F100GAANA#W0, R5F100GCANA#W0, R5F100GDANA#W0, R5F100GEANA#W0, R5F100GFANA#W0, R5F100GGANA#W0, R5F100GHANA#W0, R5F100GJANA#W0, R5F100GKANA#W0, R5F100GLANA#W0 |
| | | | D | R5F100GADNA#U0, R5F100GCDNA#U0, R5F100GDDNA#U0, R5F100GEDNA#U0, R5F100GFDNA#U0, R5F100GGDNA#U0, R5F100GHDNA#U0, R5F100GJDNA#U0, R5F100GKDNA#U0, R5F100GLDNA#U0 R5F100GADNA#W0, R5F100GCDNA#W0, R5F100GDDNA#W0, R5F100GEDNA#W0, R5F100GFDNA#W0, R5F100GGDNA#W0, R5F100GHDNA#W0, R5F100GJDNA#W0, R5F100GKDNA#W0, R5F100GLDNA#W0 |
| | | | G | R5F100GAGNA#U0, R5F100GCGNA#U0, R5F100GDGNA#U0, R5F100GEGNA#U0, R5F100GFGNA#U0, R5F100GGGNA#U0, R5F100GHGNA#U0, R5F100GJGNA#U0 R5F100GAGNA#W0, R5F100GCGNA#W0, R5F100GDGNA#W0, R5F100GEGNA#W0, R5F100GFGNA#W0, R5F100GGGNA#W0, R5F100GHGNA#W0, R5F100GJGNA#W0 |
| | | Not mounted | A | R5F101GAANA#U0, R5F101GCANA#U0, R5F101GDANA#U0, R5F101GEANA#U0, R5F101GFANA#U0, R5F101GGANA#U0, R5F101GHANA#U0, R5F101GJANA#U0, R5F101GKANA#U0, R5F101GLANA#U0 R5F101GAANA#W0, R5F101GCANA#W0, R5F101GDANA#W0, R5F101GEANA#W0, R5F101GFANA#W0, R5F101GGANA#W0, R5F101GHANA#W0, R5F101GJANA#W0, R5F101GKANA#W0, R5F101GLANA#W0 |
| | | | D | R5F101GADNA#U0, R5F101GCDNA#U0, R5F101GDDNA#U0, R5F101GEDNA#U0, R5F101GFDNA#U0, R5F101GGDNA#U0, R5F101GHDNA#U0, R5F101GJDNA#U0, R5F101GKDNA#U0, R5F101GLDNA#U0 R5F101GADNA#W0, R5F101GCDNA#W0, R5F101GDDNA#W0, R5F101GEDNA#W0, R5F101GFDNA#W0, R5F101GGDNA#W0, R5F101GHDNA#W0, R5F101GJDNA#W0, R5F101GKDNA#W0, R5F101GLDNA#W0 |

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13.**

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

Table 1-1. List of Ordering Part Numbers

(7/12)

| Pin count | Package | Data flash | Fields of Application ^{Note} | Ordering Part Number |
|-----------|--|-------------|---------------------------------------|--|
| 52 pins | 52-pin plastic LQFP (10 × 10 mm, 0.65 mm pitch) | Mounted | A | R5F100JCAFA#V0, R5F100JDAFA#V0, R5F100JEAFA#V0, R5F100JFAFA#V0, R5F100JGAFA#V0, R5F100JHAFA#V0, R5F100JJAFA#V0, R5F100JKAFA#V0, R5F100JLAFA#V0 R5F100JCAFA#X0, R5F100JDAFA#X0, R5F100JEAFA#X0, R5F100JFAFA#X0, R5F100JGAFA#X0, R5F100JHAFA#X0, R5F100JJAFA#X0, R5F100JKAFA#X0, R5F100JLAFA#X0 |
| | | | D | R5F100JCDFA#V0, R5F100JDDFA#V0, R5F100JEDFA#V0, R5F100JFDFA#V0, R5F100JGDFA#V0, R5F100JHDFA#V0, R5F100JJDFA#V0, R5F100JKDFA#V0, R5F100JLDFA#V0 R5F100JCDFA#X0, R5F100JDDFA#X0, R5F100JEDFA#X0, R5F100JFDFA#X0, R5F100JGDFA#X0, R5F100JHDFA#X0, R5F100JJDFA#X0, R5F100JKDFA#X0, R5F100JLDFA#X0 |
| | | | G | R5F100JCGFA#V0, R5F100JDGFA#V0, R5F100JEGFA#V0, R5F100JFGFA#V0, R5F100JGGFA#V0, R5F100JHGFA#V0, R5F100JJGFA#V0 R5F100JCGFA#X0, R5F100JDGFA#X0, R5F100JEGFA#X0, R5F100JFGFA#X0, R5F100JGGFA#X0, R5F100JHGFA#X0, R5F100JJGFA#X0 |
| | | Not mounted | A | R5F101JCAFA#V0, R5F101JDAFA#V0, R5F101JEAFA#V0, R5F101JFAFA#V0, R5F101JGAFA#V0, R5F101JHAFA#V0, R5F101JJAFA#V0, R5F101JKAFA#V0, R5F101JLAFA#V0 R5F101JCAFA#X0, R5F101JDAFA#X0, R5F101JEAFA#X0, R5F101JFAFA#X0, R5F101JGAFA#X0, R5F101JHAFA#X0, R5F101JJAFA#X0, R5F101JKAFA#X0, R5F101JLAFA#X0 |
| | | | D | R5F101JCDFA#V0, R5F101JDDFA#V0, R5F101JEDFA#V0, R5F101JFDFA#V0, R5F101JGDFA#V0, R5F101JHDFA#V0, R5F101JJDFA#V0, R5F101JKDFA#V0, R5F101JLDFA#V0 R5F101JCDFA#X0, R5F101JDDFA#X0, R5F101JEDFA#X0, R5F101JFDFA#X0, R5F101JGDFA#X0, R5F101JHDFA#X0, R5F101JJDFA#X0, R5F101JKDFA#X0, R5F101JLDFA#X0 |

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

Table 1-1. List of Ordering Part Numbers

(8/12)

| Pin count | Package | Data flash | Fields of Application ^{Note} | Ordering Part Number |
|-----------|--|-------------|---------------------------------------|--|
| 64 pins | 64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch) | Mounted | A | R5F100LCAFA#V0, R5F100LDAFA#V0, R5F100LEAFA#V0, R5F100LFAFA#V0, R5F100LGAF#V0, R5F100LHAF#V0, R5F100LJAF#V0, R5F100LKAF#V0, R5F100LLAF#V0 R5F100LCAFA#X0, R5F100LDAFA#X0, R5F100LEAFA#X0, R5F100LFAFA#X0, R5F100LGAF#X0, R5F100LHAF#X0, R5F100LJAF#X0, R5F100LKAF#X0, R5F100LLAF#X0 |
| | | | D | R5F100LCDFA#V0, R5F100LDDFA#V0, R5F100LEDFA#V0, R5F100LFDFA#V0, R5F100LGDF#V0, R5F100LHDF#V0, R5F100LJDF#V0, R5F100LKDF#V0, R5F100LLDF#V0 R5F100LCDFA#X0, R5F100LDDFA#X0, R5F100LEDFA#X0, R5F100LFDFA#X0, R5F100LGDF#X0, R5F100LHDF#X0, R5F100LJDF#X0, R5F100LKDF#X0, R5F100LLDF#X0 |
| | | | G | R5F100LCGFA#V0, R5F100LDGFA#V0, R5F100LEGFA#V0, R5F100LFGFA#V0 R5F100LCGFA#X0, R5F100LDGFA#X0, R5F100LEGFA#X0, R5F100LFGFA#X0 R5F100LGGFA#V0, R5F100LHGFA#V0, R5F100LJGFA#V0 R5F100LGGFA#X0, R5F100LHGFA#X0, R5F100LJGFA#X0 |
| | | Not mounted | A | R5F101LCAFA#V0, R5F101LDAFA#V0, R5F101LEAFA#V0, R5F101LFAFA#V0, R5F101LGAF#V0, R5F101LHAF#V0, R5F101LJAF#V0, R5F101LKAF#V0, R5F101LLAF#V0 R5F101LCAFA#X0, R5F101LDAFA#X0, R5F101LEAFA#X0, R5F101LFAFA#X0, R5F101LGAF#X0, R5F101LHAF#X0, R5F101LJAF#X0, R5F101LKAF#X0, R5F101LLAF#X0 |
| | | | D | R5F101LCDFA#V0, R5F101LDDFA#V0, R5F101LEDFA#V0, R5F101LFDFA#V0, R5F101LGDF#V0, R5F101LHDF#V0, R5F101LJDF#V0, R5F101LKDF#V0, R5F101LLDF#V0 R5F101LCDFA#X0, R5F101LDDFA#X0, R5F101LEDFA#X0, R5F101LFDFA#X0, R5F101LGDF#X0, R5F101LHDF#X0, R5F101LJDF#X0, R5F101LKDF#X0, R5F101LLDF#X0 |

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

Table 1-1. List of Ordering Part Numbers

(9/12)

| Pin count | Package | Data flash | Fields of Application <small>Note</small> | Ordering Part Number |
|--|---|------------|--|--|
| 64 pins | 64-pin plastic LQFP (10 × 10 mm, 0.5 mm pitch) | Mounted | A | R5F100LCAFB#V0, R5F100LDAFB#V0, R5F100LEAFB#V0, R5F100LFAFB#V0, R5F100LGAFB#V0, R5F100LHAFB#V0, R5F100LJAFB#V0, R5F100LKAFB#V0, R5F100LLAFB#V0 R5F100LCAFB#X0, R5F100LDAFB#X0, R5F100LEAFB#X0, R5F100LFAFB#X0, R5F100LGAFB#X0, R5F100LHAFB#X0, R5F100LJAFB#X0, R5F100LKAFB#X0, R5F100LLAFB#X0 |
| | | | D | R5F100LCDFB#V0, R5F100LDDFB#V0, R5F100LEDFB#V0, R5F100LFDDB#V0, R5F100LGDFB#V0, R5F100LHDFB#V0, R5F100LJDFB#V0, R5F100LKDFB#V0, R5F100LLDFB#V0 R5F100LCDFB#X0, R5F100LDDFB#X0, R5F100LEDFB#X0, R5F100LFDDB#X0, R5F100LGDFB#X0, R5F100LHDFB#X0, R5F100LJDFB#X0, R5F100LKDFB#X0, R5F100LLDFB#X0 |
| | | | G | R5F100LCGFB#V0, R5F100LDGFB#V0, R5F100LEGFB#V0, R5F100LFGFB#V0 R5F100LCGFB#X0, R5F100LDGFB#X0, R5F100LEGFB#X0, R5F100LFGFB#X0 R5F100LGGFB#V0, R5F100LHGFB#V0, R5F100LJGFB#V0 R5F100LGGFB#X0, R5F100LHGFB#X0, R5F100LJGFB#X0 |
| | Not mounted | A | R5F101LCAFB#V0, R5F101LDAFB#V0, R5F101LEAFB#V0, R5F101LFAFB#V0, R5F101LGAFB#V0, R5F101LHAFB#V0, R5F101LJAFB#V0, R5F101LKAFB#V0, R5F101LLAFB#V0 R5F101LCAFB#X0, R5F101LDAFB#X0, R5F101LEAFB#X0, R5F101LFAFB#X0, R5F101LGAFB#X0, R5F101LHAFB#X0, R5F101LJAFB#X0, R5F101LKAFB#X0, R5F101LLAFB#X0 | |
| | | D | R5F101LCDFB#V0, R5F101LDDFB#V0, R5F101LEDFB#V0, R5F101LFDDB#V0, R5F101LGDFB#V0, R5F101LHDFB#V0, R5F101LJDFB#V0, R5F101LKDFB#V0, R5F101LLDFB#V0 R5F101LCDFB#X0, R5F101LDDFB#X0, R5F101LEDFB#X0, R5F101LFDDB#X0, R5F101LGDFB#X0, R5F101LHDFB#X0, R5F101LJDFB#X0, R5F101LKDFB#X0, R5F101LLDFB#X0 | |
| | | G | R5F100LCABG#U0, R5F100LDABG#U0, R5F100LEABG#U0, R5F100LFABG#U0, R5F100LGABG#U0, R5F100LHABG#U0, R5F100LJABG#U0 R5F100LCABG#W0, R5F100LDABG#W0, R5F100LEABG#W0, R5F100LFABG#W0, R5F100LGABG#W0, R5F100LHABG#W0, R5F100LJABG#W0 | |
| 64-pin plastic VFBGA (4 × 4 mm, 0.4 mm pitch) | Mounted | A | R5F100LCABG#U0, R5F100LDABG#U0, R5F100LEABG#U0, R5F100LFABG#U0, R5F100LGABG#U0, R5F100LHABG#U0, R5F100LJABG#U0 R5F100LCABG#W0, R5F100LDABG#W0, R5F100LEABG#W0, R5F100LFABG#W0, R5F100LGABG#W0, R5F100LHABG#W0, R5F100LJABG#W0 | |
| | | G | R5F100LCGBG#U0, R5F100LDGBG#U0, R5F100LEGBG#U0, R5F100LFGGB#U0, R5F100LGGGB#U0, R5F100LHGBG#U0, R5F100LJGBG#U0 R5F100LCGBG#W0, R5F100LDGBG#W0, R5F100LEGBG#W0, R5F100LFGGB#W0, R5F100LGGGB#W0, R5F100LHGBG#W0, R5F100LJGBG#W0 | |
| | Not mounted | A | R5F101LCABG#U0, R5F101LDABG#U0, R5F101LEABG#U0, R5F101LFABG#U0, R5F101LGABG#U0, R5F101LHABG#U0, R5F101LJABG#U0 R5F101LCABG#W0, R5F101LDABG#W0, R5F101LEABG#W0, R5F101LFABG#W0, R5F101LGABG#W0, R5F101LHABG#W0, R5F101LJABG#W0 | |

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

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Table 1-1. List of Ordering Part Numbers

(10/12)

| Pin count | Package | Data flash | Fields of Application <small>Note</small> | Ordering Part Number |
|-------------|--|-------------|--|--|
| 80 pins | 80-pin plastic LQFP (14 × 14 mm, 0.65 mm pitch) | Mounted | A | R5F100MFAFA#V0, R5F100MGAGA#V0, R5F100MHAFA#V0, R5F100MJAJA#V0, R5F100MKAKA#V0, R5F100MLAFA#V0 R5F100MFAFA#X0, R5F100MGAGA#X0, R5F100MHAFA#X0, R5F100MJAJA#X0, R5F100MKAKA#X0, R5F100MLAFA#X0 |
| | | | D | R5F100MFDFA#V0, R5F100MGDFA#V0, R5F100MHDFA#V0, R5F100MJDFA#V0, R5F100MKDFA#V0, R5F100MLDFA#V0 R5F100MFDFA#X0, R5F100MGDFA#X0, R5F100MHDFA#X0, R5F100MJDFA#X0, R5F100MKDFA#X0, R5F100MLDFA#X0 |
| | | Not mounted | A | R5F101MFAFA#V0, R5F101MGAGA#V0, R5F101MHAFA#V0, R5F101MJAJA#V0, R5F101MKAKA#V0, R5F101MLAFA#V0 R5F101MFAFA#X0, R5F101MGAGA#X0, R5F101MHAFA#X0, R5F101MJAJA#X0, R5F101MKAKA#X0, R5F101MLAFA#X0 |
| | | | D | R5F101MFDFA#V0, R5F101MGDFA#V0, R5F101MHDFA#V0, R5F101MJDFA#V0, R5F101MKDFA#V0, R5F101MLDFA#V0 R5F101MFDFA#X0, R5F101MGDFA#X0, R5F101MHDFA#X0, R5F101MJDFA#X0, R5F101MKDFA#X0, R5F101MLDFA#X0 |
| | 80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch) | Mounted | A | R5F100MFAFB#V0, R5F100MGAFB#V0, R5F100MHAFB#V0, R5F100MJAFB#V0, R5F100MKAFB#V0, R5F100MLAFB#V0 R5F100MFAFB#X0, R5F100MGAFB#X0, R5F100MHAFB#X0, R5F100MJAFB#X0, R5F100MKAFB#X0, R5F100MLAFB#X0 |
| | | | D | R5F100MFDDB#V0, R5F100MGDFB#V0, R5F100MHDFB#V0, R5F100MJDDB#V0, R5F100MKDFB#V0, R5F100MLDFB#V0 R5F100MFDDB#X0, R5F100MGDFB#X0, R5F100MHDFB#X0, R5F100MJDDB#X0, R5F100MKDFB#X0, R5F100MLDFB#X0 |
| Not mounted | | A | R5F101MFAFB#V0, R5F101MGAFB#V0, R5F101MHAFB#V0, R5F101MJAFB#V0, R5F101MKAFB#V0, R5F101MLAFB#V0 R5F101MFAFB#X0, R5F101MGAFB#X0, R5F101MHAFB#X0, R5F101MJAFB#X0, R5F101MKAFB#X0, R5F101MLAFB#X0 | |
| | | D | R5F101MFDDB#V0, R5F101MGDFB#V0, R5F101MHDFB#V0, R5F101MJDDB#V0, R5F101MKDFB#V0, R5F101MLDFB#V0 R5F101MFDDB#X0, R5F101MGDFB#X0, R5F101MHDFB#X0, R5F101MJDDB#X0, R5F101MKDFB#X0, R5F101MLDFB#X0 | |

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

Table 1-1. List of Ordering Part Numbers

(11/12)

| Pin count | Package | Data flash | Fields of Application <small>Note</small> | Ordering Part Number |
|-----------|---|------------|--|--|
| 100 pins | 100-pin plastic LFQFP (14 × 14 mm, 0.5 mm pitch) | Mounted | A | R5F100PFAFB#V0, R5F100PGAFA#V0, R5F100PHAFA#V0, R5F100PJAFB#V0, R5F100PKAFB#V0, R5F100PLAFB#V0 R5F100PFAFB#X0, R5F100PGAFA#X0, R5F100PHAFA#X0, R5F100PJAFB#X0, R5F100PKAFB#X0, R5F100PLAFB#X0 |
| | | | D | R5F100PFDFB#V0, R5F100PGDFB#V0, R5F100PHDFB#V0, R5F100PJDFB#V0, R5F100PKDFB#V0, R5F100PLDFB#V0 R5F100PFDFB#X0, R5F100PGDFB#X0, R5F100PHDFB#X0, R5F100PJDFB#X0, R5F100PKDFB#X0, R5F100PLDFB#X0 |
| | | | G | R5F100PFGFB#V0, R5F100PGGFB#V0, R5F100PHGFB#V0, R5F100PJGFB#V0 R5F100PFGFB#X0, R5F100PGGFB#X0, R5F100PHGFB#X0, R5F100PJGFB#X0 |
| | | | | R5F100PFAFB#V0, R5F100PGAFA#V0, R5F100PHAFA#V0, R5F100PJAFB#V0, R5F100PKAFB#V0, R5F100PLAFB#V0 R5F100PFAFB#X0, R5F100PGAFA#X0, R5F100PHAFA#X0, R5F100PJAFB#X0, R5F100PKAFB#X0, R5F100PLAFB#X0 |
| | 100-pin plastic LQFP (14 × 20 mm, 0.65 mm pitch) | Mounted | A | R5F100PFAFA#V0, R5F100PGAFA#V0, R5F100PHAFA#V0, R5F100PJAFB#V0, R5F100PKAFB#V0, R5F100PLAFB#V0 R5F100PFAFA#X0, R5F100PGAFA#X0, R5F100PHAFA#X0, R5F100PJAFB#X0, R5F100PKAFB#X0, R5F100PLAFB#X0 |
| | | | D | R5F100PFDA#V0, R5F100PGDA#V0, R5F100PHDA#V0, R5F100PJDA#V0, R5F100PKDA#V0, R5F100PLDA#V0 R5F100PFDA#X0, R5F100PGDA#X0, R5F100PHDA#X0, R5F100PJDA#X0, R5F100PKDA#X0, R5F100PLDA#X0 |
| | Not mounted | A | R5F100PFAFA#V0, R5F100PGAFA#V0, R5F100PHAFA#V0, R5F100PJAFB#V0, R5F100PKAFB#V0, R5F100PLAFB#V0 R5F100PFAFA#X0, R5F100PGAFA#X0, R5F100PHAFA#X0, R5F100PJAFB#X0, R5F100PKAFB#X0, R5F100PLAFB#X0 | |
| | | D | R5F100PFDA#V0, R5F100PGDA#V0, R5F100PHDA#V0, R5F100PJDA#V0, R5F100PKDA#V0, R5F100PLDA#V0 R5F100PFDA#X0, R5F100PGDA#X0, R5F100PHDA#X0, R5F100PJDA#X0, R5F100PKDA#X0, R5F100PLDA#X0 | |

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13.**

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

Table 1-1. List of Ordering Part Numbers

(12/12)

| Pin count | Package | Data flash | Fields of Application ^{Note} | Ordering Part Number |
|-----------|---|-------------|---------------------------------------|---|
| 128 pins | 128-pin plastic LFQFP (14 × 20 mm, 0.5 mm pitch) | Mounted | A | R5F100SHAFB#V0, R5F100SJAFB#V0, R5F100SKAFB#V0, R5F100SLAFB#V0 |
| | | | D | R5F100SHAFB#X0, R5F100SJAFB#X0, R5F100SKAFB#X0, R5F100SLAFB#X0 R5F100SHDFB#V0, R5F100SJDFB#V0, R5F100SKDFB#V0, R5F100SLDFB#V0 R5F100SHDFB#X0, R5F100SJDFB#X0, R5F100SKDFB#X0, R5F100SLDFB#X0 |
| | | Not mounted | A | R5F101SHAFB#V0, R5F101SJAFB#V0, R5F101SKAFB#V0, R5F101SLAFB#V0 |
| | | | D | R5F101SHAFB#X0, R5F101SJAFB#X0, R5F101SKAFB#X0, R5F101SLAFB#X0 R5F101SHDFB#V0, R5F101SJDFB#V0, R5F101SKDFB#V0, R5F101SLDFB#V0 R5F101SHDFB#X0, R5F101SJDFB#X0, R5F101SKDFB#X0, R5F101SLDFB#X0 |

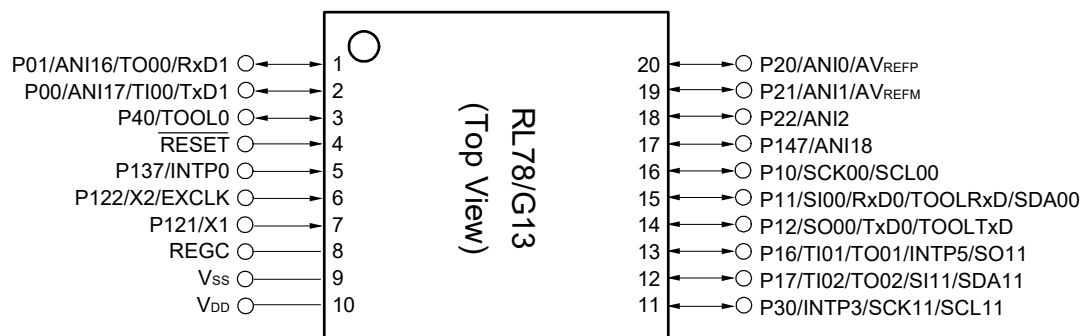
Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3 Pin Configuration (Top View)

1.3.1 20-pin products

- 20-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)

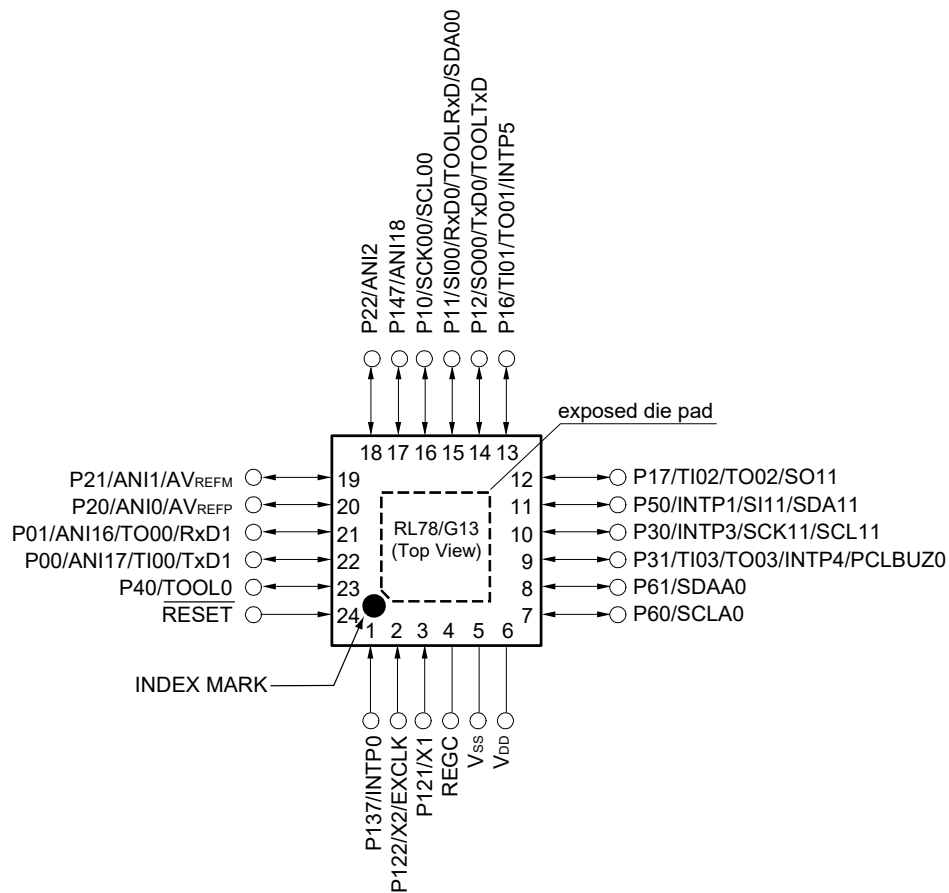


Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F).

Remark For pin identification, see 1.4 Pin Identification.

1.3.2 24-pin products

- 24-pin plastic HWQFN (4 × 4 mm, 0.5 mm pitch)



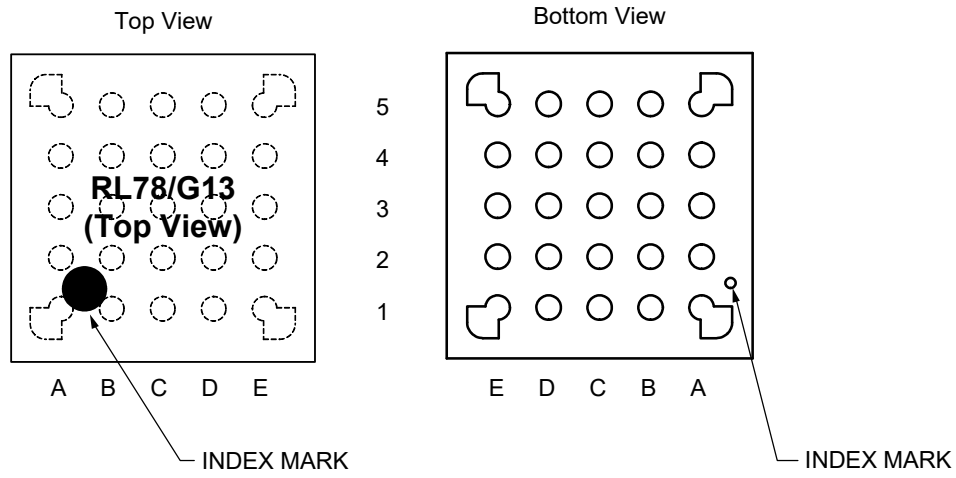
Caution Connect the REGC pin to V_{ss} via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see 1.4 Pin Identification.

2. It is recommended to connect an exposed die pad to V_{ss}.

1.3.3 25-pin products

- 25-pin plastic WFLGA (3 × 3 mm, 0.50 mm pitch)



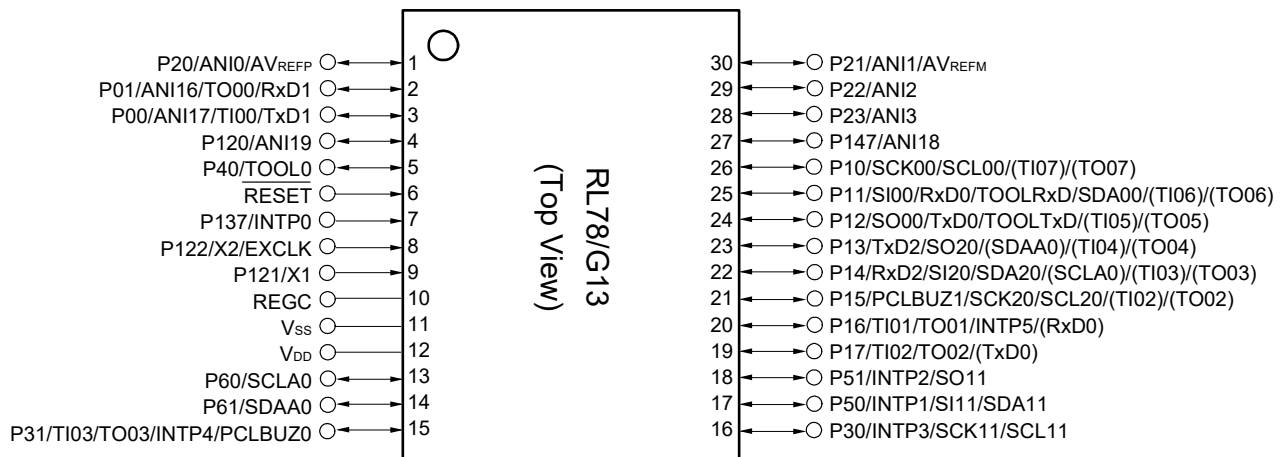
| | A | B | C | D | E | |
|---|-------------------|-----------------|-------------------------------------|-------------------------------|---|---|
| 5 | P40/TOOL0 | RESET | P01/ANI16/ TO00/RxD1 | P22/ANI2 | P147/ANI18 | 5 |
| 4 | P122/X2/ EXCLK | P137/INTP0 | P00/ANI17/ TI00/TxD1 | P21/ANI1/ AVREFM | P10/SCK00/ SCL00 | 4 |
| 3 | P121/X1 | V _{DD} | P20/ANI0/ AVREFP | P12/SO00/ TxD0/ TOOLTxD | P11/SI00/ RxD0/ TOOLRxD/ SDA00 | 3 |
| 2 | REGC | V _{SS} | P30/INTP3/ SCK11/SCL11 | P17/TI02/ TO02/SO11 | P50/INTP1/ SI11/SDA11 | 2 |
| 1 | P60/SCLA0 | P61/SDAA0 | P31/TI03/ TO03/INTP4/ PCLBUZ0 | P16/TI01/ TO01/INTP5 | P130 | 1 |
| | A | B | C | D | E | |

Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

Remark For pin identification, see 1.4 Pin Identification.

1.3.4 30-pin products

- 30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)



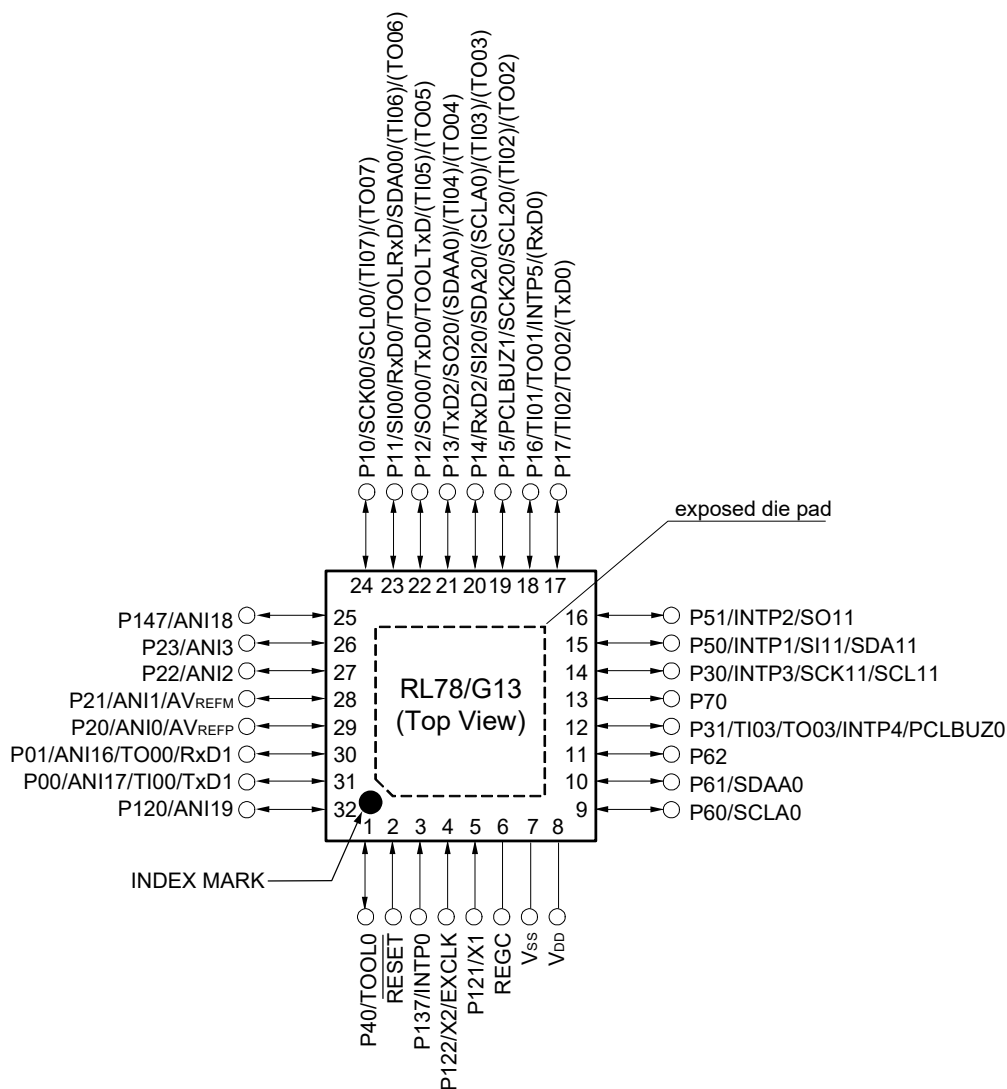
Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F).

Remarks 1. For pin identification, see 1.4 Pin Identification.

- Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.3.5 32-pin products

- 32-pin plastic HWQFN (5 × 5 mm, 0.5 mm pitch)



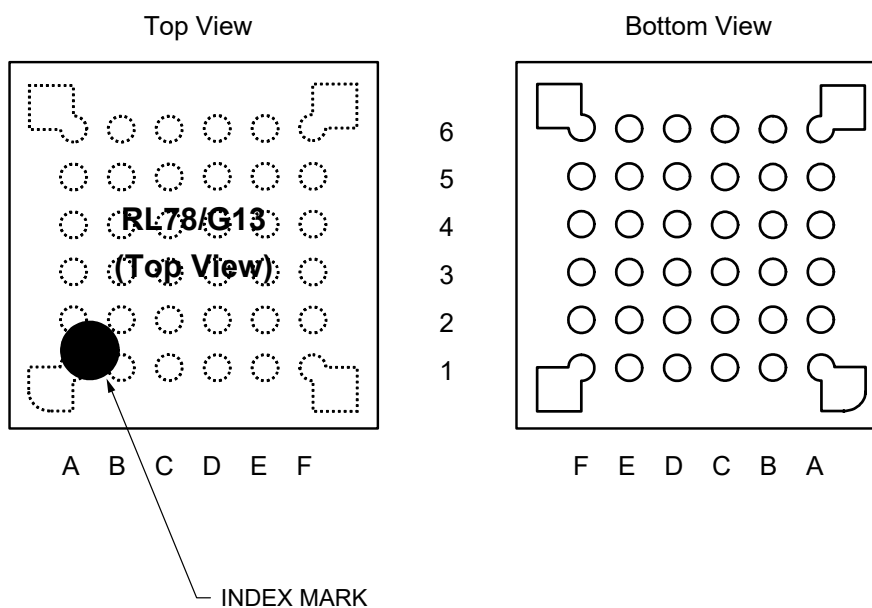
Caution Connect the REGC pin to V_{ss} via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see 1.4 Pin Identification.

- Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.
- It is recommended to connect an exposed die pad to V_{ss}.

1.3.6 36-pin products

- 36-pin plastic WFLGA (4 × 4 mm, 0.5 mm pitch)



| | A | B | C | D | E | F | |
|---|---------------------------|--------------------------------|---|---|---------------------------------|---------------------------------|---|
| 6 | P60/SCLA0 | V _{DD} | P121/X1 | P122/X2/EXCLK | P137/INTP0 | P40/TOOL0 | 6 |
| 5 | P62 | P61/SDAA0 | V _{SS} | REGC | RESET | P120/ANI19 | 5 |
| 4 | P72/SO21 | P71/SI21/ SDA21 | P14/RxD2/SI20/ SDA20/(SCLA0) /(TI03)/(TO03) | P31/TI03/TO03/ INTP4/ PCLBUZ0 | P00/TI00/TxD1 | P01/TO00/RxD1 | 4 |
| 3 | P50/INTP1/ SI11/SDA11 | P70/SCK21/ SCL21 | P15/PCLBUZ1/ SCK20/SCL20/ (TI02)/(TO02) | P22/ANI2 | P20/ANI0/ AV _{REFP} | P21/ANI1/ AV _{REFM} | 3 |
| 2 | P30/INTP3/ SCK11/SCL11 | P16/TI01/TO01/ INTP5/(RxD0) | P12/SO00/ TxD0/TOOLTxD /(TI05)/(TO05) | P11/SI00/RxD0/ TOOLRxD/ SDA00/(TI06)/ (TO06) | P24/ANI4 | P23/ANI3 | 2 |
| 1 | P51/INTP2/ SO11 | P17/TI02/TO02/ (TxD0) | P13/TxD2/ SO20/(SDAA0)/ (TI04)/(TO04) | P10/SCK00/ SCL00/(TI07)/ (TO07) | P147/ANI18 | P25/ANI5 | 1 |
| | A | B | C | D | E | F | |

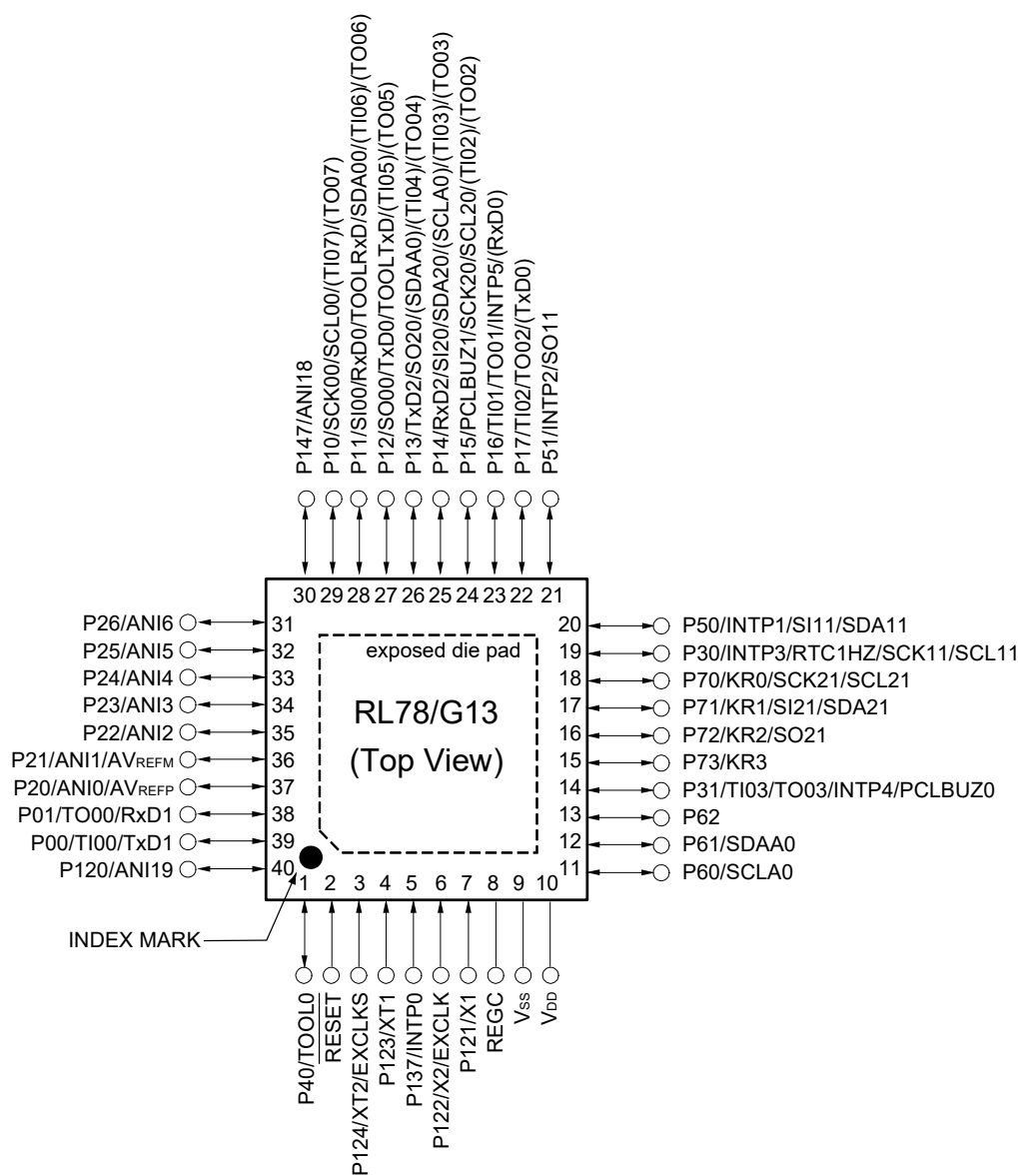
Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see 1.4 Pin Identification.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.3.7 40-pin products

- 40-pin plastic HWQFN (6 × 6 mm, 0.5 mm pitch)



Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

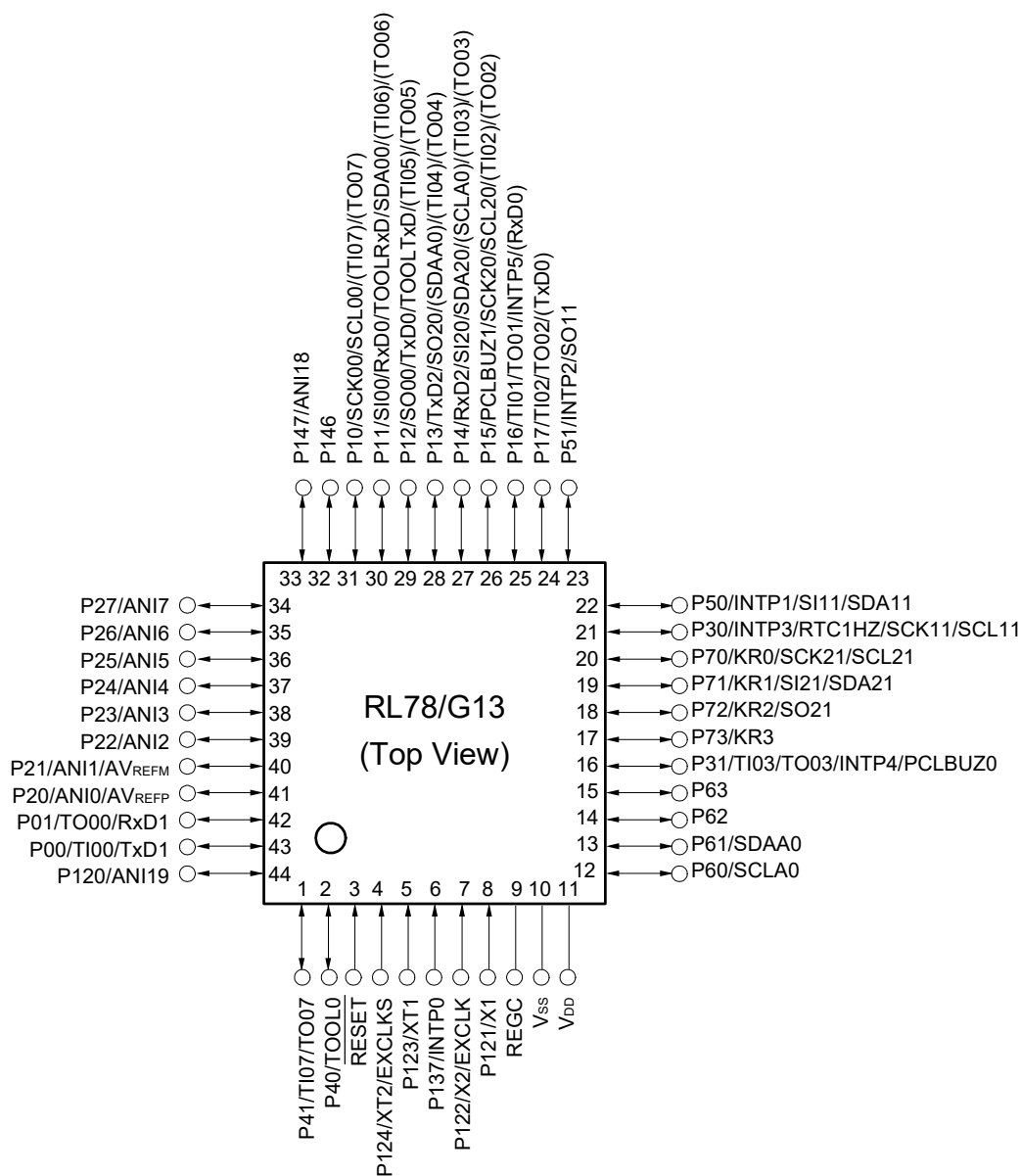
Remarks 1. For pin identification, see 1.4 Pin Identification.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

3. It is recommended to connect an exposed die pad to V_{SS}.

1.3.8 44-pin products

- 44-pin plastic LQFP (10 × 10 mm, 0.8 mm pitch)



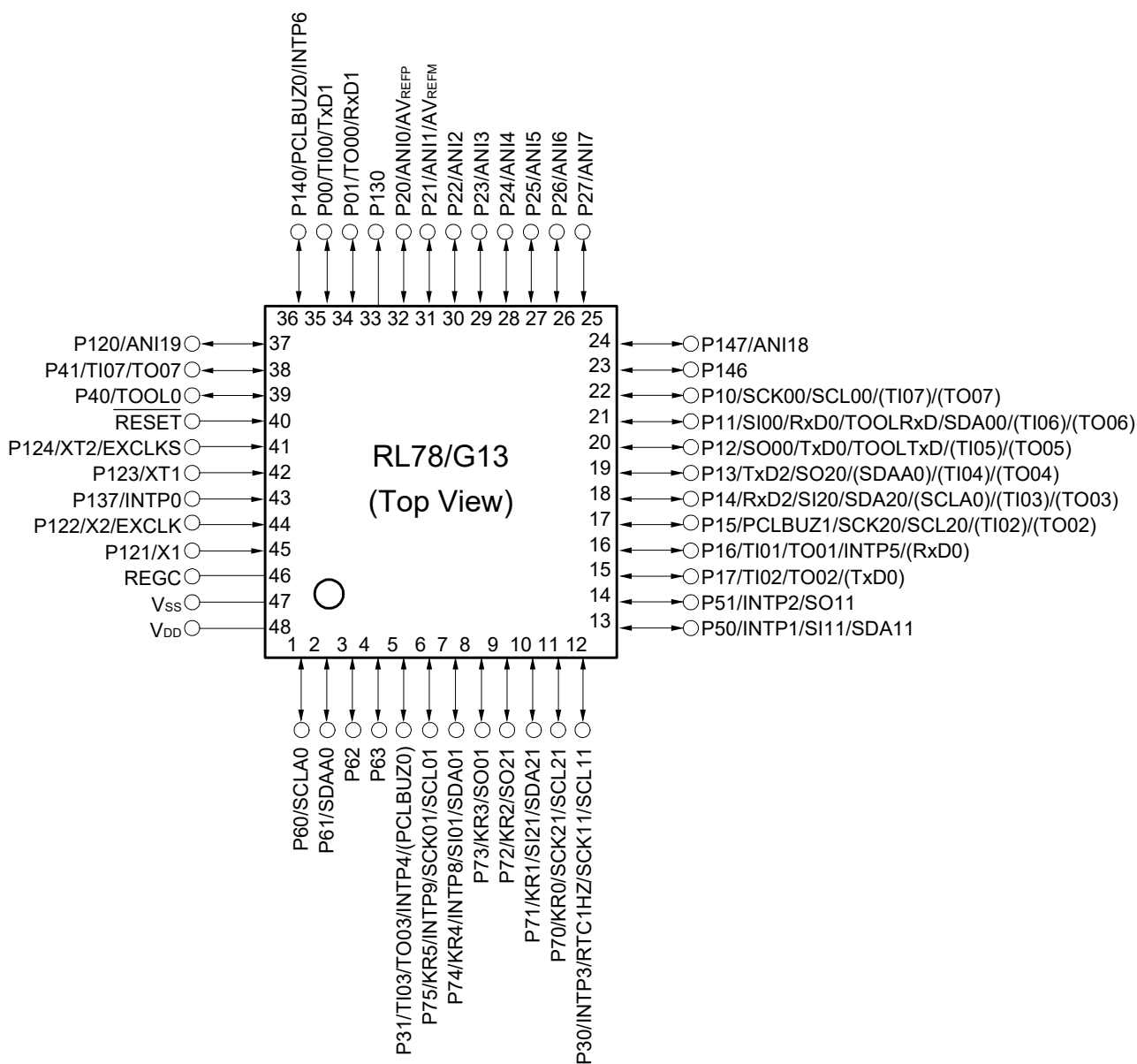
Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see 1.4 Pin Identification.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.3.9 48-pin products

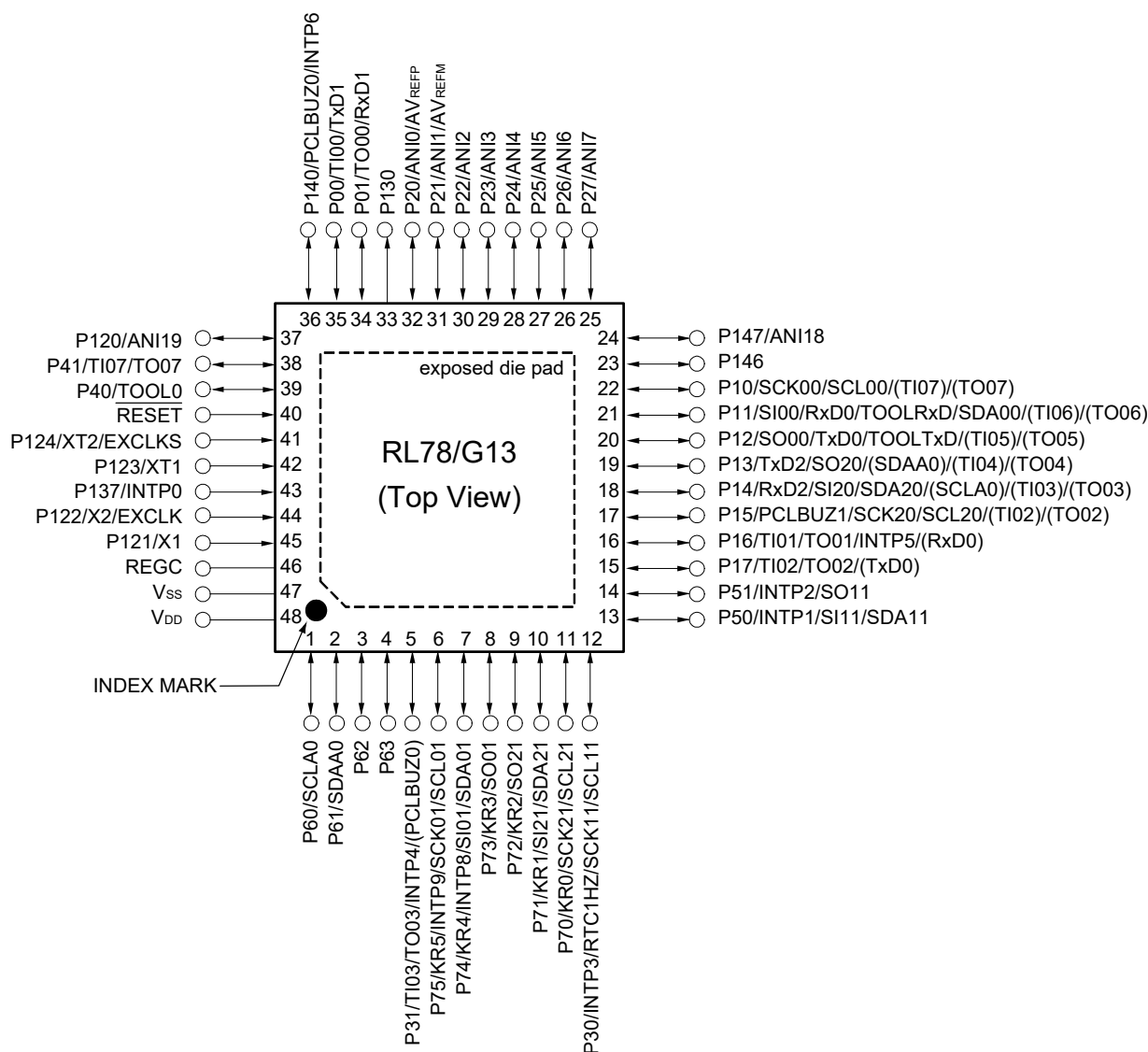
- 48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch)



Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

- Remarks 1.** For pin identification, see 1.4 Pin Identification.
- 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

- 48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch)



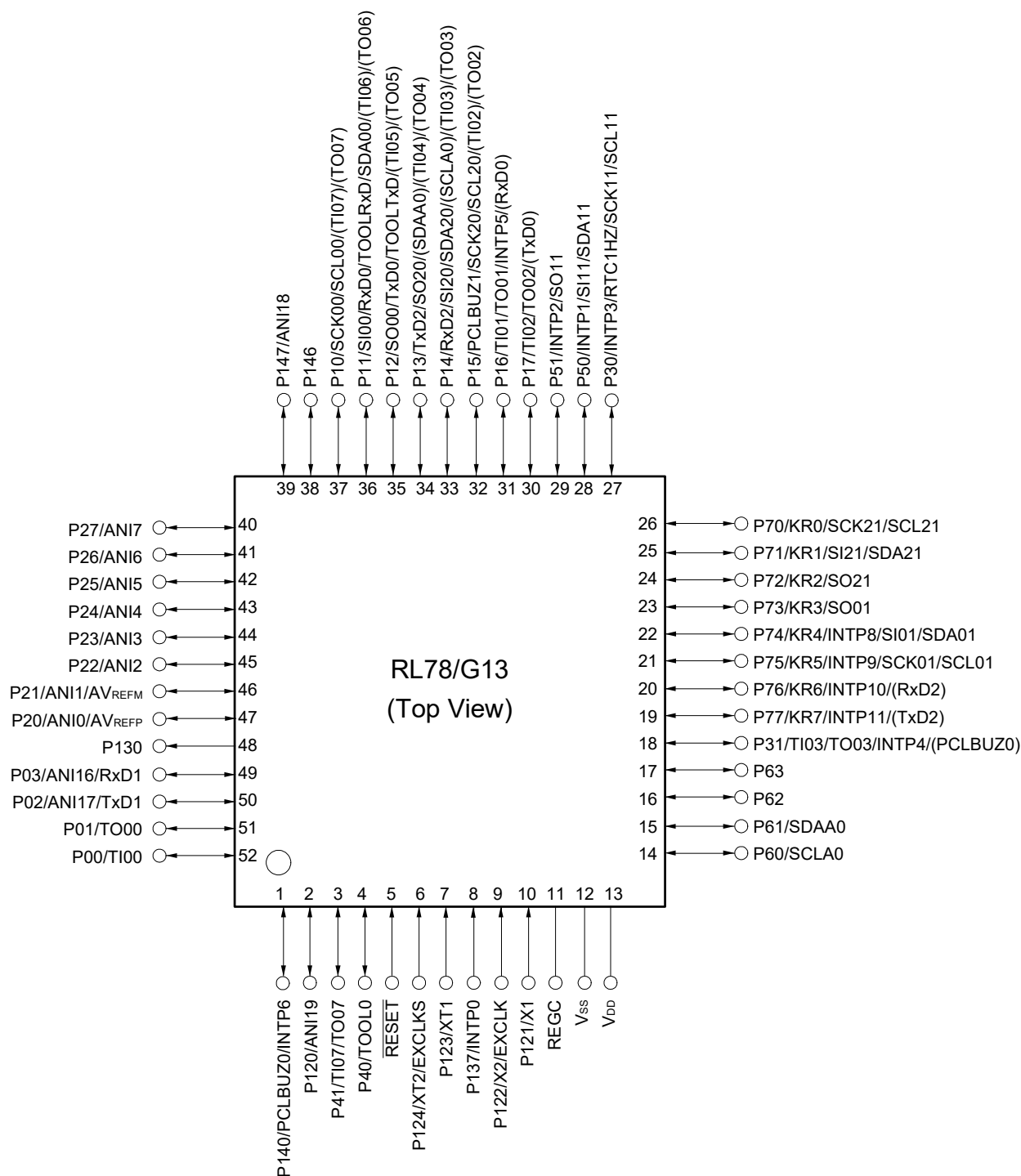
Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see 1.4 Pin Identification.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR) in the RL78/G13 User's Manual.
3. It is recommended to connect an exposed die pad to V_{SS}.

1.3.10 52-pin products

- 52-pin plastic LQFP (10 × 10 mm, 0.65 mm pitch)



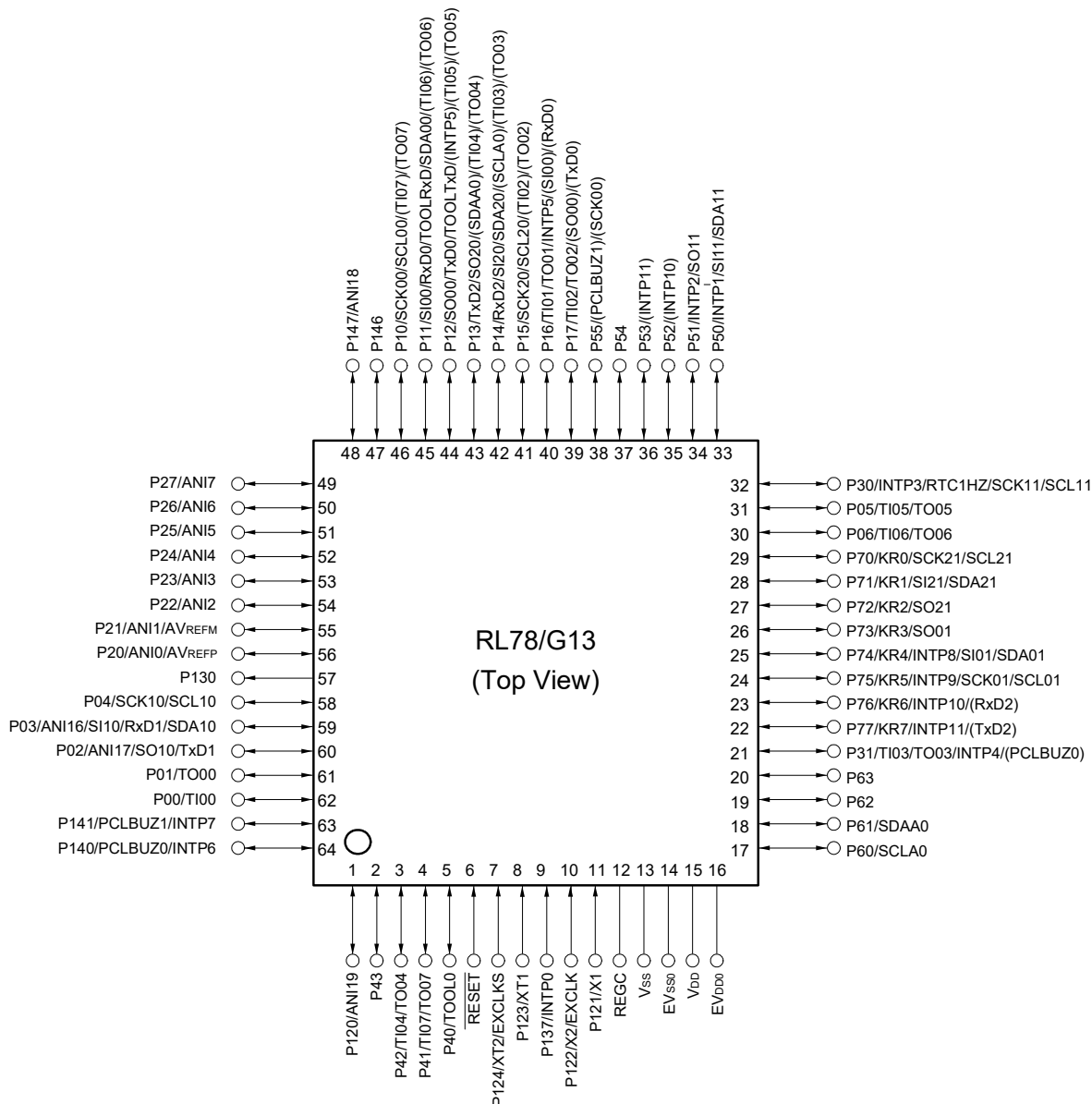
Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see 1.4 Pin Identification.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR) in the RL78/G13 User's Manual.

1.3.11 64-pin products

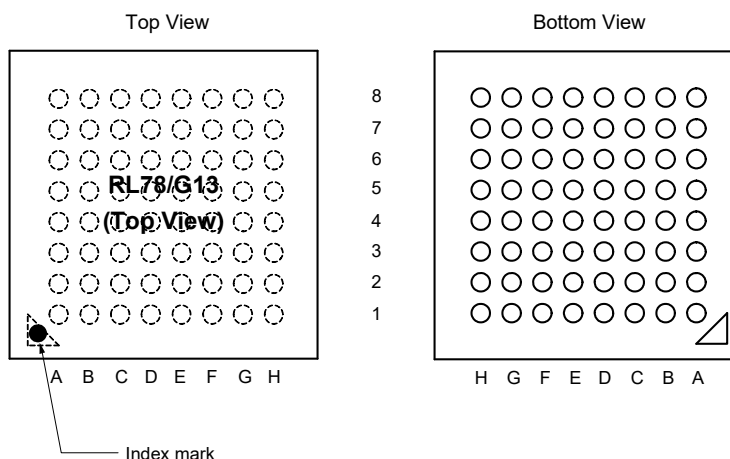
- 64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch)
- 64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)



- Cautions**
1. Make EV_{SS0} pin the same potential as V_{SS} pin.
 2. Make V_{DD} pin the potential that is higher than EV_{DD0} pin.
 3. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

- Remarks**
1. For pin identification, see 1.4 Pin Identification.
 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD0} pins and connect the V_{SS} and EV_{SS0} pins to separate ground lines.
 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

- 64-pin plastic VFBGA (4 × 4 mm, 0.4 mm pitch)



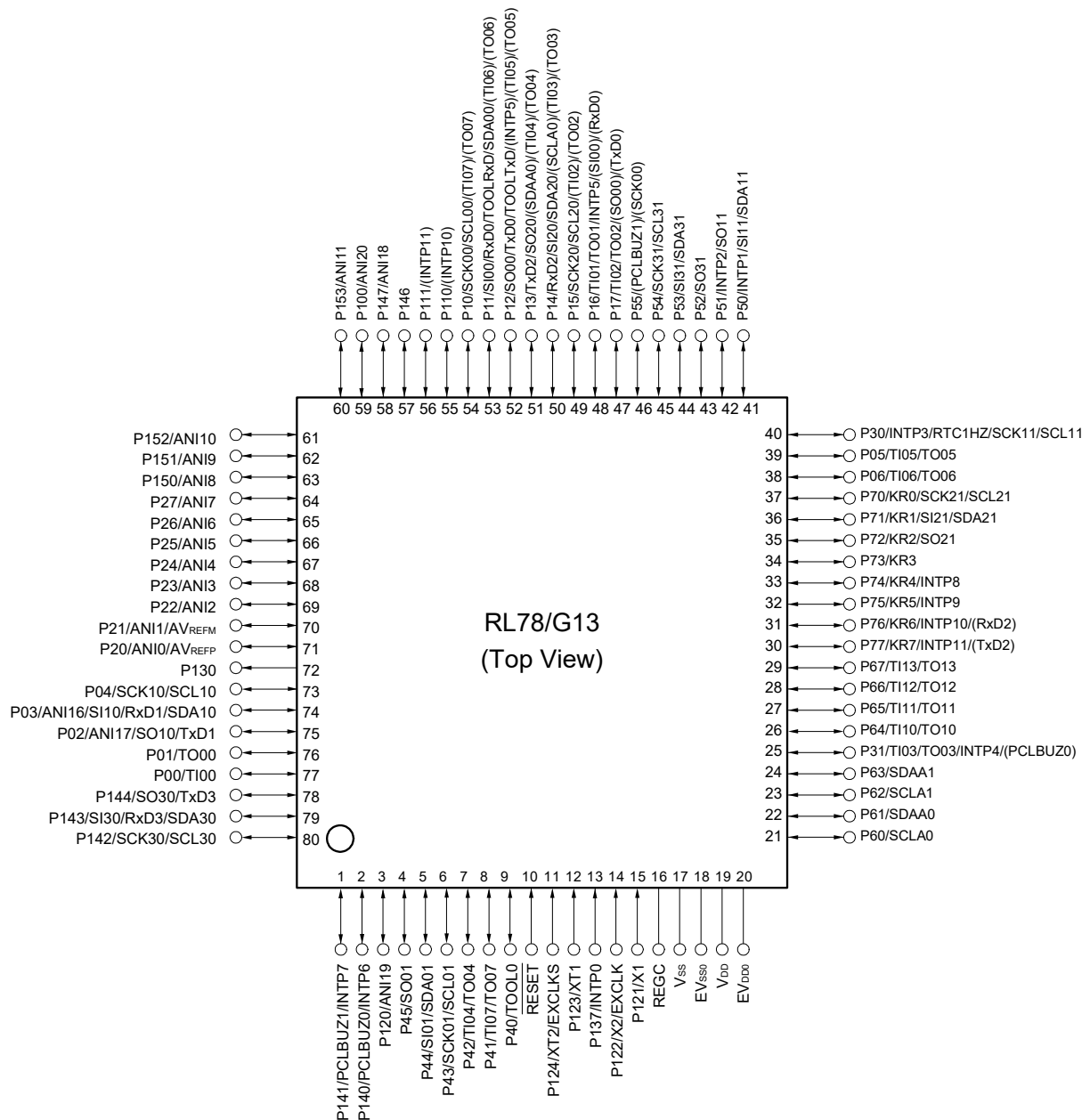
| Pin No. | Name | Pin No. | Name | Pin No. | Name | Pin No. | Name |
|---------|-----------------------------------|---------|---------------------------------|---------|---|---------|-----------------------------|
| A1 | P05/TI05/TO05 | C1 | P51/INTP2/SO11 | E1 | P13/TxD2/SO20/ (SDAA0)/(TI04)/(TO04) | G1 | P146 |
| A2 | P30/INTP3/RTC1HZ /SCK11/SCL11 | C2 | P71/KR1/SI21/SDA21 | E2 | P14/RxD2/SI20/SDA20 /(SCLA0)/(TI03)/(TO03) | G2 | P25/ANI5 |
| A3 | P70/KR0/SCK21 /SCL21 | C3 | P74/KR4/INTP8/SI01 /SDA01 | E3 | P15/SCK20/SCL20/ (TI02)/(TO02) | G3 | P24/ANI4 |
| A4 | P75/KR5/INTP9 /SCK01/SCL01 | C4 | P52/(INTP10) | E4 | P16/TI01/TO01/INTP5 /(SI00)/(RxD0) | G4 | P22/ANI2 |
| A5 | P77/KR7/INTP11/ (TxD2) | C5 | P53/(INTP11) | E5 | P03/ANI16/SI10/RxD1 /SDA10 | G5 | P130 |
| A6 | P61/SDAA0 | C6 | P63 | E6 | P41/TI07/TO07 | G6 | P02/ANI17/SO10/TxD1 |
| A7 | P60/SCLA0 | C7 | V _{SS} | E7 | RESET | G7 | P00/TI00 |
| A8 | EV _{DD0} | C8 | P121/X1 | E8 | P137/INTP0 | G8 | P124/XT2/EXCLKS |
| B1 | P50/INTP1/SI11 /SDA11 | D1 | P55/(PCLBUZ1)/ (SCK00) | F1 | P10/SCK00/SCL00/ (TI07)/(TO07) | H1 | P147/ANI18 |
| B2 | P72/KR2/SO21 | D2 | P06/TI06/TO06 | F2 | P11/SI00/RxD0 /TOOLRxD/SDA00/ (TI06)/(TO06) | H2 | P27/ANI7 |
| B3 | P73/KR3/SO01 | D3 | P17/TI02/TO02/ (SO00)/(TxD0) | F3 | P12/SO00/TxD0 /TOOLTxD/(INTP5)/ (TI05)/(TO05) | H3 | P26/ANI6 |
| B4 | P76/KR6/INTP10/ (RxD2) | D4 | P54 | F4 | P21/ANI1/AV _{REFM} | H4 | P23/ANI3 |
| B5 | P31/TI03/TO03 /INTP4/(PCLBUZ0) | D5 | P42/TI04/TO04 | F5 | P04/SCK10/SCL10 | H5 | P20/ANI0/AV _{REFP} |
| B6 | P62 | D6 | P40/TOOL0 | F6 | P43 | H6 | P141/PCLBUZ1/INTP7 |
| B7 | V _{DD} | D7 | REGC | F7 | P01/TO00 | H7 | P140/PCLBUZ0/INTP6 |
| B8 | EV _{SS0} | D8 | P122/X2/EXCLK | F8 | P123/XT1 | H8 | P120/ANI19 |

- Cautions**
1. Make EV_{SS0} pin the same potential as V_{SS} pin.
 2. Make V_{DD} pin the potential that is higher than EV_{DD0} pin.
 3. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

- Remarks**
1. For pin identification, see 1.4 Pin Identification.
 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD0} pins and connect the V_{SS} and EV_{SS0} pins to separate ground lines.
 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.3.12 80-pin products

- 80-pin plastic LQFP (14 × 14 mm, 0.65 mm pitch)
- 80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)

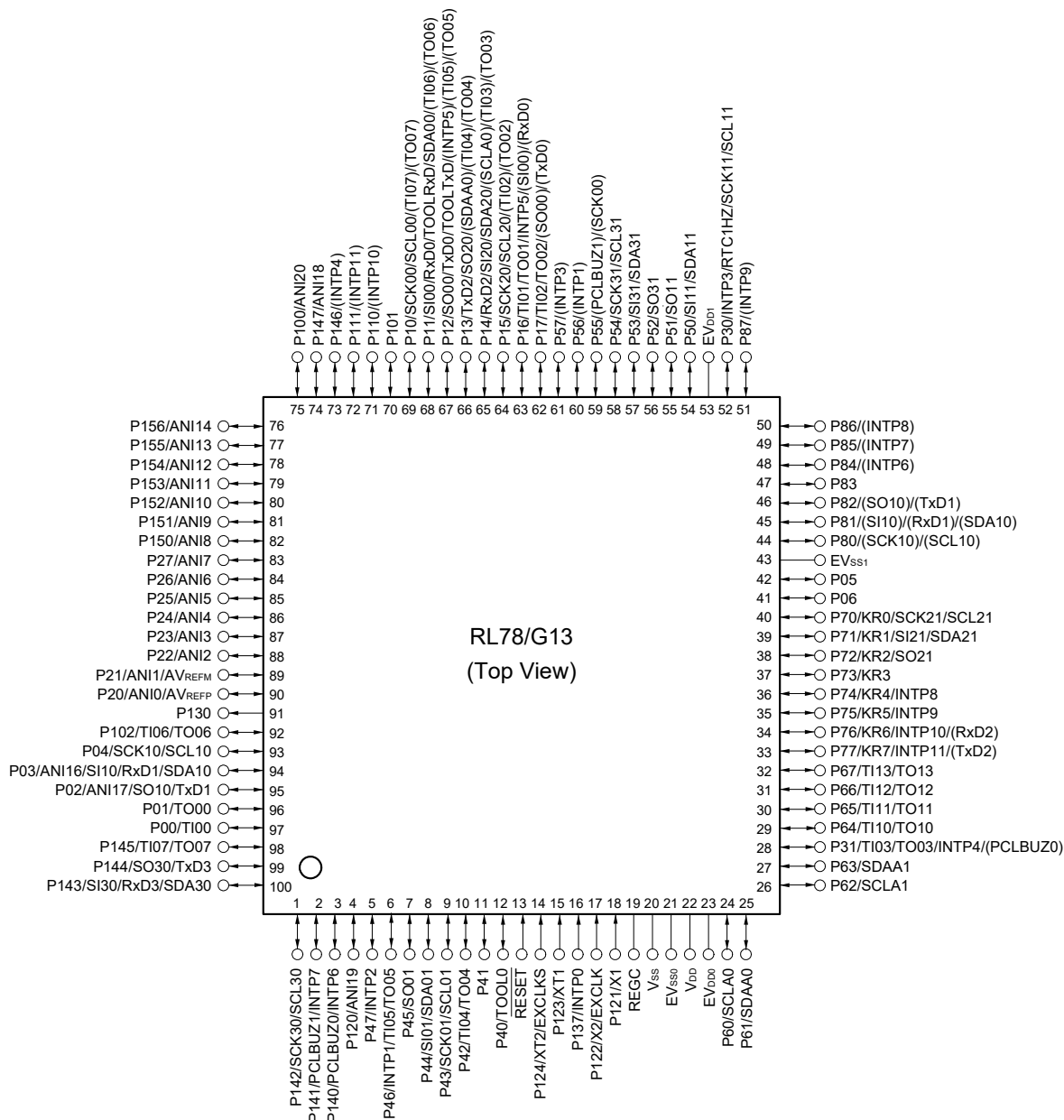


- Cautions**
1. Make EV_{SS0} pin the same potential as V_{SS} pin.
 2. Make V_{DD} pin the potential that is higher than EV_{DD0} pin.
 3. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

- Remarks**
1. For pin identification, see 1.4 Pin Identification.
 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD0} pins and connect the V_{SS} and EV_{SS0} pins to separate ground lines.
 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.3.13 100-pin products

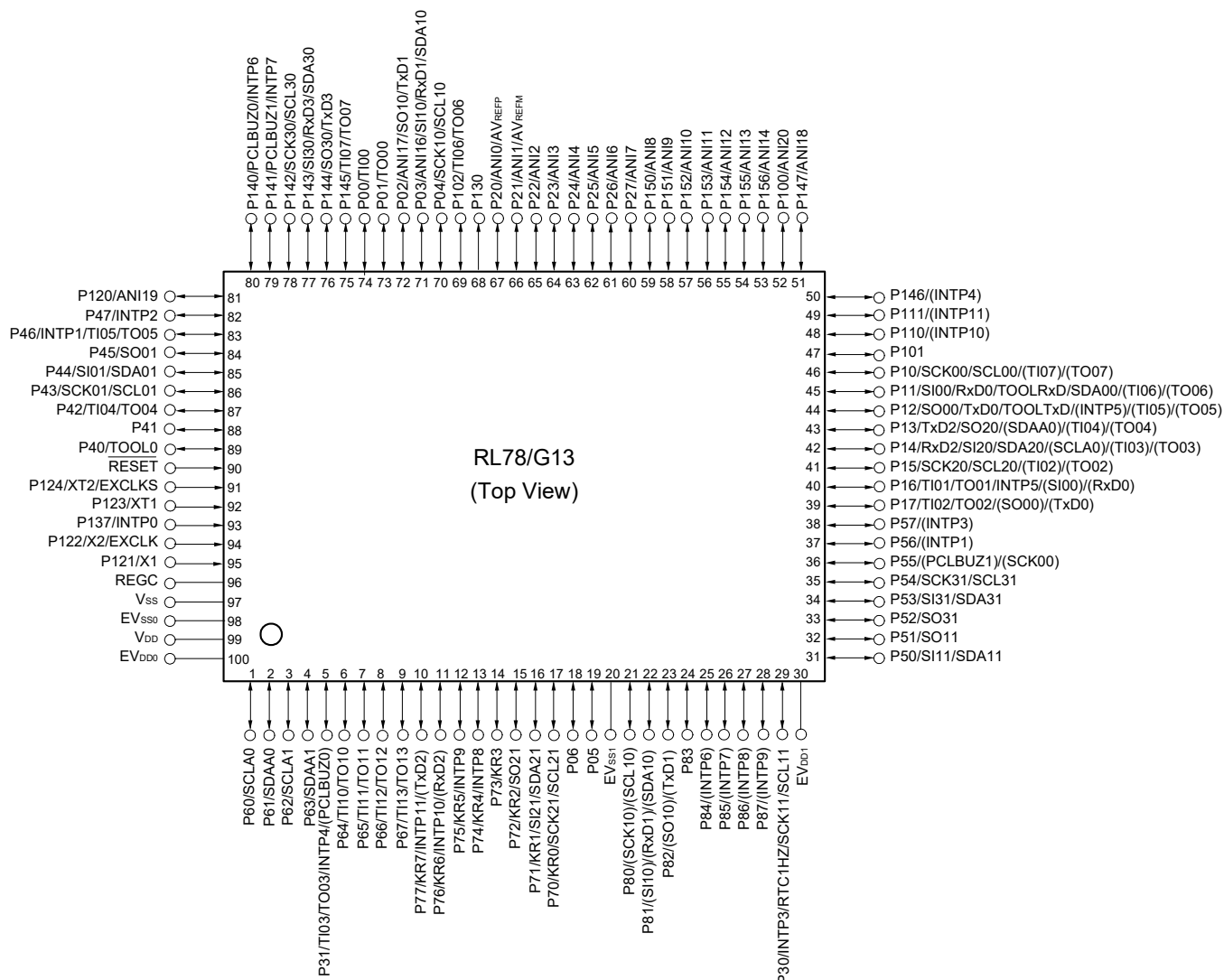
- 100-pin plastic LQFP (14 × 14 mm, 0.5 mm pitch)



- Cautions**
1. Make EV_{SS0}, EV_{SS1} pins the same potential as V_{SS} pin.
 2. Make V_{DD} pin the potential that is higher than EV_{DD0}, EV_{DD1} pins (EV_{DD0} = EV_{DD1}).
 3. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

- Remarks**
1. For pin identification, see 1.4 Pin Identification.
 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD}, EV_{DD0} and EV_{DD1} pins and connect the V_{SS}, EV_{SS0} and EV_{SS1} pins to separate ground lines.
 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

- 100-pin plastic LQFP (14 × 20 mm, 0.65 mm pitch)

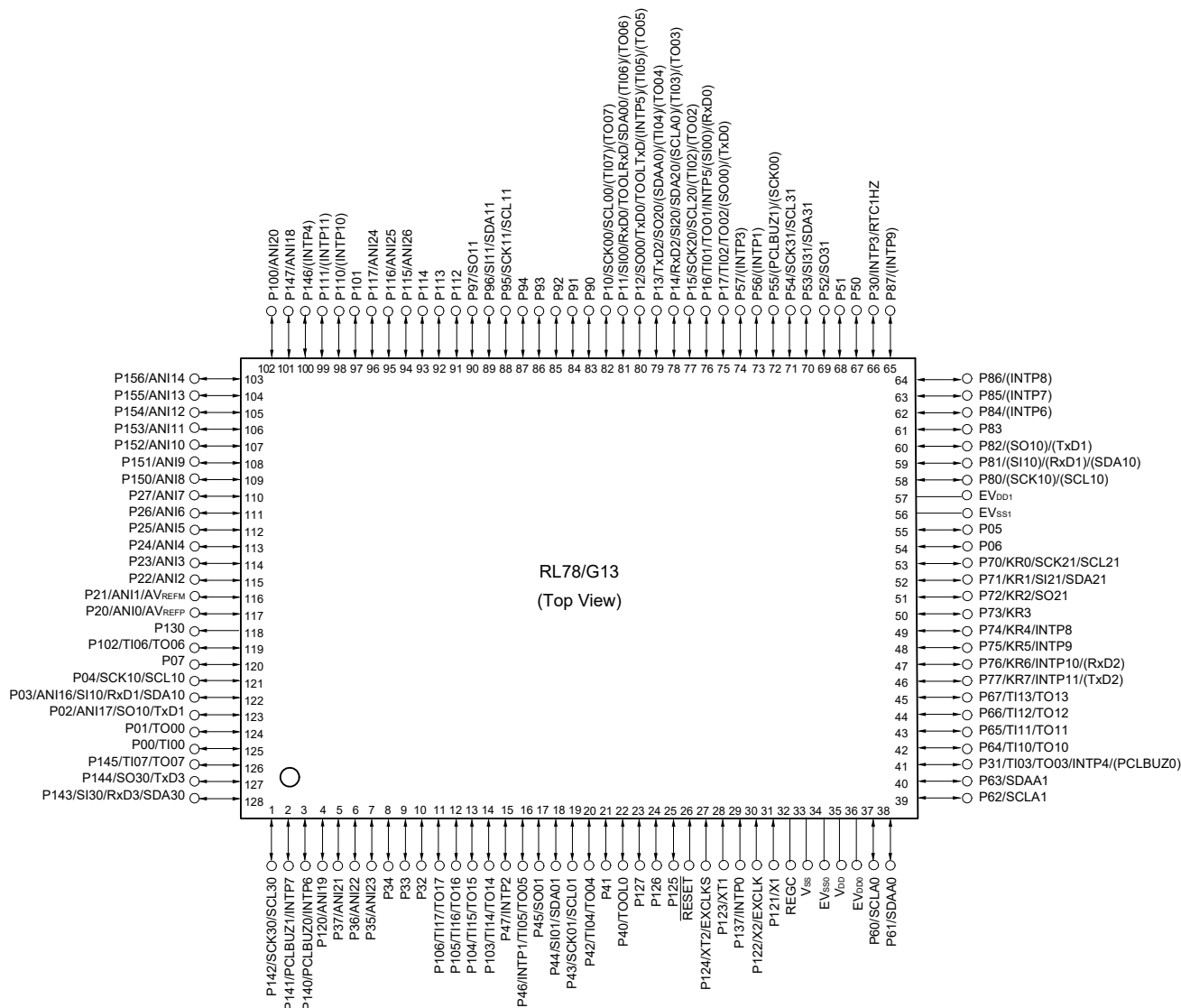


- Cautions**
1. Make EV_{SS0}, EV_{SS1} pins the same potential as V_{SS} pin.
 2. Make V_{DD} pin the potential that is higher than EV_{DD0}, EV_{DD1} pins (EV_{DD0} = EV_{DD1}).
 3. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

- Remarks**
1. For pin identification, see 1.4 Pin Identification.
 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD}, EV_{DD0} and EV_{DD1} pins and connect the V_{SS}, EV_{SS0} and EV_{SS1} pins to separate ground lines.
 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR) in the RL78/G13 User's Manual.

1.3.14 128-pin products

- 128-pin plastic LFQFP (14 × 20 mm, 0.5 mm pitch)



- Cautions**
1. Make EV_{SS0}, EV_{SS1} pins the same potential as V_{SS} pin.
 2. Make V_{DD} pin the potential that is higher than EV_{DD0}, EV_{DD1} pins (EV_{DD0} = EV_{DD1}).
 3. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

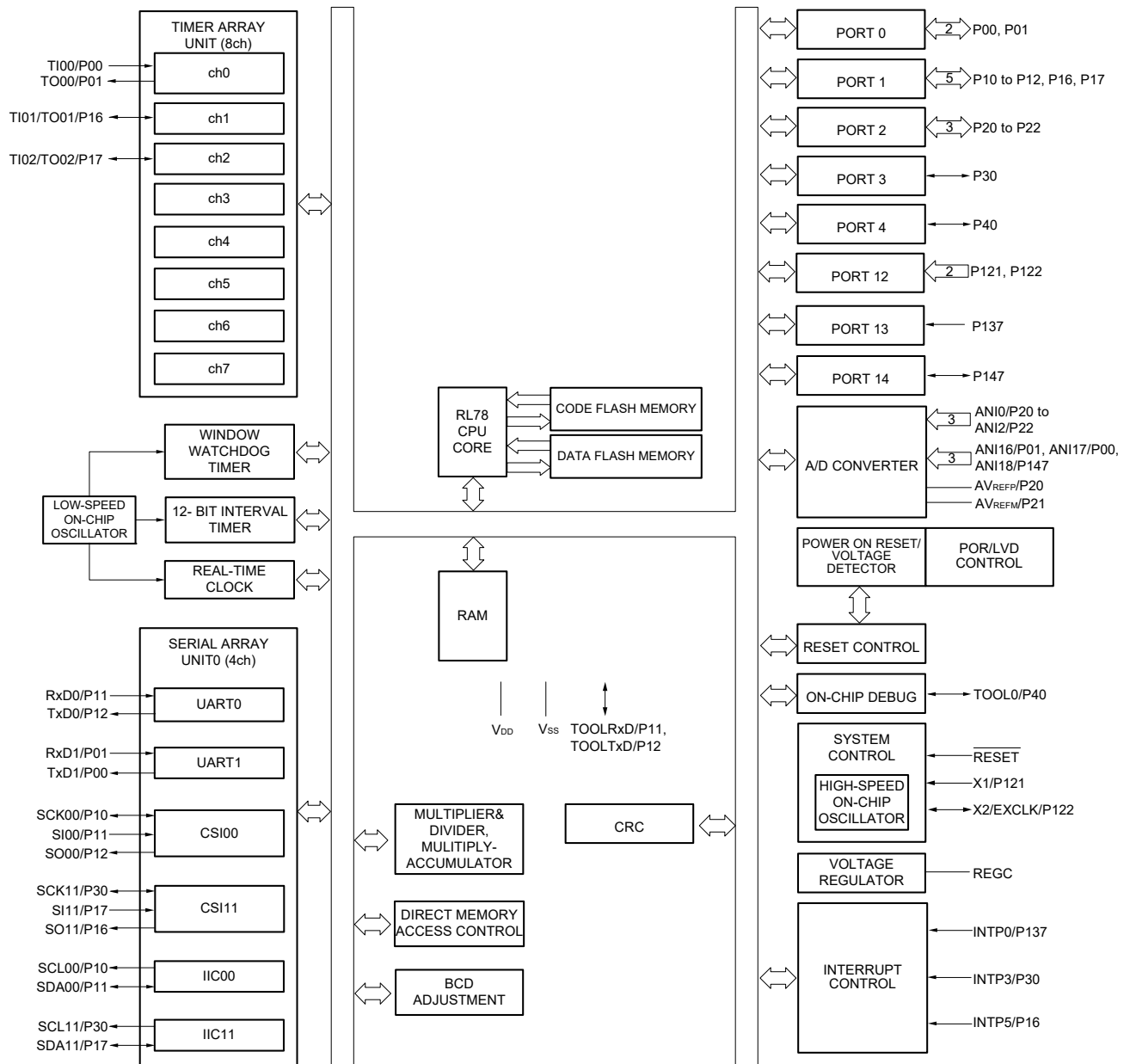
- Remarks**
1. For pin identification, see 1.4 Pin Identification.
 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD}, EV_{DD0} and EV_{DD1} pins and connect the V_{SS}, EV_{SS0} and EV_{SS1} pins to separate ground lines.
 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.4 Pin Identification

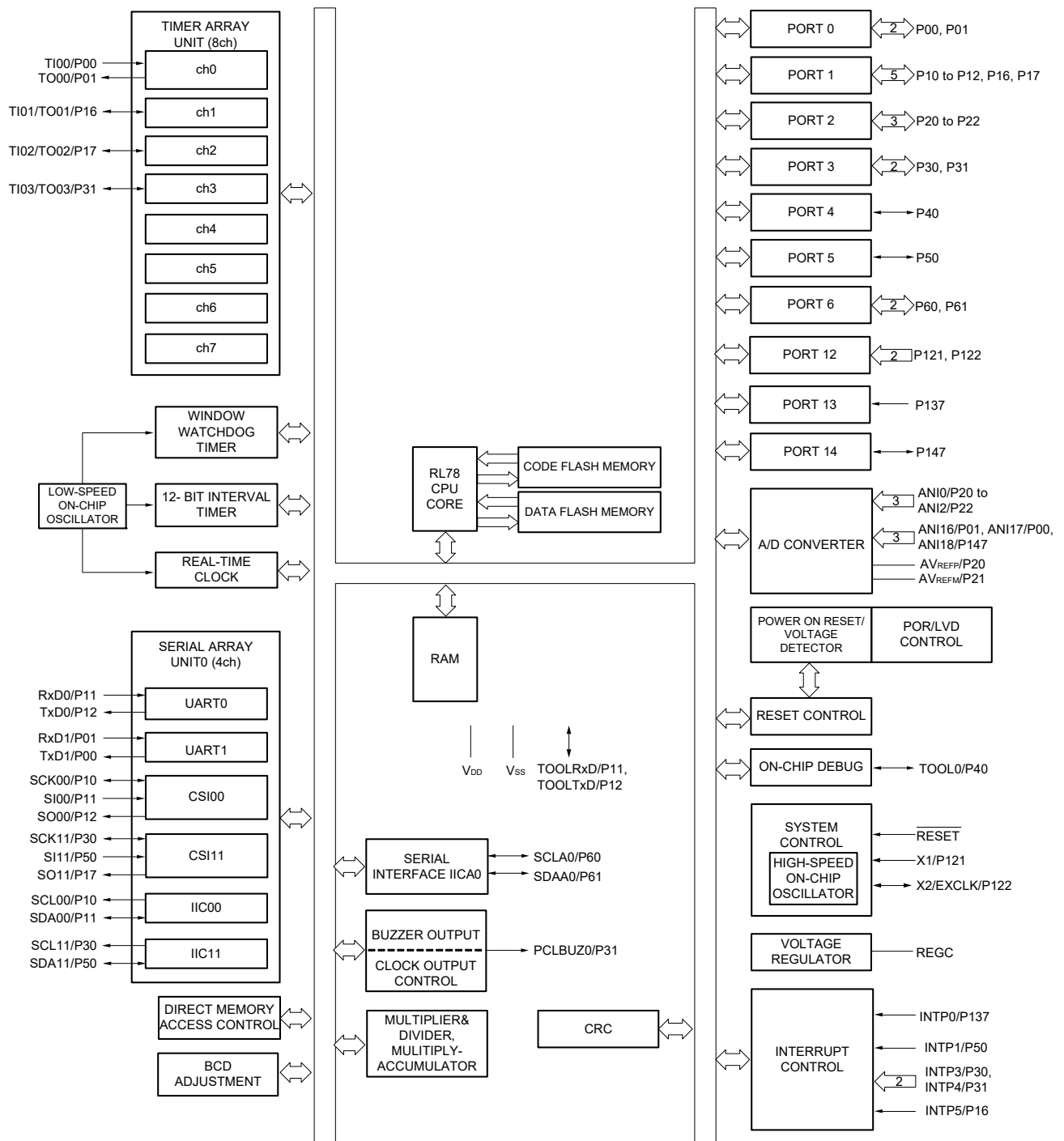
| | | | |
|-------------------|--|---|--|
| ANI0 to ANI14, | | REGC: | Regulator capacitance |
| ANI16 to ANI26: | Analog input | RESET: | Reset |
| AVREFM: | A/D converter reference potential (– side) input | RTC1HZ: | Real-time clock correction clock (1 Hz) output |
| AVREFP: | A/D converter reference potential (+ side) input | RxD0 to RxD3: | Receive data |
| EVDD0, EVDD1: | Power supply for port | SCK00, SCK01, SCK10, SCK11, SCK20, SCK21, | |
| EVSS0, EVSS1: | Ground for port | SCLA0, SCLA1: | Serial clock input/output |
| EXCLK: | External clock input (Main system clock) | SCLA0, SCLA1, SCL00, SCL01, SCL10, SCL11, SCL20, SCL21, SCL30, SCL31: | Serial clock output |
| EXCLKS: | External clock input (Subsystem clock) | SDAA0, SDAA1, SDA00, SDA01, SDA10, SDA11, SDA20, SDA21, SDA30, SDA31: | Serial data input/output |
| INTP0 to INTP11: | Interrupt request from peripheral | SI00, SI01, SI10, SI11, SI20, SI21, SI30, SI31: | Serial data input |
| KR0 to KR7: | Key return | SO00, SO01, SO10, SO11, SO20, SO21, SO30, SO31: | Serial data output |
| P00 to P07: | Port 0 | TI00 to TI07, | |
| P10 to P17: | Port 1 | TI10 to TI17: | Timer input |
| P20 to P27: | Port 2 | TO00 to TO07, | |
| P30 to P37: | Port 3 | TO10 to TO17: | Timer output |
| P40 to P47: | Port 4 | TOOL0: | Data input/output for tool |
| P50 to P57: | Port 5 | TOOLRxD, TOOLTxD: | Data input/output for external device |
| P60 to P67: | Port 6 | TxD0 to TxD3: | Transmit data |
| P70 to P77: | Port 7 | VDD: | Power supply |
| P80 to P87: | Port 8 | VSS: | Ground |
| P90 to P97: | Port 9 | X1, X2: | Crystal oscillator (main system clock) |
| P100 to P106: | Port 10 | XT1, XT2: | Crystal oscillator (subsystem clock) |
| P110 to P117: | Port 11 | | |
| P120 to P127: | Port 12 | | |
| P130, P137: | Port 13 | | |
| P140 to P147: | Port 14 | | |
| P150 to P156: | Port 15 | | |
| PCLBUZ0, PCLBUZ1: | Programmable clock output/buzzer output | | |

1.5 Block Diagram

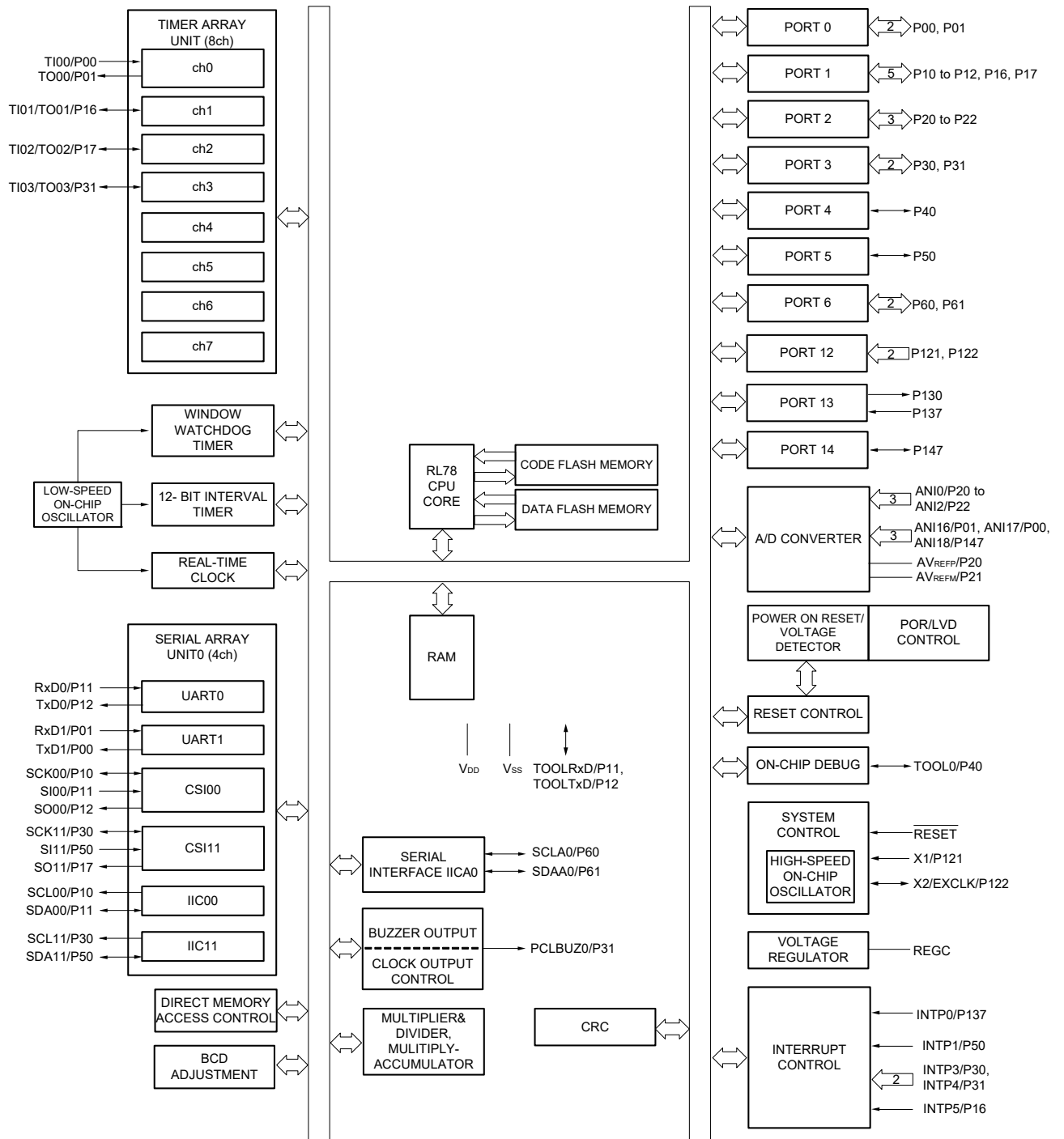
1.5.1 20-pin products



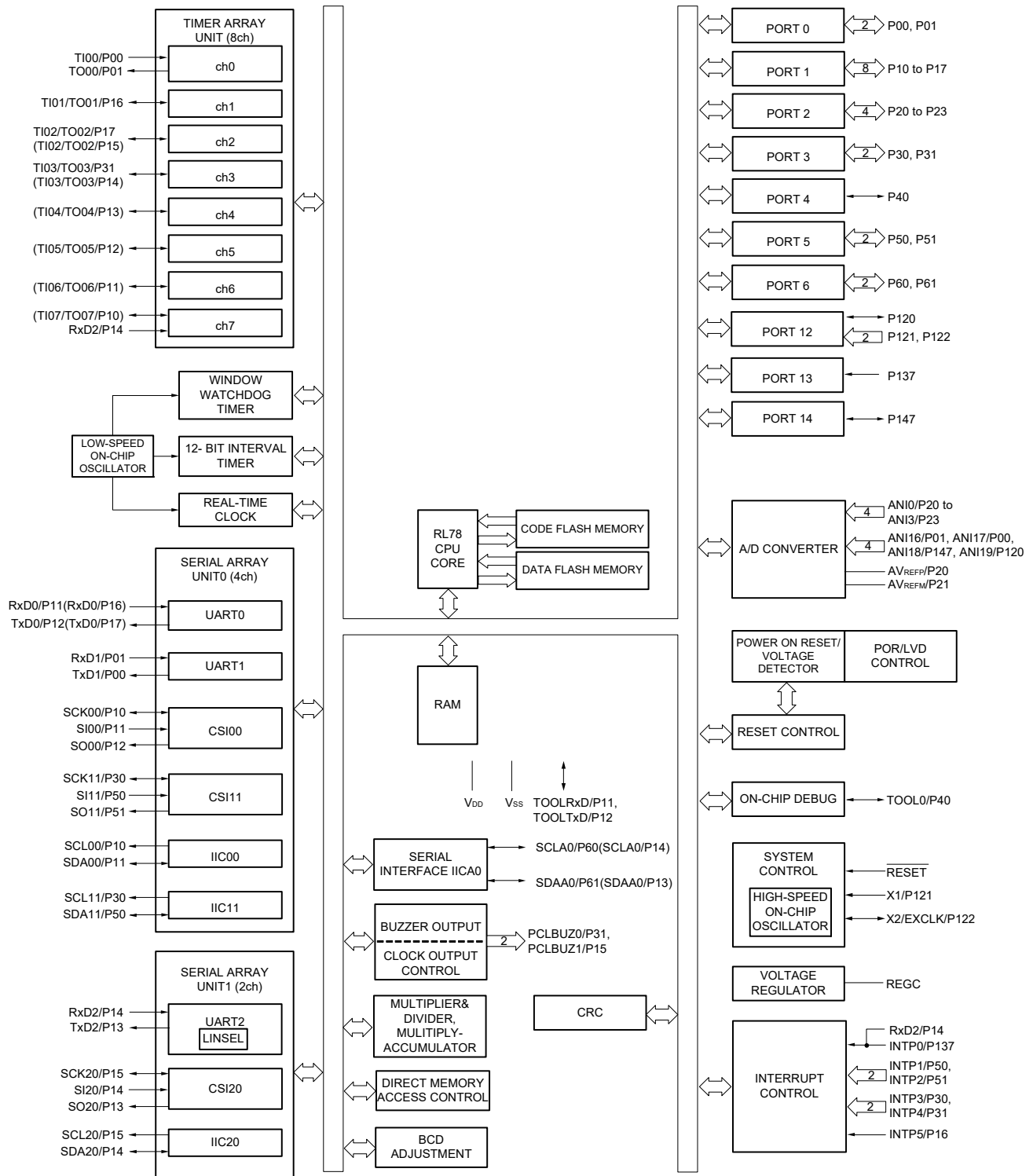
1.5.2 24-pin products



1.5.3 25-pin products

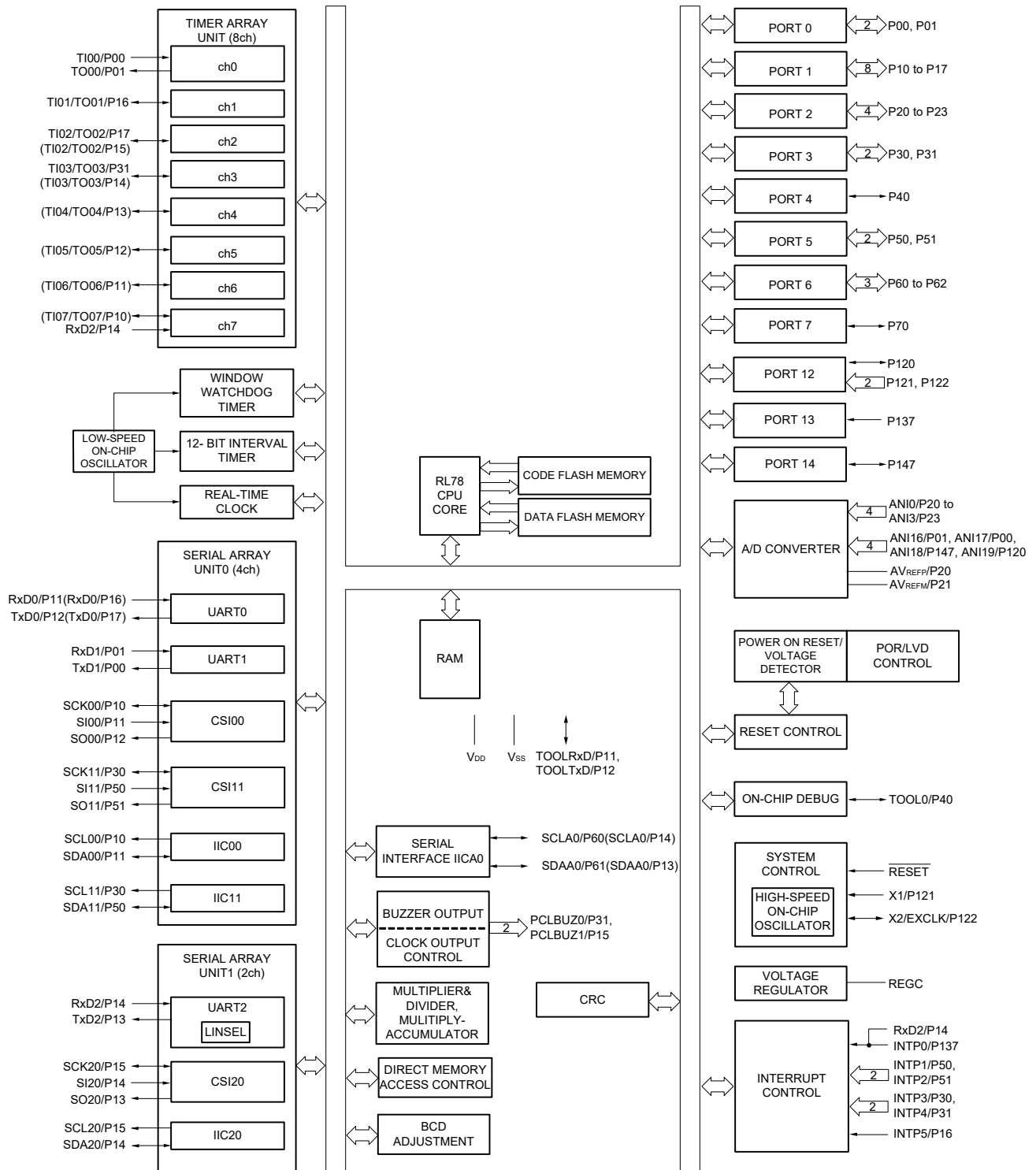


1.5.4 30-pin products



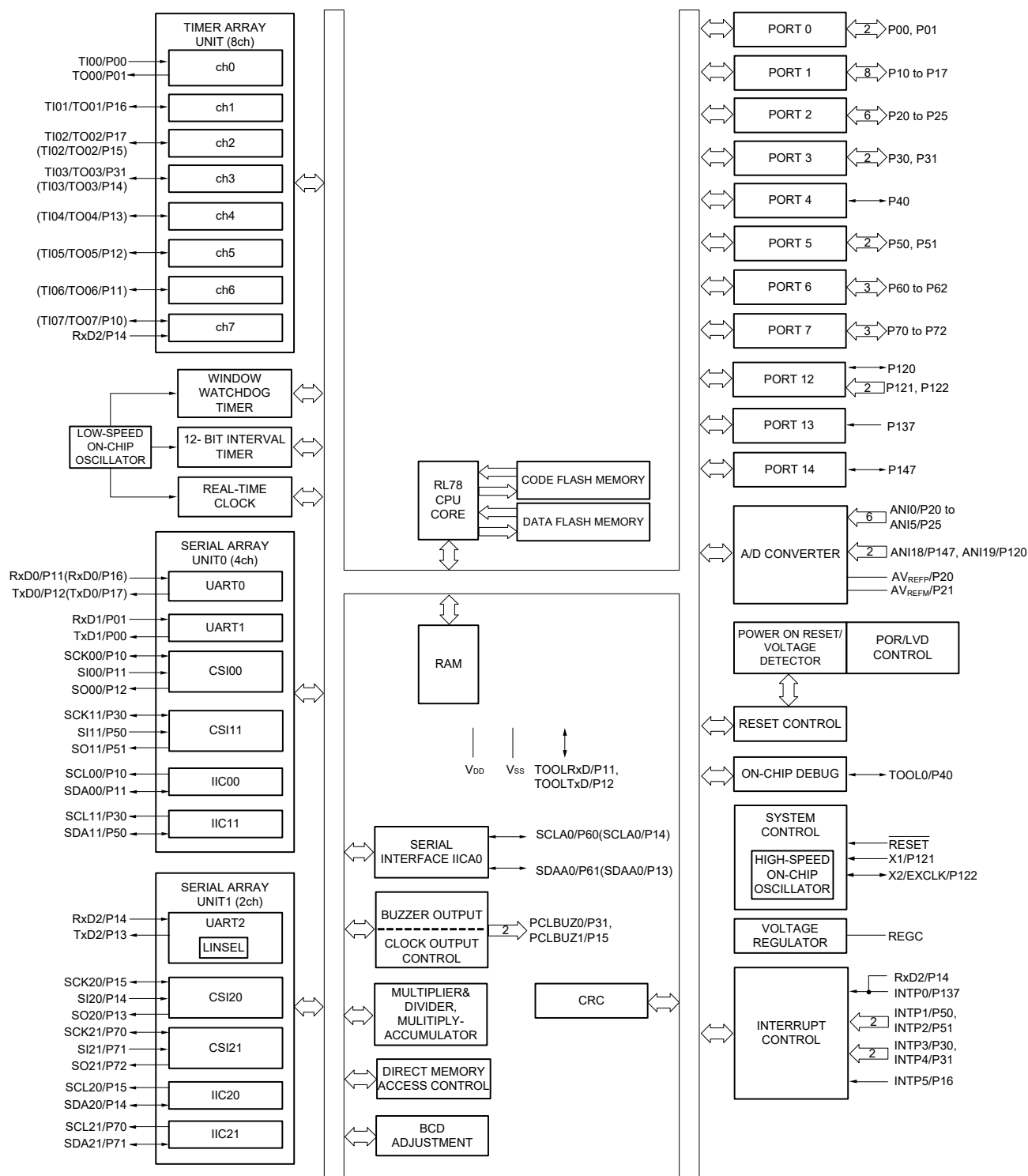
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.5.5 32-pin products



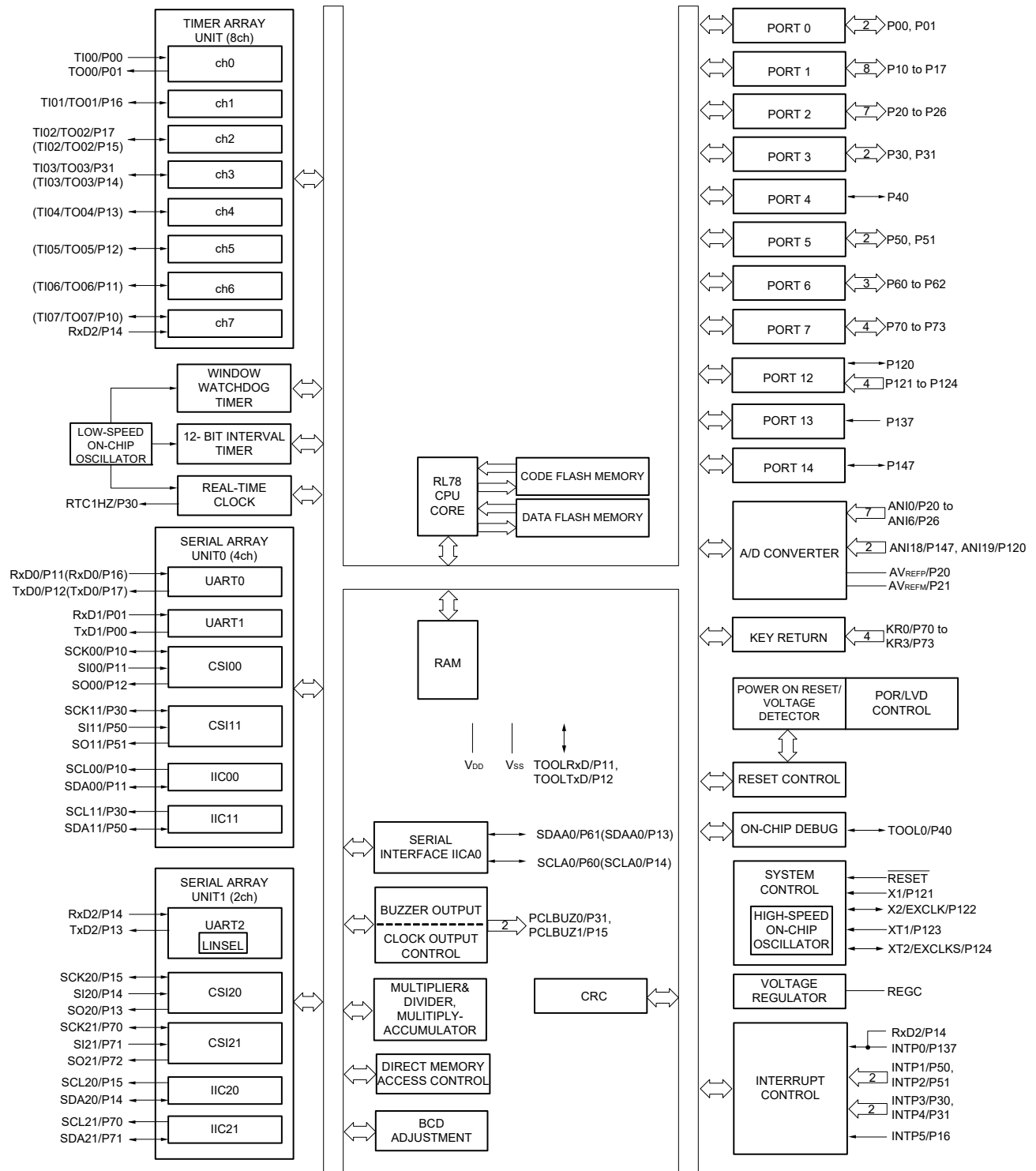
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.5.6 36-pin products



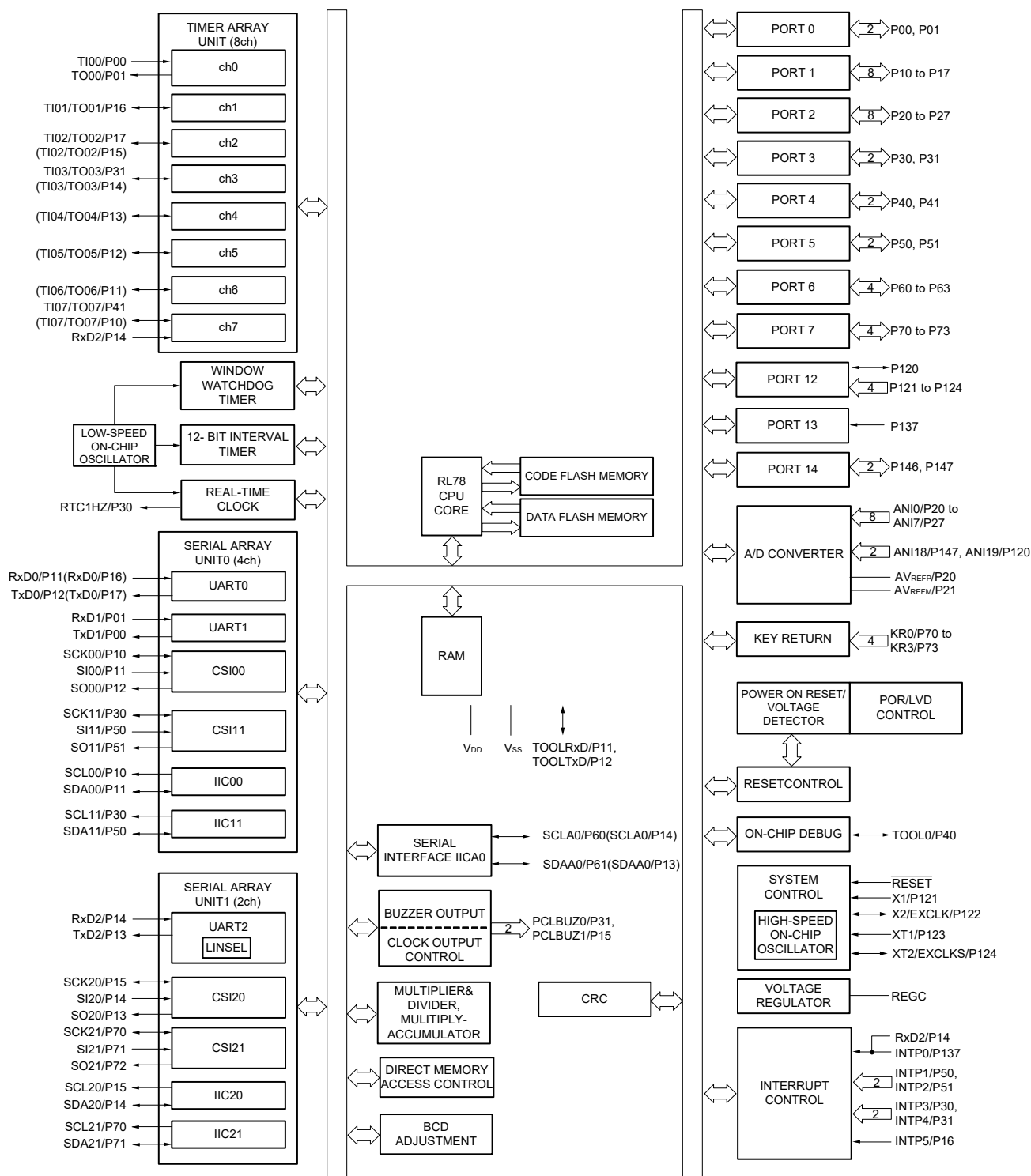
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.5.7 40-pin products



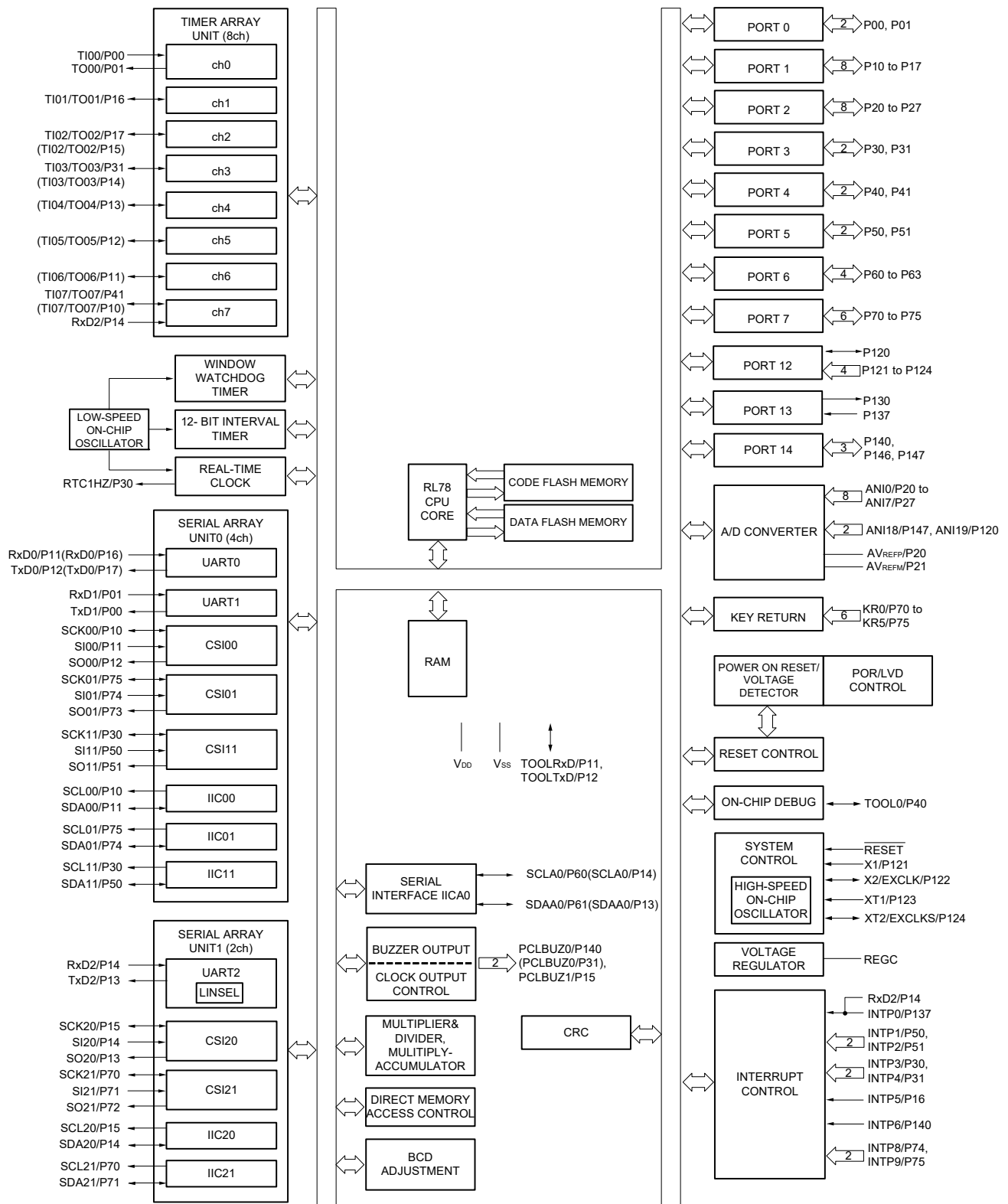
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.5.8 44-pin products



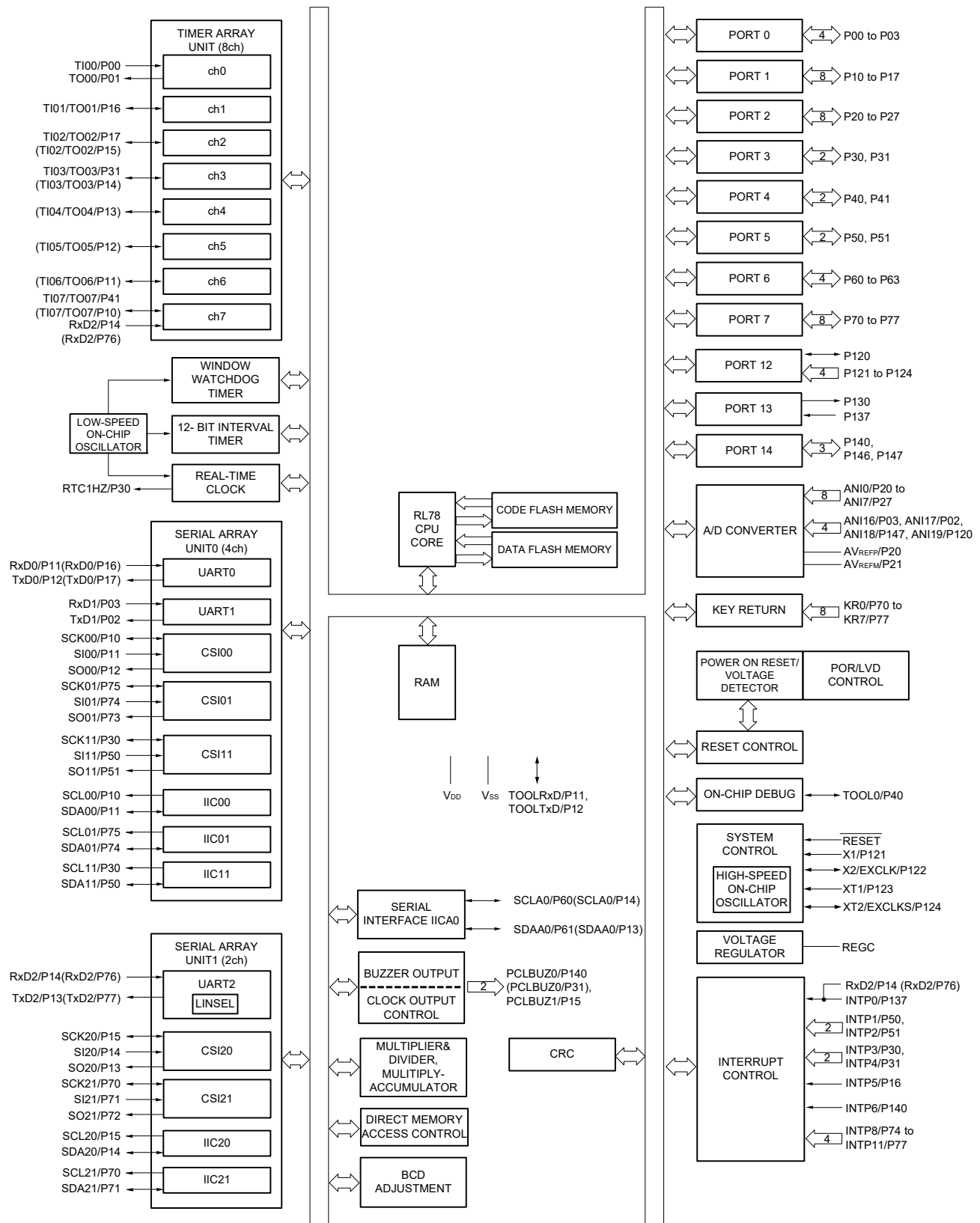
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.5.9 48-pin products



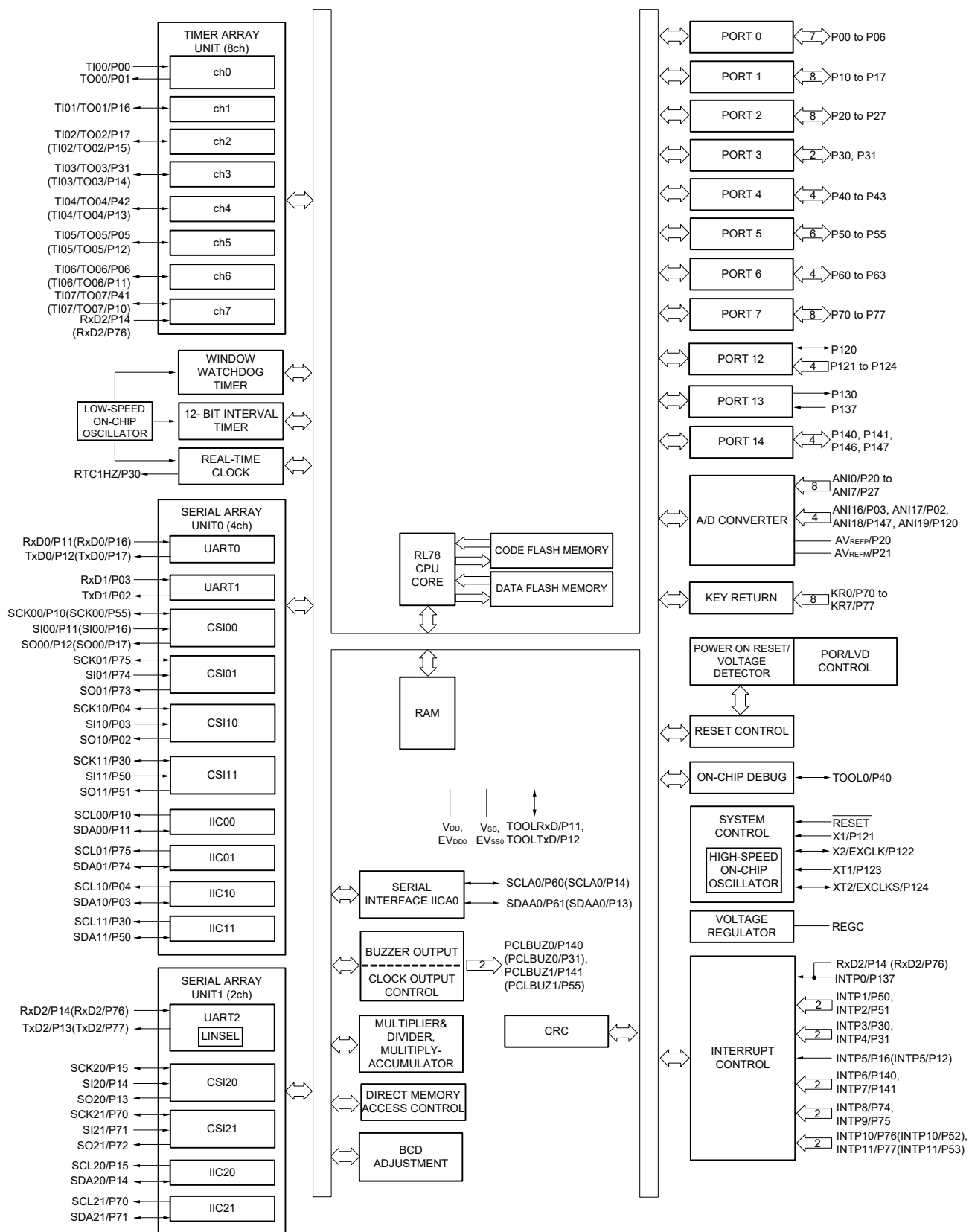
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.5.10 52-pin products



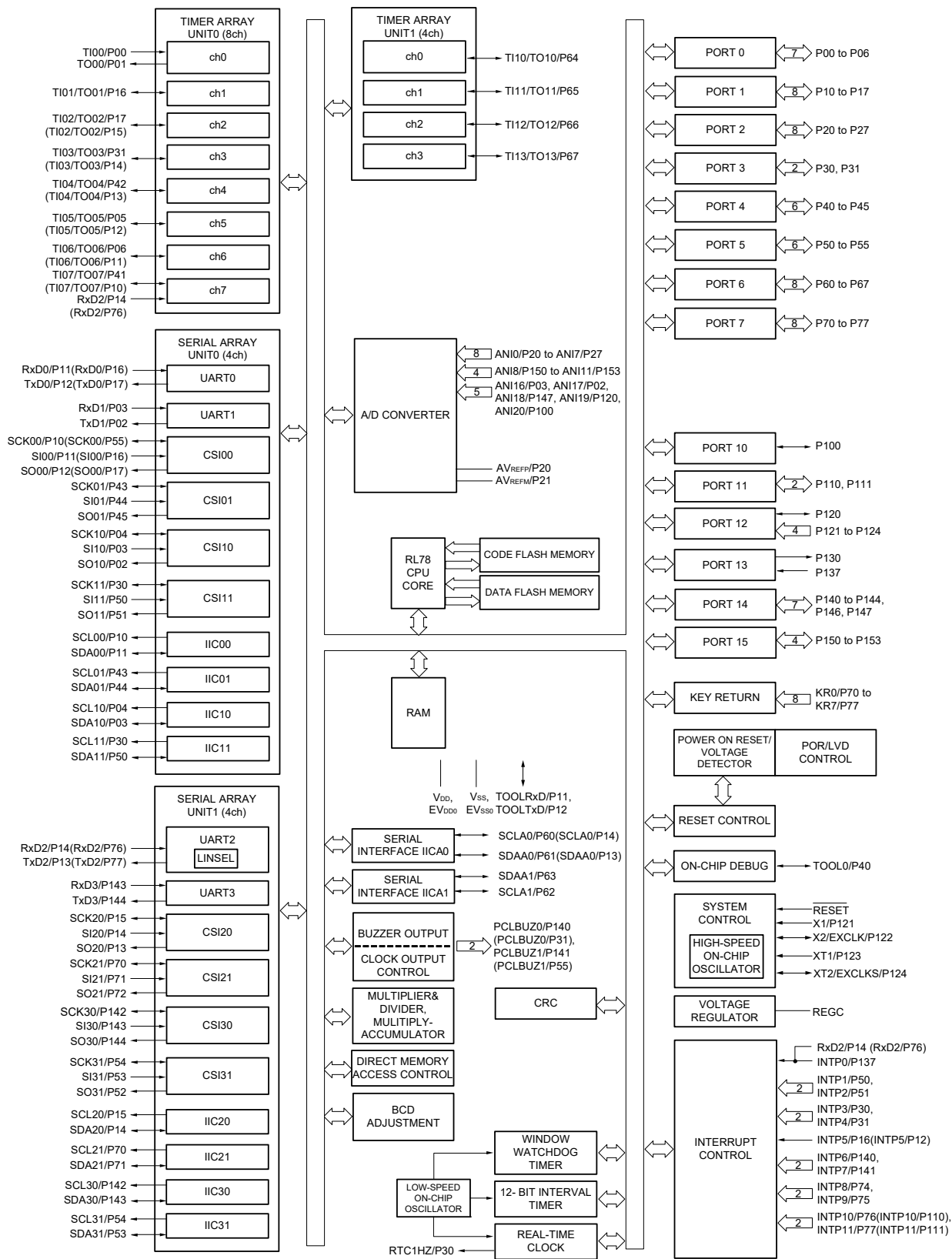
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.5.11 64-pin products



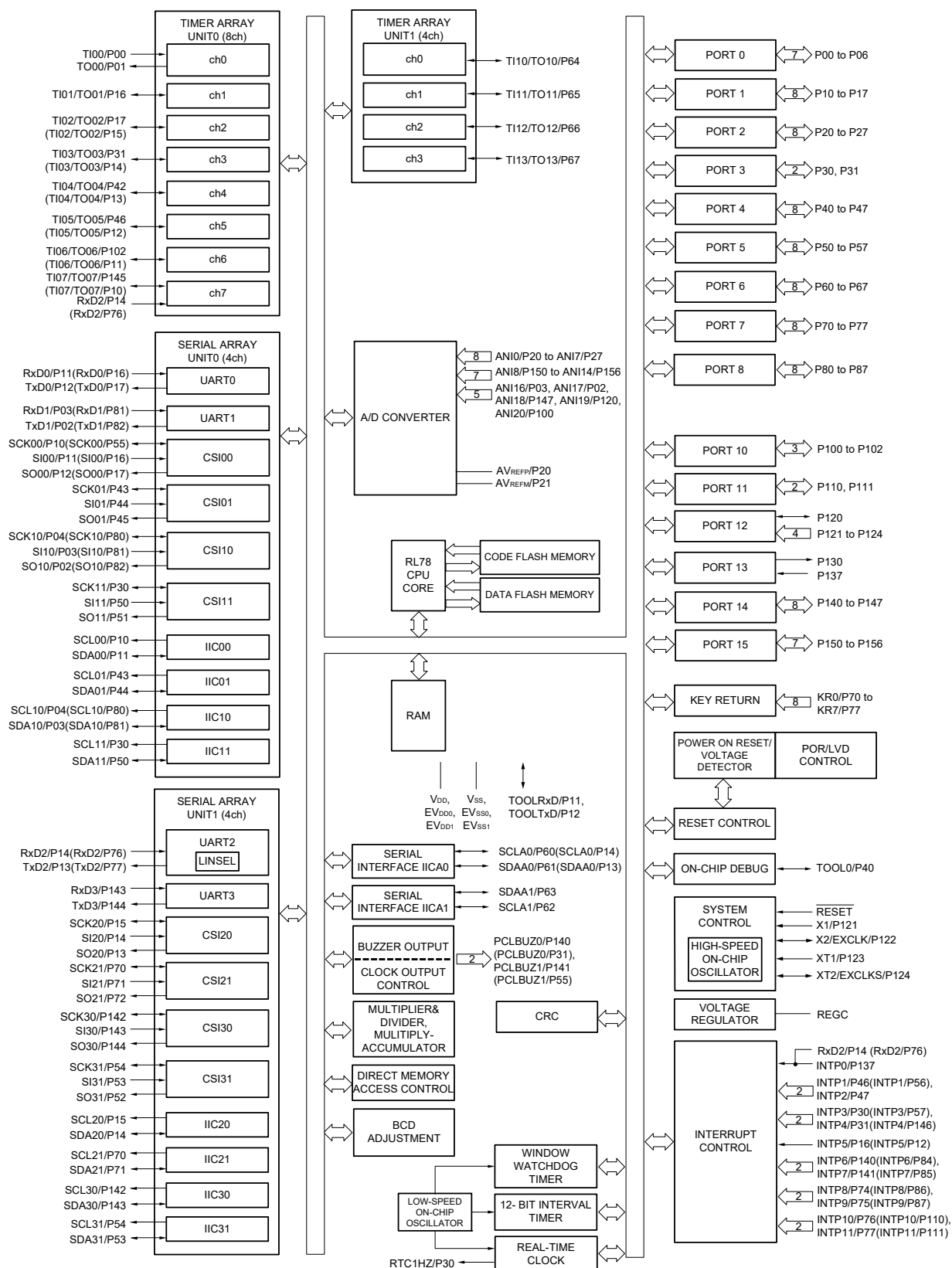
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.5.12 80-pin products



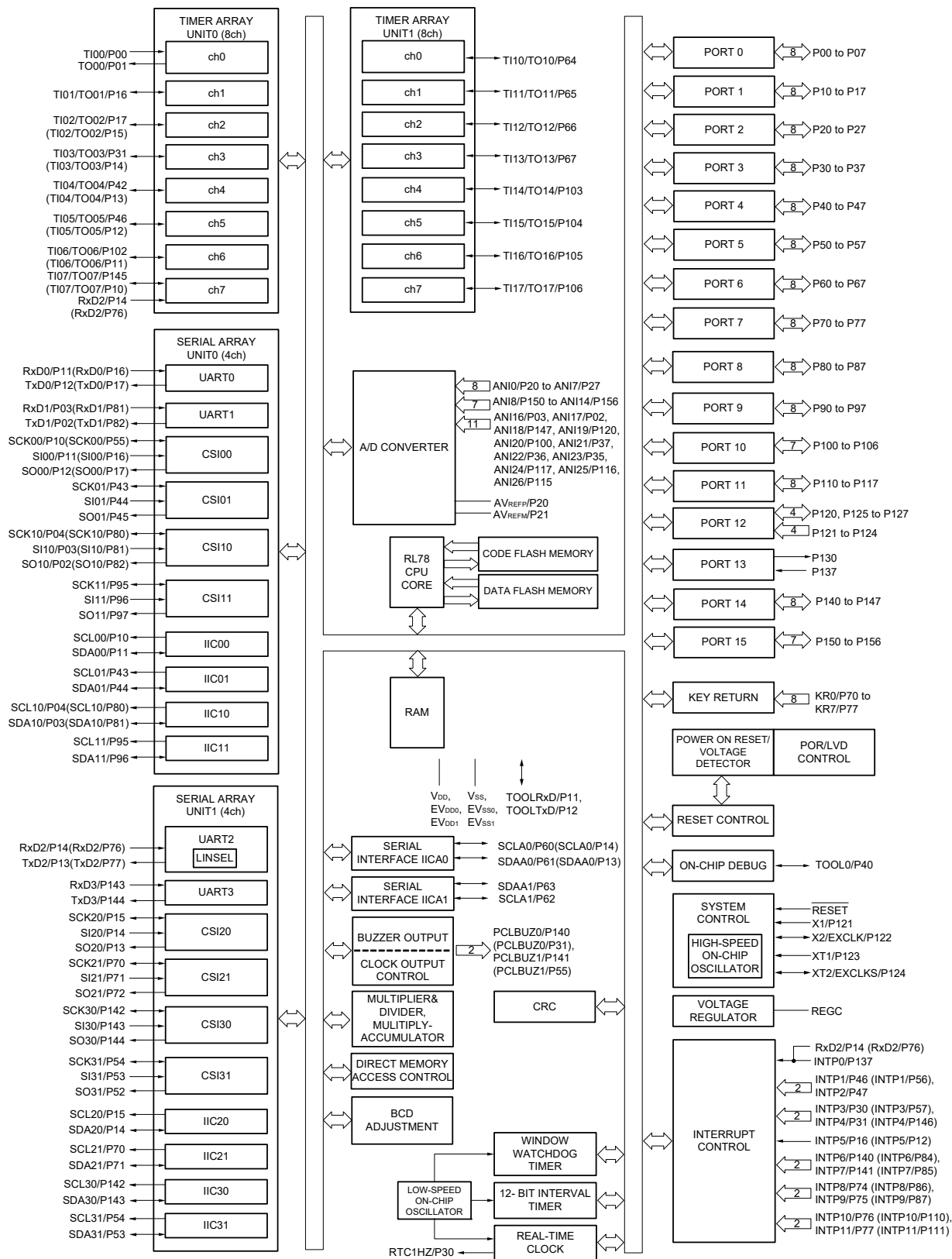
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.5.13 100-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.5.14 128-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.6 Outline of Functions

[20-pin, 24-pin, 25-pin, 30-pin, 32-pin, 36-pin products]

Caution This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

(1/2)

| Item | | 20-pin | | 24-pin | | 25-pin | | 30-pin | | 32-pin | | 36-pin | |
|------------------------------------|---|---|--|---|--|--|---|--------------------------|----------|--------------------------|----------|--------------------------|----------|
| | | R5F1006X | R5F1016X | R5F1007X | R5F1017X | R5F1008X | R5F1018X | R5F100AX | R5F101AX | R5F100BX | R5F101BX | R5F100CX | R5F101CX |
| Code flash memory (KB) | | 16 to 64 | | 16 to 64 | | 16 to 64 | | 16 to 128 | | 16 to 128 | | 16 to 128 | |
| Data flash memory (KB) | | 4 | – | 4 | – | 4 | – | 4 to 8 | – | 4 to 8 | – | 4 to 8 | – |
| RAM (KB) | | 2 to 4 ^{Note1} | | 2 to 4 ^{Note1} | | 2 to 4 ^{Note1} | | 2 to 12 ^{Note1} | | 2 to 12 ^{Note1} | | 2 to 12 ^{Note1} | |
| Address space | | 1 MB | | | | | | | | | | | |
| Main system clock | High-speed system clock | X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (High-speed main) mode: 1 to 20 MHz (V _{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V _{DD} = 1.6 to 5.5 V) | | | | | | | | | | | |
| | High-speed on-chip oscillator | HS (High-speed main) mode: 1 to 32 MHz (V _{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V _{DD} = 1.6 to 5.5 V) | | | | | | | | | | | |
| Subsystem clock | | – | | | | | | | | | | | |
| Low-speed on-chip oscillator | | 15 kHz (TYP.) | | | | | | | | | | | |
| General-purpose registers | | (8-bit register × 8) × 4 banks | | | | | | | | | | | |
| Minimum instruction execution time | | 0.03125 μs (High-speed on-chip oscillator: f _{IH} = 32 MHz operation) | | | | | | | | | | | |
| | | 0.05 μs (High-speed system clock: f _{MX} = 20 MHz operation) | | | | | | | | | | | |
| Instruction set | | <ul style="list-style-type: none"> • Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. | | | | | | | | | | | |
| I/O port | Total | 16 | 20 | 21 | 26 | 28 | 32 | | | | | | |
| | CMOS I/O | 13 (N-ch O.D. I/O [V _{DD} withstand voltage]: 5) | 15 (N-ch O.D. I/O [V _{DD} withstand voltage]: 6) | 15 (N-ch O.D. I/O [V _{DD} withstand voltage]: 6) | 21 (N-ch O.D. I/O [V _{DD} withstand voltage]: 9) | 22 (N-ch O.D. I/O [V _{DD} withstand voltage]: 9) | 26 (N-ch O.D. I/O [V _{DD} withstand voltage]: 10) | | | | | | |
| | CMOS input | 3 | 3 | 3 | 3 | 3 | 3 | | | | | | |
| | CMOS output | – | – | 1 | – | – | – | | | | | | |
| | N-ch O.D. I/O (withstand voltage: 6 V) | – | 2 | 2 | 2 | 3 | 3 | | | | | | |
| Timer | 16-bit timer | 8 channels | | | | | | | | | | | |
| | Watchdog timer | 1 channel | | | | | | | | | | | |
| | Real-time clock (RTC) | 1 channel ^{Note 2} | | | | | | | | | | | |
| | 12-bit interval timer (IT) | 1 channel | | | | | | | | | | | |
| | Timer output | 3 channels (PWM outputs: 2 ^{Note 3}) | 4 channels (PWM outputs: 3 ^{Note 3}) | 4 channels (PWM outputs: 3 ^{Note 3}), 8 channels (PWM outputs: 7 ^{Note 3}) ^{Note 4} | | | | | | | | | |
| | RTC output | – | | | | | | | | | | | |

Notes 1. The flash library uses RAM in self-programming and rewriting of the data flash memory. The target products and start address of the RAM areas used by the flash library are shown below.

R5F100xD, R5F101xD (x = 6 to 8, A to C): Start address FF300H

R5F100xE, R5F101xE (x = 6 to 8, A to C): Start address FEF00H

For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

- Notes**
- Only the constant-period interrupt function when the low-speed on-chip oscillator clock (f_{IL}) is selected
 - The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves) (see **6.9.3 Operation as multiple PWM output function** in the RL78/G13 User's Manual).
 - When setting to $PIOR = 1$

(2/2)

| Item | 20-pin | | 24-pin | | 25-pin | | 30-pin | | 32-pin | | 36-pin | | |
|---|---|----------|------------|----------|------------|----------|------------|----------|------------|----------|------------|----------|--|
| | R5F1006X | R5F1016X | R5F1007X | R5F1017X | R5F1008X | R5F1018X | R5F100AX | R5F101AX | R5F100BX | R5F101BX | R5F100CX | R5F101CX | |
| Clock output/buzzer output | - | | 1 | | 1 | | 2 | | 2 | | 2 | | |
| | <ul style="list-style-type: none"> 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN} = 20$ MHz operation) | | | | | | | | | | | | |
| 8/10-bit resolution A/D converter | 6 channels | | 6 channels | | 6 channels | | 8 channels | | 8 channels | | 8 channels | | |
| Serial interface | <p>[20-pin, 24-pin, 25-pin products]</p> <ul style="list-style-type: none"> CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel <p>[30-pin, 32-pin products]</p> <ul style="list-style-type: none"> CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel CSI: 1 channel/simplified I²C: 1 channel/UART (UART supporting LIN-bus): 1 channel <p>[36-pin products]</p> <ul style="list-style-type: none"> CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel CSI: 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel | | | | | | | | | | | | |
| I ² C bus | - | | 1 channel | | 1 channel | | 1 channel | | 1 channel | | 1 channel | | |
| Multiplier and divider/multiply-accumulator | <ul style="list-style-type: none"> 16 bits × 16 bits = 32 bits (Unsigned or signed) 32 bits ÷ 32 bits = 32 bits (Unsigned) 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed) | | | | | | | | | | | | |
| DMA controller | 2 channels | | | | | | | | | | | | |
| Vectored interrupt sources | Internal | 23 | | 24 | | 24 | | 27 | | 27 | | 27 | |
| | External | 3 | | 5 | | 5 | | 6 | | 6 | | 6 | |
| Key interrupt | - | | | | | | | | | | | | |
| Reset | <ul style="list-style-type: none"> Reset by RESET pin Internal reset by watchdog timer Internal reset by power-on-reset Internal reset by voltage detector Internal reset by illegal instruction execution ^{Note} Internal reset by RAM parity error Internal reset by illegal-memory access | | | | | | | | | | | | |
| Power-on-reset circuit | <ul style="list-style-type: none"> Power-on-reset: 1.51 V (TYP.) Power-down-reset: 1.50 V (TYP.) | | | | | | | | | | | | |
| Voltage detector | <ul style="list-style-type: none"> Rising edge : 1.67 V to 4.06 V (14 stages) Falling edge : 1.63 V to 3.98 V (14 stages) | | | | | | | | | | | | |
| On-chip debug function | Provided | | | | | | | | | | | | |
| Power supply voltage | $V_{DD} = 1.6$ to 5.5 V ($T_A = -40$ to $+85^\circ\text{C}$) $V_{DD} = 2.4$ to 5.5 V ($T_A = -40$ to $+105^\circ\text{C}$) | | | | | | | | | | | | |
| Operating ambient temperature | $T_A = 40$ to $+85^\circ\text{C}$ (A: Consumer applications, D: Industrial applications) $T_A = 40$ to $+105^\circ\text{C}$ (G: Industrial applications) | | | | | | | | | | | | |

Note The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

[40-pin, 44-pin, 48-pin, 52-pin, 64-pin products]

Caution This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

(1/2)

| Item | | 40-pin | | 44-pin | | 48-pin | | 52-pin | | 64-pin | |
|------------------------------------|---|---|----------|--|----------|---|----------|---|----------|---|----------|
| | | R5F100EX | R5F101EX | R5F100FX | R5F101FX | R5F100GX | R5F101GX | R5F100JX | R5F101JX | R5F100LX | R5F101LX |
| Code flash memory (KB) | | 16 to 192 | | 16 to 512 | | 16 to 512 | | 32 to 512 | | 32 to 512 | |
| Data flash memory (KB) | | 4 to 8 | – | 4 to 8 | – | 4 to 8 | – | 4 to 8 | – | 4 to 8 | – |
| RAM (KB) | | 2 to 16 ^{Note1} | | 2 to 32 ^{Note1} | | 2 to 32 ^{Note1} | | 2 to 32 ^{Note1} | | 2 to 32 ^{Note1} | |
| Address space | | 1 MB | | | | | | | | | |
| Main system clock | High-speed system clock | X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (High-speed main) mode: 1 to 20 MHz (V _{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V _{DD} = 1.6 to 5.5 V) | | | | | | | | | |
| | High-speed on-chip oscillator | HS (High-speed main) mode: 1 to 32 MHz (V _{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V _{DD} = 1.6 to 5.5 V) | | | | | | | | | |
| Subsystem clock | | XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz | | | | | | | | | |
| Low-speed on-chip oscillator | | 15 kHz (TYP.) | | | | | | | | | |
| General-purpose registers | | (8-bit register × 8) × 4 banks | | | | | | | | | |
| Minimum instruction execution time | | 0.03125 μs (High-speed on-chip oscillator: f _{IH} = 32 MHz operation) | | | | | | | | | |
| | | 0.05 μs (High-speed system clock: f _{MX} = 20 MHz operation) | | | | | | | | | |
| | | 30.5 μs (Subsystem clock: f _{SUB} = 32.768 kHz operation) | | | | | | | | | |
| Instruction set | | <ul style="list-style-type: none"> • Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. | | | | | | | | | |
| I/O port | Total | 36 | | 40 | | 44 | | 48 | | 58 | |
| | CMOS I/O | 28 (N-ch O.D. I/O [V _{DD} withstand voltage]: 10) | | 31 (N-ch O.D. I/O [V _{DD} withstand voltage]: 10) | | 34 (N-ch O.D. I/O [V _{DD} withstand voltage]: 11) | | 38 (N-ch O.D. I/O [V _{DD} withstand voltage]: 13) | | 48 (N-ch O.D. I/O [V _{DD} withstand voltage]: 15) | |
| | CMOS input | 5 | | 5 | | 5 | | 5 | | 5 | |
| | CMOS output | – | | – | | 1 | | 1 | | 1 | |
| | N-ch O.D. I/O (withstand voltage: 6 V) | 3 | | 4 | | 4 | | 4 | | 4 | |
| Timer | 16-bit timer | 8 channels | | | | | | | | | |
| | Watchdog timer | 1 channel | | | | | | | | | |
| | Real-time clock (RTC) | 1 channel | | | | | | | | | |
| | 12-bit interval timer (IT) | 1 channel | | | | | | | | | |
| | Timer output | 4 channels (PWM outputs: 3 ^{Note2}), 8 channels (PWM outputs: 7 ^{Note2}) ^{Note3} | | 5 channels (PWM outputs: 4 ^{Note2}), 8 channels (PWM outputs: 7 ^{Note2}) ^{Note3} | | | | | | 8 channels (PWM outputs: 7 ^{Note2}) | |
| | RTC output | 1 channel • 1 Hz (subsystem clock: f _{SUB} = 32.768 kHz) | | | | | | | | | |

Notes 1. The flash library uses RAM in self-programming and rewriting of the data flash memory. The target products and start address of the RAM areas used by the flash library are shown below.
R5F100xD, R5F101xD (x = E to G, J, L): Start address FF300H
R5F100xE, R5F101xE (x = E to G, J, L): Start address FEF00H
R5F100xJ, R5F101xJ (x = F, G, J, L): Start address FAF00H
R5F100xL, R5F101xL (x = F, G, J, L): Start address F7F00H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

- Notes**
- The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves) (see **6.9.3 Operation as multiple PWM output function** in the RL78/G13 User's Manual).
 - When setting to PIOR = 1

(2/2)

| Item | 40-pin | | 44-pin | | 48-pin | | 52-pin | | 64-pin | | |
|---|--|-----------|-------------|-----------|-------------|-----------|-------------|-----------|-------------|-----------|--|
| | R5F100EX | R5F101EX | R5F100FX | R5F101FX | R5F100GX | R5F101GX | R5F100JX | R5F101JX | R5F100LX | R5F101LX | |
| Clock output/buzzer output | 2 | | 2 | | 2 | | 2 | | 2 | | |
| | <ul style="list-style-type: none"> 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN} = 20$ MHz operation) 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: $f_{SUB} = 32.768$ kHz operation) | | | | | | | | | | |
| 8/10-bit resolution A/D converter | 9 channels | | 10 channels | | 10 channels | | 12 channels | | 12 channels | | |
| Serial interface | <p>[40-pin, 44-pin products]</p> <ul style="list-style-type: none"> CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel CSI: 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel <p>[48-pin, 52-pin products]</p> <ul style="list-style-type: none"> CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channel CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel CSI: 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel <p>[64-pin products]</p> <ul style="list-style-type: none"> CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channel CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channel CSI: 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel | | | | | | | | | | |
| | I ² C bus | 1 channel | | 1 channel | | 1 channel | | 1 channel | | 1 channel | |
| Multiplier and divider/multiply-accumulator | <ul style="list-style-type: none"> 16 bits × 16 bits = 32 bits (Unsigned or signed) 32 bits ÷ 32 bits = 32 bits (Unsigned) 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed) | | | | | | | | | | |
| DMA controller | 2 channels | | | | | | | | | | |
| Vectored interrupt sources | Internal | 27 | | 27 | | 27 | | 27 | | 27 | |
| | External | 7 | | 7 | | 10 | | 12 | | 13 | |
| Key interrupt | 4 | | 4 | | 6 | | 8 | | 8 | | |
| Reset | <ul style="list-style-type: none"> Reset by RESET pin Internal reset by watchdog timer Internal reset by power-on-reset Internal reset by voltage detector Internal reset by illegal instruction execution ^{Note} Internal reset by RAM parity error Internal reset by illegal-memory access | | | | | | | | | | |
| Power-on-reset circuit | <ul style="list-style-type: none"> Power-on-reset: 1.51 V (TYP.) Power-down-reset: 1.50 V (TYP.) | | | | | | | | | | |
| Voltage detector | <ul style="list-style-type: none"> Rising edge : 1.67 V to 4.06 V (14 stages) Falling edge : 1.63 V to 3.98 V (14 stages) | | | | | | | | | | |
| On-chip debug function | Provided | | | | | | | | | | |
| Power supply voltage | $V_{DD} = 1.6$ to 5.5 V ($T_A = -40$ to $+85^\circ\text{C}$) $V_{DD} = 2.4$ to 5.5 V ($T_A = -40$ to $+105^\circ\text{C}$) | | | | | | | | | | |
| Operating ambient temperature | $T_A = 40$ to $+85^\circ\text{C}$ (A: Consumer applications, D: Industrial applications) $T_A = 40$ to $+105^\circ\text{C}$ (G: Industrial applications) | | | | | | | | | | |

Note The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

[80-pin, 100-pin, 128-pin products]

Caution This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

(1/2)

| Item | | 80-pin | | 100-pin | | 128-pin | |
|------------------------------------|--|---|----------|--|----------|---|----------|
| | | R5F100Mx | R5F101Mx | R5F100Px | R5F101Px | R5F100Sx | R5F101Sx |
| Code flash memory (KB) | | 96 to 512 | | 96 to 512 | | 192 to 512 | |
| Data flash memory (KB) | | 8 | – | 8 | – | 8 | – |
| RAM (KB) | | 8 to 32 ^{Note 1} | | 8 to 32 ^{Note 1} | | 16 to 32 ^{Note 1} | |
| Address space | | 1 MB | | | | | |
| Main system clock | High-speed system clock | X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (High-speed main) mode: 1 to 20 MHz ($V_{DD} = 2.7$ to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz ($V_{DD} = 2.4$ to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz ($V_{DD} = 1.8$ to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz ($V_{DD} = 1.6$ to 5.5 V) | | | | | |
| | High-speed on-chip oscillator | HS (High-speed main) mode: 1 to 32 MHz ($V_{DD} = 2.7$ to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz ($V_{DD} = 2.4$ to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz ($V_{DD} = 1.8$ to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz ($V_{DD} = 1.6$ to 5.5 V) | | | | | |
| Subsystem clock | | XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz | | | | | |
| Low-speed on-chip oscillator | | 15 kHz (TYP.) | | | | | |
| General-purpose register | | (8-bit register × 8) × 4 banks | | | | | |
| Minimum instruction execution time | | 0.03125 μ s (High-speed on-chip oscillator: $f_{IH} = 32$ MHz operation) | | | | | |
| | | 0.05 μ s (High-speed system clock: $f_{MX} = 20$ MHz operation) | | | | | |
| | | 30.5 μ s (Subsystem clock: $f_{SUB} = 32.768$ kHz operation) | | | | | |
| Instruction set | | <ul style="list-style-type: none"> • Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. | | | | | |
| I/O port | Total | 74 | | 92 | | 120 | |
| | CMOS I/O | 64 (N-ch O.D. I/O [E_{VDD} withstand voltage]: 21) | | 82 (N-ch O.D. I/O [E_{VDD} withstand voltage]: 24) | | 110 (N-ch O.D. I/O [E_{VDD} withstand voltage]: 25) | |
| | CMOS input | 5 | | 5 | | 5 | |
| | CMOS output | 1 | | 1 | | 1 | |
| | N-ch O.D. I/O (withstand voltage: 6 V) | 4 | | 4 | | 4 | |
| Timer | 16-bit timer | 12 channels | | 12 channels | | 16 channels | |
| | Watchdog timer | 1 channel | | 1 channel | | 1 channel | |
| | Real-time clock (RTC) | 1 channel | | 1 channel | | 1 channel | |
| | 12-bit interval timer (IT) | 1 channel | | 1 channel | | 1 channel | |
| | Timer output | 12 channels (PWM outputs: 10 ^{Note 2}) | | 12 channels (PWM outputs: 10 ^{Note 2}) | | 16 channels (PWM outputs: 14 ^{Note 2}) | |
| | RTC output | 1 channel • 1 Hz (subsystem clock: $f_{SUB} = 32.768$ kHz) | | | | | |

Notes 1. The flash library uses RAM in self-programming and rewriting of the data flash memory.

The target products and start address of the RAM areas used by the flash library are shown below.

R5F100xJ, R5F101xJ (x = M, P): Start address FAF00H

R5F100xL, R5F101xL (x = M, P, S): Start address F7F00H

For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

Notes 2. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves) (see **6.9.3 Operation as multiple PWM output function** in the RL78/G13 User's Manual).

(2/2)

| Item | 80-pin | | 100-pin | | 128-pin | |
|---|--|----------|-------------|----------|-------------|----------|
| | R5F100Mx | R5F101Mx | R5F100Px | R5F101Px | R5F100Sx | R5F101Sx |
| Clock output/buzzer output | 2 | | 2 | | 2 | |
| | <ul style="list-style-type: none"> 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN} = 20$ MHz operation) 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: $f_{SUB} = 32.768$ kHz operation) | | | | | |
| 8/10-bit resolution A/D converter | 17 channels | | 20 channels | | 26 channels | |
| Serial interface | [80-pin, 100-pin, 128-pin products] | | | | | |
| | <ul style="list-style-type: none"> CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channel CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channel CSI: 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channel | | | | | |
| I ² C bus | 2 channels | | 2 channels | | 2 channels | |
| Multiplier and divider/multiply-accumulator | <ul style="list-style-type: none"> 16 bits × 16 bits = 32 bits (Unsigned or signed) 32 bits ÷ 32 bits = 32 bits (Unsigned) 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed) | | | | | |
| DMA controller | 4 channels | | | | | |
| Vectored interrupt sources | Internal | 37 | | 37 | | 41 |
| | External | 13 | | 13 | | 13 |
| Key interrupt | 8 | | 8 | | 8 | |
| Reset | <ul style="list-style-type: none"> Reset by \overline{RESET} pin Internal reset by watchdog timer Internal reset by power-on-reset Internal reset by voltage detector Internal reset by illegal instruction execution ^{Note} Internal reset by RAM parity error Internal reset by illegal-memory access | | | | | |
| Power-on-reset circuit | <ul style="list-style-type: none"> Power-on-reset: 1.51 V (TYP.) Power-down-reset: 1.50 V (TYP.) | | | | | |
| Voltage detector | <ul style="list-style-type: none"> Rising edge : 1.67 V to 4.06 V (14 stages) Falling edge : 1.63 V to 3.98 V (14 stages) | | | | | |
| On-chip debug function | Provided | | | | | |
| Power supply voltage | $V_{DD} = 1.6$ to 5.5 V ($T_A = -40$ to $+85^\circ\text{C}$) $V_{DD} = 2.4$ to 5.5 V ($T_A = -40$ to $+105^\circ\text{C}$) | | | | | |
| Operating ambient temperature | $T_A = 40$ to $+85^\circ\text{C}$ (A: Consumer applications, D: Industrial applications) $T_A = 40$ to $+105^\circ\text{C}$ (G: Industrial applications) | | | | | |

Note The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

2. ELECTRICAL SPECIFICATIONS ($T_A = -40$ to $+85^\circ\text{C}$)

This chapter describes the following electrical specifications.

Target products A: Consumer applications $T_A = -40$ to $+85^\circ\text{C}$

R5F100xxAxx, R5F101xxAxx

D: Industrial applications $T_A = -40$ to $+85^\circ\text{C}$

R5F100xxDxx, R5F101xxDxx

G: Industrial applications when $T_A = -40$ to $+105^\circ\text{C}$ products is used in the range of $T_A = -40$ to $+85^\circ\text{C}$

R5F100xxGxx

- Cautions**
- 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.**
 - 2. With products not provided with an EV_{DD0} , EV_{DD1} , EV_{SS0} , or EV_{SS1} pin, replace EV_{DD0} and EV_{DD1} with V_{DD} , or replace EV_{SS0} and EV_{SS1} with V_{SS} .**
 - 3. The pins mounted depend on the product. Refer to 2.1 Port Function to 2.2.1 Functions for each product in the RL78/G13 User's Manual.**

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$) (1/2)

| Parameter | Symbols | Conditions | Ratings | Unit |
|------------------------|----------------------|---|---|------|
| Supply voltage | V_{DD} | | -0.5 to +6.5 | V |
| | EV_{DD0}, EV_{DD1} | $EV_{DD0} = EV_{DD1}$ | -0.5 to +6.5 | V |
| | EV_{SS0}, EV_{SS1} | $EV_{SS0} = EV_{SS1}$ | -0.5 to +0.3 | V |
| REGC pin input voltage | V_{IREGC} | REGC | -0.3 to +2.8 and -0.3 to $V_{DD} + 0.3$ ^{Note 1} | V |
| Input voltage | V_{I1} | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147 | -0.3 to $EV_{DD0} + 0.3$ and -0.3 to $V_{DD} + 0.3$ ^{Note 2} | V |
| | V_{I2} | P60 to P63 (N-ch open-drain) | -0.3 to +6.5 | V |
| | V_{I3} | P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, RESET | -0.3 to $V_{DD} + 0.3$ ^{Note 2} | V |
| Output voltage | V_{O1} | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | -0.3 to $EV_{DD0} + 0.3$ and -0.3 to $V_{DD} + 0.3$ ^{Note 2} | V |
| | V_{O2} | P20 to P27, P150 to P156 | -0.3 to $V_{DD} + 0.3$ ^{Note 2} | V |
| Analog input voltage | V_{AI1} | ANI16 to ANI26 | -0.3 to $EV_{DD0} + 0.3$ and -0.3 to $AV_{REF(+)} + 0.3$ ^{Notes 2, 3} | V |
| | V_{AI2} | ANI0 to ANI14 | -0.3 to $V_{DD} + 0.3$ and -0.3 to $AV_{REF(+)} + 0.3$ ^{Notes 2, 3} | V |

Notes 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

2. Must be 6.5 V or lower.

3. Do not exceed $AV_{REF(+)} + 0.3$ V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. $AV_{REF(+)}$: + side reference voltage of the A/D converter.

3. V_{SS} : Reference voltage

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$) (2/2)

| Parameter | Symbols | Conditions | | Ratings | Unit |
|-------------------------------|----------------------------------|------------------------------|--|--|------------|
| Output current, high | I _{OH1} | Per pin | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | -40 | mA |
| | | Total of all pins -170 mA | P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 | -70 | mA |
| | | | P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 | -100 | mA |
| | I _{OH2} | Per pin | P20 to P27, P150 to P156 | -0.5 | mA |
| | | Total of all pins | | -2 | mA |
| | Output current, low | I _{OL1} | Per pin | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | 40 |
| Total of all pins 170 mA | | | P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 | 70 | mA |
| | | | P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 | 100 | mA |
| I _{OL2} | | Per pin | P20 to P27, P150 to P156 | 1 | mA |
| | | Total of all pins | | 5 | mA |
| Operating ambient temperature | | T _A | In normal operation mode | | -40 to +85 |
| | In flash memory programming mode | | | | |
| Storage temperature | T _{stg} | | | -65 to +150 | °C |

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.2 Oscillator Characteristics

2.2.1 X1, XT1 oscillator characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

| Parameter | Resonator | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|--|------|--------|------|------|
| X1 clock oscillation frequency (f_x) ^{Note} | Ceramic resonator/ crystal resonator | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 1.0 | | 20.0 | MHz |
| | | $2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$ | 1.0 | | 16.0 | MHz |
| | | $1.8\text{ V} \leq V_{DD} < 2.4\text{ V}$ | 1.0 | | 8.0 | MHz |
| | | $1.6\text{ V} \leq V_{DD} < 1.8\text{ V}$ | 1.0 | | 4.0 | MHz |
| XT1 clock oscillation frequency (f_x) ^{Note} | Crystal resonator | | 32 | 32.768 | 35 | kHz |

Note Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator and XT1 oscillator, refer to **5.4 System Clock Oscillator** in the RL78/G13 User's Manual.

2.2.2 On-chip oscillator characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

| Oscillators | Parameters | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|------------|------------------------------|--|------|------|------|------|
| High-speed on-chip oscillator clock frequency ^{Notes 1, 2} | f_{IH} | | | 1 | | 32 | MHz |
| High-speed on-chip oscillator clock frequency accuracy | | -20 to $+85^\circ\text{C}$ | $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | -1.0 | | +1.0 | % |
| | | | $1.6\text{ V} \leq V_{DD} < 1.8\text{ V}$ | -5.0 | | +5.0 | % |
| | | -40 to -20°C | $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | -1.5 | | +1.5 | % |
| | | | $1.6\text{ V} \leq V_{DD} < 1.8\text{ V}$ | -5.5 | | +5.5 | % |
| Low-speed on-chip oscillator clock frequency | f_{IL} | | | | 15 | | kHz |
| Low-speed on-chip oscillator clock frequency accuracy | | | | -15 | | +15 | % |

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

2. This indicates the oscillator characteristics only. Refer to AC Characteristics for instruction execution time.

2.3 DC Characteristics

2.3.1 Pin characteristics

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/5)

| Items | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | | |
|--|------------------|--|---|---------------------------------|------|------------------|------------------------|----|
| Output current, high ^{Note 1} | I _{OH1} | Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | 1.6 V ≤ EV _{DD0} ≤ 5.5 V | | | -10.0 Note 2 | mA | |
| | | Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (When duty ≤ 70% ^{Note 3}) | 4.0 V ≤ EV _{DD0} ≤ 5.5 V | | | -55.0 | mA | |
| | | | 2.7 V ≤ EV _{DD0} < 4.0 V | | | -10.0 | mA | |
| | | | 1.8 V ≤ EV _{DD0} < 2.7 V | | | -5.0 | mA | |
| | | | 1.6 V ≤ EV _{DD0} < 1.8 V | | | -2.5 | mA | |
| | | Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (When duty ≤ 70% ^{Note 3}) | 4.0 V ≤ EV _{DD0} ≤ 5.5 V | | | -80.0 | mA | |
| | | | 2.7 V ≤ EV _{DD0} < 4.0 V | | | -19.0 | mA | |
| | | | 1.8 V ≤ EV _{DD0} < 2.7 V | | | -10.0 | mA | |
| | | Total of all pins (When duty ≤ 70% ^{Note 3}) | 1.6 V ≤ EV _{DD0} ≤ 5.5 V | | | -135.0 Note 4 | mA | |
| | | I _{OH2} | Per pin for P20 to P27, P150 to P156 | 1.6 V ≤ V _{DD} ≤ 5.5 V | | | -0.1 ^{Note 2} | mA |
| | | | Total of all pins (When duty ≤ 70% ^{Note 3}) | 1.6 V ≤ V _{DD} ≤ 5.5 V | | | -1.5 | mA |

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the EV_{DD0}, EV_{DD1}, V_{DD} pins to an output pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = -10.0 mA

$$\text{Total output current of pins} = (-10.0 \times 0.7)/(80 \times 0.01) \cong -8.7 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

4. The applied current for the products for industrial application (R5F100xxDxx, R5F101xxDxx, R5F100xxGxx) is -100 mA.

Caution P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/5)

| Items | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|---|---|--|-----------------------------------|------|------------------------|------|----|
| Output current, I _{OL} ^{Note 1} | I _{OL1} | Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | | | 20.0 ^{Note 2} | mA | |
| | | Per pin for P60 to P63 | | | 15.0 ^{Note 2} | mA | |
| | | Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (When duty ≤ 70% ^{Note 3}) | 4.0 V ≤ EV _{DD0} ≤ 5.5 V | | | 70.0 | mA |
| | | | 2.7 V ≤ EV _{DD0} < 4.0 V | | | 15.0 | mA |
| | | | 1.8 V ≤ EV _{DD0} < 2.7 V | | | 9.0 | mA |
| | | | 1.6 V ≤ EV _{DD0} < 1.8 V | | | 4.5 | mA |
| | | Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (When duty ≤ 70% ^{Note 3}) | 4.0 V ≤ EV _{DD0} ≤ 5.5 V | | | 80.0 | mA |
| | | | 2.7 V ≤ EV _{DD0} < 4.0 V | | | 35.0 | mA |
| | | | 1.8 V ≤ EV _{DD0} < 2.7 V | | | 20.0 | mA |
| | | | 1.6 V ≤ EV _{DD0} < 1.8 V | | | 10.0 | mA |
| | Total of all pins (When duty ≤ 70% ^{Note 3}) | | | | 150.0 | mA | |
| I _{OL2} | Per pin for P20 to P27, P150 to P156 | | | | 0.4 ^{Note 2} | mA | |
| | Total of all pins (When duty ≤ 70% ^{Note 3}) | 1.6 V ≤ V _{DD} ≤ 5.5 V | | | 5.0 | mA | |

- Notes**
- Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EV_{SS0}, EV_{SS1} and V_{SS} pin.
 - However, do not exceed the total current value.
 - Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA

$$\text{Total output current of pins} = (10.0 \times 0.7)/(80 \times 0.01) \cong 8.7 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$) (3/5)

| Items | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|---------------------|--|--|--|-----------------------------|------------------------|-----------------------------|---|
| Input voltage, high | $V_{\text{IH}1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147 | Normal input buffer | $0.8\text{EV}_{\text{DD}0}$ | | $\text{EV}_{\text{DD}0}$ | V |
| | $V_{\text{IH}2}$ | P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143 | TTL input buffer $4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | 2.2 | | $\text{EV}_{\text{DD}0}$ | V |
| | | | TTL input buffer $3.3\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$ | 2.0 | | $\text{EV}_{\text{DD}0}$ | V |
| | | | TTL input buffer $1.6\text{ V} \leq \text{EV}_{\text{DD}0} < 3.3\text{ V}$ | 1.5 | | $\text{EV}_{\text{DD}0}$ | V |
| | $V_{\text{IH}3}$ | P20 to P27, P150 to P156 | | 0.7V_{DD} | | V_{DD} | V |
| | $V_{\text{IH}4}$ | P60 to P63 | | $0.7\text{EV}_{\text{DD}0}$ | | 6.0 | V |
| $V_{\text{IH}5}$ | P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$ | | 0.8V_{DD} | | V_{DD} | V | |
| Input voltage, low | $V_{\text{IL}1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147 | Normal input buffer | 0 | | $0.2\text{EV}_{\text{DD}0}$ | V |
| | $V_{\text{IL}2}$ | P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143 | TTL input buffer $4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | 0 | | 0.8 | V |
| | | | TTL input buffer $3.3\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$ | 0 | | 0.5 | V |
| | | | TTL input buffer $1.6\text{ V} \leq \text{EV}_{\text{DD}0} < 3.3\text{ V}$ | 0 | | 0.32 | V |
| | $V_{\text{IL}3}$ | P20 to P27, P150 to P156 | | 0 | | 0.3V_{DD} | V |
| | $V_{\text{IL}4}$ | P60 to P63 | | 0 | | $0.3\text{EV}_{\text{DD}0}$ | V |
| | $V_{\text{IL}5}$ | P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$ | | 0 | | 0.2V_{DD} | V |

Caution The maximum value of V_{IH} of pins P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 is $\text{EV}_{\text{DD}0}$, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$) (4/5)

| Items | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|----------------------|------------------|--|---|------------------|------|------|
| Output voltage, high | V _{OH1} | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | $4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OH1} = -10.0\text{ mA}$ | $EV_{DD0} - 1.5$ | | V |
| | | | $4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OH1} = -3.0\text{ mA}$ | $EV_{DD0} - 0.7$ | | V |
| | | | $2.7\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OH1} = -2.0\text{ mA}$ | $EV_{DD0} - 0.6$ | | V |
| | | | $1.8\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OH1} = -1.5\text{ mA}$ | $EV_{DD0} - 0.5$ | | V |
| | | | $1.6\text{ V} \leq EV_{DD0} < 5.5\text{ V}$, $I_{OH1} = -1.0\text{ mA}$ | $EV_{DD0} - 0.5$ | | V |
| | V _{OH2} | P20 to P27, P150 to P156 | $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH2} = -100\text{ }\mu\text{A}$ | $V_{DD} - 0.5$ | | V |
| Output voltage, low | V _{OL1} | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | $4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OL1} = 20\text{ mA}$ | | 1.3 | V |
| | | | $4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OL1} = 8.5\text{ mA}$ | | 0.7 | V |
| | | | $2.7\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OL1} = 3.0\text{ mA}$ | | 0.6 | V |
| | | | $2.7\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OL1} = 1.5\text{ mA}$ | | 0.4 | V |
| | | | $1.8\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OL1} = 0.6\text{ mA}$ | | 0.4 | V |
| | | | $1.6\text{ V} \leq EV_{DD0} < 5.5\text{ V}$, $I_{OL1} = 0.3\text{ mA}$ | | 0.4 | V |
| | V _{OL2} | P20 to P27, P150 to P156 | $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL2} = 400\text{ }\mu\text{A}$ | | 0.4 | V |
| | V _{OL3} | P60 to P63 | $4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OL3} = 15.0\text{ mA}$ | | 2.0 | V |
| | | | $4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OL3} = 5.0\text{ mA}$ | | 0.4 | V |
| | | | $2.7\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OL3} = 3.0\text{ mA}$ | | 0.4 | V |
| | | | $1.8\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OL3} = 2.0\text{ mA}$ | | 0.4 | V |
| | | | $1.6\text{ V} \leq EV_{DD0} < 5.5\text{ V}$, $I_{OL3} = 1.0\text{ mA}$ | | 0.4 | V |

Caution P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$) (5/5)

| Items | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | | |
|-----------------------------|------------|--|----------------------------------|---------------------------------------|------|---------------|-----|------------------|
| Input leakage current, high | I_{LH1} | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147 | $V_i = EV_{DD0}$ | | 1 | μA | | |
| | I_{LH2} | P20 to P27, P137, P150 to P156, $\overline{\text{RESET}}$ | $V_i = V_{DD}$ | | 1 | μA | | |
| | I_{LH3} | P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS) | $V_i = V_{DD}$ | In input port or external clock input | 1 | μA | | |
| | | | | In resonator connection | 10 | μA | | |
| Input leakage current, low | I_{LIL1} | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147 | $V_i = EV_{SS0}$ | | -1 | μA | | |
| | I_{LIL2} | P20 to P27, P137, P150 to P156, $\overline{\text{RESET}}$ | $V_i = V_{SS}$ | | -1 | μA | | |
| | I_{LIL3} | P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS) | $V_i = V_{SS}$ | In input port or external clock input | -1 | μA | | |
| | | | | In resonator connection | -10 | μA | | |
| On-chip pll-up resistance | R_U | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147 | $V_i = EV_{SS0}$, In input port | | 10 | 20 | 100 | $\text{k}\Omega$ |

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.3.2 Supply current characteristics

(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (1/2)

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit | |
|---|---|---|---|--|-------------------------|-------------------------|------|------|------|----|
| Supply current ^{Note 1} | I _{DD1} | Operating mode | HS (high-speed main) mode ^{Note 5} | f _{IH} = 32 MHz ^{Note 3} | Basic operation | V _{DD} = 5.0 V | | 2.1 | | mA |
| | | | | | | V _{DD} = 3.0 V | | 2.1 | | mA |
| | | | | | Normal operation | V _{DD} = 5.0 V | | 4.6 | 7.0 | mA |
| | | | | V _{DD} = 3.0 V | | | 4.6 | 7.0 | mA | |
| | | | | f _{IH} = 24 MHz ^{Note 3} | Normal operation | V _{DD} = 5.0 V | | 3.7 | 5.5 | mA |
| | | | | | | V _{DD} = 3.0 V | | 3.7 | 5.5 | mA |
| | | | f _{IH} = 16 MHz ^{Note 3} | Normal operation | V _{DD} = 5.0 V | | 2.7 | 4.0 | mA | |
| | | | | | V _{DD} = 3.0 V | | 2.7 | 4.0 | mA | |
| | | | LS (low-speed main) mode ^{Note 5} | f _{IH} = 8 MHz ^{Note 3} | Normal operation | V _{DD} = 3.0 V | | 1.2 | 1.8 | mA |
| | | | | | | V _{DD} = 2.0 V | | 1.2 | 1.8 | mA |
| | | | LV (low-voltage main) mode ^{Note 5} | f _{IH} = 4 MHz ^{Note 3} | Normal operation | V _{DD} = 3.0 V | | 1.2 | 1.7 | mA |
| | | | | | | V _{DD} = 2.0 V | | 1.2 | 1.7 | mA |
| | | HS (high-speed main) mode ^{Note 5} | f _{MX} = 20 MHz ^{Note 2} , V _{DD} = 5.0 V | Normal operation | Square wave input | | 3.0 | 4.6 | mA | |
| | | | | | Resonator connection | | 3.2 | 4.8 | mA | |
| | | | | Normal operation | Square wave input | | 3.0 | 4.6 | mA | |
| | | | | | Resonator connection | | 3.2 | 4.8 | mA | |
| | | | f _{MX} = 10 MHz ^{Note 2} , V _{DD} = 5.0 V | Normal operation | Square wave input | | 1.9 | 2.7 | mA | |
| | | | | | Resonator connection | | 1.9 | 2.7 | mA | |
| | | | f _{MX} = 10 MHz ^{Note 2} , V _{DD} = 3.0 V | Normal operation | Square wave input | | 1.9 | 2.7 | mA | |
| | | | | | Resonator connection | | 1.9 | 2.7 | mA | |
| | | LS (low-speed main) mode ^{Note 5} | f _{MX} = 8 MHz ^{Note 2} , V _{DD} = 3.0 V | Normal operation | Square wave input | | 1.1 | 1.7 | mA | |
| | | | | | Resonator connection | | 1.1 | 1.7 | mA | |
| | | | f _{MX} = 8 MHz ^{Note 2} , V _{DD} = 2.0 V | Normal operation | Square wave input | | 1.1 | 1.7 | mA | |
| | | | | | Resonator connection | | 1.1 | 1.7 | mA | |
| Subsystem clock operation | f _{SUB} = 32.768 kHz ^{Note 4} T _A = -40°C | Normal operation | Square wave input | | 4.1 | 4.9 | μA | | | |
| | | | Resonator connection | | 4.2 | 5.0 | μA | | | |
| | f _{SUB} = 32.768 kHz ^{Note 4} T _A = +25°C | Normal operation | Square wave input | | 4.1 | 4.9 | μA | | | |
| | | | Resonator connection | | 4.2 | 5.0 | μA | | | |
| | f _{SUB} = 32.768 kHz ^{Note 4} T _A = +50°C | Normal operation | Square wave input | | 4.2 | 5.5 | μA | | | |
| | | | Resonator connection | | 4.3 | 5.6 | μA | | | |
| | f _{SUB} = 32.768 kHz ^{Note 4} T _A = +70°C | Normal operation | Square wave input | | 4.3 | 6.3 | μA | | | |
| | | | Resonator connection | | 4.4 | 6.4 | μA | | | |
| f _{SUB} = 32.768 kHz ^{Note 4} T _A = +85°C | Normal operation | Square wave input | | 4.6 | 7.7 | μA | | | | |
| | | Resonator connection | | 4.7 | 7.8 | μA | | | | |

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD} and EV_{DD0} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD0} or V_{SS} , EV_{SS0} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. When high-speed on-chip oscillator and subsystem clock are stopped.
 3. When high-speed system clock and subsystem clock are stopped.
 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 - HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
 - LS (low-speed main) mode: $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }8\text{ MHz}$
 - LV (low-voltage main) mode: $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }4\text{ MHz}$

- Remarks**
1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH} : High-speed on-chip oscillator clock frequency
 3. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation, temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (2/2)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit | | |
|--|----------------------------|------------------------|-----------------------------------|--|-------------------------|------|------|------|----|
| Supply current Note 1 | I _{DD2} Note 2 | HALT mode | HS (high-speed main) mode Note 7 | f _{IH} = 32 MHz Note 4 | V _{DD} = 5.0 V | | 0.54 | 1.63 | mA |
| | | | | | V _{DD} = 3.0 V | | 0.54 | 1.63 | mA |
| | | | | f _{IH} = 24 MHz Note 4 | V _{DD} = 5.0 V | | 0.44 | 1.28 | mA |
| | | | | | V _{DD} = 3.0 V | | 0.44 | 1.28 | mA |
| | | | | f _{IH} = 16 MHz Note 4 | V _{DD} = 5.0 V | | 0.40 | 1.00 | mA |
| | | | | | V _{DD} = 3.0 V | | 0.40 | 1.00 | mA |
| | | | LS (low-speed main) mode Note 7 | f _{IH} = 8 MHz Note 4 | V _{DD} = 3.0 V | | 260 | 530 | μA |
| | | | | | V _{DD} = 2.0 V | | 260 | 530 | μA |
| | | | LV (low-voltage main) mode Note 7 | f _{IH} = 4 MHz Note 4 | V _{DD} = 3.0 V | | 420 | 640 | μA |
| | | | | | V _{DD} = 2.0 V | | 420 | 640 | μA |
| | | | HS (high-speed main) mode Note 7 | f _{MX} = 20 MHz Note 3, V _{DD} = 5.0 V | Square wave input | | 0.28 | 1.00 | mA |
| | | | | | Resonator connection | | 0.45 | 1.17 | mA |
| | | | | f _{MX} = 20 MHz Note 3, V _{DD} = 3.0 V | Square wave input | | 0.28 | 1.00 | mA |
| | | | | | Resonator connection | | 0.45 | 1.17 | mA |
| | | | | f _{MX} = 10 MHz Note 3, V _{DD} = 5.0 V | Square wave input | | 0.19 | 0.60 | mA |
| | | | | | Resonator connection | | 0.26 | 0.67 | mA |
| | | | | f _{MX} = 10 MHz Note 3, V _{DD} = 3.0 V | Square wave input | | 0.19 | 0.60 | mA |
| | | | | | Resonator connection | | 0.26 | 0.67 | mA |
| | | | LS (low-speed main) mode Note 7 | f _{MX} = 8 MHz Note 3, V _{DD} = 3.0 V | Square wave input | | 95 | 330 | μA |
| | | | | | Resonator connection | | 145 | 380 | μA |
| | | | | f _{MX} = 8 MHz Note 3, V _{DD} = 2.0 V | Square wave input | | 95 | 330 | μA |
| | | | | | Resonator connection | | 145 | 380 | μA |
| | | | Subsystem clock operation | f _{SUB} = 32.768 kHz Note 5 T _A = -40°C | Square wave input | | 0.25 | 0.57 | μA |
| | | | | | Resonator connection | | 0.44 | 0.76 | μA |
| | | | | f _{SUB} = 32.768 kHz Note 5 T _A = +25°C | Square wave input | | 0.30 | 0.57 | μA |
| | | | | | Resonator connection | | 0.49 | 0.76 | μA |
| | | | | f _{SUB} = 32.768 kHz Note 5 T _A = +50°C | Square wave input | | 0.37 | 1.17 | μA |
| | | | | | Resonator connection | | 0.56 | 1.36 | μA |
| f _{SUB} = 32.768 kHz Note 5 T _A = +70°C | Square wave input | | | 0.53 | 1.97 | μA | | | |
| | Resonator connection | | | 0.72 | 2.16 | μA | | | |
| f _{SUB} = 32.768 kHz Note 5 T _A = +85°C | Square wave input | | 0.82 | 3.37 | μA | | | | |
| | Resonator connection | | 1.01 | 3.56 | μA | | | | |
| I _{DD3} Note 6 | STOP mode Note 8 | T _A = -40°C | | | 0.18 | 0.50 | μA | | |
| | | T _A = +25°C | | | 0.23 | 0.50 | μA | | |
| | | T _A = +50°C | | | 0.30 | 1.10 | μA | | |
| | | T _A = +70°C | | | 0.46 | 1.90 | μA | | |
| | | T _A = +85°C | | | 0.75 | 3.30 | μA | | |

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD} and EV_{DD0} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD0} or V_{SS} , EV_{SS0} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. During HALT instruction execution by flash memory.
 3. When high-speed on-chip oscillator and subsystem clock are stopped.
 4. When high-speed system clock and subsystem clock are stopped.
 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When $RTCLPC = 1$ and setting ultra-low current consumption ($AMPHS1 = 1$). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 - HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
 - LS (low-speed main) mode: $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }8\text{ MHz}$
 - LV (low-voltage main) mode: $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }4\text{ MHz}$
 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks**
1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH} : High-speed on-chip oscillator clock frequency
 3. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/2)

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit | |
|---|-------------------------|-------------------------|-------------------------------------|---|------------------|-------------------------|------|------|------|----|
| Supply current Note 1 | I _{DD1} | Operating mode | HS (high-speed main) mode Note 5 | f _{IH} = 32 MHz Note 3 | Basic operation | V _{DD} = 5.0 V | | 2.3 | | mA |
| | | | | | | V _{DD} = 3.0 V | | 2.3 | | mA |
| | | | | | Normal operation | V _{DD} = 5.0 V | | 5.2 | 8.5 | mA |
| | | | | | | V _{DD} = 3.0 V | | 5.2 | 8.5 | mA |
| | | | | | Normal operation | V _{DD} = 5.0 V | | 4.1 | 6.6 | mA |
| | | | | | | V _{DD} = 3.0 V | | 4.1 | 6.6 | mA |
| | | | | f _{IH} = 24 MHz Note 3 | Normal operation | V _{DD} = 5.0 V | | 3.0 | 4.7 | mA |
| | | | | | | V _{DD} = 3.0 V | | 3.0 | 4.7 | mA |
| | | | | | Normal operation | V _{DD} = 5.0 V | | 1.3 | 2.1 | mA |
| | | | | | | V _{DD} = 2.0 V | | 1.3 | 2.1 | mA |
| | | | | | Normal operation | V _{DD} = 3.0 V | | 1.3 | 1.8 | mA |
| | | | | | | V _{DD} = 2.0 V | | 1.3 | 1.8 | mA |
| | | | LS (low-speed main) mode Note 5 | f _{IH} = 8 MHz Note 3 | Normal operation | V _{DD} = 3.0 V | | 1.3 | 1.8 | mA |
| | | | | | | V _{DD} = 2.0 V | | 1.3 | 1.8 | mA |
| | | | | | Normal operation | V _{DD} = 3.0 V | | 3.4 | 5.5 | mA |
| | | | | | | V _{DD} = 2.0 V | | 3.4 | 5.5 | mA |
| | | | | | Normal operation | V _{DD} = 5.0 V | | 2.1 | 3.2 | mA |
| | | | | | | V _{DD} = 3.0 V | | 2.1 | 3.2 | mA |
| | | | | f _{IH} = 4 MHz Note 3 | Normal operation | V _{DD} = 3.0 V | | 1.2 | 2.0 | mA |
| | | | | | | V _{DD} = 2.0 V | | 1.2 | 2.0 | mA |
| | | | | | Normal operation | V _{DD} = 3.0 V | | 1.2 | 2.0 | mA |
| | | | | | | V _{DD} = 2.0 V | | 1.2 | 2.0 | mA |
| | | | | | Normal operation | V _{DD} = 3.0 V | | 1.2 | 2.0 | mA |
| | | | | | | V _{DD} = 2.0 V | | 1.2 | 2.0 | mA |
| | | | Subsystem clock operation | f _{SUB} = 32.768 kHz Note 4 | Normal operation | V _{DD} = 5.0 V | | 4.8 | 5.9 | μA |
| | | | | | | V _{DD} = 3.0 V | | 4.9 | 6.0 | μA |
| | | | | | Normal operation | V _{DD} = 5.0 V | | 4.9 | 5.9 | μA |
| | | | | | | V _{DD} = 3.0 V | | 5.0 | 6.0 | μA |
| Normal operation | V _{DD} = 5.0 V | | | | 5.0 | 7.6 | μA | | | |
| | V _{DD} = 3.0 V | | | | 5.1 | 7.7 | μA | | | |
| f _{SUB} = 32.768 kHz Note 4 | Normal operation | V _{DD} = 5.0 V | | | 5.2 | 9.3 | μA | | | |
| | | V _{DD} = 3.0 V | | | 5.3 | 9.4 | μA | | | |
| | Normal operation | V _{DD} = 5.0 V | | | 5.7 | 13.3 | μA | | | |
| | | V _{DD} = 3.0 V | | | 5.8 | 13.4 | μA | | | |
| | Normal operation | V _{DD} = 5.0 V | | | 5.7 | 13.3 | μA | | | |
| | | V _{DD} = 3.0 V | | | 5.8 | 13.4 | μA | | | |

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD} , EV_{DD0} , and EV_{DD1} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD0} , and EV_{DD1} , or V_{SS} , EV_{SS0} , and EV_{SS1} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. When high-speed on-chip oscillator and subsystem clock are stopped.
 3. When high-speed system clock and subsystem clock are stopped.
 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.
 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 - HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
 - LS (low-speed main) mode: $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }8\text{ MHz}$
 - LV (low-voltage main) mode: $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }4\text{ MHz}$

- Remarks**
1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH} : High-speed on-chip oscillator clock frequency
 3. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation, temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/2)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit | | |
|---|-----------------------------|------------------------------------|---|---|-------------------------|------|------|------|----|
| Supply current Note 1 | I _{DD2} Note 2 | HALT mode Note 7 | HS (high-speed main) mode Note 7 | f _{IH} = 32 MHz ^{Note 4} | V _{DD} = 5.0 V | | 0.62 | 1.86 | mA |
| | | | | | V _{DD} = 3.0 V | | 0.62 | 1.86 | mA |
| | | | | f _{IH} = 24 MHz ^{Note 4} | V _{DD} = 5.0 V | | 0.50 | 1.45 | mA |
| | | | | | V _{DD} = 3.0 V | | 0.50 | 1.45 | mA |
| | | | | f _{IH} = 16 MHz ^{Note 4} | V _{DD} = 5.0 V | | 0.44 | 1.11 | mA |
| | | | | | V _{DD} = 3.0 V | | 0.44 | 1.11 | mA |
| | | | LS (low-speed main) mode Note 7 | f _{IH} = 8 MHz ^{Note 4} | V _{DD} = 3.0 V | | 290 | 620 | μA |
| | | | | V _{DD} = 2.0 V | | 290 | 620 | μA | |
| | | | LV (low-voltage main) mode Note 7 | f _{IH} = 4 MHz ^{Note 4} | V _{DD} = 3.0 V | | 440 | 680 | μA |
| | | | | | V _{DD} = 2.0 V | | 440 | 680 | μA |
| | | | HS (high-speed main) mode Note 7 | f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 5.0 V | Square wave input | | 0.31 | 1.08 | mA |
| | | | | | Resonator connection | | 0.48 | 1.28 | mA |
| | | | | | Square wave input | | 0.31 | 1.08 | mA |
| | | | | | Resonator connection | | 0.48 | 1.28 | mA |
| | | | | f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 5.0 V | Square wave input | | 0.21 | 0.63 | mA |
| | | | | | Resonator connection | | 0.28 | 0.71 | mA |
| | | | | f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 3.0 V | Square wave input | | 0.21 | 0.63 | mA |
| | | | | | Resonator connection | | 0.28 | 0.71 | mA |
| | | LS (low-speed main) mode Note 7 | f _{MX} = 8 MHz ^{Note 3} , V _{DD} = 3.0 V | Square wave input | | 110 | 360 | μA | |
| | | | | Resonator connection | | 160 | 420 | μA | |
| | | | f _{MX} = 8 MHz ^{Note 3} , V _{DD} = 2.0 V | Square wave input | | 110 | 360 | μA | |
| | | | | Resonator connection | | 160 | 420 | μA | |
| | | Subsystem clock operation | f _{SUB} = 32.768 kHz ^{Note 5} T _A = -40°C | Square wave input | | 0.28 | 0.61 | μA | |
| | | | | Resonator connection | | 0.47 | 0.80 | μA | |
| | | | f _{SUB} = 32.768 kHz ^{Note 5} T _A = +25°C | Square wave input | | 0.34 | 0.61 | μA | |
| | | | | Resonator connection | | 0.53 | 0.80 | μA | |
| | | | f _{SUB} = 32.768 kHz ^{Note 5} T _A = +50°C | Square wave input | | 0.41 | 2.30 | μA | |
| | | | | Resonator connection | | 0.60 | 2.49 | μA | |
| | | | f _{SUB} = 32.768 kHz ^{Note 5} T _A = +70°C | Square wave input | | 0.64 | 4.03 | μA | |
| | | | | Resonator connection | | 0.83 | 4.22 | μA | |
| f _{SUB} = 32.768 kHz ^{Note 5} T _A = +85°C | Square wave input | | 1.09 | 8.04 | μA | | | | |
| | Resonator connection | | 1.28 | 8.23 | μA | | | | |
| I _{DD3} ^{Note 6} | STOP mode ^{Note 8} | T _A = -40°C | | | 0.19 | 0.52 | μA | | |
| | | T _A = +25°C | | | 0.25 | 0.52 | μA | | |
| | | T _A = +50°C | | | 0.32 | 2.21 | μA | | |
| | | T _A = +70°C | | | 0.55 | 3.94 | μA | | |
| | | T _A = +85°C | | | 1.00 | 7.95 | μA | | |

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD} , EV_{DD0} , and EV_{DD1} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD0} , and EV_{DD1} , or V_{SS} , EV_{SS0} , and EV_{SS1} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. During HALT instruction execution by flash memory.
 3. When high-speed on-chip oscillator and subsystem clock are stopped.
 4. When high-speed system clock and subsystem clock are stopped.
 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When $RTCLPC = 1$ and setting ultra-low current consumption ($AMPHS1 = 1$). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 - HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
 - LS (low-speed main) mode: $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }8\text{ MHz}$
 - LV (low-voltage main) mode: $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }4\text{ MHz}$

R5F Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks**
1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH} : High-speed on-chip oscillator clock frequency
 3. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

(3) 128-pin products, and flash ROM: 384 to 512 KB of 44- to 100-pin products

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/2)

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit | |
|---|------------------|--|---|--|-------------------------|-------------------------|------|------|------|----|
| Supply current ^{Note 1} | I _{DD1} | Operating mode | HS (high-speed main) mode ^{Note 5} | f _{IH} = 32 MHz ^{Note 3} | Basic operation | V _{DD} = 5.0 V | | 2.6 | | mA |
| | | | | | | V _{DD} = 3.0 V | | 2.6 | | mA |
| | | | | Normal operation | V _{DD} = 5.0 V | | 6.1 | 9.5 | mA | |
| | | | | | V _{DD} = 3.0 V | | 6.1 | 9.5 | mA | |
| | | | | f _{IH} = 24 MHz ^{Note 3} | Normal operation | V _{DD} = 5.0 V | | 4.8 | 7.4 | mA |
| | | | | | | V _{DD} = 3.0 V | | 4.8 | 7.4 | mA |
| | | | f _{IH} = 16 MHz ^{Note 3} | Normal operation | V _{DD} = 5.0 V | | 3.5 | 5.3 | mA | |
| | | | | | V _{DD} = 3.0 V | | 3.5 | 5.3 | mA | |
| | | | LS (low-speed main) mode ^{Note 5} | f _{IH} = 8 MHz ^{Note 3} | Normal operation | V _{DD} = 3.0 V | | 1.5 | 2.3 | mA |
| | | | | | | V _{DD} = 2.0 V | | 1.5 | 2.3 | mA |
| | | | LV (low-voltage main) mode ^{Note 5} | f _{IH} = 4 MHz ^{Note 3} | Normal operation | V _{DD} = 3.0 V | | 1.5 | 2.0 | mA |
| | | | | | | V _{DD} = 2.0 V | | 1.5 | 2.0 | mA |
| | | | HS (high-speed main) mode ^{Note 5} | f _{MX} = 20 MHz ^{Note 2} , V _{DD} = 5.0 V | Normal operation | Square wave input | | 3.9 | 6.1 | mA |
| | | | | | | Resonator connection | | 4.1 | 6.3 | mA |
| | | Normal operation | | | Square wave input | | 3.9 | 6.1 | mA | |
| | | | | | Resonator connection | | 4.1 | 6.3 | mA | |
| | | f _{MX} = 10 MHz ^{Note 2} , V _{DD} = 5.0 V | | Normal operation | Square wave input | | 2.5 | 3.7 | mA | |
| | | | | | Resonator connection | | 2.5 | 3.7 | mA | |
| | | | | Normal operation | Square wave input | | 2.5 | 3.7 | mA | |
| | | | | | Resonator connection | | 2.5 | 3.7 | mA | |
| | | LS (low-speed main) mode ^{Note 5} | f _{MX} = 8 MHz ^{Note 2} , V _{DD} = 3.0 V | Normal operation | Square wave input | | 1.4 | 2.2 | mA | |
| | | | | | Resonator connection | | 1.4 | 2.2 | mA | |
| | | | f _{MX} = 8 MHz ^{Note 2} , V _{DD} = 2.0 V | Normal operation | Square wave input | | 1.4 | 2.2 | mA | |
| | | | | | Resonator connection | | 1.4 | 2.2 | mA | |
| | | Subsystem clock operation | f _{SUB} = 32.768 kHz ^{Note 4} T _A = -40°C | Normal operation | Square wave input | | 5.4 | 6.5 | μA | |
| | | | | | Resonator connection | | 5.5 | 6.6 | μA | |
| | | | f _{SUB} = 32.768 kHz ^{Note 4} T _A = +25°C | Normal operation | Square wave input | | 5.5 | 6.5 | μA | |
| | | | | | Resonator connection | | 5.6 | 6.6 | μA | |
| f _{SUB} = 32.768 kHz ^{Note 4} T _A = +50°C | Normal operation | | Square wave input | | 5.6 | 9.4 | μA | | | |
| | | | Resonator connection | | 5.7 | 9.5 | μA | | | |
| f _{SUB} = 32.768 kHz ^{Note 4} T _A = +70°C | Normal operation | | Square wave input | | 5.9 | 12.0 | μA | | | |
| | | | Resonator connection | | 6.0 | 12.1 | μA | | | |
| f _{SUB} = 32.768 kHz ^{Note 4} T _A = +85°C | Normal operation | | Square wave input | | 6.6 | 16.3 | μA | | | |
| | | | Resonator connection | | 6.7 | 16.4 | μA | | | |

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. When high-speed on-chip oscillator and subsystem clock are stopped.
 3. When high-speed system clock and subsystem clock are stopped.
 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 - HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V @ 1 MHz to 32 MHz
 - 2.4 V ≤ V_{DD} ≤ 5.5 V @ 1 MHz to 16 MHz
 - LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 5.5 V @ 1 MHz to 8 MHz
 - LV (low-voltage main) mode: 1.6 V ≤ V_{DD} ≤ 5.5 V @ 1 MHz to 4 MHz

- Remarks**
1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH}: High-speed on-chip oscillator clock frequency
 3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

(3) 128-pin products, and flash ROM: 384 to 512 KB of 44- to 100-pin products

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/2)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit | | |
|---|----------------------------|---|---|--|-------------------------|-------|------|------|----|
| Supply current Note 1 | I _{DD2} Note 2 | HALT mode | HS (high-speed main) mode Note 7 | f _{IH} = 32 MHz Note 4 | V _{DD} = 5.0 V | | 0.62 | 1.89 | mA |
| | | | | | V _{DD} = 3.0 V | | 0.62 | 1.89 | mA |
| | | | | f _{IH} = 24 MHz Note 4 | V _{DD} = 5.0 V | | 0.50 | 1.48 | mA |
| | | | | | V _{DD} = 3.0 V | | 0.50 | 1.48 | mA |
| | | | | f _{IH} = 16 MHz Note 4 | V _{DD} = 5.0 V | | 0.44 | 1.12 | mA |
| | | | | | V _{DD} = 3.0 V | | 0.44 | 1.12 | mA |
| | | | LS (low-speed main) mode Note 7 | f _{IH} = 8 MHz Note 4 | V _{DD} = 3.0 V | | 290 | 620 | μA |
| | | | | | V _{DD} = 2.0 V | | 290 | 620 | μA |
| | | | LV (low-voltage main) mode Note 7 | f _{IH} = 4 MHz Note 4 | V _{DD} = 3.0 V | | 460 | 700 | μA |
| | | | | | V _{DD} = 2.0 V | | 460 | 700 | μA |
| | | | HS (high-speed main) mode Note 7 | f _{MX} = 20 MHz Note 3, V _{DD} = 5.0 V | Square wave input | | 0.31 | 1.14 | mA |
| | | | | | Resonator connection | | 0.48 | 1.34 | mA |
| | | | | | Square wave input | | 0.31 | 1.14 | mA |
| | | | | | Resonator connection | | 0.48 | 1.34 | mA |
| | | | | f _{MX} = 10 MHz Note 3, V _{DD} = 5.0 V | Square wave input | | 0.21 | 0.68 | mA |
| | | | | | Resonator connection | | 0.28 | 0.76 | mA |
| | | | | f _{MX} = 10 MHz Note 3, V _{DD} = 3.0 V | Square wave input | | 0.21 | 0.68 | mA |
| | | | | | Resonator connection | | 0.28 | 0.76 | mA |
| | | | LS (low-speed main) mode Note 7 | f _{MX} = 8 MHz Note 3, V _{DD} = 3.0 V | Square wave input | | 110 | 390 | μA |
| | | | | | Resonator connection | | 160 | 450 | μA |
| | | f _{MX} = 8 MHz Note 3, V _{DD} = 2.0 V | | Square wave input | | 110 | 390 | μA | |
| | | | | Resonator connection | | 160 | 450 | μA | |
| | | Subsystem clock operation | f _{SUB} = 32.768 kHz Note 5 T _A = -40°C | Square wave input | | 0.31 | 0.66 | μA | |
| | | | | Resonator connection | | 0.50 | 0.85 | μA | |
| | | | f _{SUB} = 32.768 kHz Note 5 T _A = +25°C | Square wave input | | 0.38 | 0.66 | μA | |
| | | | | Resonator connection | | 0.57 | 0.85 | μA | |
| | | | f _{SUB} = 32.768 kHz Note 5 T _A = +50°C | Square wave input | | 0.47 | 3.49 | μA | |
| | | | | Resonator connection | | 0.66 | 3.68 | μA | |
| | | | f _{SUB} = 32.768 kHz Note 5 T _A = +70°C | Square wave input | | 0.80 | 6.10 | μA | |
| | | | | Resonator connection | | 0.99 | 6.29 | μA | |
| f _{SUB} = 32.768 kHz Note 5 T _A = +85°C | Square wave input | | 1.52 | 10.46 | μA | | | | |
| | Resonator connection | | 1.71 | 10.65 | μA | | | | |
| I _{DD3} Note 6 | STOP mode Note 8 | T _A = -40°C | | | 0.19 | 0.54 | μA | | |
| | | T _A = +25°C | | | 0.26 | 0.54 | μA | | |
| | | T _A = +50°C | | | 0.35 | 3.37 | μA | | |
| | | T _A = +70°C | | | 0.68 | 5.98 | μA | | |
| | | T _A = +85°C | | | 1.40 | 10.34 | μA | | |

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD} , EV_{DD0} , and EV_{DD1} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD0} , and EV_{DD1} , or V_{SS} , EV_{SS0} , and EV_{SS1} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. During HALT instruction execution by flash memory.
 3. When high-speed on-chip oscillator and subsystem clock are stopped.
 4. When high-speed system clock and subsystem clock are stopped.
 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When $RTCLPC = 1$ and setting ultra-low current consumption ($AMPHS1 = 1$). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 - HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
 - LS (low-speed main) mode: $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }8\text{ MHz}$
 - LV (low-voltage main) mode: $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }4\text{ MHz}$
 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks**
1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH} : High-speed on-chip oscillator clock frequency
 3. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

(4) Peripheral Functions (Common to all products)**($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|--|---|----------------------------------|--|------|------|-------|---------------|
| Low-speed on-chip oscillator operating current | I_{FIL} ^{Note 1} | | | | 0.20 | | μA |
| RTC operating current | I_{RTC} ^{Notes 1, 2, 3} | | | | 0.02 | | μA |
| 12-bit interval timer operating current | I_{IT} ^{Notes 1, 2, 4} | | | | 0.02 | | μA |
| Watchdog timer operating current | I_{WDT} ^{Notes 1, 2, 5} | $f_{\text{IL}} = 15\text{ kHz}$ | | | 0.22 | | μA |
| A/D converter operating current | I_{ADC} ^{Notes 1, 6} | When conversion at maximum speed | Normal mode, $\text{AV}_{\text{REFP}} = \text{V}_{\text{DD}} = 5.0\text{ V}$ | | 1.3 | 1.7 | mA |
| | | | Low voltage mode, $\text{AV}_{\text{REFP}} = \text{V}_{\text{DD}} = 3.0\text{ V}$ | | 0.5 | 0.7 | mA |
| A/D converter reference voltage current | I_{ADREF} ^{Note 1} | | | | 75.0 | | μA |
| Temperature sensor operating current | I_{TMPS} ^{Note 1} | | | | 75.0 | | μA |
| LVD operating current | I_{LVI} ^{Notes 1, 7} | | | | 0.08 | | μA |
| Self-programming operating current | I_{FSP} ^{Notes 1, 9} | | | | 2.50 | 12.20 | mA |
| BGO operating current | I_{BGO} ^{Notes 1, 8} | | | | 2.50 | 12.20 | mA |
| SNOOZE operating current | I_{SNOZ} ^{Note 1} | ADC operation | The mode is performed ^{Note 10} | | 0.50 | 0.60 | mA |
| | | | The A/D conversion operations are performed, Low voltage mode, $\text{AV}_{\text{REFP}} = \text{V}_{\text{DD}} = 3.0\text{ V}$ | | 1.20 | 1.44 | mA |
| | | CSI/UART operation | | | 0.70 | 0.84 | mA |

Notes 1. Current flowing to V_{DD} .

- When high speed on-chip oscillator and high-speed system clock are stopped.
- Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either $I_{\text{DD}1}$ or $I_{\text{DD}2}$, and I_{RTC} , when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. $I_{\text{DD}2}$ subsystem clock operation includes the operational current of the real-time clock.
- Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either $I_{\text{DD}1}$ or $I_{\text{DD}2}$, and I_{IT} , when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.
- Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of $I_{\text{DD}1}$, $I_{\text{DD}2}$ or $I_{\text{DD}3}$ and I_{WDT} when the watchdog timer is in operation.
- Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of $I_{\text{DD}1}$ or $I_{\text{DD}2}$ and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

- Notes**
7. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of I_{DD1} , I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit is in operation.
 8. Current flowing only during data flash rewrite.
 9. Current flowing only during self programming.
 10. For shift time to the SNOOZE mode, see **18.3.3 SNOOZE mode** in the RL78/G13 User's Manual.

- Remarks**
1. f_{IL} : Low-speed on-chip oscillator clock frequency
 2. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 3. f_{CLK} : CPU/peripheral hardware clock frequency
 4. Temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

2.4 AC Characteristics

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit | |
|--|---------------------------------------|--|-----------------------------------|---------------------------------|---------|------|--------------------|----|
| Instruction cycle (minimum instruction execution time) | T _{CY} | Main system clock (f _{MAIN}) operation | HS (high-speed main) mode | 2.7 V ≤ V _{DD} ≤ 5.5 V | 0.03125 | 1 | μs | |
| | | | | 2.4 V ≤ V _{DD} < 2.7 V | 0.0625 | 1 | μs | |
| | | | LS (low-speed main) mode | 1.8 V ≤ V _{DD} ≤ 5.5 V | 0.125 | 1 | μs | |
| | | | | 1.6 V ≤ V _{DD} < 1.8 V | 0.25 | 1 | μs | |
| | | Subsystem clock (f _{SUB}) operation | | 1.8 V ≤ V _{DD} ≤ 5.5 V | 28.5 | 30.5 | 31.3 | μs |
| | | In the self programming mode | HS (high-speed main) mode | 2.7 V ≤ V _{DD} ≤ 5.5 V | 0.03125 | 1 | μs | |
| | | | | 2.4 V ≤ V _{DD} < 2.7 V | 0.0625 | 1 | μs | |
| | | | LS (low-speed main) mode | 1.8 V ≤ V _{DD} ≤ 5.5 V | 0.125 | 1 | μs | |
| 1.6 V ≤ V _{DD} < 1.8 V | 0.25 | | | 1 | μs | | | |
| External system clock frequency | f _{EX} | 2.7 V ≤ V _{DD} ≤ 5.5 V | | 1.0 | | 20.0 | MHz | |
| | | 2.4 V ≤ V _{DD} < 2.7 V | | 1.0 | | 16.0 | MHz | |
| | | 1.8 V ≤ V _{DD} < 2.4 V | | 1.0 | | 8.0 | MHz | |
| | | 1.6 V ≤ V _{DD} < 1.8 V | | 1.0 | | 4.0 | MHz | |
| | f _{EXS} | | | 32 | | 35 | kHz | |
| External system clock input high-level width, low-level width | t _{EXH} , t _{EXL} | 2.7 V ≤ V _{DD} ≤ 5.5 V | | 24 | | | ns | |
| | | 2.4 V ≤ V _{DD} < 2.7 V | | 30 | | | ns | |
| | | 1.8 V ≤ V _{DD} < 2.4 V | | 60 | | | ns | |
| | | 1.6 V ≤ V _{DD} < 1.8 V | | 120 | | | ns | |
| | t _{EXHS} , t _{EXLS} | | | 13.7 | | | μs | |
| TI00 to TI07, TI10 to TI17 input high-level width, low-level width | t _{TIH} , t _{TIL} | | | 1/f _{MCK} +10 | | | ns ^{Note} | |
| TO00 to TO07, TO10 to TO17 output frequency | f _{TO} | HS (high-speed main) mode | 4.0 V ≤ EV _{DD0} ≤ 5.5 V | | | 16 | MHz | |
| | | | 2.7 V ≤ EV _{DD0} < 4.0 V | | | 8 | MHz | |
| | | | 1.8 V ≤ EV _{DD0} < 2.7 V | | | 4 | MHz | |
| | | | 1.6 V ≤ EV _{DD0} < 1.8 V | | | 2 | MHz | |
| | | LS (low-speed main) mode | 1.8 V ≤ EV _{DD0} ≤ 5.5 V | | | 4 | MHz | |
| | | | 1.6 V ≤ EV _{DD0} < 1.8 V | | | 2 | MHz | |
| | | LV (low-voltage main) mode | 1.6 V ≤ EV _{DD0} ≤ 5.5 V | | | 2 | MHz | |
| PCLBUZ0, PCLBUZ1 output frequency | f _{PCL} | HS (high-speed main) mode | 4.0 V ≤ EV _{DD0} ≤ 5.5 V | | | 16 | MHz | |
| | | | 2.7 V ≤ EV _{DD0} < 4.0 V | | | 8 | MHz | |
| | | | 1.8 V ≤ EV _{DD0} < 2.7 V | | | 4 | MHz | |
| | | | 1.6 V ≤ EV _{DD0} < 1.8 V | | | 2 | MHz | |
| | | LS (low-speed main) mode | 1.8 V ≤ EV _{DD0} ≤ 5.5 V | | | 4 | MHz | |
| | | | 1.6 V ≤ EV _{DD0} < 1.8 V | | | 2 | MHz | |
| | | LV (low-voltage main) mode | 1.8 V ≤ EV _{DD0} ≤ 5.5 V | | | 4 | MHz | |
| 1.6 V ≤ EV _{DD0} < 1.8 V | | | 2 | MHz | | | | |
| Interrupt input high-level width, low-level width | t _{INTH} , t _{INTL} | INTP0 | 1.6 V ≤ V _{DD} ≤ 5.5 V | 1 | | | μs | |
| | | INTP1 to INTP11 | 1.6 V ≤ EV _{DD0} ≤ 5.5 V | 1 | | | μs | |
| Key interrupt input low-level width | t _{KR} | KR0 to KR7 | 1.8 V ≤ EV _{DD0} ≤ 5.5 V | 250 | | | ns | |
| | | | 1.6 V ≤ EV _{DD0} < 1.8 V | 1 | | | μs | |
| RESET low-level width | t _{RSL} | | | 10 | | | μs | |

(Note and Remark are listed on the next page.)

Note The following conditions are required for low voltage interface when E_{VDD0} < V_{DD}

1.8 V ≤ E_{VDD0} < 2.7 V : MIN. 125 ns

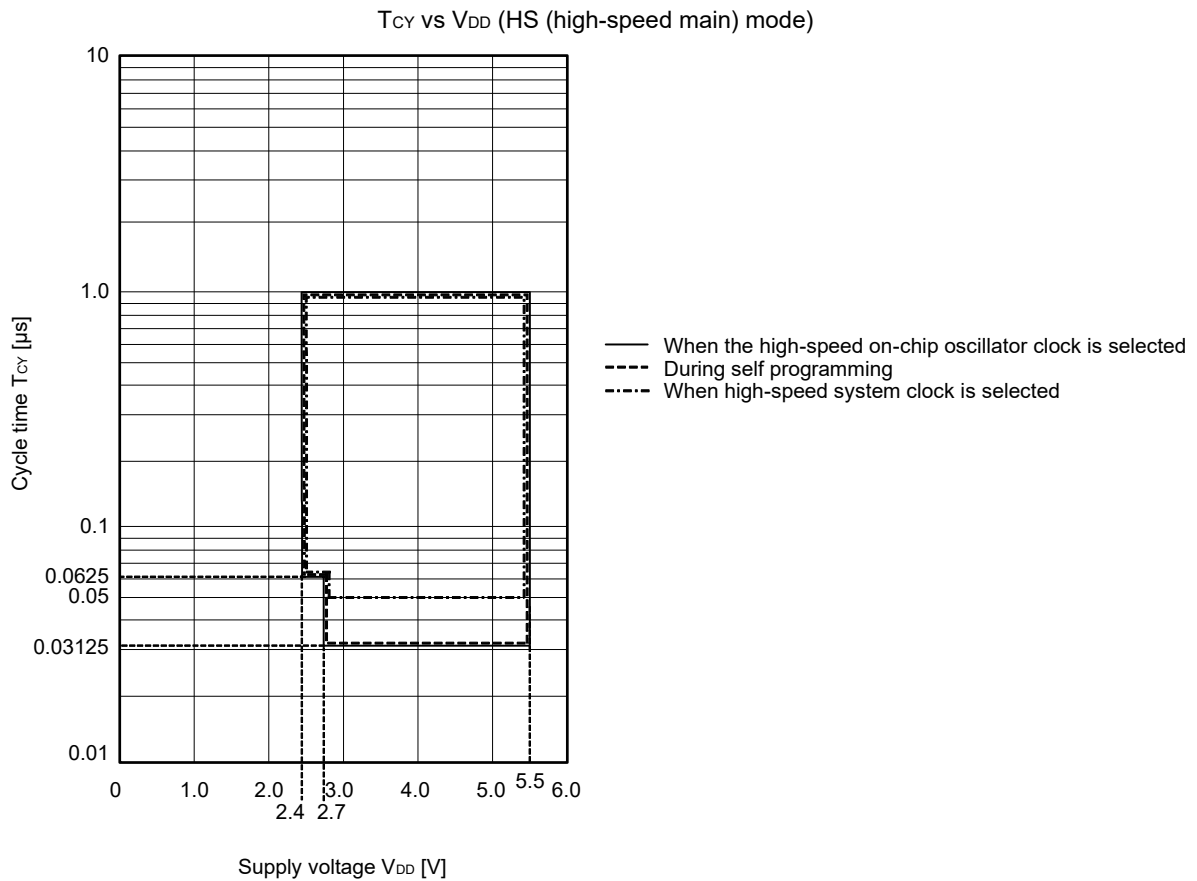
1.6 V ≤ E_{VDD0} < 1.8 V : MIN. 250 ns

Remark f_{MCK}: Timer array unit operation clock frequency

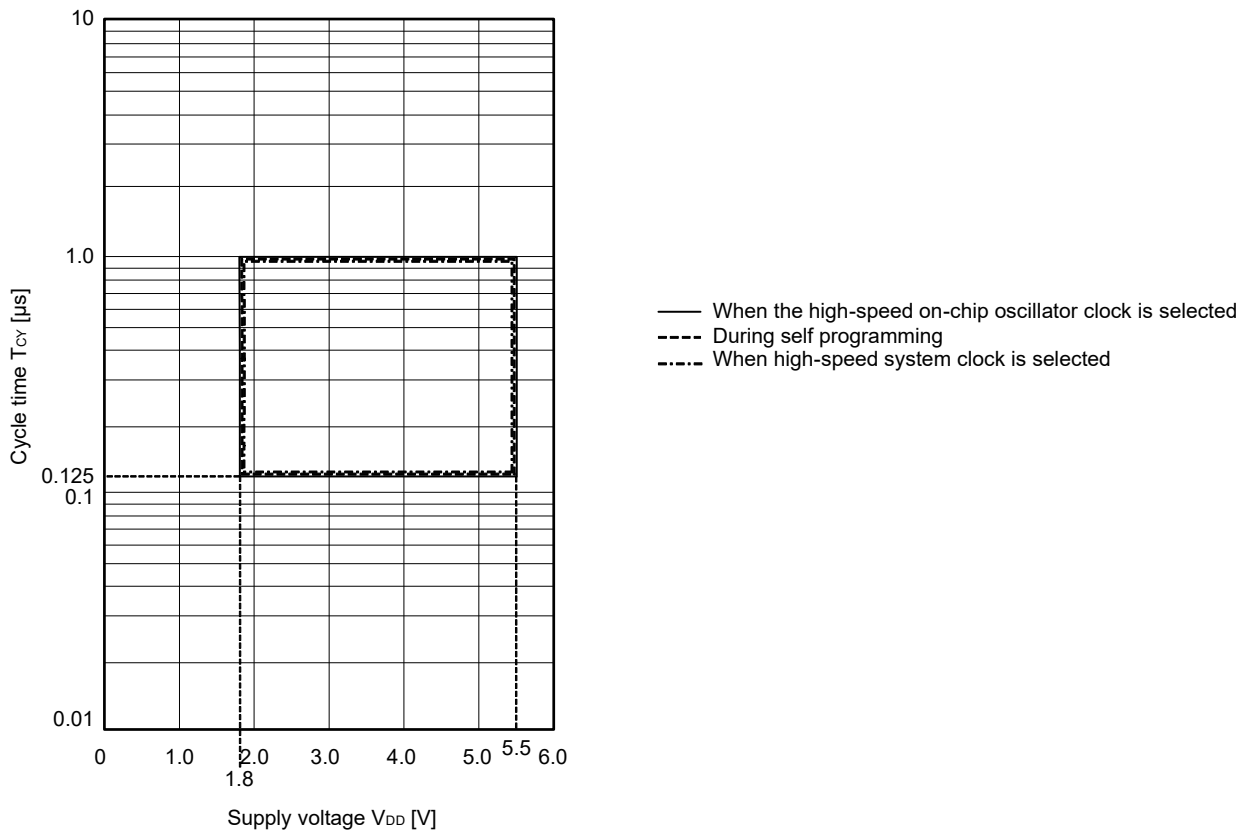
(Operation clock to be set by the CKS_{mn0}, CKS_{mn1} bits of timer mode register mn (TMR_{mn}).

m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7))

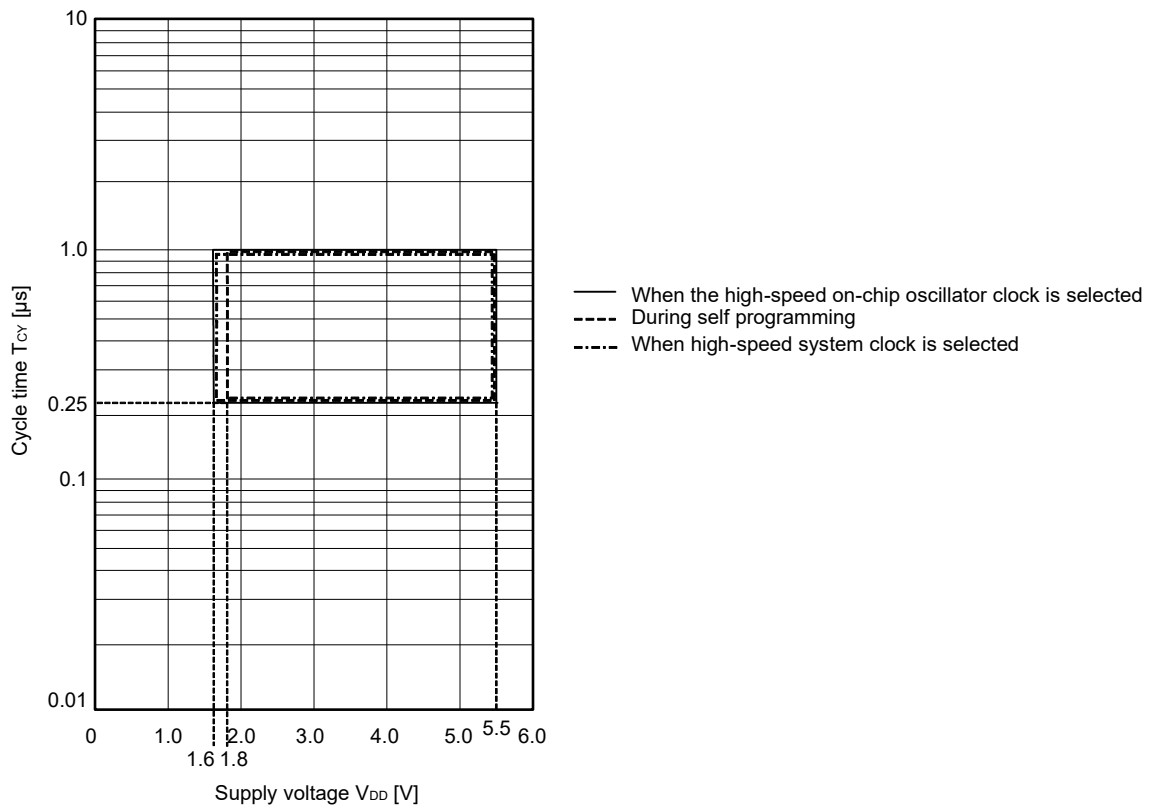
Minimum Instruction Execution Time during Main System Clock Operation



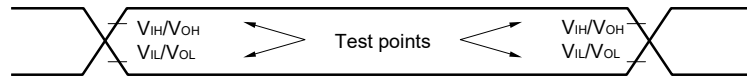
T_{CY} vs V_{DD} (LS (low-speed main) mode)



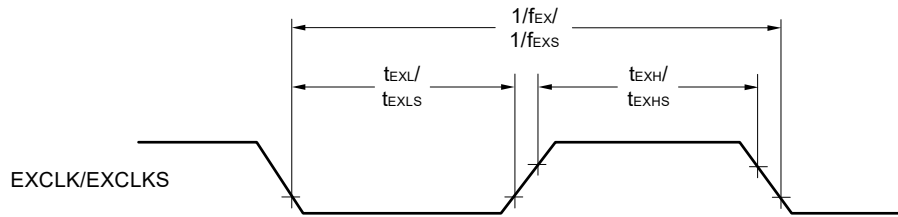
T_{CY} vs V_{DD} (LV (low-voltage main) mode)



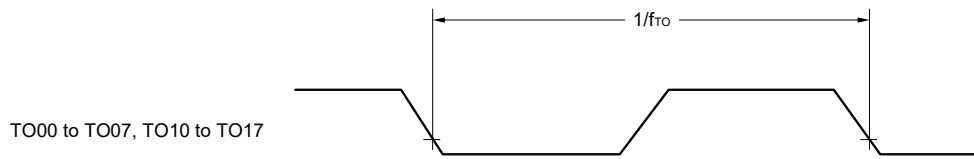
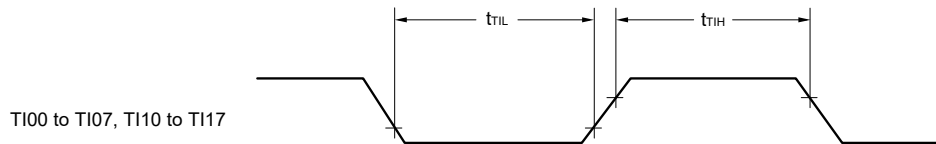
AC Timing Test Points



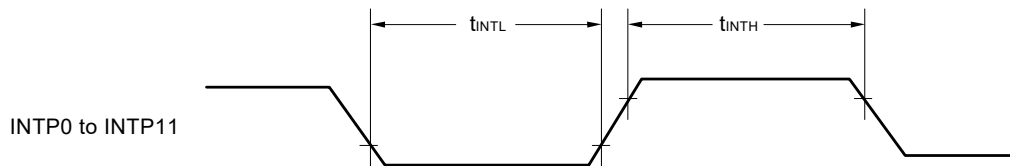
External System Clock Timing



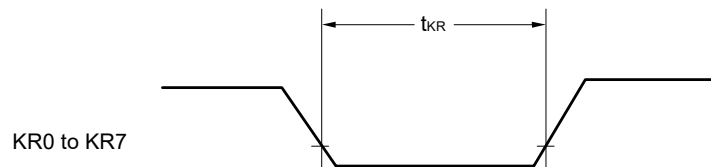
TI/TO Timing



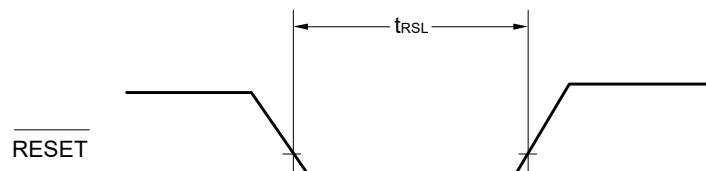
Interrupt Request Input Timing



Key Interrupt Input Timing

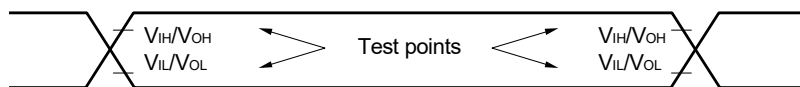


RESET Input Timing



2.5 Peripheral Functions Characteristics

AC Timing Test Points



2.5.1 Serial array unit

(1) During communication at same potential (UART mode)

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|-----------------------------------|---|---|---------------------------|--|--------------------------|--|----------------------------|---------------------|------|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Transfer rate ^{Note 1} | | 2.4 V ≤ EV _{DD0} ≤ 5.5 V | | f _{MCK} /6 ^{Note 2} | | f _{MCK} /6 | | f _{MCK} /6 | bps |
| | | Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} ^{Note 3} | | 5.3 | | 1.3 | | 0.6 | Mbps |
| | | 1.8 V ≤ EV _{DD0} ≤ 5.5 V | | f _{MCK} /6 ^{Note 2} | | f _{MCK} /6 | | f _{MCK} /6 | bps |
| | | Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} ^{Note 3} | | 5.3 | | 1.3 | | 0.6 | Mbps |
| | | 1.7 V ≤ EV _{DD0} ≤ 5.5 V | | f _{MCK} /6 ^{Note 2} | | f _{MCK} /6 ^{Note 2} | | f _{MCK} /6 | bps |
| | | Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} ^{Note 3} | | 5.3 | | 1.3 | | 0.6 | Mbps |
| 1.6 V ≤ EV _{DD0} ≤ 5.5 V | | – | | f _{MCK} /6 ^{Note 2} | | f _{MCK} /6 | bps | | |
| | Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} ^{Note 3} | | – | | 1.3 | | 0.6 | Mbps | |

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

2. The following conditions are required for low voltage interface when EV_{DD0} < V_{DD}.

2.4 V ≤ EV_{DD0} < 2.7 V : MAX. 2.6 Mbps

1.8 V ≤ EV_{DD0} < 2.4 V : MAX. 1.3 Mbps

1.6 V ≤ EV_{DD0} < 1.8 V : MAX. 0.6 Mbps

3. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:

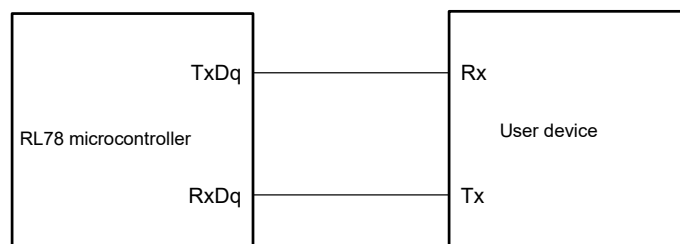
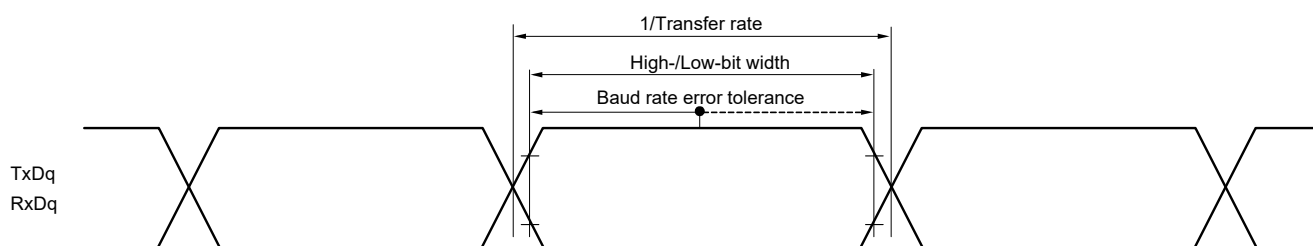
HS (high-speed main) mode: 32 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)

16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)

LS (low-speed main) mode: 8 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)

LV (low-voltage main) mode: 4 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)**UART mode bit width (during communication at same potential) (reference)**

- Remarks 1.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)
- 2.** f_{MCK} : Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
 n: Channel number (mn = 00 to 03, 10 to 13))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

($T_A = -40$ to $+85^\circ\text{C}$, $2.7\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$)

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|--|--|--|------|--------------------------|------|----------------------------|------|------|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | $t_{\text{KCY}1}$ | $t_{\text{KCY}1} \geq 2/f_{\text{CLK}}$ | $4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | 62.5 | | 250 | | 500 | ns |
| | | | $2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | 83.3 | | 250 | | 500 | ns |
| SCKp high-/low-level width | $t_{\text{KH}1}$, $t_{\text{KL}1}$ | $4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | $t_{\text{KCY}1}/2 - 7$ | | $t_{\text{KCY}1}/2 - 50$ | | $t_{\text{KCY}1}/2 - 50$ | | ns |
| | | $2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | $t_{\text{KCY}1}/2 - 10$ | | $t_{\text{KCY}1}/2 - 50$ | | $t_{\text{KCY}1}/2 - 50$ | | ns |
| Slp setup time (to SCKp \uparrow) Note 1 | $t_{\text{SIK}1}$ | $4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | 23 | | 110 | | 110 | | ns |
| | | $2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | 33 | | 110 | | 110 | | ns |
| Slp hold time (from SCKp \downarrow) Note 2 | $t_{\text{KS}1}$ | $2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | 10 | | 10 | | 10 | | ns |
| Delay time from SCKp \downarrow to SOp output Note 3 | $t_{\text{KS}01}$ | $C = 20\text{ pF}$ Note 4 | | 10 | | 10 | | 10 | ns |

- Notes**
1. When $\text{DAP}_{\text{mn}} = 0$ and $\text{CKP}_{\text{mn}} = 0$, or $\text{DAP}_{\text{mn}} = 1$ and $\text{CKP}_{\text{mn}} = 1$. The Slp setup time becomes “to SCKp \downarrow ” when $\text{DAP}_{\text{mn}} = 0$ and $\text{CKP}_{\text{mn}} = 1$, or $\text{DAP}_{\text{mn}} = 1$ and $\text{CKP}_{\text{mn}} = 0$.
 2. When $\text{DAP}_{\text{mn}} = 0$ and $\text{CKP}_{\text{mn}} = 0$, or $\text{DAP}_{\text{mn}} = 1$ and $\text{CKP}_{\text{mn}} = 1$. The Slp hold time becomes “from SCKp \downarrow ” when $\text{DAP}_{\text{mn}} = 0$ and $\text{CKP}_{\text{mn}} = 1$, or $\text{DAP}_{\text{mn}} = 1$ and $\text{CKP}_{\text{mn}} = 0$.
 3. When $\text{DAP}_{\text{mn}} = 0$ and $\text{CKP}_{\text{mn}} = 0$, or $\text{DAP}_{\text{mn}} = 1$ and $\text{CKP}_{\text{mn}} = 1$. The delay time to SOp output becomes “from SCKp \uparrow ” when $\text{DAP}_{\text{mn}} = 0$ and $\text{CKP}_{\text{mn}} = 1$, or $\text{DAP}_{\text{mn}} = 1$ and $\text{CKP}_{\text{mn}} = 0$.
 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. This value is valid only when CSI00's peripheral I/O redirect function is not used.
 2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0),
g: PIM and POM numbers (g = 1)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

(3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)**($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|--|--|--|------|---------------------------|------|----------------------------|------|------|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | $t_{\text{KCY}1}$ | $t_{\text{KCY}1} \geq 4/f_{\text{CLK}}$ | $2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | 125 | | 500 | | 1000 | ns |
| | | | $2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | 250 | | 500 | | 1000 | ns |
| | | | $1.8\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | 500 | | 500 | | 1000 | ns |
| | | | $1.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | 1000 | | 1000 | | 1000 | ns |
| | | | $1.6\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | – | | 1000 | | 1000 | ns |
| SCKp high-/low-level width | $t_{\text{KH}1}$, $t_{\text{KL}1}$ | $4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | $t_{\text{KCY}1}/2 - 12$ | | $t_{\text{KCY}1}/2 - 50$ | | $t_{\text{KCY}1}/2 - 50$ | ns | |
| | | $2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | $t_{\text{KCY}1}/2 - 18$ | | $t_{\text{KCY}1}/2 - 50$ | | $t_{\text{KCY}1}/2 - 50$ | ns | |
| | | $2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | $t_{\text{KCY}1}/2 - 38$ | | $t_{\text{KCY}1}/2 - 50$ | | $t_{\text{KCY}1}/2 - 50$ | ns | |
| | | $1.8\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | $t_{\text{KCY}1}/2 - 50$ | | $t_{\text{KCY}1}/2 - 50$ | | $t_{\text{KCY}1}/2 - 50$ | ns | |
| | | $1.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | $t_{\text{KCY}1}/2 - 100$ | | $t_{\text{KCY}1}/2 - 100$ | | $t_{\text{KCY}1}/2 - 100$ | ns | |
| | | $1.6\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | – | | $t_{\text{KCY}1}/2 - 100$ | | $t_{\text{KCY}1}/2 - 100$ | ns | |
| Slp setup time (to SCKp \uparrow) Note 1 | $t_{\text{SIK}1}$ | $4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | 44 | | 110 | | 110 | ns | |
| | | $2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | 44 | | 110 | | 110 | ns | |
| | | $2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | 75 | | 110 | | 110 | ns | |
| | | $1.8\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | 110 | | 110 | | 110 | ns | |
| | | $1.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | 220 | | 220 | | 220 | ns | |
| | | $1.6\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | – | | 220 | | 220 | ns | |
| Slp hold time (from SCKp \uparrow) Note 2 | $t_{\text{SH}1}$ | $1.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | 19 | | 19 | | 19 | ns | |
| | | $1.6\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | – | | 19 | | 19 | ns | |
| Delay time from SCKp \downarrow to SOp output Note 3 | $t_{\text{KSO}1}$ | $1.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ $C = 30\text{ pF}$ ^{Note 4} | | 25 | | 25 | | 25 | ns |
| | | $1.6\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ $C = 30\text{ pF}$ ^{Note 4} | | – | | 25 | | 25 | ns |

- Notes**
1. When $\text{DAP}_{\text{mn}} = 0$ and $\text{CKP}_{\text{mn}} = 0$, or $\text{DAP}_{\text{mn}} = 1$ and $\text{CKP}_{\text{mn}} = 1$. The Slp setup time becomes “to SCKp \downarrow ” when $\text{DAP}_{\text{mn}} = 0$ and $\text{CKP}_{\text{mn}} = 1$, or $\text{DAP}_{\text{mn}} = 1$ and $\text{CKP}_{\text{mn}} = 0$.
 2. When $\text{DAP}_{\text{mn}} = 0$ and $\text{CKP}_{\text{mn}} = 0$, or $\text{DAP}_{\text{mn}} = 1$ and $\text{CKP}_{\text{mn}} = 1$. The Slp hold time becomes “from SCKp \downarrow ” when $\text{DAP}_{\text{mn}} = 0$ and $\text{CKP}_{\text{mn}} = 1$, or $\text{DAP}_{\text{mn}} = 1$ and $\text{CKP}_{\text{mn}} = 0$.
 3. When $\text{DAP}_{\text{mn}} = 0$ and $\text{CKP}_{\text{mn}} = 0$, or $\text{DAP}_{\text{mn}} = 1$ and $\text{CKP}_{\text{mn}} = 1$. The delay time to SOp output becomes “from SCKp \uparrow ” when $\text{DAP}_{\text{mn}} = 0$ and $\text{CKP}_{\text{mn}} = 1$, or $\text{DAP}_{\text{mn}} = 1$ and $\text{CKP}_{\text{mn}} = 0$.
 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 1, 4, 5, 8, 14)
- 2.** f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (1/2)

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|----------------------------|--------------------------|--|------------------------------|-------------------------|--------------------------|-------------------------|----------------------------|-------------------------|------|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time Note 5 | t_{KCY2} | $4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ | $20\text{ MHz} < f_{MCK}$ | $8/f_{MCK}$ | | – | | – | ns |
| | | | $f_{MCK} \leq 20\text{ MHz}$ | $6/f_{MCK}$ | | $6/f_{MCK}$ | | $6/f_{MCK}$ | ns |
| | | $2.7\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ | $16\text{ MHz} < f_{MCK}$ | $8/f_{MCK}$ | | – | | – | ns |
| | | | $f_{MCK} \leq 16\text{ MHz}$ | $6/f_{MCK}$ | | $6/f_{MCK}$ | | $6/f_{MCK}$ | ns |
| | | $2.4\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ | | $6/f_{MCK}$ and 500 | | $6/f_{MCK}$ and 500 | | $6/f_{MCK}$ and 500 | ns |
| | | $1.8\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ | | $6/f_{MCK}$ and 750 | | $6/f_{MCK}$ and 750 | | $6/f_{MCK}$ and 750 | ns |
| | | $1.7\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ | | $6/f_{MCK}$ and 1500 | | $6/f_{MCK}$ and 1500 | | $6/f_{MCK}$ and 1500 | ns |
| | | $1.6\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ | | – | | $6/f_{MCK}$ and 1500 | | $6/f_{MCK}$ and 1500 | ns |
| SCKp high-/low-level width | t_{KH2} , t_{KL2} | $4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ | | $t_{KCY2}/2 - 7$ | | $t_{KCY2}/2 - 7$ | | $t_{KCY2}/2 - 7$ | ns |
| | | $2.7\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ | | $t_{KCY2}/2 - 8$ | | $t_{KCY2}/2 - 8$ | | $t_{KCY2}/2 - 8$ | ns |
| | | $1.8\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ | | $t_{KCY2}/2 - 18$ | | $t_{KCY2}/2 - 18$ | | $t_{KCY2}/2 - 18$ | ns |
| | | $1.7\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ | | $t_{KCY2}/2 - 66$ | | $t_{KCY2}/2 - 66$ | | $t_{KCY2}/2 - 66$ | ns |
| | | $1.6\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ | | – | | $t_{KCY2}/2 - 66$ | | $t_{KCY2}/2 - 66$ | ns |

(Notes, Caution, and Remarks are listed on the next page.)

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (2/2)**(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)**

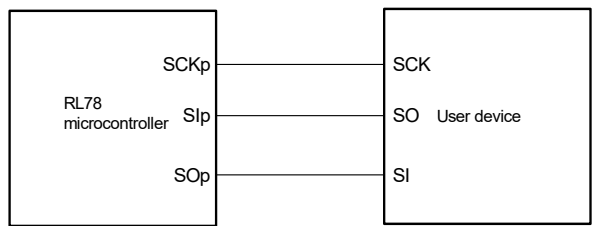
| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|-------------------|-----------------------------------|-----------------------------------|-------------------------|--------------------------|-------------------------|----------------------------|-------------------------|-------------------------|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Slp setup time (to SCKp↑) ^{Note 1} | t _{SIK2} | 2.7 V ≤ EV _{DD0} ≤ 5.5 V | | 1/f _{MCK} +20 | | 1/f _{MCK} +30 | | 1/f _{MCK} +30 | ns |
| | | 1.8 V ≤ EV _{DD0} ≤ 5.5 V | | 1/f _{MCK} +30 | | 1/f _{MCK} +30 | | 1/f _{MCK} +30 | ns |
| | | 1.7 V ≤ EV _{DD0} ≤ 5.5 V | | 1/f _{MCK} +40 | | 1/f _{MCK} +40 | | 1/f _{MCK} +40 | ns |
| | | 1.6 V ≤ EV _{DD0} ≤ 5.5 V | | – | | 1/f _{MCK} +40 | | 1/f _{MCK} +40 | ns |
| Slp hold time (from SCKp↑) ^{Note 2} | t _{KS12} | 1.8 V ≤ EV _{DD0} ≤ 5.5 V | | 1/f _{MCK} +31 | | 1/f _{MCK} +31 | | 1/f _{MCK} +31 | ns |
| | | 1.7 V ≤ EV _{DD0} ≤ 5.5 V | | 1/f _{MCK} +250 | | 1/f _{MCK} +250 | | 1/f _{MCK} +250 | ns |
| | | 1.6 V ≤ EV _{DD0} ≤ 5.5 V | | – | | 1/f _{MCK} +250 | | 1/f _{MCK} +250 | ns |
| Delay time from SCKp↓ to SOp output ^{Note 3} | t _{KSO2} | C = 30 pF ^{Note 4} | 2.7 V ≤ EV _{DD0} ≤ 5.5 V | | | 2/f _{MCK} +44 | | 2/f _{MCK} +110 | ns |
| | | | 2.4 V ≤ EV _{DD0} ≤ 5.5 V | | | 2/f _{MCK} +75 | | 2/f _{MCK} +110 | ns |
| | | | 1.8 V ≤ EV _{DD0} ≤ 5.5 V | | | 2/f _{MCK} +110 | | 2/f _{MCK} +110 | ns |
| | | | 1.7 V ≤ EV _{DD0} ≤ 5.5 V | | | 2/f _{MCK} +220 | | 2/f _{MCK} +220 | ns |
| | | | 1.6 V ≤ EV _{DD0} ≤ 5.5 V | | | – | | 2/f _{MCK} +220 | 2/f _{MCK} +220 |

- Notes**
1. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The Slp setup time becomes “to SCKp↓” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.
 2. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The Slp hold time becomes “from SCKp↓” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.
 3. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The delay time to SOp output becomes “from SCKp↑” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.
 4. C is the load capacitance of the SOp output lines.
 5. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

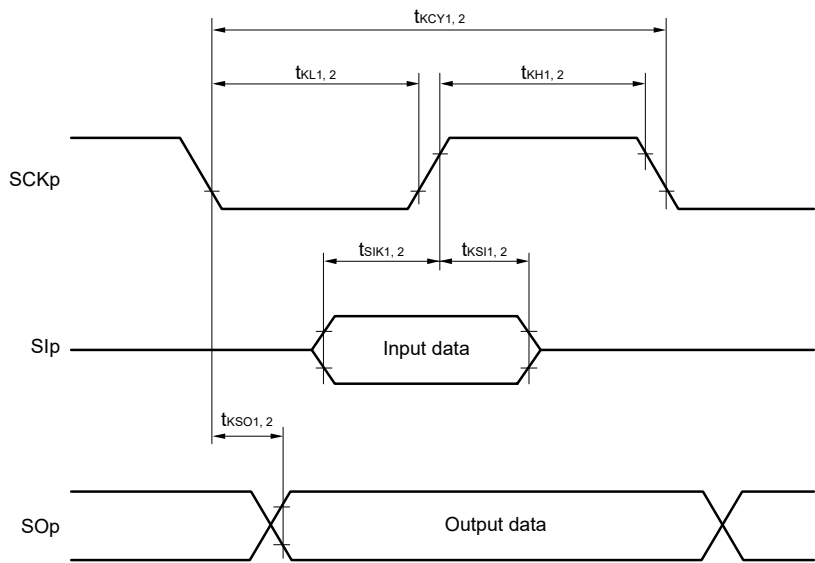
Caution Select the normal input buffer for the Slp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 4, 5, 8, 14)
 2. f_{MCK}: Serial array unit operation clock frequency (Operation clock to be set by the CKS_{mn} bit of serial mode register mn (SMR_{mn}). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

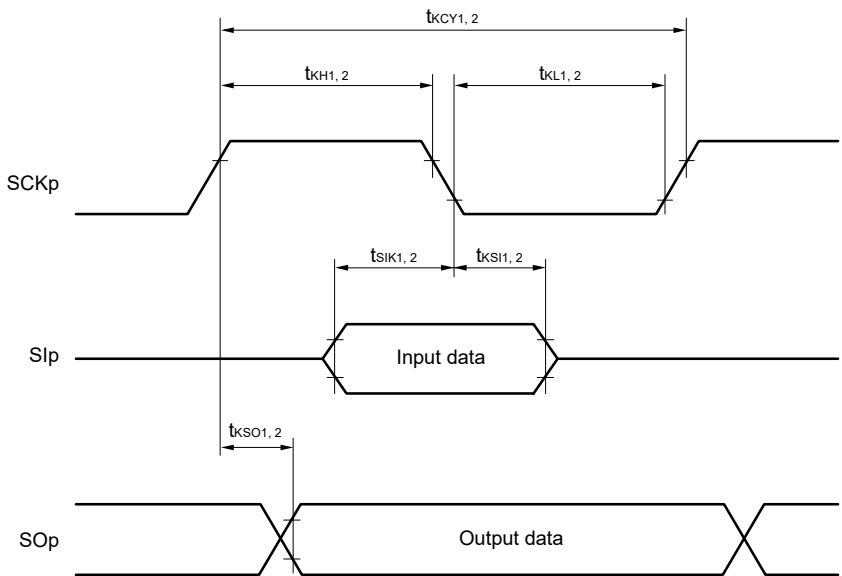
CSI mode connection diagram (during communication at same potential)



**CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



- 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)
- 2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

(5) During communication at same potential (simplified I²C mode) (1/2) $(T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---------------------------|-------------------|---|---------------------------|----------------|--------------------------|---------------|----------------------------|---------------|------|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLr clock frequency | f _{SCL} | 2.7 V \leq EV _{DD0} \leq 5.5 V, C _b = 50 pF, R _b = 2.7 k Ω | | 1000 Note 1 | | 400 Note 1 | | 400 Note 1 | kHz |
| | | 1.8 V \leq EV _{DD0} \leq 5.5 V, C _b = 100 pF, R _b = 3 k Ω | | 400 Note 1 | | 400 Note 1 | | 400 Note 1 | kHz |
| | | 1.8 V \leq EV _{DD0} < 2.7 V, C _b = 100 pF, R _b = 5 k Ω | | 300 Note 1 | | 300 Note 1 | | 300 Note 1 | kHz |
| | | 1.7 V \leq EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 k Ω | | 250 Note 1 | | 250 Note 1 | | 250 Note 1 | kHz |
| | | 1.6 V \leq EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 k Ω | | – | | 250 Note 1 | | 250 Note 1 | kHz |
| Hold time when SCLr = "L" | t _{LOW} | 2.7 V \leq EV _{DD0} \leq 5.5 V, C _b = 50 pF, R _b = 2.7 k Ω | 475 | | 1150 | | 1150 | | ns |
| | | 1.8 V \leq EV _{DD0} \leq 5.5 V, C _b = 100 pF, R _b = 3 k Ω | 1150 | | 1150 | | 1150 | | ns |
| | | 1.8 V \leq EV _{DD0} < 2.7 V, C _b = 100 pF, R _b = 5 k Ω | 1550 | | 1550 | | 1550 | | ns |
| | | 1.7 V \leq EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 k Ω | 1850 | | 1850 | | 1850 | | ns |
| | | 1.6 V \leq EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 k Ω | – | | 1850 | | 1850 | | ns |
| Hold time when SCLr = "H" | t _{HIGH} | 2.7 V \leq EV _{DD0} \leq 5.5 V, C _b = 50 pF, R _b = 2.7 k Ω | 475 | | 1150 | | 1150 | | ns |
| | | 1.8 V \leq EV _{DD0} \leq 5.5 V, C _b = 100 pF, R _b = 3 k Ω | 1150 | | 1150 | | 1150 | | ns |
| | | 1.8 V \leq EV _{DD0} < 2.7 V, C _b = 100 pF, R _b = 5 k Ω | 1550 | | 1550 | | 1550 | | ns |
| | | 1.7 V \leq EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 k Ω | 1850 | | 1850 | | 1850 | | ns |
| | | 1.6 V \leq EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 k Ω | – | | 1850 | | 1850 | | ns |

(Notes and Caution are listed on the next page, and Remarks are listed on the page after the next page.)

(5) During communication at same potential (simplified I²C mode) (2/2)(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

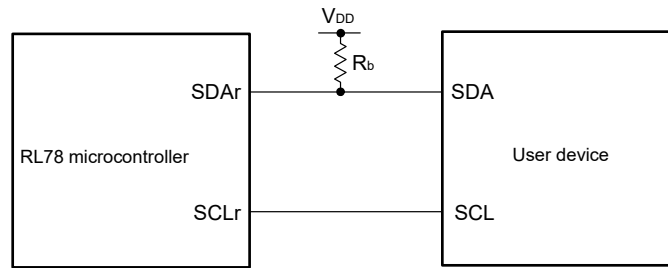
| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|-------------------------------|---------------------|---|-----------------------------------|------|-----------------------------------|------|-----------------------------------|------|------|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Data setup time (reception) | t _{SU:DAT} | 2.7 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ | 1/f _{MCK} + 85 Note2 | | 1/f _{MCK} + 145 Note2 | | 1/f _{MCK} + 145 Note2 | | ns |
| | | 1.8 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ | 1/f _{MCK} + 145 Note2 | | 1/f _{MCK} + 145 Note2 | | 1/f _{MCK} + 145 Note2 | | ns |
| | | 1.8 V ≤ EV _{DD0} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ | 1/f _{MCK} + 230 Note2 | | 1/f _{MCK} + 230 Note2 | | 1/f _{MCK} + 230 Note2 | | ns |
| | | 1.7 V ≤ EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ | 1/f _{MCK} + 290 Note2 | | 1/f _{MCK} + 290 Note2 | | 1/f _{MCK} + 290 Note2 | | ns |
| | | 1.6 V ≤ EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ | – | | 1/f _{MCK} + 290 Note2 | | 1/f _{MCK} + 290 Note2 | | ns |
| Data hold time (transmission) | t _{HD:DAT} | 2.7 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ | 0 | 305 | 0 | 305 | 0 | 305 | ns |
| | | 1.8 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ | 0 | 355 | 0 | 355 | 0 | 355 | ns |
| | | 1.8 V ≤ EV _{DD0} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ | 0 | 405 | 0 | 405 | 0 | 405 | ns |
| | | 1.7 V ≤ EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ | 0 | 405 | 0 | 405 | 0 | 405 | ns |
| | | 1.6 V ≤ EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ | – | | 0 | 405 | 0 | 405 | ns |

- Notes**
1. The value must also be equal to or less than f_{MCK}/4.
 2. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

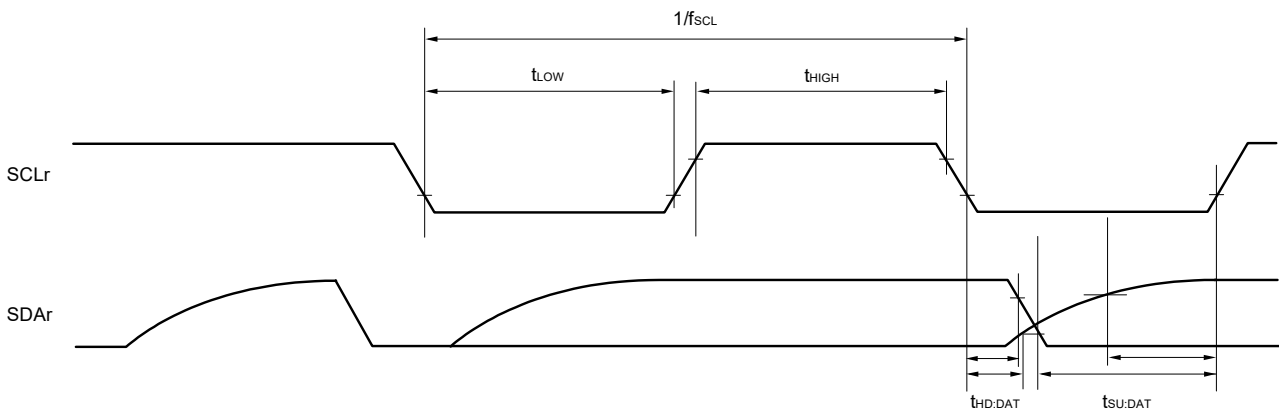
Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/EV_{DD} tolerance (When 64- to 128-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

(Remarks are listed on the next page.)

Simplified I²C mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



- Remarks**
1. $R_b[\Omega]$: Communication line (SDAr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance
 2. r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 4, 5, 8, 14), h: POM number (g = 0, 1, 4, 5, 7 to 9, 14)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)**($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|--------|---|---------------------------|----------------------------------|--------------------------|----------------------------------|----------------------------|------------------------------|------|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Transfer rate | | Reception $4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$ | | $f_{\text{MCK}}/6$ Note 1 | | $f_{\text{MCK}}/6$ Note 1 | | $f_{\text{MCK}}/6$ Note 1 | bps |
| | | | | 5.3 | | 1.3 | | 0.6 | Mbps |
| | | $2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$ | | $f_{\text{MCK}}/6$ Note 1 | | $f_{\text{MCK}}/6$ Note 1 | | $f_{\text{MCK}}/6$ Note 1 | bps |
| | | | | 5.3 | | 1.3 | | 0.6 | Mbps |
| $1.8\text{ V} \leq \text{EV}_{\text{DD}0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ | | $f_{\text{MCK}}/6$ Notes 1 to 3 | | $f_{\text{MCK}}/6$ Notes 1, 2 | | $f_{\text{MCK}}/6$ Notes 1, 2 | bps | | |
| | | 5.3 | | 1.3 | | 0.6 | Mbps | | |

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.**2.** Use it with $\text{EV}_{\text{DD}0} \geq \text{V}_b$.**3.** The following conditions are required for low voltage interface when $\text{EV}_{\text{DD}0} < \text{V}_{\text{DD}}$. $2.4\text{ V} \leq \text{EV}_{\text{DD}0} < 2.7\text{ V}$: MAX. 2.6 Mbps $1.8\text{ V} \leq \text{EV}_{\text{DD}0} < 2.4\text{ V}$: MAX. 1.3 Mbps**4.** The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:HS (high-speed main) mode: 32 MHz ($2.7\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$)16 MHz ($2.4\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$)LS (low-speed main) mode: 8 MHz ($1.8\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$)LV (low-voltage main) mode: 4 MHz ($1.6\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$)

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/ EV_{DD} tolerance (When 64- to 128-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

Remarks 1. $\text{V}_b[\text{V}]$: Communication line voltage**2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)**3.** f_{MCK} : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

n: Channel number (mn = 00 to 03, 10 to 13)

4. UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)

(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit | | |
|---------------|--------|--------------|---|------|--------------------------|-------------------|----------------------------|-------------------|------|-------------------|------|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | | |
| Transfer rate | | Transmission | 4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V | | | Note 1 | | Note 1 | | Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 1.4 kΩ, V _b = 2.7 V | | | 2.8 Note 2 | | 2.8 Note 2 | | 2.8 Note 2 | Mbps |
| | | | 2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V | | | Note 3 | | Note 3 | | Note 3 | bps |
| | | | Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 2.7 kΩ, V _b = 2.3 V | | | 1.2 Note 4 | | 1.2 Note 4 | | 1.2 Note 4 | Mbps |
| | | | 1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V | | | Notes 5, 6 | | Notes 5, 6 | | Notes 5, 6 | bps |
| | | | Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 5.5 kΩ, V _b = 1.6 V | | | 0.43 Note 7 | | 0.43 Note 7 | | 0.43 Note 7 | Mbps |

Notes 1. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ EV_{DD0} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

- This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

Notes 3. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$ and $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.
5. Use it with $EV_{DD0} \geq V_b$.
6. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $1.8\text{ V} \leq EV_{DD0} < 3.3\text{ V}$ and $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

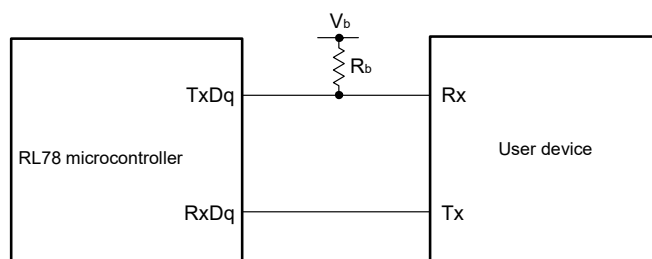
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

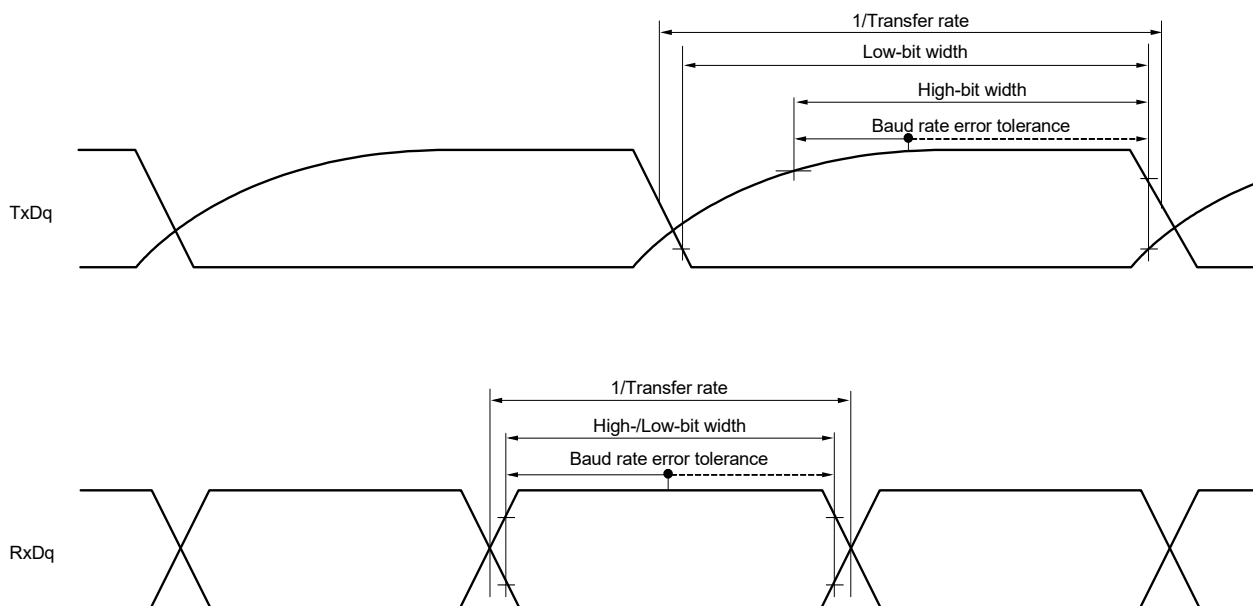
7. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 6 above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/EV_{DD} tolerance (When 64- to 128-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



- Remarks 1.** $R_b[\Omega]$: Communication line (TxDq) pull-up resistance,
 $C_b[F]$: Communication line (TxDq) load capacitance, $V_b[V]$: Communication line voltage
- 2.** q : UART number ($q = 0$ to 3), g : PIM and POM number ($g = 0, 1, 8, 14$)
- 3.** f_{MCK} : Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
 m : Unit number, n : Channel number ($mn = 00$ to $03, 10$ to 13))
- 4.** UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only) (1/2)**($T_A = -40$ to $+85^\circ\text{C}$, $2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|-------------------|--|---------------------------|------|---------------------------|------|----------------------------|------|------|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | t_{KCY1} | $t_{\text{KCY1}} \geq 2/f_{\text{CLK}}$ $4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | 200 | | 1150 | | 1150 | | ns |
| | | | 300 | | 1150 | | 1150 | | ns |
| SCKp high-level width | t_{KH1} | $4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | $t_{\text{KCY1}}/2 - 50$ | | $t_{\text{KCY1}}/2 - 50$ | | $t_{\text{KCY1}}/2 - 50$ | | ns |
| | | | $t_{\text{KCY1}}/2 - 120$ | | $t_{\text{KCY1}}/2 - 120$ | | $t_{\text{KCY1}}/2 - 120$ | | ns |
| SCKp low-level width | t_{KL1} | $4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | $t_{\text{KCY1}}/2 - 7$ | | $t_{\text{KCY1}}/2 - 50$ | | $t_{\text{KCY1}}/2 - 50$ | | ns |
| | | | $t_{\text{KCY1}}/2 - 10$ | | $t_{\text{KCY1}}/2 - 50$ | | $t_{\text{KCY1}}/2 - 50$ | | ns |
| Slp setup time (to SCKp \uparrow) ^{Note 1} | t_{SIK1} | $4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | 58 | | 479 | | 479 | | ns |
| | | | 121 | | 479 | | 479 | | ns |
| Slp hold time (from SCKp \uparrow) ^{Note 1} | t_{SH1} | $4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | 10 | | 10 | | 10 | | ns |
| | | | 10 | | 10 | | 10 | | ns |
| Delay time from SCKp \downarrow to SOP output ^{Note 1} | t_{KSO1} | $4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | | 60 | | 60 | | 60 | ns |
| | | | | 130 | | 130 | | 130 | ns |

(Notes, Caution, and Remarks are listed on the next page.)

(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only) (2/2)

(T_A = -40 to +85°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|-------------------|--|---------------------------|------|--------------------------|------|----------------------------|------|------|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Slp setup time (to SCKp↓) ^{Note 2} | t _{SIK1} | 4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ | 23 | | 110 | | 110 | | ns |
| | | 2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ | 33 | | 110 | | 110 | | ns |
| Slp hold time (from SCKp↓) ^{Note 2} | t _{KSI1} | 4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ | 10 | | 10 | | 10 | | ns |
| | | 2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ | 10 | | 10 | | 10 | | ns |
| Delay time from SCKp↑ to SO _p output ^{Note 2} | t _{KSO1} | 4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ | | 10 | 10 | | 10 | | ns |
| | | 2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ | | 10 | 10 | | 10 | | ns |

Notes 1. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1.

2. When DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/EV_{DD} tolerance (When 64- to 128-pin products)) mode for the SO_p pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

- Remarks**
- R_b[Ω]: Communication line (SCKp, SO_p) pull-up resistance, C_b[F]: Communication line (SCKp, SO_p) load capacitance, V_b[V]: Communication line voltage
 - p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0),
g: PIM and POM number (g = 1)
 - f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKS_{mn} bit of serial mode register mn (SMR_{mn}). m: Unit number, n: Channel number (mn = 00))
 - This value is valid only when CSI00's peripheral I/O redirect function is not used.

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/3)
($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit | |
|-----------------------|------------|--|---|--------------------|--------------------------|--------------------|----------------------------|--------------------|------|----|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| SCKp cycle time | t_{KCY1} | $t_{KCY1} \geq 4/f_{CLK}$ | $4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | 300 | | 1150 | | 1150 | | ns |
| | | | $2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | 500 | | 1150 | | 1150 | | ns |
| | | | $1.8\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ^{Note} , $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$ | 1150 | | 1150 | | 1150 | | ns |
| SCKp high-level width | t_{KH1} | $4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | $t_{KCY1}/2 - 75$ | | $t_{KCY1}/2 - 75$ | | $t_{KCY1}/2 - 75$ | | ns | |
| | | | $2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | $t_{KCY1}/2 - 170$ | | $t_{KCY1}/2 - 170$ | | $t_{KCY1}/2 - 170$ | | ns |
| | | | $1.8\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ^{Note} , $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$ | $t_{KCY1}/2 - 458$ | | $t_{KCY1}/2 - 458$ | | $t_{KCY1}/2 - 458$ | | ns |
| SCKp low-level width | t_{KL1} | $4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | $t_{KCY1}/2 - 12$ | | $t_{KCY1}/2 - 50$ | | $t_{KCY1}/2 - 50$ | | ns | |
| | | | $2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | $t_{KCY1}/2 - 18$ | | $t_{KCY1}/2 - 50$ | | $t_{KCY1}/2 - 50$ | | ns |
| | | | $1.8\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ^{Note} , $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$ | $t_{KCY1}/2 - 50$ | | $t_{KCY1}/2 - 50$ | | $t_{KCY1}/2 - 50$ | | ns |

Note Use it with $EV_{DD0} \geq V_b$.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/ EV_{DD} tolerance (When 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

(Remarks are listed two pages after the next page.)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (2/3)
($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$)

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|-------------------|--|---------------------------|------|--------------------------|------|----------------------------|------|------|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Slp setup time (to SCKp \uparrow) ^{Note 1} | t_{SIK1} | $4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 1.4\text{ k}\Omega$ | 81 | | 479 | | 479 | | ns |
| | | $2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$ | 177 | | 479 | | 479 | | ns |
| | | $1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ ^{Note 2} , $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$ | 479 | | 479 | | 479 | | ns |
| Slp hold time (from SCKp \uparrow) ^{Note 1} | t_{KSI1} | $4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 1.4\text{ k}\Omega$ | 19 | | 19 | | 19 | | ns |
| | | $2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$ | 19 | | 19 | | 19 | | ns |
| | | $1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ ^{Note 2} , $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$ | 19 | | 19 | | 19 | | ns |
| Delay time from SCKp \downarrow to SOp output ^{Note 1} | t_{KSO1} | $4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 1.4\text{ k}\Omega$ | | 100 | | 100 | | 100 | ns |
| | | $2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$ | | 195 | | 195 | | 195 | ns |
| | | $1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ ^{Note 2} , $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$ | | 483 | | 483 | | 483 | ns |

- Notes**
1. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$.
 2. Use it with $\text{EV}_{\text{DD0}} \geq \text{V}_b$.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/ EV_{DD} tolerance (When 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the page after the next page.)

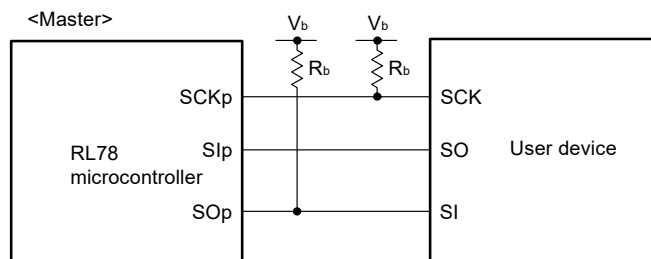
(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (3/3)
($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$)

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|-------------------|--|---------------------------|------|--------------------------|------|----------------------------|------|------|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Slp setup time (to SCKp↓) ^{Note 1} | t_{SIK1} | $4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 1.4\text{ k}\Omega$ | 44 | | 110 | | 110 | | ns |
| | | $2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$ | 44 | | 110 | | 110 | | ns |
| | | $1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ ^{Note 2} , $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$ | 110 | | 110 | | 110 | | ns |
| Slp hold time (from SCKp↓) ^{Note 1} | t_{KSI1} | $4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 1.4\text{ k}\Omega$ | 19 | | 19 | | 19 | | ns |
| | | $2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$ | 19 | | 19 | | 19 | | ns |
| | | $1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ ^{Note 2} , $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$ | 19 | | 19 | | 19 | | ns |
| Delay time from SCKp↑ to SOp output ^{Note 1} | t_{KSO1} | $4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 1.4\text{ k}\Omega$ | | 25 | | 25 | | 25 | ns |
| | | $2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$ | | 25 | | 25 | | 25 | ns |
| | | $1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ ^{Note 2} , $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$ | | 25 | | 25 | | 25 | ns |

- Notes**
1. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.
 2. Use it with $\text{EV}_{\text{DD0}} \geq \text{V}_b$.

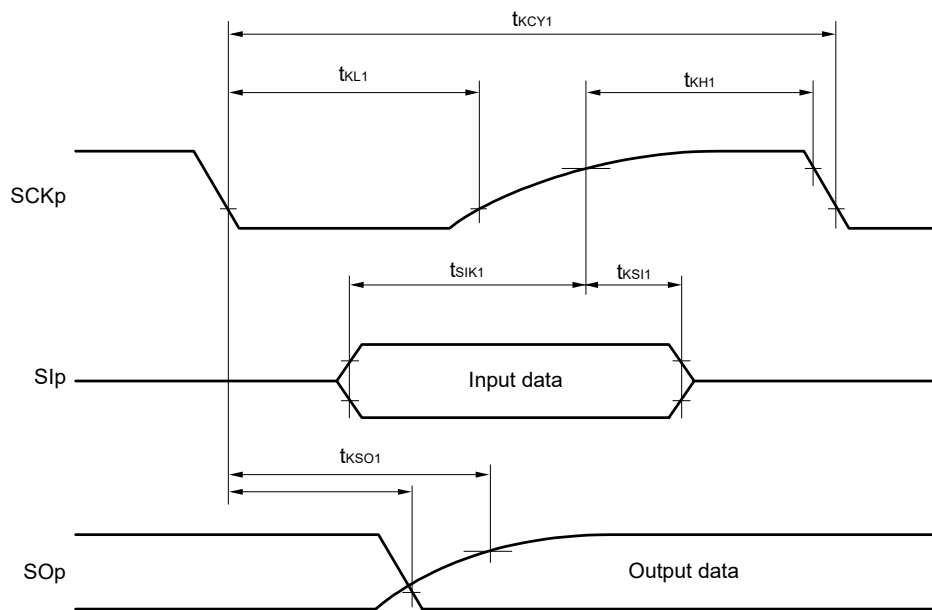
Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/ EV_{DD} tolerance (When 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

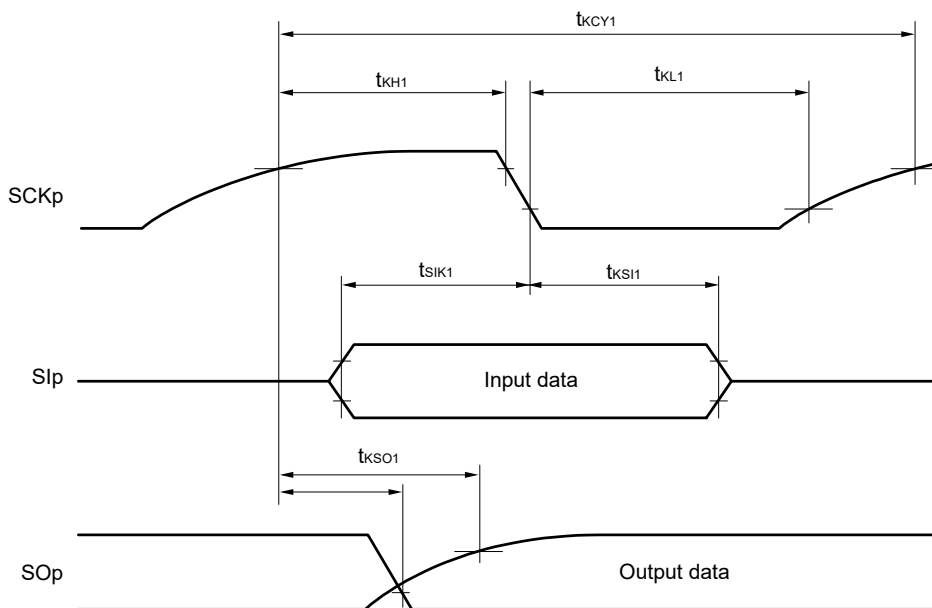
CSI mode connection diagram (during communication at different potential)

- Remarks**
- $R_b[\Omega]$: Communication line (SCKp, SOp) pull-up resistance, $C_b[\text{F}]$: Communication line (SCKp, SOp) load capacitance, $V_b[\text{V}]$: Communication line voltage
 - p: CSI number ($p = 00, 01, 10, 20, 30, 31$), m: Unit number, n: Channel number ($mn = 00, 01, 02, 10, 12, 13$), g: PIM and POM number ($g = 0, 1, 4, 5, 8, 14$)
 - f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number ($mn = 00$))
 - CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



- Remarks**
1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
 2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)
($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$) (1/2)

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|-----------------------------------|------------|--|--|---------------------------|------|--------------------------|------|----------------------------|------|------|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time ^{Note 1} | t_{KCY2} | $4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ | $24\text{ MHz} < f_{MCK}$ | 14/ f_{MCK} | | – | | – | | ns |
| | | | $20\text{ MHz} < f_{MCK} \leq 24\text{ MHz}$ | 12/ f_{MCK} | | – | | – | | ns |
| | | | $8\text{ MHz} < f_{MCK} \leq 20\text{ MHz}$ | 10/ f_{MCK} | | – | | – | | ns |
| | | | $4\text{ MHz} < f_{MCK} \leq 8\text{ MHz}$ | 8/ f_{MCK} | | 16/ f_{MCK} | | – | | ns |
| | | | $f_{MCK} \leq 4\text{ MHz}$ | 6/ f_{MCK} | | 10/ f_{MCK} | | 10/ f_{MCK} | | ns |
| | | $2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ | $24\text{ MHz} < f_{MCK}$ | 20/ f_{MCK} | | – | | – | | ns |
| | | | $20\text{ MHz} < f_{MCK} \leq 24\text{ MHz}$ | 16/ f_{MCK} | | – | | – | | ns |
| | | | $16\text{ MHz} < f_{MCK} \leq 20\text{ MHz}$ | 14/ f_{MCK} | | – | | – | | ns |
| | | | $8\text{ MHz} < f_{MCK} \leq 16\text{ MHz}$ | 12/ f_{MCK} | | – | | – | | ns |
| | | | $4\text{ MHz} < f_{MCK} \leq 8\text{ MHz}$ | 8/ f_{MCK} | | 16/ f_{MCK} | | – | | ns |
| | | | $f_{MCK} \leq 4\text{ MHz}$ | 6/ f_{MCK} | | 10/ f_{MCK} | | 10/ f_{MCK} | | ns |
| | | $1.8\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ^{Note 2} | $24\text{ MHz} < f_{MCK}$ | 48/ f_{MCK} | | – | | – | | ns |
| | | | $20\text{ MHz} < f_{MCK} \leq 24\text{ MHz}$ | 36/ f_{MCK} | | – | | – | | ns |
| | | | $16\text{ MHz} < f_{MCK} \leq 20\text{ MHz}$ | 32/ f_{MCK} | | – | | – | | ns |
| | | | $8\text{ MHz} < f_{MCK} \leq 16\text{ MHz}$ | 26/ f_{MCK} | | – | | – | | ns |
| | | | $4\text{ MHz} < f_{MCK} \leq 8\text{ MHz}$ | 16/ f_{MCK} | | 16/ f_{MCK} | | – | | ns |
| | | | $f_{MCK} \leq 4\text{ MHz}$ | 10/ f_{MCK} | | 10/ f_{MCK} | | 10/ f_{MCK} | | ns |

(Notes and Caution are listed on the next page, and Remarks are listed on the page after the next page.)

(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)
(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/2)

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|--|---|------------------------------|-----------------------------|------------------------------|-----------------------------|------------------------------|-----------------------------|------|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp high-/low-level width | t _{KH2} , t _{KL2} | 4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V | t _{KCY2} /2 – 12 | | t _{KCY2} /2 – 50 | | t _{KCY2} /2 – 50 | | ns |
| | | 2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V | t _{KCY2} /2 – 18 | | t _{KCY2} /2 – 50 | | t _{KCY2} /2 – 50 | | ns |
| | | 1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} | t _{KCY2} /2 – 50 | | t _{KCY2} /2 – 50 | | t _{KCY2} /2 – 50 | | ns |
| Slp setup time (to SCKp↑) ^{Note 3} | t _{SIK2} | 4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V | 1/f _{MCK} + 20 | | 1/f _{MCK} + 30 | | 1/f _{MCK} + 30 | | ns |
| | | 2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V | 1/f _{MCK} + 20 | | 1/f _{MCK} + 30 | | 1/f _{MCK} + 30 | | ns |
| | | 1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} | 1/f _{MCK} + 30 | | 1/f _{MCK} + 30 | | 1/f _{MCK} + 30 | | ns |
| Slp hold time (from SCKp↑) ^{Note 4} | t _{SI2} | | 1/f _{MCK} + 31 | | 1/f _{MCK} + 31 | | 1/f _{MCK} + 31 | | ns |
| Delay time from SCKp↓ to SOP output ^{Note 5} | t _{KSO2} | 4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ | | 2/f _{MCK} + 120 | | 2/f _{MCK} + 573 | | 2/f _{MCK} + 573 | ns |
| | | 2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ | | 2/f _{MCK} + 214 | | 2/f _{MCK} + 573 | | 2/f _{MCK} + 573 | ns |
| | | 1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 30 pF, R _b = 5.5 kΩ | | 2/f _{MCK} + 573 | | 2/f _{MCK} + 573 | | 2/f _{MCK} + 573 | ns |

Notes 1. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

2. Use it with EV_{DD0} ≥ V_b.

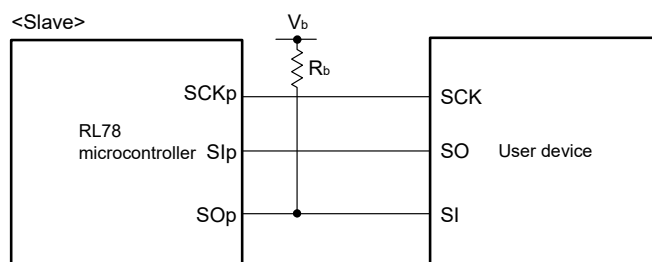
3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOP output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

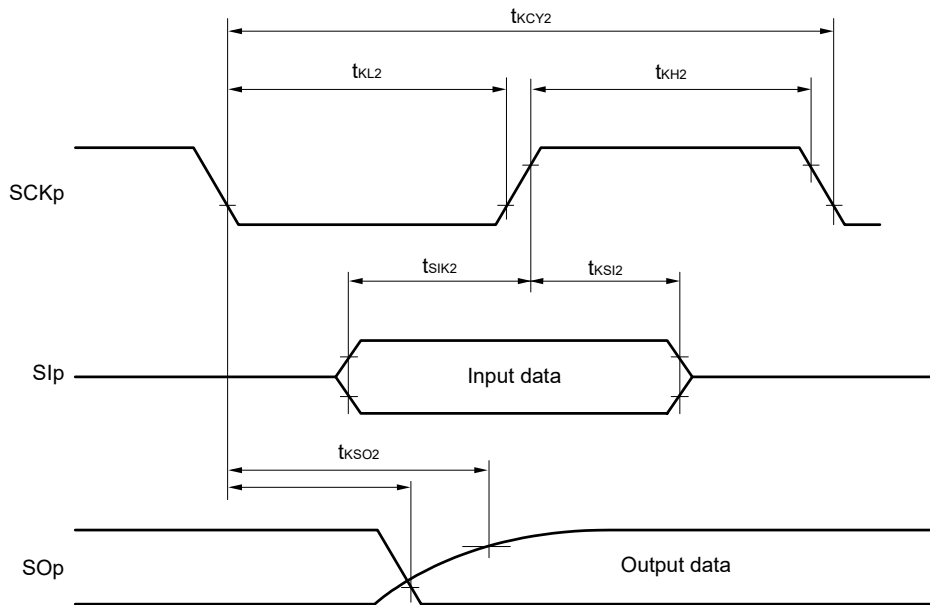
Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/EV_{DD} tolerance (for the 64- to 128-pin products)) mode for the SOP pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

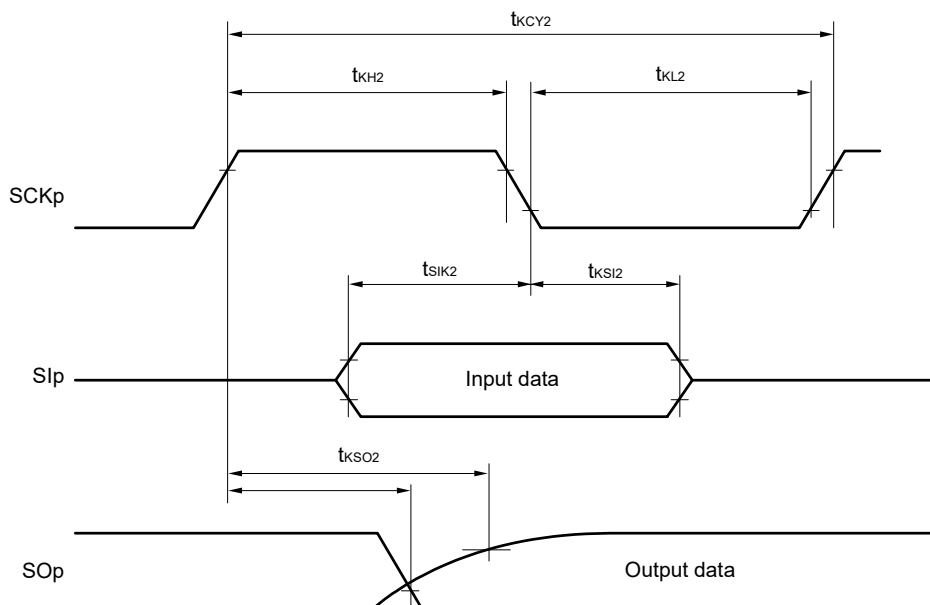
CSI mode connection diagram (during communication at different potential)

- Remarks**
- $R_b[\Omega]$: Communication line (SO_p) pull-up resistance, $C_b[F]$: Communication line (SO_p) load capacitance, $V_b[V]$: Communication line voltage
 - p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
 - f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKS_{mn} bit of serial mode register mn (SMR_{mn}).
m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))
 - CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



- Remarks 1.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number,
 n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
- 2.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode) (1/2) $(T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$)

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---------------------------|-------------------|---|---------------------------|----------------|--------------------------|---------------|----------------------------|---------------|------|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLr clock frequency | f_{SCL} | $4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 50\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$ | | 1000 Note 1 | | 300 Note 1 | | 300 Note 1 | kHz |
| | | $2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 50\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$ | | 1000 Note 1 | | 300 Note 1 | | 300 Note 1 | kHz |
| | | $4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 2.8\text{ k}\Omega$ | | 400 Note 1 | | 300 Note 1 | | 300 Note 1 | kHz |
| | | $2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$ | | 400 Note 1 | | 300 Note 1 | | 300 ote 1 | kHz |
| | | $1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ ^{Note 2} , $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$ | | 300 Note 1 | | 300 Note 1 | | 300 Note 1 | kHz |
| Hold time when SCLr = "L" | t_{LOW} | $4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 50\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$ | 475 | | 1550 | | 1550 | | ns |
| | | $2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 50\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$ | 475 | | 1550 | | 1550 | | ns |
| | | $4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 2.8\text{ k}\Omega$ | 1150 | | 1550 | | 1550 | | ns |
| | | $2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$ | 1150 | | 1550 | | 1550 | | ns |
| | | $1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ ^{Note 2} , $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$ | 1550 | | 1550 | | 1550 | | ns |
| Hold time when SCLr = "H" | t_{HIGH} | $4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 50\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$ | 245 | | 610 | | 610 | | ns |
| | | $2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 50\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$ | 200 | | 610 | | 610 | | ns |
| | | $4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 2.8\text{ k}\Omega$ | 675 | | 610 | | 610 | | ns |
| | | $2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$ | 600 | | 610 | | 610 | | ns |
| | | $1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ ^{Note 2} , $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$ | 610 | | 610 | | 610 | | ns |

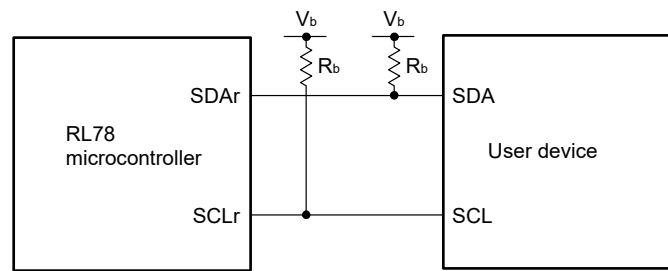
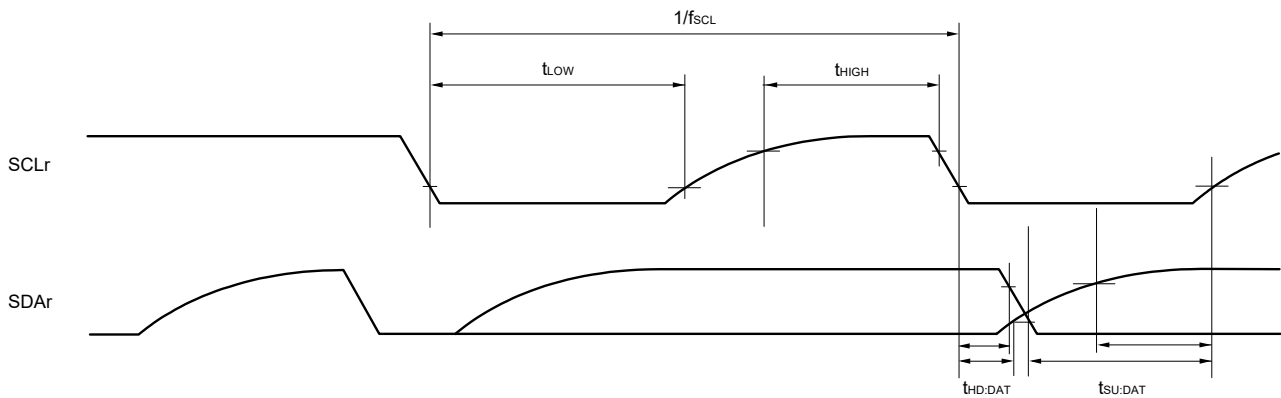
(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode) (2/2)**(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|-------------------------------|---------------------|--|---|------|--|------|--|------|------|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Data setup time (reception) | t _{SU:DAT} | 4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ | 1/f _{MCK} + 135 ^{Note 3} | | 1/f _{MCK} + 190 ^{Note 3} | | 1/f _{MCK} + 190 ^{Note 3} | | kHz |
| | | 2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ | 1/f _{MCK} + 135 ^{Note 3} | | 1/f _{MCK} + 190 ^{Note 3} | | 1/f _{MCK} + 190 ^{Note 3} | | kHz |
| | | 4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ | 1/f _{MCK} + 190 ^{Note 3} | | 1/f _{MCK} + 190 ^{Note 3} | | 1/f _{MCK} + 190 ^{Note 3} | | kHz |
| | | 2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ | 1/f _{MCK} + 190 ^{Note 3} | | 1/f _{MCK} + 190 ^{Note 3} | | 1/f _{MCK} + 190 ^{Note 3} | | kHz |
| | | 1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 100 pF, R _b = 5.5 kΩ | 1/f _{MCK} + 190 ^{Note 3} | | 1/f _{MCK} + 190 ^{Note 3} | | 1/f _{MCK} + 190 ^{Note 3} | | kHz |
| Data hold time (transmission) | t _{HD:DAT} | 4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ | 0 | 305 | 0 | 305 | 0 | 305 | ns |
| | | 2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ | 0 | 305 | 0 | 305 | 0 | 305 | ns |
| | | 4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ | 0 | 355 | 0 | 355 | 0 | 355 | ns |
| | | 2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ | 0 | 355 | 0 | 355 | 0 | 355 | ns |
| | | 1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 100 pF, R _b = 5.5 kΩ | 0 | 405 | 0 | 405 | 0 | 405 | ns |

- Notes**
- The value must also be equal to or less than f_{MCK}/4.
 - Use it with EV_{DD0} ≥ V_b.
 - Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/EV_{DD} tolerance (for the 64- to 128-pin products)) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/EV_{DD} tolerance (for the 64- to 128-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

Simplified I²C mode connection diagram (during communication at different potential)Simplified I²C mode serial transfer timing (during communication at different potential)

- Remarks**
1. $R_b[\Omega]$: Communication line (SDAr, SCLr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance, $V_b[V]$: Communication line voltage
 2. r: IIC number (r = 00, 01, 10, 20, 30, 31), g: PIM, POM number (g = 0, 1, 4, 5, 8, 14)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))

2.5.2 Serial interface IICA

(1) I²C standard mode(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit | |
|---|---------------------|--|-----------------------------------|------|--------------------------|------|----------------------------|------|------|-----|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| SCLA0 clock frequency | f _{SCL} | Standard mode: f _{CLK} ≥ 1 MHz | 2.7 V ≤ EV _{DD0} ≤ 5.5 V | 0 | 100 | 0 | 100 | 0 | 100 | kHz |
| | | | 1.8 V ≤ EV _{DD0} ≤ 5.5 V | 0 | 100 | 0 | 100 | 0 | 100 | kHz |
| | | | 1.7 V ≤ EV _{DD0} ≤ 5.5 V | 0 | 100 | 0 | 100 | 0 | 100 | kHz |
| | | | 1.6 V ≤ EV _{DD0} ≤ 5.5 V | - | | 0 | 100 | 0 | 100 | kHz |
| Setup time of restart condition | t _{SU:STA} | 2.7 V ≤ EV _{DD0} ≤ 5.5 V | 4.7 | | 4.7 | | 4.7 | | μs | |
| | | 1.8 V ≤ EV _{DD0} ≤ 5.5 V | 4.7 | | 4.7 | | 4.7 | | μs | |
| | | 1.7 V ≤ EV _{DD0} ≤ 5.5 V | 4.7 | | 4.7 | | 4.7 | | μs | |
| | | 1.6 V ≤ EV _{DD0} ≤ 5.5 V | - | | 4.7 | | 4.7 | | μs | |
| Hold time ^{Note 1} | t _{HD:STA} | 2.7 V ≤ EV _{DD0} ≤ 5.5 V | 4.0 | | 4.0 | | 4.0 | | μs | |
| | | 1.8 V ≤ EV _{DD0} ≤ 5.5 V | 4.0 | | 4.0 | | 4.0 | | μs | |
| | | 1.7 V ≤ EV _{DD0} ≤ 5.5 V | 4.0 | | 4.0 | | 4.0 | | μs | |
| | | 1.6 V ≤ EV _{DD0} ≤ 5.5 V | - | | 4.0 | | 4.0 | | μs | |
| Hold time when SCLA0 = "L" | t _{LOW} | 2.7 V ≤ EV _{DD0} ≤ 5.5 V | 4.7 | | 4.7 | | 4.7 | | μs | |
| | | 1.8 V ≤ EV _{DD0} ≤ 5.5 V | 4.7 | | 4.7 | | 4.7 | | μs | |
| | | 1.7 V ≤ EV _{DD0} ≤ 5.5 V | 4.7 | | 4.7 | | 4.7 | | μs | |
| | | 1.6 V ≤ EV _{DD0} ≤ 5.5 V | - | | 4.7 | | 4.7 | | μs | |
| Hold time when SCLA0 = "H" | t _{HIGH} | 2.7 V ≤ EV _{DD0} ≤ 5.5 V | 4.0 | | 4.0 | | 4.0 | | μs | |
| | | 1.8 V ≤ EV _{DD0} ≤ 5.5 V | 4.0 | | 4.0 | | 4.0 | | μs | |
| | | 1.7 V ≤ EV _{DD0} ≤ 5.5 V | 4.0 | | 4.0 | | 4.0 | | μs | |
| | | 1.6 V ≤ EV _{DD0} ≤ 5.5 V | - | | 4.0 | | 4.0 | | μs | |
| Data setup time (reception) | t _{SU:DAT} | 2.7 V ≤ EV _{DD0} ≤ 5.5 V | 250 | | 250 | | 250 | | ns | |
| | | 1.8 V ≤ EV _{DD0} ≤ 5.5 V | 250 | | 250 | | 250 | | ns | |
| | | 1.7 V ≤ EV _{DD0} ≤ 5.5 V | 250 | | 250 | | 250 | | ns | |
| | | 1.6 V ≤ EV _{DD0} ≤ 5.5 V | - | | 250 | | 250 | | ns | |
| Data hold time (transmission) ^{Note 2} | t _{HD:DAT} | 2.7 V ≤ EV _{DD0} ≤ 5.5 V | 0 | 3.45 | 0 | 3.45 | 0 | 3.45 | μs | |
| | | 1.8 V ≤ EV _{DD0} ≤ 5.5 V | 0 | 3.45 | 0 | 3.45 | 0 | 3.45 | μs | |
| | | 1.7 V ≤ EV _{DD0} ≤ 5.5 V | 0 | 3.45 | 0 | 3.45 | 0 | 3.45 | μs | |
| | | 1.6 V ≤ EV _{DD0} ≤ 5.5 V | - | | 0 | 3.45 | 0 | 3.45 | μs | |
| Setup time of stop condition | t _{SU:STO} | 2.7 V ≤ EV _{DD0} ≤ 5.5 V | 4.0 | | 4.0 | | 4.0 | | μs | |
| | | 1.8 V ≤ EV _{DD0} ≤ 5.5 V | 4.0 | | 4.0 | | 4.0 | | μs | |
| | | 1.7 V ≤ EV _{DD0} ≤ 5.5 V | 4.0 | | 4.0 | | 4.0 | | μs | |
| | | 1.6 V ≤ EV _{DD0} ≤ 5.5 V | - | | 4.0 | | 4.0 | | μs | |
| Bus-free time | t _{BUF} | 2.7 V ≤ EV _{DD0} ≤ 5.5 V | 4.7 | | 4.7 | | 4.7 | | μs | |
| | | 1.8 V ≤ EV _{DD0} ≤ 5.5 V | 4.7 | | 4.7 | | 4.7 | | μs | |
| | | 1.7 V ≤ EV _{DD0} ≤ 5.5 V | 4.7 | | 4.7 | | 4.7 | | μs | |
| | | 1.6 V ≤ EV _{DD0} ≤ 5.5 V | - | | 4.7 | | 4.7 | | μs | |

(Notes, Caution and Remark are listed on the next page.)

- Notes**
1. The first clock pulse is generated after this period when the start/restart condition is detected.
 2. The maximum value (MAX.) of t_{HD:DAT} is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

(2) I²C fast mode(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit | |
|---|---------------------|--|-----------------------------------|------|--------------------------|------|----------------------------|------|------|-----|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| SCLA0 clock frequency | f _{SCL} | Fast mode: f _{CLK} ≥ 3.5 MHz | 2.7 V ≤ EV _{DD0} ≤ 5.5 V | 0 | 400 | 0 | 400 | 0 | 400 | kHz |
| | | | 1.8 V ≤ EV _{DD0} ≤ 5.5 V | 0 | 400 | 0 | 400 | 0 | 400 | kHz |
| Setup time of restart condition | t _{SU:STA} | 2.7 V ≤ EV _{DD0} ≤ 5.5 V | 0.6 | | 0.6 | | 0.6 | | μs | |
| | | 1.8 V ≤ EV _{DD0} ≤ 5.5 V | 0.6 | | 0.6 | | 0.6 | | μs | |
| Hold time ^{Note 1} | t _{HD:STA} | 2.7 V ≤ EV _{DD0} ≤ 5.5 V | 0.6 | | 0.6 | | 0.6 | | μs | |
| | | 1.8 V ≤ EV _{DD0} ≤ 5.5 V | 0.6 | | 0.6 | | 0.6 | | μs | |
| Hold time when SCLA0 = "L" | t _{LOW} | 2.7 V ≤ EV _{DD0} ≤ 5.5 V | 1.3 | | 1.3 | | 1.3 | | μs | |
| | | 1.8 V ≤ EV _{DD0} ≤ 5.5 V | 1.3 | | 1.3 | | 1.3 | | μs | |
| Hold time when SCLA0 = "H" | t _{HIGH} | 2.7 V ≤ EV _{DD0} ≤ 5.5 V | 0.6 | | 0.6 | | 0.6 | | μs | |
| | | 1.8 V ≤ EV _{DD0} ≤ 5.5 V | 0.6 | | 0.6 | | 0.6 | | μs | |
| Data setup time (reception) | t _{SU:DAT} | 2.7 V ≤ EV _{DD0} ≤ 5.5 V | 100 | | 100 | | 100 | | μs | |
| | | 1.8 V ≤ EV _{DD0} ≤ 5.5 V | 100 | | 100 | | 100 | | μs | |
| Data hold time (transmission) ^{Note 2} | t _{HD:DAT} | 2.7 V ≤ EV _{DD0} ≤ 5.5 V | 0 | 0.9 | 0 | 0.9 | 0 | 0.9 | μs | |
| | | 1.8 V ≤ EV _{DD0} ≤ 5.5 V | 0 | 0.9 | 0 | 0.9 | 0 | 0.9 | μs | |
| Setup time of stop condition | t _{SU:STO} | 2.7 V ≤ EV _{DD0} ≤ 5.5 V | 0.6 | | 0.6 | | 0.6 | | μs | |
| | | 1.8 V ≤ EV _{DD0} ≤ 5.5 V | 0.6 | | 0.6 | | 0.6 | | μs | |
| Bus-free time | t _{BUF} | 2.7 V ≤ EV _{DD0} ≤ 5.5 V | 1.3 | | 1.3 | | 1.3 | | μs | |
| | | 1.8 V ≤ EV _{DD0} ≤ 5.5 V | 1.3 | | 1.3 | | 1.3 | | μs | |

- Notes**
- The first clock pulse is generated after this period when the start/restart condition is detected.
 - The maximum value (MAX.) of t_{HD:DAT} is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

(3) I²C fast mode plus

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---------------------|---|---------------------------|------|--------------------------|------|----------------------------|------|------|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | f _{SCL} | Fast mode plus: f _{CLK} ≥ 10 MHz 2.7 V ≤ EV _{DD0} ≤ 5.5 V | 0 | 1000 | – | – | – | – | kHz |
| Setup time of restart condition | t _{SU:STA} | 2.7 V ≤ EV _{DD0} ≤ 5.5 V | 0.26 | | – | – | – | – | μs |
| Hold time ^{Note 1} | t _{HD:STA} | 2.7 V ≤ EV _{DD0} ≤ 5.5 V | 0.26 | | – | – | – | – | μs |
| Hold time when SCLA0 = "L" | t _{LOW} | 2.7 V ≤ EV _{DD0} ≤ 5.5 V | 0.5 | | – | – | – | – | μs |
| Hold time when SCLA0 = "H" | t _{HIGH} | 2.7 V ≤ EV _{DD0} ≤ 5.5 V | 0.26 | | – | – | – | – | μs |
| Data setup time (reception) | t _{SU:DAT} | 2.7 V ≤ EV _{DD0} ≤ 5.5 V | 50 | | – | – | – | – | μs |
| Data hold time (transmission) ^{Note 2} | t _{HD:DAT} | 2.7 V ≤ EV _{DD0} ≤ 5.5 V | 0 | 0.45 | – | – | – | – | μs |
| Setup time of stop condition | t _{SU:STO} | 2.7 V ≤ EV _{DD0} ≤ 5.5 V | 0.26 | | – | – | – | – | μs |
| Bus-free time | t _{BUF} | 2.7 V ≤ EV _{DD0} ≤ 5.5 V | 0.5 | | – | – | – | – | μs |

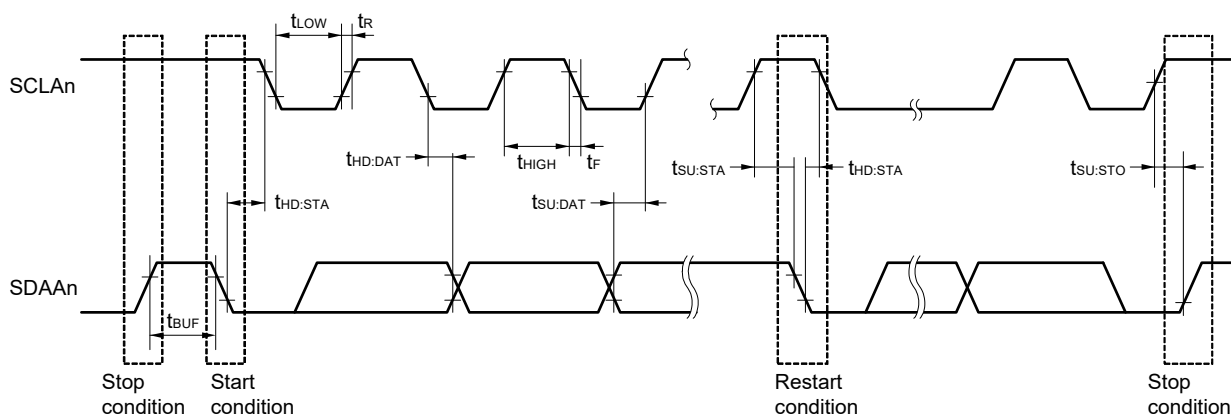
- Notes**
- The first clock pulse is generated after this period when the start/restart condition is detected.
 - The maximum value (MAX.) of t_{HD:DAT} is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ

I²C serial transfer timing



Remark n = 0, 1

2.6 Analog Characteristics

2.6.1 A/D converter characteristics

Classification of A/D converter characteristics

| Input channel | Reference Voltage | | |
|--|--|--|--|
| | Reference voltage (+) = AV_{REFP} Reference voltage (-) = AV_{REFM} | Reference voltage (+) = V_{DD} Reference voltage (-) = V_{SS} | Reference voltage (+) = V_{BGR} Reference voltage (-) = AV_{REFM} |
| ANI0 to ANI14 | Refer to 2.6.1 (1). | Refer to 2.6.1 (3). | Refer to 2.6.1 (4). |
| ANI16 to ANI26 | Refer to 2.6.1 (2). | | |
| Internal reference voltage Temperature sensor output voltage | Refer to 2.6.1 (1). | | — |

(1) When reference voltage (+) = $AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), reference voltage (-) = $AV_{REFM}/ANI1$ ($ADREFM = 1$), target pin : ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|--|-----------------|---|---|--------|--------------------------------|-------------|---------------|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error ^{Note 1} | AINL | 10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3} | $1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ | | 1.2 | ± 3.5 | LSB |
| | | | $1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ ^{Note 4} | | 1.2 | ± 7.0 | LSB |
| Conversion time | t_{CONV} | 10-bit resolution Target pin: ANI2 to ANI14 | $3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 2.125 | | 39 | μs |
| | | | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 3.1875 | | 39 | μs |
| | | | $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 17 | | 39 | μs |
| | | | $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 57 | | 95 | μs |
| | | 10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode) | $3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 2.375 | | 39 | μs |
| | | | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 3.5625 | | 39 | μs |
| Zero-scale error ^{Notes 1, 2} | E _{ZS} | 10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3} | $1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ | | | ± 0.25 | %FSR |
| | | | $1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ ^{Note 4} | | | ± 0.50 | %FSR |
| Full-scale error ^{Notes 1, 2} | E _{FS} | 10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3} | $1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ | | | ± 0.25 | %FSR |
| | | | $1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ ^{Note 4} | | | ± 0.50 | %FSR |
| Integral linearity error ^{Note 1} | ILE | 10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3} | $1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ | | | ± 2.5 | LSB |
| | | | $1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ ^{Note 4} | | | ± 5.0 | LSB |
| Differential linearity error ^{Note 1} | DLE | 10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3} | $1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ | | | ± 1.5 | LSB |
| | | | $1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ ^{Note 4} | | | ± 2.0 | LSB |
| Analog input voltage | V_{AIN} | ANI2 to ANI14 | | 0 | | AV_{REFP} | V |
| | | Internal reference voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode) | | | V_{BGR} ^{Note 5} | | V |
| | | Temperature sensor output voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode) | | | V_{TMPS25} ^{Note 5} | | V |

(Notes are listed on the next page.)

- Notes**
1. Excludes quantization error ($\pm 1/2$ LSB).
 2. This value is indicated as a ratio (%FSR) to the full-scale value.
 3. When $AV_{REFP} < V_{DD}$, the MAX. values are as follows.
Overall error: Add ± 1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.
Zero-scale error/Full-scale error: Add $\pm 0.05\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.
Integral linearity error/ Differential linearity error: Add ± 0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.
 4. Values when the conversion time is set to $57 \mu\text{s}$ (min.) and $95 \mu\text{s}$ (max.).
 5. Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

(2) When reference voltage (+) = $AV_{REFP}/ANI0$ ($ADREFP1 = 0, ADREFP0 = 1$), reference voltage (-) = $AV_{REFM}/ANI1$ ($ADREFM = 1$), target pin : ANI16 to ANI26

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $1.6\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|--|-----------------|---|--|--------|-------------------------------|------------|---------------|
| Resolution | RES | | 8 | | 10 | bit | |
| Overall error ^{Note 1} | AINL | 10-bit resolution $EV_{DD0} = AV_{REFP} = V_{DD}$ Notes 3, 4 | $1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ | | 1.2 | ± 5.0 | LSB |
| | | | $1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5 | | 1.2 | ± 8.5 | LSB |
| Conversion time | t_{CONV} | 10-bit resolution Target ANI pin : ANI16 to ANI26 | $3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 2.125 | | 39 | μs |
| | | | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 3.1875 | | 39 | μs |
| | | | $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 17 | | 39 | μs |
| | | | $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 57 | | 95 | μs |
| Zero-scale error ^{Notes 1, 2} | E _{ZS} | 10-bit resolution $EV_{DD0} = AV_{REFP} = V_{DD}$ Notes 3, 4 | $1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ | | | ± 0.35 | %FSR |
| | | | $1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5 | | | ± 0.60 | %FSR |
| Full-scale error ^{Notes 1, 2} | E _{FS} | 10-bit resolution $EV_{DD0} = AV_{REFP} = V_{DD}$ Notes 3, 4 | $1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ | | | ± 0.35 | %FSR |
| | | | $1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5 | | | ± 0.60 | %FSR |
| Integral linearity error ^{Note 1} | ILE | 10-bit resolution $EV_{DD0} = AV_{REFP} = V_{DD}$ Notes 3, 4 | $1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ | | | ± 3.5 | LSB |
| | | | $1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5 | | | ± 6.0 | LSB |
| Differential linearity error ^{Note 1} | DLE | 10-bit resolution $EV_{DD0} = AV_{REFP} = V_{DD}$ Notes 3, 4 | $1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ | | | ± 2.0 | LSB |
| | | | $1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5 | | | ± 2.5 | LSB |
| Analog input voltage | V_{AIN} | ANI16 to ANI26 | 0 | | AV_{REFP} and EV_{DD0} | V | |

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When $AV_{REFP} < V_{DD}$, the MAX. values are as follows.

Overall error: Add ± 1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Zero-scale error/Full-scale error: Add $\pm 0.05\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.

Integral linearity error/ Differential linearity error: Add ± 0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

4. When $AV_{REFP} < EV_{DD0} \leq V_{DD}$, the MAX. values are as follows.

Overall error: Add ± 4.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Zero-scale error/Full-scale error: Add $\pm 0.20\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.

Integral linearity error/ Differential linearity error: Add ± 2.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

5. When the conversion time is set to 57 μs (min.) and 95 μs (max.).

(3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = V_{SS} (ADREFM = 0), target pin : ANI0 to ANI14, ANI16 to ANI26, internal reference voltage, and temperature sensor output voltage

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$, Reference voltage (+) = V_{DD} , Reference voltage (-) = V_{SS})

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|--|------------|--|--|--------|------------|------------|---------------|
| Resolution | RES | | 8 | | 10 | bit | |
| Overall error ^{Note 1} | AINL | 10-bit resolution | $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | 1.2 | ± 7.0 | LSB |
| | | | $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ Note 3 | | 1.2 | ± 10.5 | LSB |
| Conversion time | t_{CONV} | 10-bit resolution Target pin: ANI0 to ANI14, ANI16 to ANI26 | $3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 2.125 | | 39 | μs |
| | | | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 3.1875 | | 39 | μs |
| | | | $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 17 | | 39 | μs |
| | | | $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 57 | | 95 | μs |
| Conversion time | t_{CONV} | 10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode) | $3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 2.375 | | 39 | μs |
| | | | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 3.5625 | | 39 | μs |
| | | | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 17 | | 39 | μs |
| Zero-scale error ^{Notes 1, 2} | E_{ZS} | 10-bit resolution | $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | | ± 0.60 | %FSR |
| | | | $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ Note 3 | | | ± 0.85 | %FSR |
| Full-scale error ^{Notes 1, 2} | E_{FS} | 10-bit resolution | $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | | ± 0.60 | %FSR |
| | | | $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ Note 3 | | | ± 0.85 | %FSR |
| Integral linearity error ^{Note 1} | ILE | 10-bit resolution | $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | | ± 4.0 | LSB |
| | | | $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ Note 3 | | | ± 6.5 | LSB |
| Differential linearity error ^{Note 1} | DLE | 10-bit resolution | $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | | ± 2.0 | LSB |
| | | | $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ Note 3 | | | ± 2.5 | LSB |
| Analog input voltage | V_{AIN} | ANI0 to ANI14 | 0 | | V_{DD} | V | |
| | | ANI16 to ANI26 | 0 | | EV_{DD0} | V | |
| | | Internal reference voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode) | V_{BGR} Note 4 | | | | V |
| | | Temperature sensor output voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode) | V_{TMPS25} Note 4 | | | | V |

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When the conversion time is set to 57 μs (min.) and 95 μs (max.).

4. Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = $AV_{REFM}/ANI1$ (ADREFM = 1), target pin : ANI0, ANI2 to ANI14, ANI16 to ANI26

($T_A = -40$ to $+85^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$, Reference voltage (+) = V_{BGR} ^{Note 3}, Reference voltage (-) = $AV_{REFM} = 0\text{ V}$ ^{Note 4}, HS (high-speed main) mode)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|--|------------|------------------|--|------|------|-----------------------------|---------------|
| Resolution | RES | | | 8 | | | bit |
| Conversion time | t_{CONV} | 8-bit resolution | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 17 | | 39 | μs |
| Zero-scale error ^{Notes 1, 2} | E_{ZS} | 8-bit resolution | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | | ± 0.60 | %FSR |
| Integral linearity error ^{Note 1} | ILE | 8-bit resolution | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | | ± 2.0 | LSB |
| Differential linearity error ^{Note 1} | DLE | 8-bit resolution | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | | ± 1.0 | LSB |
| Analog input voltage | V_{AIN} | | | 0 | | V_{BGR} ^{Note 3} | V |

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

4. When reference voltage (-) = V_{SS} , the MAX. values are as follows.

Zero-scale error: Add $\pm 0.35\%$ FSR to the MAX. value when reference voltage (-) = AV_{REFM} .

Integral linearity error: Add ± 0.5 LSB to the MAX. value when reference voltage (-) = AV_{REFM} .

Differential linearity error: Add ± 0.2 LSB to the MAX. value when reference voltage (-) = AV_{REFM} .

2.6.2 Temperature sensor/internal reference voltage characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, HS (high-speed main) mode)

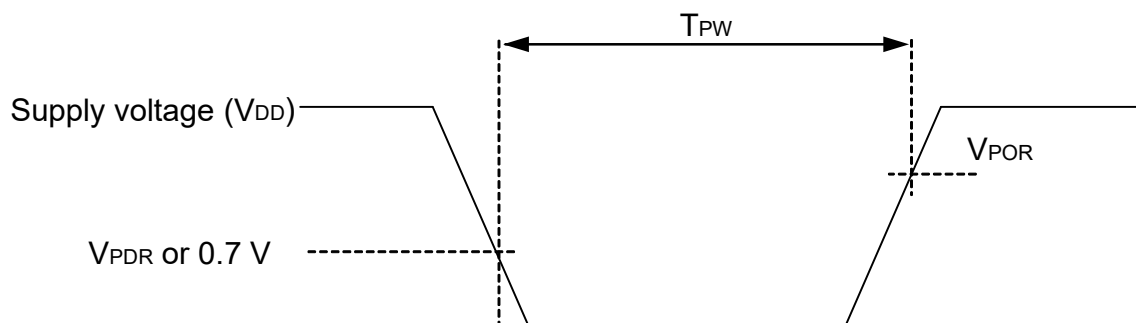
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-----------------------------------|--------------|---|------|------|------|----------------------|
| Temperature sensor output voltage | V_{TMP25} | Setting ADS register = 80H, $T_A = +25^\circ\text{C}$ | | 1.05 | | V |
| Internal reference voltage | V_{BGR} | Setting ADS register = 81H | 1.38 | 1.45 | 1.5 | V |
| Temperature coefficient | F_{VTMP25} | Temperature sensor that depends on the temperature | | -3.6 | | mV/ $^\circ\text{C}$ |
| Operation stabilization wait time | t_{AMP} | | 5 | | | μs |

2.6.3 POR circuit characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0\text{ V}$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-------------------------------------|-----------|------------------------|------|------|------|---------------|
| Detection voltage | V_{POR} | Power supply rise time | 1.47 | 1.51 | 1.55 | V |
| | V_{PDR} | Power supply fall time | 1.46 | 1.50 | 1.54 | V |
| Minimum pulse width ^{Note} | T_{PW} | | 300 | | | μs |

Note Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR} . This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7 V to when V_{DD} exceeds V_{POR} while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



2.6.4 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode

($T_A = -40$ to $+85^\circ\text{C}$, $V_{PDR} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|----------------------|------------------------|------------------------|------------------------|------|------|---------------|---|
| Detection voltage | Supply voltage level | V_{LVD0} | Power supply rise time | 3.98 | 4.06 | 4.14 | V |
| | | | Power supply fall time | 3.90 | 3.98 | 4.06 | V |
| | V_{LVD1} | Power supply rise time | 3.68 | 3.75 | 3.82 | V | |
| | | Power supply fall time | 3.60 | 3.67 | 3.74 | V | |
| | V_{LVD2} | Power supply rise time | 3.07 | 3.13 | 3.19 | V | |
| | | Power supply fall time | 3.00 | 3.06 | 3.12 | V | |
| | V_{LVD3} | Power supply rise time | 2.96 | 3.02 | 3.08 | V | |
| | | Power supply fall time | 2.90 | 2.96 | 3.02 | V | |
| | V_{LVD4} | Power supply rise time | 2.86 | 2.92 | 2.97 | V | |
| | | Power supply fall time | 2.80 | 2.86 | 2.91 | V | |
| | V_{LVD5} | Power supply rise time | 2.76 | 2.81 | 2.87 | V | |
| | | Power supply fall time | 2.70 | 2.75 | 2.81 | V | |
| | V_{LVD6} | Power supply rise time | 2.66 | 2.71 | 2.76 | V | |
| | | Power supply fall time | 2.60 | 2.65 | 2.70 | V | |
| | V_{LVD7} | Power supply rise time | 2.56 | 2.61 | 2.66 | V | |
| | | Power supply fall time | 2.50 | 2.55 | 2.60 | V | |
| | V_{LVD8} | Power supply rise time | 2.45 | 2.50 | 2.55 | V | |
| | | Power supply fall time | 2.40 | 2.45 | 2.50 | V | |
| | V_{LVD9} | Power supply rise time | 2.05 | 2.09 | 2.13 | V | |
| | | Power supply fall time | 2.00 | 2.04 | 2.08 | V | |
| | V_{LVD10} | Power supply rise time | 1.94 | 1.98 | 2.02 | V | |
| | | Power supply fall time | 1.90 | 1.94 | 1.98 | V | |
| | V_{LVD11} | Power supply rise time | 1.84 | 1.88 | 1.91 | V | |
| | | Power supply fall time | 1.80 | 1.84 | 1.87 | V | |
| | V_{LVD12} | Power supply rise time | 1.74 | 1.77 | 1.81 | V | |
| | | Power supply fall time | 1.70 | 1.73 | 1.77 | V | |
| V_{LVD13} | Power supply rise time | 1.64 | 1.67 | 1.70 | V | | |
| | Power supply fall time | 1.60 | 1.63 | 1.66 | V | | |
| Minimum pulse width | t_{LW} | | 300 | | | μs | |
| Detection delay time | | | | | 300 | μs | |

LVD Detection Voltage of Interrupt & Reset Mode**($T_A = -40$ to $+85^\circ\text{C}$, $V_{PDR} \leq V_{DD} \leq 5.5$ V, $V_{SS} = 0$ V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|--------------------------|---------------------|--|------------------------------|------|------|------|---|
| Interrupt and reset mode | VLVDA0 | $V_{POC2}, V_{POC1}, V_{POC0} = 0, 0, 0$, falling reset voltage | 1.60 | 1.63 | 1.66 | V | |
| | VLVDA1 | LVIS1, LVIS0 = 1, 0 | Rising release reset voltage | 1.74 | 1.77 | 1.81 | V |
| | | | Falling interrupt voltage | 1.70 | 1.73 | 1.77 | V |
| | VLVDA2 | LVIS1, LVIS0 = 0, 1 | Rising release reset voltage | 1.84 | 1.88 | 1.91 | V |
| | | | Falling interrupt voltage | 1.80 | 1.84 | 1.87 | V |
| | VLVDA3 | LVIS1, LVIS0 = 0, 0 | Rising release reset voltage | 2.86 | 2.92 | 2.97 | V |
| | | | Falling interrupt voltage | 2.80 | 2.86 | 2.91 | V |
| | VLVDB0 | $V_{POC2}, V_{POC1}, V_{POC0} = 0, 0, 1$, falling reset voltage | 1.80 | 1.84 | 1.87 | V | |
| | VLVDB1 | LVIS1, LVIS0 = 1, 0 | Rising release reset voltage | 1.94 | 1.98 | 2.02 | V |
| | | | Falling interrupt voltage | 1.90 | 1.94 | 1.98 | V |
| | VLVDB2 | LVIS1, LVIS0 = 0, 1 | Rising release reset voltage | 2.05 | 2.09 | 2.13 | V |
| | | | Falling interrupt voltage | 2.00 | 2.04 | 2.08 | V |
| | VLVDB3 | LVIS1, LVIS0 = 0, 0 | Rising release reset voltage | 3.07 | 3.13 | 3.19 | V |
| | | | Falling interrupt voltage | 3.00 | 3.06 | 3.12 | V |
| | VLVDC0 | $V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 0$, falling reset voltage | 2.40 | 2.45 | 2.50 | V | |
| | VLVDC1 | LVIS1, LVIS0 = 1, 0 | Rising release reset voltage | 2.56 | 2.61 | 2.66 | V |
| | | | Falling interrupt voltage | 2.50 | 2.55 | 2.60 | V |
| | VLVDC2 | LVIS1, LVIS0 = 0, 1 | Rising release reset voltage | 2.66 | 2.71 | 2.76 | V |
| | | | Falling interrupt voltage | 2.60 | 2.65 | 2.70 | V |
| | VLVDC3 | LVIS1, LVIS0 = 0, 0 | Rising release reset voltage | 3.68 | 3.75 | 3.82 | V |
| | | | Falling interrupt voltage | 3.60 | 3.67 | 3.74 | V |
| | VLVDD0 | $V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 1$, falling reset voltage | 2.70 | 2.75 | 2.81 | V | |
| | VLVDD1 | LVIS1, LVIS0 = 1, 0 | Rising release reset voltage | 2.86 | 2.92 | 2.97 | V |
| | | | Falling interrupt voltage | 2.80 | 2.86 | 2.91 | V |
| VLVDD2 | LVIS1, LVIS0 = 0, 1 | Rising release reset voltage | 2.96 | 3.02 | 3.08 | V | |
| | | Falling interrupt voltage | 2.90 | 2.96 | 3.02 | V | |
| VLVDD3 | LVIS1, LVIS0 = 0, 0 | Rising release reset voltage | 3.98 | 4.06 | 4.14 | V | |
| | | Falling interrupt voltage | 3.90 | 3.98 | 4.06 | V | |

2.6.5 Power supply voltage rising slope characteristics**($T_A = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0$ V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-----------------------------------|-----------|------------|------|------|------|------|
| Power supply voltage rising slope | S_{VDD} | | | | 54 | V/ms |

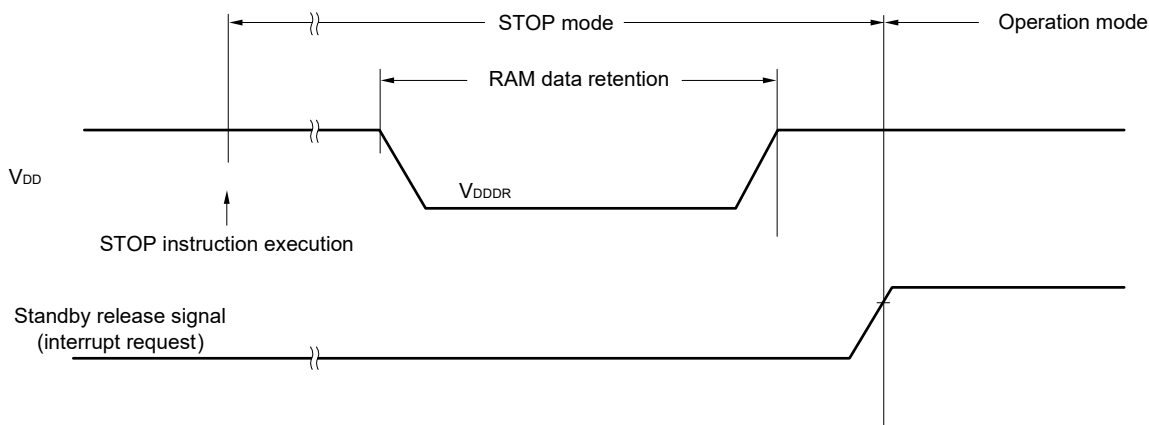
Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 2.4 AC Characteristics.

2.7 RAM Data Retention Characteristics

(T_A = -40 to +85°C, V_{SS} = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-------------------------------|-------------------|------------|----------------------|------|------|------|
| Data retention supply voltage | V _{DDDR} | | 1.46 ^{Note} | | 5.5 | V |

Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



2.8 Flash Memory Programming Characteristics

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|-------------------|--|---------|-----------|------|-------|
| CPU/peripheral hardware clock frequency | f _{CLK} | 1.8 V ≤ V _{DD} ≤ 5.5 V | 1 | | 32 | MHz |
| Number of code flash rewrites <small>Notes 1, 2, 3</small> | C _{erwr} | Retained for 20 years T _A = 85°C | 1,000 | | | Times |
| Number of data flash rewrites <small>Notes 1, 2, 3</small> | | Retained for 1 years T _A = 25°C | | 1,000,000 | | |
| | | Retained for 5 years T _A = 85°C | 100,000 | | | |
| | | Retained for 20 years T _A = 85°C | 10,000 | | | |

- Notes**
- 1 erase + 1 write after the erase is regarded as 1 rewrite.
The retaining years are until next rewrite after the rewrite.
 2. When using flash memory programmer and Renesas Electronics self programming library
 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

2.9 Dedicated Flash Memory Programmer Communication (UART)

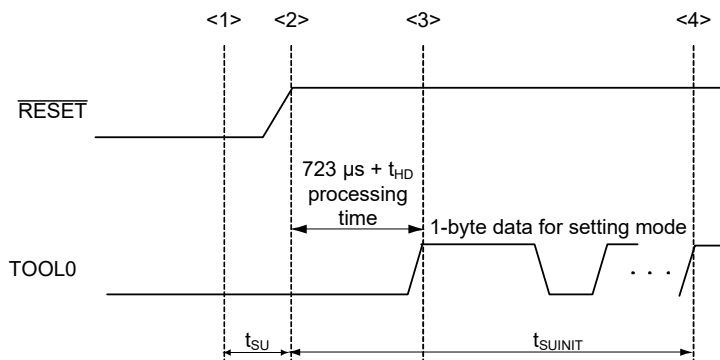
(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---------------|--------|---------------------------|---------|------|-----------|------|
| Transfer rate | | During serial programming | 115,200 | | 1,000,000 | bps |

2.10 Timing of Entry to Flash Memory Programming Modes

(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--|---------------------|---|------|------|------|------|
| Time to complete the communication for the initial setting after the external reset is released | t _{SUINIT} | POR and LVD reset must be released before the external reset is released. | | | 100 | ms |
| Time to release the external reset after the TOOL0 pin is set to the low level | t _{SU} | POR and LVD reset must be released before the external reset is released. | 10 | | | μs |
| Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory) | t _{HD} | POR and LVD reset must be released before the external reset is released. | 1 | | | ms |



- <1> The low level is input to the TOOL0 pin.
- <2> The external reset is released (POR and LVD reset must be released before the external reset is released.).
- <3> The TOOL0 pin is set to the high level.
- <4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

t_{SU}: Time to release the external reset after the TOOL0 pin is set to the low level

t_{HD}: Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

3. ELECTRICAL SPECIFICATIONS

(G: INDUSTRIAL APPLICATIONS $T_A = -40$ to $+105^\circ\text{C}$)

This chapter describes the following electrical specifications.

Target products G: Industrial applications $T_A = -40$ to $+105^\circ\text{C}$

R5F100xxGxx

- Cautions**
1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.
 2. With products not provided with an $\text{EV}_{\text{DD}0}$, $\text{EV}_{\text{DD}1}$, $\text{EV}_{\text{SS}0}$, or $\text{EV}_{\text{SS}1}$ pin, replace $\text{EV}_{\text{DD}0}$ and $\text{EV}_{\text{DD}1}$ with V_{DD} , or replace $\text{EV}_{\text{SS}0}$ and $\text{EV}_{\text{SS}1}$ with V_{SS} .
 3. The pins mounted depend on the product. Refer to 2.1 Port Function to 2.2.1 Functions for each product in the RL78/G13 User's Manual.
 4. Please contact Renesas Electronics sales office for derating of operation under $T_A = +85^\circ\text{C}$ to $+105^\circ\text{C}$. Derating is the systematic reduction of load for the sake of improved reliability.

Remark When RL78/G13 is used in the range of $T_A = -40$ to $+85^\circ\text{C}$, see 2. ELECTRICAL SPECIFICATIONS ($T_A = -40$ to $+85^\circ\text{C}$).

There are following differences between the products "G: Industrial applications ($T_A = -40$ to $+105^\circ\text{C}$)" and the products "A: Consumer applications, and D: Industrial applications".

| Parameter | Application | |
|--|--|--|
| | A: Consumer applications, D: Industrial applications | G: Industrial applications |
| Operating ambient temperature | $T_A = -40$ to $+85^\circ\text{C}$ | $T_A = -40$ to $+105^\circ\text{C}$ |
| Operating mode Operating voltage range | HS (high-speed main) mode: $2.7\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$ $2.4\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$ LS (low-speed main) mode: $1.8\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}@1\text{ MHz to }8\text{ MHz}$ LV (low-voltage main) mode: $1.6\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}@1\text{ MHz to }4\text{ MHz}$ | HS (high-speed main) mode only: $2.7\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$ $2.4\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$ |
| High-speed on-chip oscillator clock accuracy | $1.8\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$ $\pm 1.0\% @ T_A = -20$ to $+85^\circ\text{C}$ $\pm 1.5\% @ T_A = -40$ to -20°C $1.6\text{ V} \leq V_{\text{DD}} < 1.8\text{ V}$ $\pm 5.0\% @ T_A = -20$ to $+85^\circ\text{C}$ $\pm 5.5\% @ T_A = -40$ to -20°C | $2.4\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$ $\pm 2.0\% @ T_A = +85$ to $+105^\circ\text{C}$ $\pm 1.0\% @ T_A = -20$ to $+85^\circ\text{C}$ $\pm 1.5\% @ T_A = -40$ to -20°C |
| Serial array unit | UART CSI: $f_{\text{CLK}}/2$ (supporting 16 Mbps), $f_{\text{CLK}}/4$ Simplified I ² C communication | UART CSI: $f_{\text{CLK}}/4$ Simplified I ² C communication |
| IICA | Normal mode Fast mode Fast mode plus | Normal mode Fast mode |
| Voltage detector | Rise detection voltage: 1.67 V to 4.06 V (14 levels) Fall detection voltage: 1.63 V to 3.98 V (14 levels) | Rise detection voltage: 2.61 V to 4.06 V (8 levels) Fall detection voltage: 2.55 V to 3.98 V (8 levels) |

(Remark is listed on the next page.)

Remark The electrical characteristics of the products G: Industrial applications ($T_A = -40$ to $+105^\circ\text{C}$) are different from those of the products “A: Consumer applications, and D: Industrial applications”. For details, refer to **3.1** to **3.10**.

3.1 Absolute Maximum Ratings

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$) (1/2)

| Parameter | Symbols | Conditions | Ratings | Unit |
|------------------------|----------------------|---|---|------|
| Supply voltage | V_{DD} | | -0.5 to +6.5 | V |
| | EV_{DD0}, EV_{DD1} | $EV_{DD0} = EV_{DD1}$ | -0.5 to +6.5 | V |
| | EV_{SS0}, EV_{SS1} | $EV_{SS0} = EV_{SS1}$ | -0.5 to +0.3 | V |
| REGC pin input voltage | V_{IREGC} | REGC | -0.3 to +2.8 and -0.3 to $V_{DD} + 0.3$ ^{Note 1} | V |
| Input voltage | V_{I1} | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147 | -0.3 to $EV_{DD0} + 0.3$ and -0.3 to $V_{DD} + 0.3$ ^{Note 2} | V |
| | V_{I2} | P60 to P63 (N-ch open-drain) | -0.3 to +6.5 | V |
| | V_{I3} | P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, RESET | -0.3 to $V_{DD} + 0.3$ ^{Note 2} | V |
| Output voltage | V_{O1} | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | -0.3 to $EV_{DD0} + 0.3$ and -0.3 to $V_{DD} + 0.3$ ^{Note 2} | V |
| | V_{O2} | P20 to P27, P150 to P156 | -0.3 to $V_{DD} + 0.3$ ^{Note 2} | V |
| Analog input voltage | V_{AI1} | ANI16 to ANI26 | -0.3 to $EV_{DD0} + 0.3$ and -0.3 to $AV_{REF(+)} + 0.3$ ^{Notes 2, 3} | V |
| | V_{AI2} | ANI0 to ANI14 | -0.3 to $V_{DD} + 0.3$ and -0.3 to $AV_{REF(+)} + 0.3$ ^{Notes 2, 3} | V |

- Notes 1.** Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.
- 2.** Must be 6.5 V or lower.
- 3.** Do not exceed $AV_{REF(+)} + 0.3$ V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

- Remarks 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
- 2.** $AV_{REF(+)}$: + side reference voltage of the A/D converter.
- 3.** V_{SS} : Reference voltage

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$) (2/2)

| Parameter | Symbols | Conditions | | Ratings | Unit |
|-------------------------------|----------------------------------|------------------------------|--|--|------|
| Output current, high | I _{OH1} | Per pin | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | -40 | mA |
| | | Total of all pins -170 mA | P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 | -70 | mA |
| | | | P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 | -100 | mA |
| | I _{OH2} | Per pin | P20 to P27, P150 to P156 | -0.5 | mA |
| | | Total of all pins | | -2 | mA |
| | Output current, low | I _{OL1} | Per pin | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | 40 |
| Total of all pins 170 mA | | | P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 | 70 | mA |
| | | | P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 | 100 | mA |
| I _{OL2} | | Per pin | P20 to P27, P150 to P156 | 1 | mA |
| | | Total of all pins | | 5 | mA |
| Operating ambient temperature | | T _A | In normal operation mode | -40 to +105 | °C |
| | In flash memory programming mode | | | | |
| Storage temperature | T _{stg} | | -65 to +150 | °C | |

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.2 Oscillator Characteristics

3.2.1 X1, XT1 oscillator characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

| Parameter | Resonator | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|--|------|--------|------|------|
| X1 clock oscillation frequency (f_x) ^{Note} | Ceramic resonator/ crystal resonator | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 1.0 | | 20.0 | MHz |
| | | $2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$ | 1.0 | | 16.0 | MHz |
| XT1 clock oscillation frequency (f_x) ^{Note} | Crystal resonator | | 32 | 32.768 | 35 | kHz |

Note Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator and XT1 oscillator, refer to **5.4 System Clock Oscillator** in the RL78/G13 User's Manual.

3.2.2 On-chip oscillator characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

| Oscillators | Parameters | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|------------|-------------------------------|--|------|------|------|------|
| High-speed on-chip oscillator clock frequency ^{Notes 1, 2} | f_{IH} | | | 1 | | 32 | MHz |
| High-speed on-chip oscillator clock frequency accuracy | | -20 to $+85^\circ\text{C}$ | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | -1.0 | | +1.0 | % |
| | | -40 to -20°C | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | -1.5 | | +1.5 | % |
| | | $+85$ to $+105^\circ\text{C}$ | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | -2.0 | | +2.0 | % |
| Low-speed on-chip oscillator clock frequency | f_{IL} | | | | 15 | | kHz |
| Low-speed on-chip oscillator clock frequency accuracy | | | | -15 | | +15 | % |

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

2. This indicates the oscillator characteristics only. Refer to AC Characteristics for instruction execution time.

3.3 DC Characteristics

3.3.1 Pin characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$) (1/5)

| Items | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|--|---|--|--|------|-------|------------------------|----|
| Output current, high ^{Note 1} | IOH1 | Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | $2.4\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ | | | -3.0 ^{Note 2} | mA |
| | | Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (When duty $\leq 70\%$ ^{Note 3}) | $4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ | | | -30.0 | mA |
| | | | $2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$ | | | -10.0 | mA |
| | | | $2.4\text{ V} \leq EV_{DD0} < 2.7\text{ V}$ | | | -5.0 | mA |
| | | Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (When duty $\leq 70\%$ ^{Note 3}) | $4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ | | | -30.0 | mA |
| | | | $2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$ | | | -19.0 | mA |
| | $2.4\text{ V} \leq EV_{DD0} < 2.7\text{ V}$ | | | | -10.0 | mA | |
| | Total of all pins (When duty $\leq 70\%$ ^{Note 3}) | $2.4\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ | | | -60.0 | mA | |
| | IOH2 | Per pin for P20 to P27, P150 to P156 | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | | -0.1 ^{Note 2} | mA |
| | | Total of all pins (When duty $\leq 70\%$ ^{Note 3}) | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | | -1.5 | mA |

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the EV_{DD0} , EV_{DD1} , V_{DD} pins to an output pin.

2. Do not exceed the total current value.

3. Specification under conditions where the duty factor $\leq 70\%$.

The output current value that has changed to the duty factor $> 70\%$ the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to $n\%$).

- Total output current of pins = $(I_{OH} \times 0.7)/(n \times 0.01)$

<Example> Where $n = 80\%$ and $I_{OH} = -10.0\text{ mA}$

$$\text{Total output current of pins} = (-10.0 \times 0.7)/(80 \times 0.01) \cong -8.7\text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$) (2/5)

| Items | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|---|---|--|--|------|------------------------|-----------------------|----|
| Output current, I_{OL} ^{Note 1} | I _{OL1} | Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | | | 8.5 ^{Note 2} | mA | |
| | | Per pin for P60 to P63 | | | 15.0 ^{Note 2} | mA | |
| | | Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (When duty $\leq 70\%$ ^{Note 3}) | $4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ | | | 40.0 | mA |
| | | | $2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$ | | | 15.0 | mA |
| | | | $2.4\text{ V} \leq EV_{DD0} < 2.7\text{ V}$ | | | 9.0 | mA |
| | | Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (When duty $\leq 70\%$ ^{Note 3}) | $4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ | | | 40.0 | mA |
| | | | $2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$ | | | 35.0 | mA |
| | $2.4\text{ V} \leq EV_{DD0} < 2.7\text{ V}$ | | | | 20.0 | mA | |
| | Total of all pins (When duty $\leq 70\%$ ^{Note 3}) | | | | 80.0 | mA | |
| | I _{OL2} | Per pin for P20 to P27, P150 to P156 | | | | 0.4 ^{Note 2} | mA |
| Total of all pins (When duty $\leq 70\%$ ^{Note 3}) | | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | | 5.0 | mA | |

- Notes**
- Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EV_{SS0} , EV_{SS1} and V_{SS} pin.
 - Do not exceed the total current value.
 - Specification under conditions where the duty factor $\leq 70\%$.

The output current value that has changed to the duty factor $> 70\%$ the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = $(I_{OL} \times 0.7)/(n \times 0.01)$

<Example> Where $n = 80\%$ and $I_{OL} = 10.0\text{ mA}$

$$\text{Total output current of pins} = (10.0 \times 0.7)/(80 \times 0.01) \cong 8.7\text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$) (3/5)

| Items | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|---------------------|--|--|--|---------------|-------------|---------------|---|
| Input voltage, high | V_{IH1} | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147 | Normal input buffer | $0.8EV_{DD0}$ | | EV_{DD0} | V |
| | V_{IH2} | P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143 | TTL input buffer $4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ | 2.2 | | EV_{DD0} | V |
| | | | TTL input buffer $3.3\text{ V} \leq EV_{DD0} < 4.0\text{ V}$ | 2.0 | | EV_{DD0} | V |
| | | | TTL input buffer $2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$ | 1.5 | | EV_{DD0} | V |
| | V_{IH3} | P20 to P27, P150 to P156 | | $0.7V_{DD}$ | | V_{DD} | V |
| | V_{IH4} | P60 to P63 | | $0.7EV_{DD0}$ | | 6.0 | V |
| V_{IH5} | P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$ | | $0.8V_{DD}$ | | V_{DD} | V | |
| Input voltage, low | V_{IL1} | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147 | Normal input buffer | 0 | | $0.2EV_{DD0}$ | V |
| | V_{IL2} | P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143 | TTL input buffer $4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ | 0 | | 0.8 | V |
| | | | TTL input buffer $3.3\text{ V} \leq EV_{DD0} < 4.0\text{ V}$ | 0 | | 0.5 | V |
| | | | TTL input buffer $2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$ | 0 | | 0.32 | V |
| | V_{IL3} | P20 to P27, P150 to P156 | | 0 | | $0.3V_{DD}$ | V |
| | V_{IL4} | P60 to P63 | | 0 | | $0.3EV_{DD0}$ | V |
| V_{IL5} | P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$ | | 0 | | $0.2V_{DD}$ | V | |

Caution The maximum value of V_{IH} of pins P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 is EV_{DD0} , even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$) (4/5)

| Items | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|----------------------|------------------|--|---|------------------|------|------|
| Output voltage, high | V _{OH1} | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | $4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OH1} = -3.0\text{ mA}$ | $EV_{DD0} - 0.7$ | | V |
| | | | $2.7\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OH1} = -2.0\text{ mA}$ | $EV_{DD0} - 0.6$ | | V |
| | | | $2.4\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OH1} = -1.5\text{ mA}$ | $EV_{DD0} - 0.5$ | | V |
| | V _{OH2} | P20 to P27, P150 to P156 | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH2} = -100\text{ }\mu\text{A}$ | $V_{DD} - 0.5$ | | V |
| Output voltage, low | V _{OL1} | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | $4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OL1} = 8.5\text{ mA}$ | | 0.7 | V |
| | | | $4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OL1} = 3.0\text{ mA}$ | | 0.6 | V |
| | | | $2.7\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OL1} = 1.5\text{ mA}$ | | 0.4 | V |
| | | | $2.4\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OL1} = 0.6\text{ mA}$ | | 0.4 | V |
| | V _{OL2} | P20 to P27, P150 to P156 | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL2} = 400\text{ }\mu\text{A}$ | | 0.4 | V |
| | V _{OL3} | P60 to P63 | $4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OL3} = 15.0\text{ mA}$ | | 2.0 | V |
| | | | $4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OL3} = 5.0\text{ mA}$ | | 0.4 | V |
| | | | $2.7\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OL3} = 3.0\text{ mA}$ | | 0.4 | V |
| | | | $2.4\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OL3} = 2.0\text{ mA}$ | | 0.4 | V |

Caution P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$) (5/5)

| Items | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | | |
|-----------------------------|-------------------|--|---------------------------------------|------|------|------|---------------|------------|
| Input leakage current, high | I _{LIH1} | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147 | $V_i = EV_{DD0}$ | | | 1 | μA | |
| | I _{LIH2} | P20 to P27, P137, P150 to P156, RESET | $V_i = V_{DD}$ | | | 1 | μA | |
| | I _{LIH3} | P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS) | In input port or external clock input | | | 1 | μA | |
| | | | In resonator connection | | | 10 | μA | |
| Input leakage current, low | I _{LIL1} | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147 | $V_i = EV_{SS0}$ | | | -1 | μA | |
| | I _{LIL2} | P20 to P27, P137, P150 to P156, RESET | $V_i = V_{SS}$ | | | -1 | μA | |
| | I _{LIL3} | P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS) | In input port or external clock input | | | -1 | μA | |
| | | | In resonator connection | | | -10 | μA | |
| On-chip pll-up resistance | R _U | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147 | $V_i = EV_{SS0}$, In input port | | 10 | 20 | 100 | k Ω |

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.3.2 Supply current characteristics

(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products

 $(T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = 0\text{ V})$ (1/2)

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit | |
|--|------------------|--|---|--|---------------------------------------|---------------------------------------|---------------|------|---------------|----|
| Supply current Note 1 | I _{DD1} | Operating mode | HS (high-speed main) mode Note 5 | $f_{\text{IH}} = 32\text{ MHz}$ Note 3 | Basic operation | $\text{V}_{\text{DD}} = 5.0\text{ V}$ | | 2.1 | | mA |
| | | | | | | $\text{V}_{\text{DD}} = 3.0\text{ V}$ | | 2.1 | | mA |
| | | | | Normal operation | $\text{V}_{\text{DD}} = 5.0\text{ V}$ | | 4.6 | 7.5 | mA | |
| | | | | | $\text{V}_{\text{DD}} = 3.0\text{ V}$ | | 4.6 | 7.5 | mA | |
| | | | | $f_{\text{IH}} = 24\text{ MHz}$ Note 3 | Normal operation | $\text{V}_{\text{DD}} = 5.0\text{ V}$ | | 3.7 | 5.8 | mA |
| | | | | | | $\text{V}_{\text{DD}} = 3.0\text{ V}$ | | 3.7 | 5.8 | mA |
| | | | $f_{\text{IH}} = 16\text{ MHz}$ Note 3 | Normal operation | $\text{V}_{\text{DD}} = 5.0\text{ V}$ | | 2.7 | 4.2 | mA | |
| | | | | | $\text{V}_{\text{DD}} = 3.0\text{ V}$ | | 2.7 | 4.2 | mA | |
| | | | HS (high-speed main) mode Note 5 | $f_{\text{MX}} = 20\text{ MHz}$ Note 2, $\text{V}_{\text{DD}} = 5.0\text{ V}$ | Normal operation | Square wave input | | 3.0 | 4.9 | mA |
| | | | | | | Resonator connection | | 3.2 | 5.0 | mA |
| | | | | $f_{\text{MX}} = 20\text{ MHz}$ Note 2, $\text{V}_{\text{DD}} = 3.0\text{ V}$ | Normal operation | Square wave input | | 3.0 | 4.9 | mA |
| | | | | | | Resonator connection | | 3.2 | 5.0 | mA |
| | | $f_{\text{MX}} = 10\text{ MHz}$ Note 2, $\text{V}_{\text{DD}} = 5.0\text{ V}$ | | Normal operation | Square wave input | | 1.9 | 2.9 | mA | |
| | | | | | Resonator connection | | 1.9 | 2.9 | mA | |
| | | $f_{\text{MX}} = 10\text{ MHz}$ Note 2, $\text{V}_{\text{DD}} = 3.0\text{ V}$ | | Normal operation | Square wave input | | 1.9 | 2.9 | mA | |
| | | | | | Resonator connection | | 1.9 | 2.9 | mA | |
| | | Subsystem clock operation | $f_{\text{SUB}} = 32.768\text{ kHz}$ Note 4 $T_A = -40^\circ\text{C}$ | Normal operation | Square wave input | | 4.1 | 4.9 | μA | |
| | | | | | Resonator connection | | 4.2 | 5.0 | μA | |
| | | | $f_{\text{SUB}} = 32.768\text{ kHz}$ Note 4 $T_A = +25^\circ\text{C}$ | Normal operation | Square wave input | | 4.1 | 4.9 | μA | |
| | | | | | Resonator connection | | 4.2 | 5.0 | μA | |
| | | | $f_{\text{SUB}} = 32.768\text{ kHz}$ Note 4 $T_A = +50^\circ\text{C}$ | Normal operation | Square wave input | | 4.2 | 5.5 | μA | |
| Resonator connection | | | | | 4.3 | 5.6 | μA | | | |
| $f_{\text{SUB}} = 32.768\text{ kHz}$ Note 4 $T_A = +70^\circ\text{C}$ | Normal operation | | Square wave input | | 4.3 | 6.3 | μA | | | |
| | | | Resonator connection | | 4.4 | 6.4 | μA | | | |
| $f_{\text{SUB}} = 32.768\text{ kHz}$ Note 4 $T_A = +85^\circ\text{C}$ | Normal operation | | Square wave input | | 4.6 | 7.7 | μA | | | |
| | | | Resonator connection | | 4.7 | 7.8 | μA | | | |
| $f_{\text{SUB}} = 32.768\text{ kHz}$ Note 4 $T_A = +105^\circ\text{C}$ | Normal operation | | Square wave input | | 6.9 | 19.7 | μA | | | |
| | | | Resonator connection | | 7.0 | 19.8 | μA | | | |

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD} and EV_{DD0} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD0} or V_{SS} , EV_{SS0} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. When high-speed on-chip oscillator and subsystem clock are stopped.
 3. When high-speed system clock and subsystem clock are stopped.
 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$

- Remarks**
1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH} : High-speed on-chip oscillator clock frequency
 3. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation, temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products

 $(T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD0} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = 0\text{ V}$) (2/2)

| Parameter | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit | |
|--|----------------------------|---|-------------------------------------|--|-------------------------|------|-------|------|----|
| Supply current Note 1 | I _{DD2} Note 2 | HALT mode | HS (high-speed main) mode Note 7 | f _{IH} = 32 MHz Note 4 | V _{DD} = 5.0 V | | 0.54 | 2.90 | mA |
| | | | | | V _{DD} = 3.0 V | | 0.54 | 2.90 | mA |
| | | | | f _{IH} = 24 MHz Note 4 | V _{DD} = 5.0 V | | 0.44 | 2.30 | mA |
| | | | | | V _{DD} = 3.0 V | | 0.44 | 2.30 | mA |
| | | | | f _{IH} = 16 MHz Note 4 | V _{DD} = 5.0 V | | 0.40 | 1.70 | mA |
| | | | | | V _{DD} = 3.0 V | | 0.40 | 1.70 | mA |
| | | | HS (high-speed main) mode Note 7 | f _{MX} = 20 MHz Note 3, V _{DD} = 5.0 V | Square wave input | | 0.28 | 1.90 | mA |
| | | | | | Resonator connection | | 0.45 | 2.00 | mA |
| | | | | f _{MX} = 20 MHz Note 3, V _{DD} = 3.0 V | Square wave input | | 0.28 | 1.90 | mA |
| | | | | | Resonator connection | | 0.45 | 2.00 | mA |
| | | | | f _{MX} = 10 MHz Note 3, V _{DD} = 5.0 V | Square wave input | | 0.19 | 1.02 | mA |
| | | | | | Resonator connection | | 0.26 | 1.10 | mA |
| | | | | f _{MX} = 10 MHz Note 3, V _{DD} = 3.0 V | Square wave input | | 0.19 | 1.02 | mA |
| | | | | | Resonator connection | | 0.26 | 1.10 | mA |
| | Subsystem clock operation | f _{SUB} = 32.768 kHz Note 5 T _A = -40°C | Square wave input | | 0.25 | 0.57 | μA | | |
| | | | Resonator connection | | 0.44 | 0.76 | μA | | |
| | | f _{SUB} = 32.768 kHz Note 5 T _A = +25°C | Square wave input | | 0.30 | 0.57 | μA | | |
| | | | Resonator connection | | 0.49 | 0.76 | μA | | |
| | | f _{SUB} = 32.768 kHz Note 5 T _A = +50°C | Square wave input | | 0.37 | 1.17 | μA | | |
| | | | Resonator connection | | 0.56 | 1.36 | μA | | |
| | | f _{SUB} = 32.768 kHz Note 5 T _A = +70°C | Square wave input | | 0.53 | 1.97 | μA | | |
| | | | Resonator connection | | 0.72 | 2.16 | μA | | |
| | | f _{SUB} = 32.768 kHz Note 5 T _A = +85°C | Square wave input | | 0.82 | 3.37 | μA | | |
| Resonator connection | | | | 1.01 | 3.56 | μA | | | |
| f _{SUB} = 32.768 kHz Note 5 T _A = +105°C | Square wave input | | 3.01 | 15.37 | μA | | | | |
| | Resonator connection | | 3.20 | 15.56 | μA | | | | |
| I _{DD3} Note 6 | STOP mode Note 8 | T _A = -40°C | | | | 0.18 | 0.50 | μA | |
| | | T _A = +25°C | | | | 0.23 | 0.50 | μA | |
| | | T _A = +50°C | | | | 0.30 | 1.10 | μA | |
| | | T _A = +70°C | | | | 0.46 | 1.90 | μA | |
| | | T _A = +85°C | | | | 0.75 | 3.30 | μA | |
| | | T _A = +105°C | | | | 2.94 | 15.30 | μA | |

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD} and EV_{DD0} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD0} or V_{SS} , EV_{SS0} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. During HALT instruction execution by flash memory.
 3. When high-speed on-chip oscillator and subsystem clock are stopped.
 4. When high-speed system clock and subsystem clock are stopped.
 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When $RTCLPC = 1$ and setting ultra-low current consumption ($AMPHS1 = 1$). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
 8. Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks**
1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH} : High-speed on-chip oscillator clock frequency
 3. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

 $(T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$) (1/2)

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit | | |
|---|------------------|--|--|-------------------------------------|--|-------------------------|----------------------|------|---------------|-----|----|
| Supply current Note 1 | I _{DD1} | Operating mode | HS (high-speed main) mode Note 5 | $f_{IH} = 32\text{ MHz}$ Note 3 | Basic operation | $V_{DD} = 5.0\text{ V}$ | | 2.3 | | mA | |
| | | | | | | $V_{DD} = 3.0\text{ V}$ | | 2.3 | | mA | |
| | | | | Normal operation | $V_{DD} = 5.0\text{ V}$ | | 5.2 | 9.2 | mA | | |
| | | | | | $V_{DD} = 3.0\text{ V}$ | | 5.2 | 9.2 | mA | | |
| | | | | $f_{IH} = 24\text{ MHz}$ Note 3 | Normal operation | $V_{DD} = 5.0\text{ V}$ | | 4.1 | 7.0 | mA | |
| | | | | | | $V_{DD} = 3.0\text{ V}$ | | 4.1 | 7.0 | mA | |
| | | | $f_{IH} = 16\text{ MHz}$ Note 3 | Normal operation | $V_{DD} = 5.0\text{ V}$ | | 3.0 | 5.0 | mA | | |
| | | | | | $V_{DD} = 3.0\text{ V}$ | | 3.0 | 5.0 | mA | | |
| | | | | HS (high-speed main) mode Note 5 | $f_{MX} = 20\text{ MHz}$ Note 2, $V_{DD} = 5.0\text{ V}$ | Normal operation | Square wave input | | 3.4 | 5.9 | mA |
| | | | | | | | Resonator connection | | 3.6 | 6.0 | mA |
| | | $f_{MX} = 20\text{ MHz}$ Note 2, $V_{DD} = 3.0\text{ V}$ | Normal operation | | Square wave input | | 3.4 | 5.9 | mA | | |
| | | | | | Resonator connection | | 3.6 | 6.0 | mA | | |
| | | $f_{MX} = 10\text{ MHz}$ Note 2, $V_{DD} = 5.0\text{ V}$ | Normal operation | Square wave input | | 2.1 | 3.5 | mA | | | |
| | | | | Resonator connection | | 2.1 | 3.5 | mA | | | |
| | | Subsystem clock operation | $f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = -40^\circ\text{C}$ | Normal operation | Square wave input | | 4.8 | 5.9 | μA | | |
| | | | | | Resonator connection | | 4.9 | 6.0 | μA | | |
| | | | $f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = +25^\circ\text{C}$ | Normal operation | Square wave input | | 4.9 | 5.9 | μA | | |
| | | | | | Resonator connection | | 5.0 | 6.0 | μA | | |
| | | | $f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = +50^\circ\text{C}$ | Normal operation | Square wave input | | 5.0 | 7.6 | μA | | |
| | | | | | Resonator connection | | 5.1 | 7.7 | μA | | |
| $f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = +70^\circ\text{C}$ | Normal operation | | Square wave input | | 5.2 | 9.3 | μA | | | | |
| | | | Resonator connection | | 5.3 | 9.4 | μA | | | | |
| $f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = +85^\circ\text{C}$ | Normal operation | Square wave input | | 5.7 | 13.3 | μA | | | | | |
| | | Resonator connection | | 5.8 | 13.4 | μA | | | | | |
| $f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = +105^\circ\text{C}$ | Normal operation | Square wave input | | 10.0 | 46.0 | μA | | | | | |
| | | Resonator connection | | 10.0 | 46.0 | μA | | | | | |

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD} , EV_{DD0} , and EV_{DD1} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD0} , and EV_{DD1} , or V_{SS} , EV_{SS0} , and EV_{SS1} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. When high-speed on-chip oscillator and subsystem clock are stopped.
 3. When high-speed system clock and subsystem clock are stopped.
 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When $AMPHS1 = 1$ (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.
 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$

- Remarks**
1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH} : High-speed on-chip oscillator clock frequency
 3. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation, temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$) (2/2)**

| Parameter | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit | |
|--|---------------------------|---|-------------------------------------|---|-------------------------|---------------|---------------|---------------|----|
| Supply current Note 1 | I_{DD2} Note 2 | HALT mode | HS (high-speed main) mode Note 7 | $f_{IH} = 32\text{ MHz}$ Note 4 | $V_{DD} = 5.0\text{ V}$ | | 0.62 | 3.40 | mA |
| | | | | | $V_{DD} = 3.0\text{ V}$ | | 0.62 | 3.40 | mA |
| | | | | $f_{IH} = 24\text{ MHz}$ Note 4 | $V_{DD} = 5.0\text{ V}$ | | 0.50 | 2.70 | mA |
| | | | | | $V_{DD} = 3.0\text{ V}$ | | 0.50 | 2.70 | mA |
| | | | | $f_{IH} = 16\text{ MHz}$ Note 4 | $V_{DD} = 5.0\text{ V}$ | | 0.44 | 1.90 | mA |
| | | | | | $V_{DD} = 3.0\text{ V}$ | | 0.44 | 1.90 | mA |
| | | | HS (high-speed main) mode Note 7 | $f_{MX} = 20\text{ MHz}$ Note 3, $V_{DD} = 5.0\text{ V}$ | Square wave input | | 0.31 | 2.10 | mA |
| | | | | | Resonator connection | | 0.48 | 2.20 | mA |
| | | | | $f_{MX} = 20\text{ MHz}$ Note 3, $V_{DD} = 3.0\text{ V}$ | Square wave input | | 0.31 | 2.10 | mA |
| | | | | | Resonator connection | | 0.48 | 2.20 | mA |
| | | | | $f_{MX} = 10\text{ MHz}$ Note 3, $V_{DD} = 5.0\text{ V}$ | Square wave input | | 0.21 | 1.10 | mA |
| | | | | | Resonator connection | | 0.28 | 1.20 | mA |
| | | | | $f_{MX} = 10\text{ MHz}$ Note 3, $V_{DD} = 3.0\text{ V}$ | Square wave input | | 0.21 | 1.10 | mA |
| | | | | | Resonator connection | | 0.28 | 1.20 | mA |
| | Subsystem clock operation | $f_{SUB} = 32.768\text{ kHz}$ Note 5 $T_A = -40^\circ\text{C}$ | Square wave input | | 0.28 | 0.61 | μA | | |
| | | | Resonator connection | | 0.47 | 0.80 | μA | | |
| | | $f_{SUB} = 32.768\text{ kHz}$ Note 5 $T_A = +25^\circ\text{C}$ | Square wave input | | 0.34 | 0.61 | μA | | |
| | | | Resonator connection | | 0.53 | 0.80 | μA | | |
| | | $f_{SUB} = 32.768\text{ kHz}$ Note 5 $T_A = +50^\circ\text{C}$ | Square wave input | | 0.41 | 2.30 | μA | | |
| | | | Resonator connection | | 0.60 | 2.49 | μA | | |
| $f_{SUB} = 32.768\text{ kHz}$ Note 5 $T_A = +70^\circ\text{C}$ | | Square wave input | | 0.64 | 4.03 | μA | | | |
| | | Resonator connection | | 0.83 | 4.22 | μA | | | |
| $f_{SUB} = 32.768\text{ kHz}$ Note 5 $T_A = +85^\circ\text{C}$ | | Square wave input | | 1.09 | 8.04 | μA | | | |
| | | Resonator connection | | 1.28 | 8.23 | μA | | | |
| $f_{SUB} = 32.768\text{ kHz}$ Note 5 $T_A = +105^\circ\text{C}$ | Square wave input | | 5.50 | 41.00 | μA | | | | |
| | Resonator connection | | 5.50 | 41.00 | μA | | | | |
| I_{DD3} Note 6 | STOP mode Note 8 | $T_A = -40^\circ\text{C}$ | | | | 0.19 | 0.52 | μA | |
| | | $T_A = +25^\circ\text{C}$ | | | | 0.25 | 0.52 | μA | |
| | | $T_A = +50^\circ\text{C}$ | | | | 0.32 | 2.21 | μA | |
| | | $T_A = +70^\circ\text{C}$ | | | | 0.55 | 3.94 | μA | |
| | | $T_A = +85^\circ\text{C}$ | | | | 1.00 | 7.95 | μA | |
| | | $T_A = +105^\circ\text{C}$ | | | | 5.00 | 40.00 | μA | |

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD} , EV_{DD0} , and EV_{DD1} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD0} , and EV_{DD1} , or V_{SS} , EV_{SS0} , and EV_{SS1} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. During HALT instruction execution by flash memory.
 3. When high-speed on-chip oscillator and subsystem clock are stopped.
 4. When high-speed system clock and subsystem clock are stopped.
 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When $RTCLPC = 1$ and setting ultra-low current consumption ($AMPHS1 = 1$). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
 8. Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks**
1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH} : High-speed on-chip oscillator clock frequency
 3. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

(3) Peripheral Functions (Common to all products)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|--|-----------------------------------|----------------------------------|--|------|------|-------|---------------|
| Low-speed on-chip oscillator operating current | I_{FIL} Note 1 | | | | 0.20 | | μA |
| RTC operating current | I_{RTC} Notes 1, 2, 3 | | | | 0.02 | | μA |
| 12-bit interval timer operating current | I_{IT} Notes 1, 2, 4 | | | | 0.02 | | μA |
| Watchdog timer operating current | I_{WDT} Notes 1, 2, 5 | $f_{\text{IL}} = 15\text{ kHz}$ | | | 0.22 | | μA |
| A/D converter operating current | I_{ADC} Notes 1, 6 | When conversion at maximum speed | Normal mode, $\text{AV}_{\text{REFP}} = \text{V}_{\text{DD}} = 5.0\text{ V}$ | | 1.3 | 1.7 | mA |
| | | | Low voltage mode, $\text{AV}_{\text{REFP}} = \text{V}_{\text{DD}} = 3.0\text{ V}$ | | 0.5 | 0.7 | mA |
| A/D converter reference voltage current | I_{ADREF} Note 1 | | | | 75.0 | | μA |
| Temperature sensor operating current | I_{TMS} Note 1 | | | | 75.0 | | μA |
| LVD operating current | I_{LVD} Notes 1, 7 | | | | 0.08 | | μA |
| Self programming operating current | I_{FSP} Notes 1, 9 | | | | 2.50 | 12.20 | mA |
| BGO operating current | I_{BGO} Notes 1, 8 | | | | 2.50 | 12.20 | mA |
| SNOOZE operating current | I_{SNOZ} Note 1 | ADC operation | The mode is performed ^{Note 10} | | 0.50 | 1.10 | mA |
| | | | The A/D conversion operations are performed, Low voltage mode, $\text{AV}_{\text{REFP}} = \text{V}_{\text{DD}} = 3.0\text{ V}$ | | 1.20 | 2.04 | mA |
| | | CSI/UART operation | | | 0.70 | 1.54 | mA |

Notes 1. Current flowing to the V_{DD} .

- When high speed on-chip oscillator and high-speed system clock are stopped.
- Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either $I_{\text{DD}1}$ or $I_{\text{DD}2}$, and I_{RTC} , when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. $I_{\text{DD}2}$ subsystem clock operation includes the operational current of the real-time clock.
- Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either $I_{\text{DD}1}$ or $I_{\text{DD}2}$, and I_{IT} , when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.
- Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 is the sum of $I_{\text{DD}1}$, $I_{\text{DD}2}$ or $I_{\text{DD}3}$ and I_{WDT} when the watchdog timer operates.
- Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of $I_{\text{DD}1}$ or $I_{\text{DD}2}$ and I_{ADC} when the A/D converter is in operation.

- Notes**
7. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of I_{DD1} , I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit is in operation.
 8. Current flowing only during data flash rewrite.
 9. Current flowing only during self programming.
 10. For shift time to the SNOOZE mode, see **18.3.3 SNOOZE mode** in the RL78/G13 User's Manual.

- Remarks**
1. f_{IL} : Low-speed on-chip oscillator clock frequency
 2. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 3. f_{CLK} : CPU/peripheral hardware clock frequency
 4. Temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

3.4 AC Characteristics

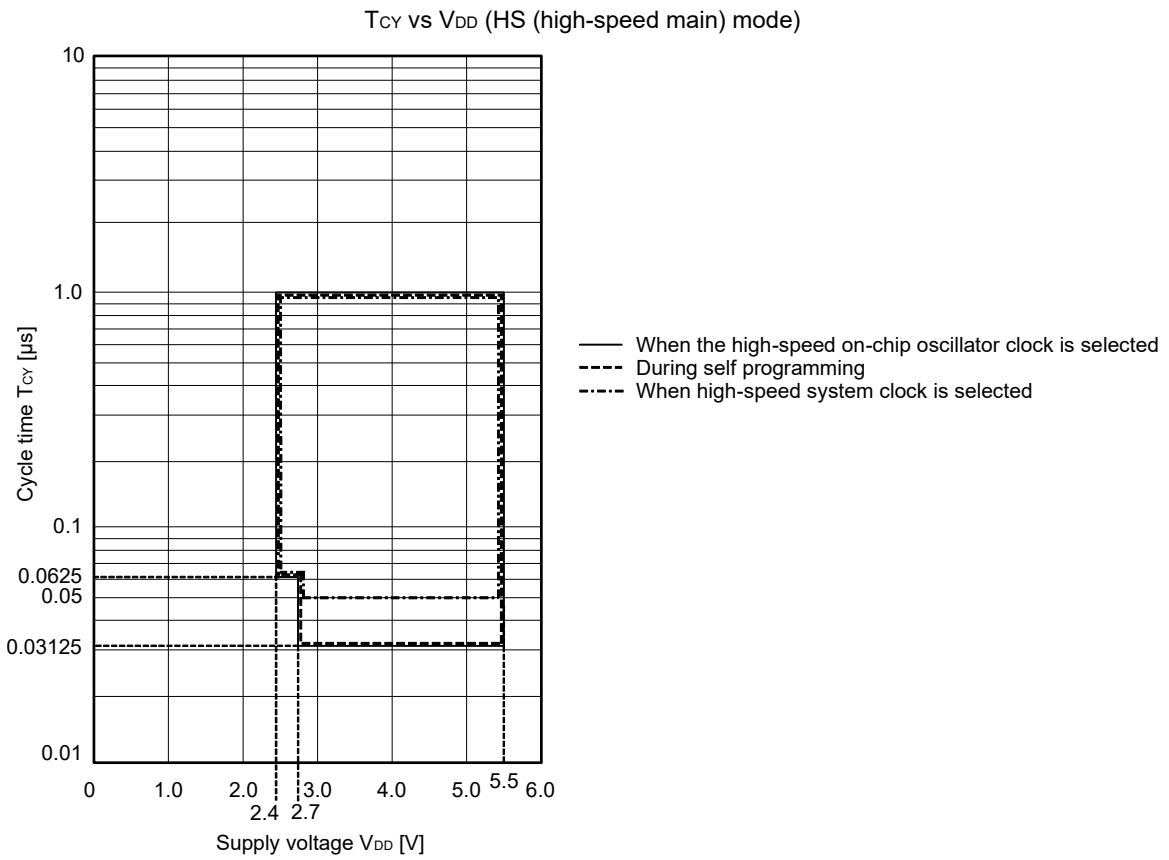
($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit | |
|--|---|--|--|--|---------|---------------|--------------------|---------------|
| Instruction cycle (minimum instruction execution time) | T_{CY} | Main system clock (f_{MAIN}) operation | HS (high-speed main) mode | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 0.03125 | | 1 | μs |
| | | | | $2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$ | 0.0625 | | 1 | μs |
| | | Subsystem clock (f_{SUB}) operation | | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 28.5 | 30.5 | 31.3 | μs |
| | | In the self programming mode | HS (high-speed main) mode | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 0.03125 | | 1 | μs |
| | $2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$ | | 0.0625 | | 1 | μs | | |
| External system clock frequency | f_{EX} | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | 1.0 | | 20.0 | MHz | |
| | | $2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$ | | 1.0 | | 16.0 | MHz | |
| | f_{EXS} | | | 32 | | 35 | kHz | |
| External system clock input high-level width, low-level width | t_{EXH} , t_{EXL} | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | 24 | | | ns | |
| | | $2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$ | | 30 | | | ns | |
| | t_{EXHS} , t_{EXLS} | | | 13.7 | | | μs | |
| TI00 to TI07, TI10 to TI17 input high-level width, low-level width | t_{TIH} , t_{TIL} | | | $1/f_{MCK}+10$ | | | ns ^{Note} | |
| TO00 to TO07, TO10 to TO17 output frequency | f_{TO} | HS (high-speed main) mode | $4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ | | | 16 | MHz | |
| | | | $2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$ | | | 8 | MHz | |
| | | | $2.4\text{ V} \leq EV_{DD0} < 2.7\text{ V}$ | | | 4 | MHz | |
| PCLBUZ0, PCLBUZ1 output frequency | f_{PCL} | HS (high-speed main) mode | $4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ | | | 16 | MHz | |
| | | | $2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$ | | | 8 | MHz | |
| | | | $2.4\text{ V} \leq EV_{DD0} < 2.7\text{ V}$ | | | 4 | MHz | |
| Interrupt input high-level width, low-level width | t_{INTH} , t_{INTL} | INTP0 | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 1 | | | μs | |
| | | INTP1 to INTP11 | $2.4\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ | 1 | | | μs | |
| Key interrupt input low-level width | t_{KR} | KR0 to KR7 | $2.4\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ | 250 | | | ns | |
| RESET low-level width | t_{RSL} | | | 10 | | | μs | |

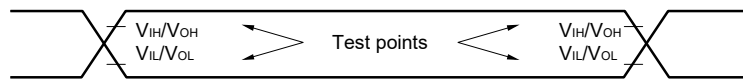
Note The following conditions are required for low voltage interface when $EV_{DD0} < V_{DD}$
 $2.4\text{ V} \leq EV_{DD0} < 2.7\text{ V}$: MIN. 125 ns

Remark f_{MCK} : Timer array unit operation clock frequency
 (Operation clock to be set by the CKSmn0, CKSmn1 bits of timer mode register mn (TMRmn).
 m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7))

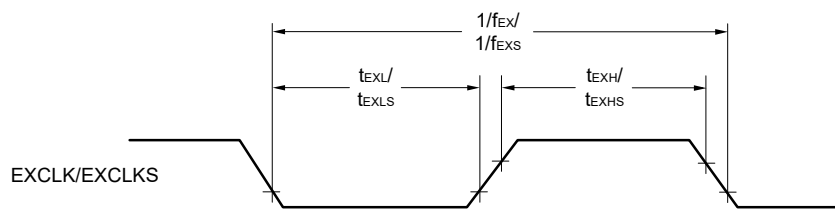
Minimum Instruction Execution Time during Main System Clock Operation



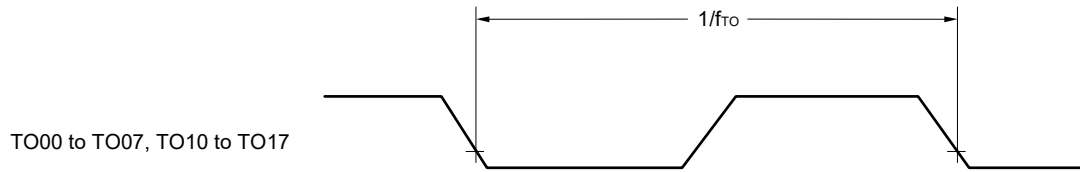
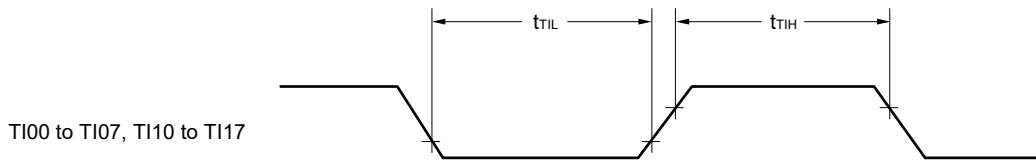
AC Timing Test Points



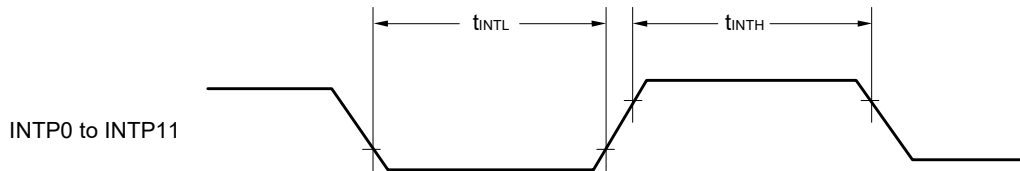
External System Clock Timing



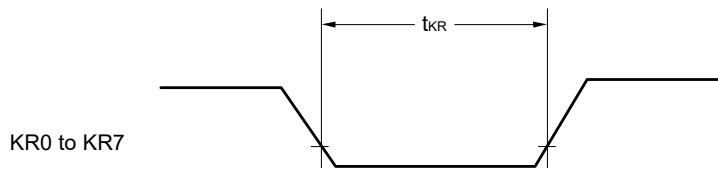
TI/TO Timing



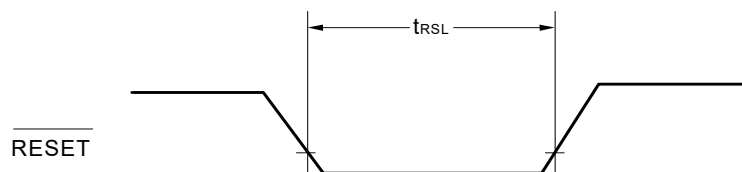
Interrupt Request Input Timing



Key Interrupt Input Timing

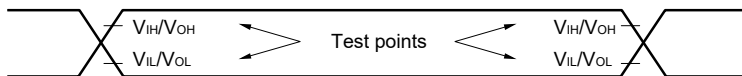


RESET Input Timing



3.5 Peripheral Functions Characteristics

AC Timing Test Points



3.5.1 Serial array unit

(1) During communication at same potential (UART mode)

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq E_{VDD0} = E_{VDD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = E_{VSS0} = E_{VSS1} = 0\text{ V}$)

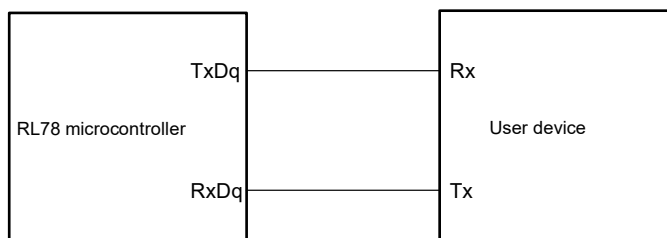
| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---------------------------------|--------|---|---------------------------|--------------------------------|------|
| | | | MIN. | MAX. | |
| Transfer rate ^{Note 1} | | Theoretical value of the maximum transfer rate $f_{CLK} = 32\text{ MHz}$, $f_{MCK} = f_{CLK}$ | | $f_{MCK}/12$ ^{Note 2} | bps |
| | | | | 2.6 | Mbps |

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

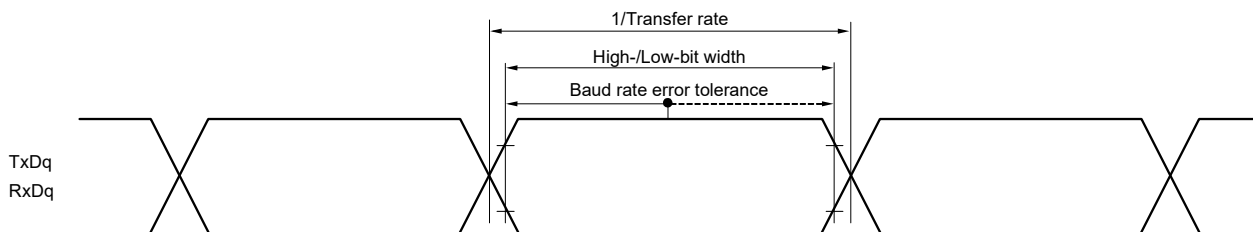
2. The following conditions are required for low voltage interface when $E_{VDD0} < V_{DD}$.
 $2.4\text{ V} \leq E_{VDD0} < 2.7\text{ V}$: MAX. 1.3 Mbps

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Remarks 1. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

2. f_{MCK} : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit | |
|---|--|--|--|------|------|----|
| | | | MIN. | MAX. | | |
| SCKp cycle time | $t_{\text{CY}1}$ | $t_{\text{CY}1} \geq 4/f_{\text{CLK}}$ | $2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | 250 | | ns |
| | | | $2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | 500 | | ns |
| SCKp high-/low-level width | $t_{\text{KH}1}$, $t_{\text{KL}1}$ | $4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | $t_{\text{CY}1}/2 - 24$ | | | ns |
| | | $2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | $t_{\text{CY}1}/2 - 36$ | | | ns |
| | | $2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | $t_{\text{CY}1}/2 - 76$ | | | ns |
| Slp setup time (to SCKp \uparrow) ^{Note 1} | $t_{\text{SIK}1}$ | $4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | 66 | | | ns |
| | | $2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | 66 | | | ns |
| | | $2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | 113 | | | ns |
| Slp hold time (from SCKp \uparrow) ^{Note 2} | $t_{\text{KSI}1}$ | | 38 | | | ns |
| Delay time from SCKp \downarrow to SOp output ^{Note 3} | $t_{\text{KSO}1}$ | $C = 30\text{ pF}$ ^{Note 4} | | 50 | | ns |

- Notes**
1. When $\text{DAP}_{\text{mn}} = 0$ and $\text{CKP}_{\text{mn}} = 0$, or $\text{DAP}_{\text{mn}} = 1$ and $\text{CKP}_{\text{mn}} = 1$. The Slp setup time becomes “to SCKp \downarrow ” when $\text{DAP}_{\text{mn}} = 0$ and $\text{CKP}_{\text{mn}} = 1$, or $\text{DAP}_{\text{mn}} = 1$ and $\text{CKP}_{\text{mn}} = 0$.
 2. When $\text{DAP}_{\text{mn}} = 0$ and $\text{CKP}_{\text{mn}} = 0$, or $\text{DAP}_{\text{mn}} = 1$ and $\text{CKP}_{\text{mn}} = 1$. The Slp hold time becomes “from SCKp \downarrow ” when $\text{DAP}_{\text{mn}} = 0$ and $\text{CKP}_{\text{mn}} = 1$, or $\text{DAP}_{\text{mn}} = 1$ and $\text{CKP}_{\text{mn}} = 0$.
 3. When $\text{DAP}_{\text{mn}} = 0$ and $\text{CKP}_{\text{mn}} = 0$, or $\text{DAP}_{\text{mn}} = 1$ and $\text{CKP}_{\text{mn}} = 1$. The delay time to SOp output becomes “from SCKp \uparrow ” when $\text{DAP}_{\text{mn}} = 0$ and $\text{CKP}_{\text{mn}} = 1$, or $\text{DAP}_{\text{mn}} = 1$ and $\text{CKP}_{\text{mn}} = 0$.
 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 1, 4, 5, 8, 14)
 2. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

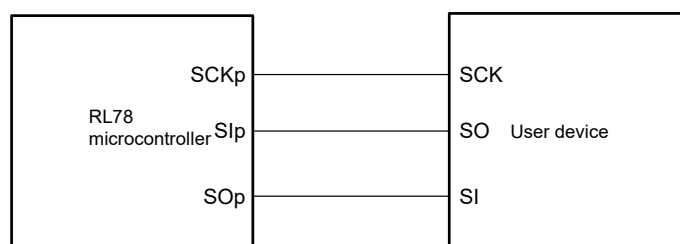
(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | Unit |
|---|--|--|--|---------------------------|------------------------|------|
| | | | | MIN. | MAX. | |
| SCKp cycle time ^{Note 5} | $t_{\text{KCY}2}$ | $4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | $20\text{ MHz} < f_{\text{MCK}}$ | $16/f_{\text{MCK}}$ | | ns |
| | | | $f_{\text{MCK}} \leq 20\text{ MHz}$ | $12/f_{\text{MCK}}$ | | ns |
| | | $2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | $16\text{ MHz} < f_{\text{MCK}}$ | $16/f_{\text{MCK}}$ | | ns |
| | | | $f_{\text{MCK}} \leq 16\text{ MHz}$ | $12/f_{\text{MCK}}$ | | ns |
| | | $2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | | $16/f_{\text{MCK}}$ | | ns |
| | $12/f_{\text{MCK}}$ and 1000 | | | ns | | |
| SCKp high-/low-level width | $t_{\text{KH}2}$, $t_{\text{KL}2}$ | $4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | | $t_{\text{KCY}2}/2 - 14$ | | ns |
| | | $2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | | $t_{\text{KCY}2}/2 - 16$ | | ns |
| | | $2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | | $t_{\text{KCY}2}/2 - 36$ | | ns |
| Slp setup time (to SCKp \uparrow) ^{Note 1} | $t_{\text{SIK}2}$ | $2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | | $1/f_{\text{MCK}}+40$ | | ns |
| | | $2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | | $1/f_{\text{MCK}}+60$ | | ns |
| Slp hold time (from SCKp \uparrow) ^{Note 2} | $t_{\text{KSI}2}$ | $2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | | $1/f_{\text{MCK}}+62$ | | ns |
| Delay time from SCKp \downarrow to SOp output ^{Note 3} | $t_{\text{KSO}2}$ | $C = 30\text{ pF}$ ^{Note 4} | $2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | | $2/f_{\text{MCK}}+66$ | ns |
| | | | $2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ | | $2/f_{\text{MCK}}+113$ | ns |

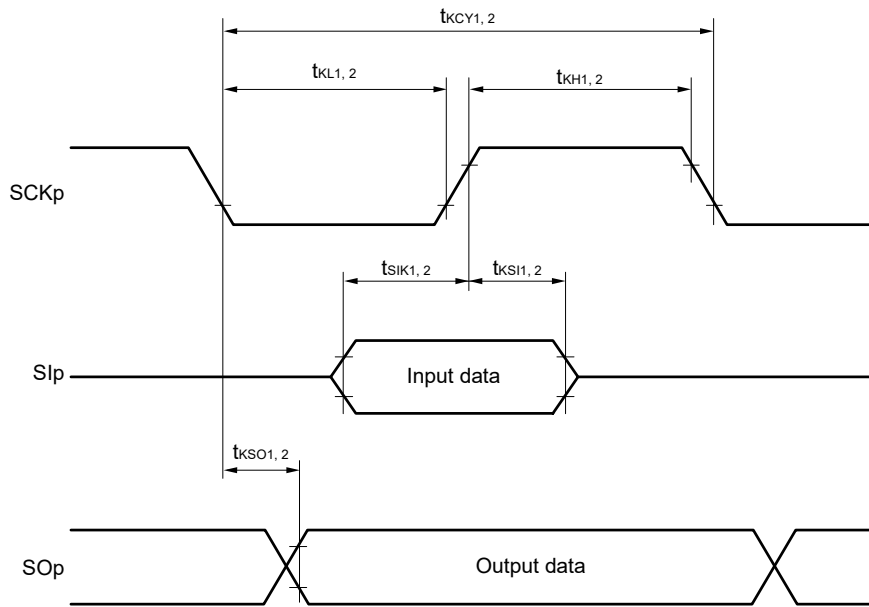
- Notes**
1. When $\text{DAP}_{\text{mn}} = 0$ and $\text{CKP}_{\text{mn}} = 0$, or $\text{DAP}_{\text{mn}} = 1$ and $\text{CKP}_{\text{mn}} = 1$. The Slp setup time becomes “to SCKp \downarrow ” when $\text{DAP}_{\text{mn}} = 0$ and $\text{CKP}_{\text{mn}} = 1$, or $\text{DAP}_{\text{mn}} = 1$ and $\text{CKP}_{\text{mn}} = 0$.
 2. When $\text{DAP}_{\text{mn}} = 0$ and $\text{CKP}_{\text{mn}} = 0$, or $\text{DAP}_{\text{mn}} = 1$ and $\text{CKP}_{\text{mn}} = 1$. The Slp hold time becomes “from SCKp \downarrow ” when $\text{DAP}_{\text{mn}} = 0$ and $\text{CKP}_{\text{mn}} = 1$, or $\text{DAP}_{\text{mn}} = 1$ and $\text{CKP}_{\text{mn}} = 0$.
 3. When $\text{DAP}_{\text{mn}} = 0$ and $\text{CKP}_{\text{mn}} = 0$, or $\text{DAP}_{\text{mn}} = 1$ and $\text{CKP}_{\text{mn}} = 1$. The delay time to SOp output becomes “from SCKp \uparrow ” when $\text{DAP}_{\text{mn}} = 0$ and $\text{CKP}_{\text{mn}} = 1$, or $\text{DAP}_{\text{mn}} = 1$ and $\text{CKP}_{\text{mn}} = 0$.
 4. C is the load capacitance of the SOp output lines.
 5. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

Caution Select the normal input buffer for the Slp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

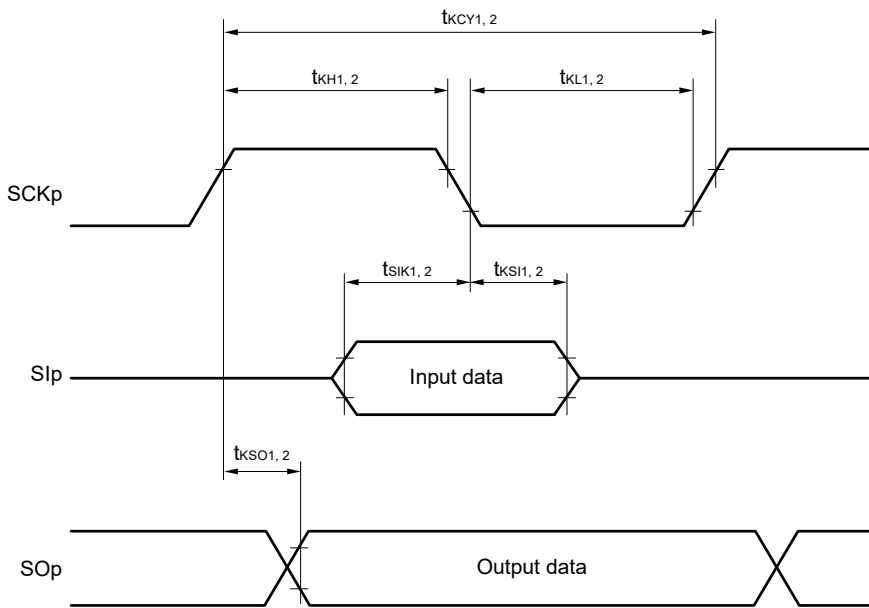
- Remarks**
1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 4, 5, 8, 14)
 2. f_{MCK} : Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

CSI mode connection diagram (during communication at same potential)

CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



- Remarks 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)
2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

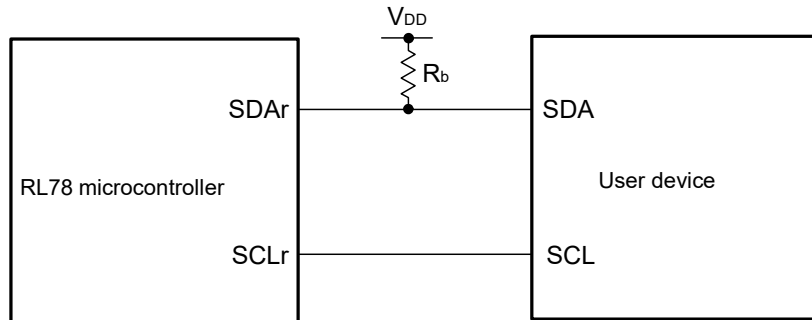
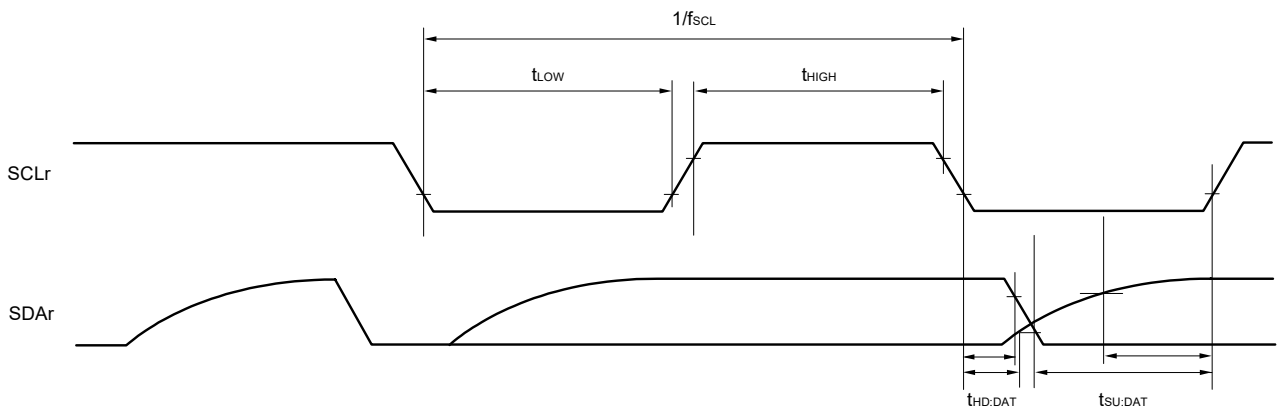
(4) During communication at same potential (simplified I²C mode)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|-------------------------------|---------------------|---|---|----------------------|------|
| | | | MIN. | MAX. | |
| SCLr clock frequency | f _{SCL} | 2.7 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ | | 400 ^{Note1} | kHz |
| | | 2.4 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ | | 100 ^{Note1} | kHz |
| Hold time when SCLr = "L" | t _{LOW} | 2.7 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ | 1200 | | ns |
| | | 2.4 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ | 4600 | | ns |
| Hold time when SCLr = "H" | t _{HIGH} | 2.7 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ | 1200 | | ns |
| | | 2.4 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ | 4600 | | ns |
| Data setup time (reception) | t _{SU:DAT} | 2.7 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ | 1/f _{MCK} + 220 ^{Note2} | | ns |
| | | 2.4 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ | 1/f _{MCK} + 580 ^{Note2} | | ns |
| Data hold time (transmission) | t _{HD:DAT} | 2.7 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ | 0 | 770 | ns |
| | | 2.4 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ | 0 | 1420 | ns |

Notes 1. The value must also be equal to or less than f_{MCK}/4.2. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

(Remarks are listed on the next page.)

Simplified I²C mode connection diagram (during communication at same potential)**Simplified I²C mode serial transfer timing (during communication at same potential)**

- Remarks**
- $R_b[\Omega]$: Communication line (SDAr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance
 - r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 4, 5, 8, 14),
h: POM number (g = 0, 1, 4, 5, 7 to 9, 14)
 - f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit | |
|---------------|--------|------------|--|------|---|------|
| | | | MIN. | MAX. | | |
| Transfer rate | | Reception | $4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$ | | $f_{\text{MCK}}/12$ ^{Note 1} | bps |
| | | | Theoretical value of the maximum transfer rate $f_{\text{CLK}} = 32\text{ MHz}$, $f_{\text{MCK}} = f_{\text{CLK}}$ | | 2.6 | Mbps |
| | | | $2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$ | | $f_{\text{MCK}}/12$ ^{Note 1} | bps |
| | | | Theoretical value of the maximum transfer rate $f_{\text{CLK}} = 32\text{ MHz}$, $f_{\text{MCK}} = f_{\text{CLK}}$ | | 2.6 | Mbps |
| | | | $2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ | | $f_{\text{MCK}}/12$ ^{Notes 1,2} | bps |
| | | | Theoretical value of the maximum transfer rate $f_{\text{CLK}} = 32\text{ MHz}$, $f_{\text{MCK}} = f_{\text{CLK}}$ | | 2.6 | Mbps |

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.**2.** The following conditions are required for low voltage interface when $\text{EV}_{\text{DD0}} < \text{V}_{\text{DD}}$. $2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 2.7\text{ V}$: MAX. 1.3 Mbps

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/ EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

Remarks 1. $\text{V}_b[\text{V}]$: Communication line voltage**2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)**3.** f_{MCK} : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

4. UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)**(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit | |
|---------------|--------|--------------|---|------|------------------------|------|
| | | | MIN. | MAX. | | |
| Transfer rate | | Transmission | 4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V | | Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 1.4 kΩ, V _b = 2.7 V | | 2.6 ^{Note 2} | Mbps |
| | | | 2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V | | Note 3 | bps |
| | | | Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 2.7 kΩ, V _b = 2.3 V | | 1.2 ^{Note 4} | Mbps |
| | | | 2.4 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V | | Note 5 | bps |
| | | | Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 5.5 kΩ, V _b = 1.6 V | | 0.43 ^{Note 6} | Mbps |

Notes 1. The smaller maximum transfer rate derived by using f_{MCK}/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ EV_{DD0} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{\left(\frac{1}{\text{Transfer rate}}\right) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

2. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

3. The smaller maximum transfer rate derived by using f_{MCK}/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ EV_{DD0} < 4.0 V and 2.4 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{\left(\frac{1}{\text{Transfer rate}}\right) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

Notes 5. The smaller maximum transfer rate derived by using $f_{\text{MCK}}/12$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$ and $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

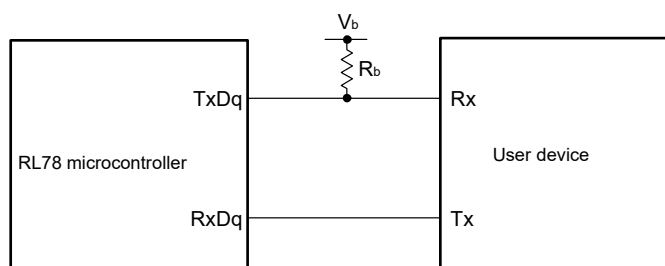
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

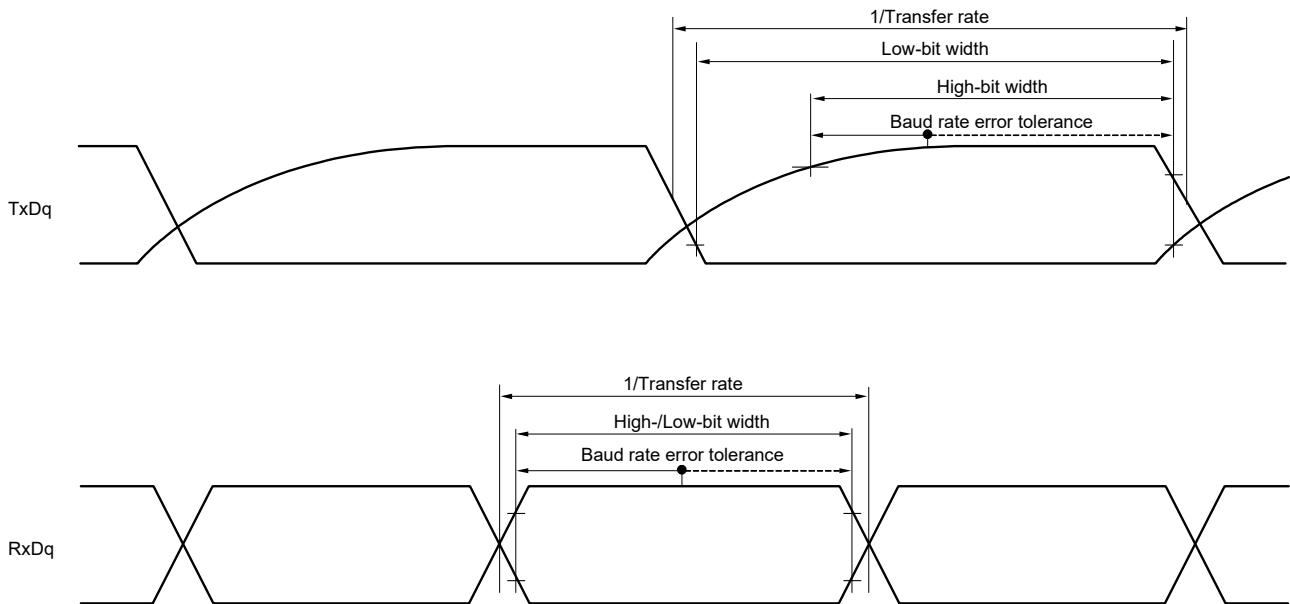
* This value is the theoretical value of the relative difference between the transmission and reception sides.

6. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 5 above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/ EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)

- Remarks 1.** $R_b[\Omega]$: Communication line (TxDq) pull-up resistance,
 $C_b[F]$: Communication line (TxDq) load capacitance, $V_b[V]$: Communication line voltage
2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)
 3. f_{MCK} : Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
 m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))
 4. UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/3)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|-----------------------|-------------------|---|---------------------------|------|------|
| | | | MIN. | MAX. | |
| SCKp cycle time | t_{KCY1} | $t_{\text{KCY1}} \geq 4/f_{\text{CLK}}$ $4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | 600 | | ns |
| | | $2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | 1000 | | ns |
| | | $2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$ | 2300 | | ns |
| SCKp high-level width | t_{KH1} | $4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | $t_{\text{KCY1}}/2 - 150$ | | ns |
| | | $2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | $t_{\text{KCY1}}/2 - 340$ | | ns |
| | | $2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$ | $t_{\text{KCY1}}/2 - 916$ | | ns |
| SCKp low-level width | t_{KL1} | $4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | $t_{\text{KCY1}}/2 - 24$ | | ns |
| | | $2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | $t_{\text{KCY1}}/2 - 36$ | | ns |
| | | $2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$ | $t_{\text{KCY1}}/2 - 100$ | | ns |

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/ EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

(Remarks are listed two pages after the next page.)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (2/3)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|--|------------|---|---------------------------|------|------|
| | | | MIN. | MAX. | |
| Slp setup time (to SCKp \uparrow) ^{Note} | t_{SIK1} | $4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | 162 | | ns |
| | | $2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | 354 | | ns |
| | | $2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$ | 958 | | ns |
| Slp hold time (from SCKp \uparrow) ^{Note} | t_{KSI1} | $4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | 38 | | ns |
| | | $2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | 38 | | ns |
| | | $2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | 38 | | ns |
| Delay time from SCKp \downarrow to SOp output ^{Note} | t_{KSO1} | $4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | | 200 | ns |
| | | $2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | | 390 | ns |
| | | $2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$ | | 966 | ns |

Note When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/ EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the page after the next page.)

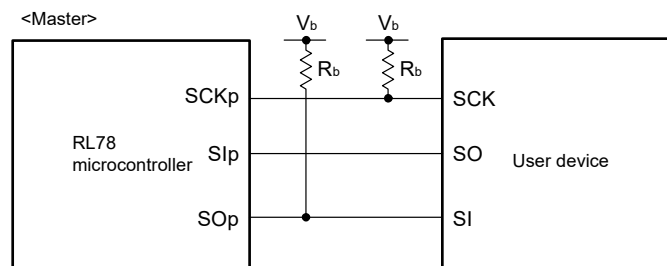
(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (3/3)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|--|-------------------|--|---------------------------|------|------|
| | | | MIN. | MAX. | |
| Slp setup time (to SCKp↓) ^{Note} | $t_{\text{SIK}1}$ | $4.0\text{ V} \leq \text{EV}_{\text{DD}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | 88 | | ns |
| | | $2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | 88 | | ns |
| | | $2.4\text{ V} \leq \text{EV}_{\text{DD}0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$ | 220 | | ns |
| Slp hold time (from SCKp↓) ^{Note} | $t_{\text{SH}1}$ | $4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | 38 | | ns |
| | | $2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | 38 | | ns |
| | | $2.4\text{ V} \leq \text{EV}_{\text{DD}0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$ | 38 | | ns |
| Delay time from SCKp↑ to SOp output ^{Note} | $t_{\text{KSO}1}$ | $4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | | 50 | ns |
| | | $2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | | 50 | ns |
| | | $2.4\text{ V} \leq \text{EV}_{\text{DD}0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$ | | 50 | ns |

Note When $\text{DAP}_{\text{mn}} = 0$ and $\text{CKP}_{\text{mn}} = 1$, or $\text{DAP}_{\text{mn}} = 1$ and $\text{CKP}_{\text{mn}} = 0$.

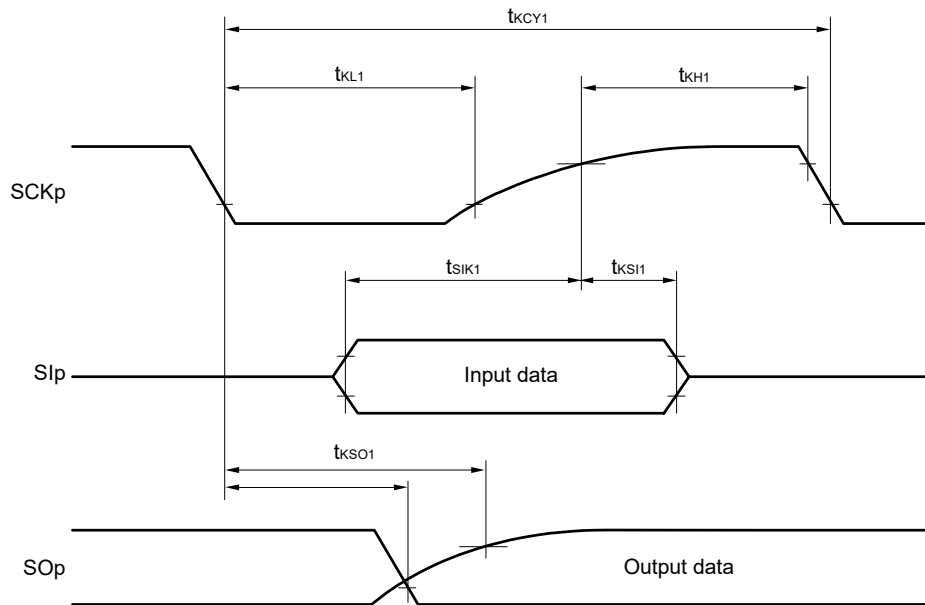
Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/ EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

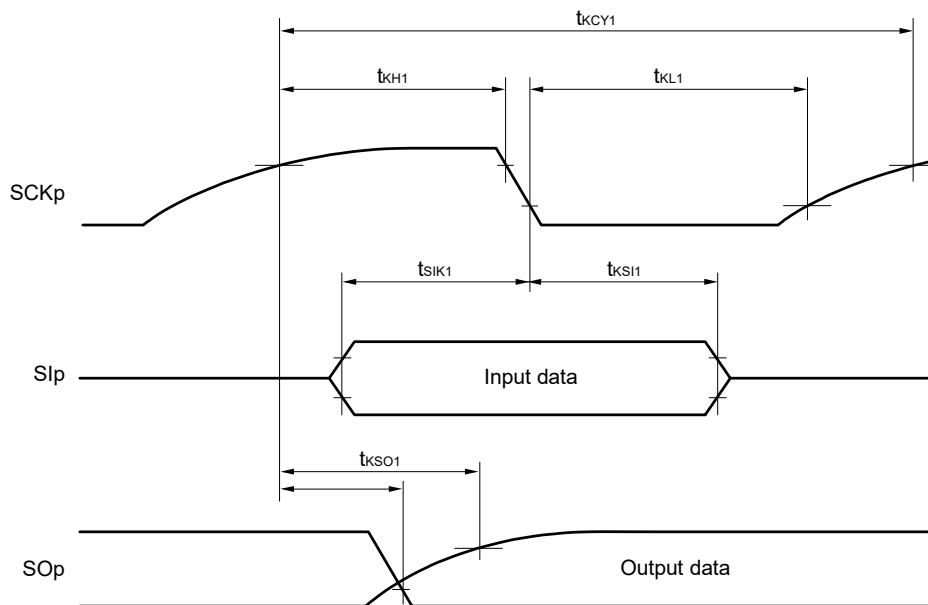
CSI mode connection diagram (during communication at different potential)

- Remarks**
1. $R_b[\Omega]$: Communication line (SCKp, SOp) pull-up resistance, $C_b[F]$: Communication line (SCKp, SOp) load capacitance, $V_b[V]$: Communication line voltage
 2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00))
 4. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



- Remarks**
1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 00, 01, 02, 10, 12, 13), n: Channel number (n = 0, 2), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
 2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)
($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$)

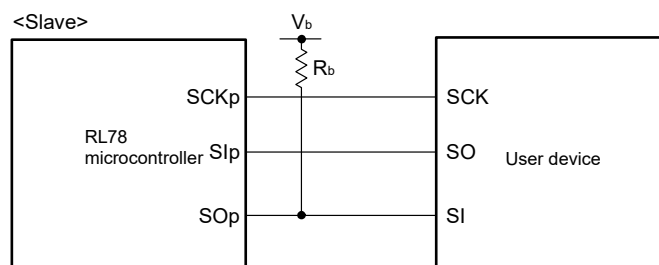
| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit | |
|--|--|--|---|---------------------------|------|----|
| | | | MIN. | MAX. | | |
| SCKp cycle time ^{Note 1} | t_{KCY2} | $4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$ | $24\text{ MHz} < f_{\text{MCK}}$ | $28/f_{\text{MCK}}$ | | ns |
| | | | $20\text{ MHz} < f_{\text{MCK}} \leq 24\text{ MHz}$ | $24/f_{\text{MCK}}$ | | ns |
| | | | $8\text{ MHz} < f_{\text{MCK}} \leq 20\text{ MHz}$ | $20/f_{\text{MCK}}$ | | ns |
| | | | $4\text{ MHz} < f_{\text{MCK}} \leq 8\text{ MHz}$ | $16/f_{\text{MCK}}$ | | ns |
| | | | $f_{\text{MCK}} \leq 4\text{ MHz}$ | $12/f_{\text{MCK}}$ | | ns |
| | | $2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$ | $24\text{ MHz} < f_{\text{MCK}}$ | $40/f_{\text{MCK}}$ | | ns |
| | | | $20\text{ MHz} < f_{\text{MCK}} \leq 24\text{ MHz}$ | $32/f_{\text{MCK}}$ | | ns |
| | | | $16\text{ MHz} < f_{\text{MCK}} \leq 20\text{ MHz}$ | $28/f_{\text{MCK}}$ | | ns |
| | | | $8\text{ MHz} < f_{\text{MCK}} \leq 16\text{ MHz}$ | $24/f_{\text{MCK}}$ | | ns |
| | | | $4\text{ MHz} < f_{\text{MCK}} \leq 8\text{ MHz}$ | $16/f_{\text{MCK}}$ | | ns |
| | | $2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ | $f_{\text{MCK}} \leq 4\text{ MHz}$ | $12/f_{\text{MCK}}$ | | ns |
| | | | $24\text{ MHz} < f_{\text{MCK}}$ | $96/f_{\text{MCK}}$ | | ns |
| | | | $20\text{ MHz} < f_{\text{MCK}} \leq 24\text{ MHz}$ | $72/f_{\text{MCK}}$ | | ns |
| | | | $16\text{ MHz} < f_{\text{MCK}} \leq 20\text{ MHz}$ | $64/f_{\text{MCK}}$ | | ns |
| | | | $8\text{ MHz} < f_{\text{MCK}} \leq 16\text{ MHz}$ | $52/f_{\text{MCK}}$ | | ns |
| SCKp high-/low-level width | t_{KH2} , t_{KL2} | $4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$ | $t_{\text{KCY2}}/2 - 24$ | | ns | |
| | | $2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$ | $t_{\text{KCY2}}/2 - 36$ | | ns | |
| | | $2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ ^{Note 2} | $t_{\text{KCY2}}/2 - 100$ | | ns | |
| Slp setup time (to SCKp \uparrow) ^{Note 2} | t_{SIK2} | $4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$ | $1/f_{\text{MCK}} + 40$ | | ns | |
| | | $2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$ | $1/f_{\text{MCK}} + 40$ | | ns | |
| | | $2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ | $1/f_{\text{MCK}} + 60$ | | ns | |
| Slp hold time (from SCKp \uparrow) ^{Note 3} | t_{KSI2} | | $1/f_{\text{MCK}} + 62$ | | ns | |
| Delay time from SCKp \downarrow to SOp output ^{Note 4} | t_{KSO2} | $4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$ | | $2/f_{\text{MCK}} + 240$ | ns | |
| | | $2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | | $2/f_{\text{MCK}} + 428$ | ns | |
| | | $2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$ | | $2/f_{\text{MCK}} + 1146$ | ns | |

(Notes, Caution and Remarks are listed on the next page.)

- Notes**
1. Transfer rate in the SNOOZE mode : MAX. 1 Mbps
 2. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The Slp setup time becomes “to $\text{SCKp}\downarrow$ ” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.
 3. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The Slp hold time becomes “from $\text{SCKp}\downarrow$ ” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.
 4. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The delay time to SOp output becomes “from $\text{SCKp}\uparrow$ ” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.

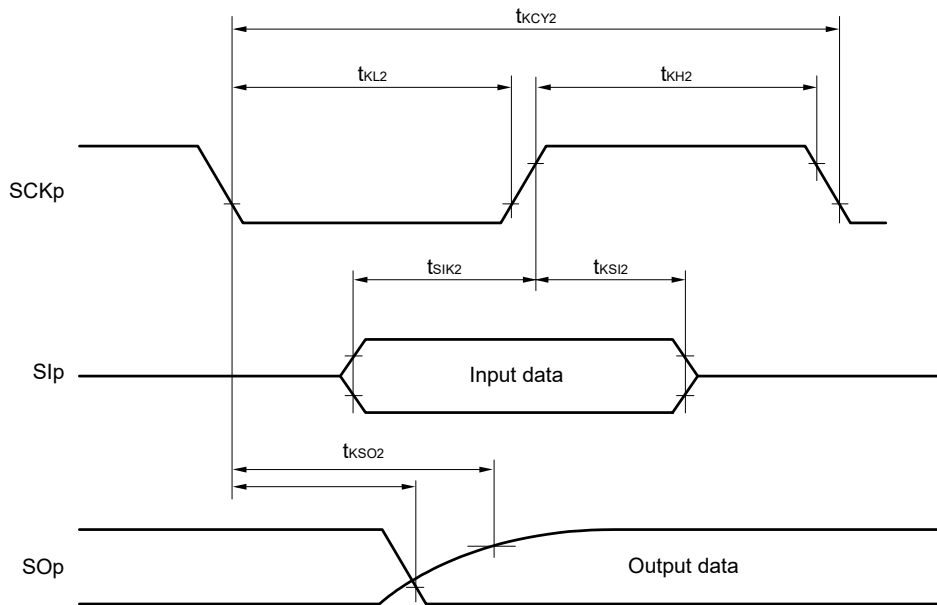
Caution Select the TTL input buffer for the Slp pin and SCKp pin and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/ EV_{DD} tolerance (for the 64- to 128-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)

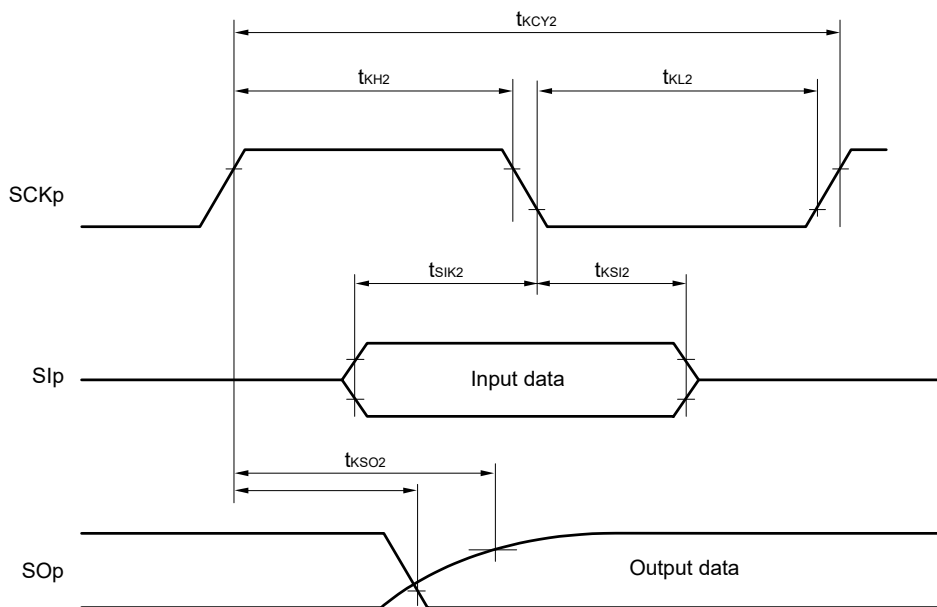


- Remarks**
1. $R_b[\Omega]$: Communication line (SOp) pull-up resistance, $C_b[\text{F}]$: Communication line (SOp) load capacitance, $V_b[\text{V}]$: Communication line voltage
 2. p: CSI number ($p = 00, 01, 10, 20, 30, 31$), m: Unit number ($m = 0, 1$), n: Channel number ($n = 00, 01, 02, 10, 12, 13$), g: PIM and POM number ($g = 0, 1, 4, 5, 8, 14$)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number ($mn = 00, 01, 02, 10, 12, 13$))
 4. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

**CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



- Remarks 1.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number,
n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
- 2.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode) (1/2)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---------------------------|-------------------|---|---------------------------|-----------------------|------|
| | | | MIN. | MAX. | |
| SCLr clock frequency | f _{SCL} | 4.0 V \leq EV _{DD0} \leq 5.5 V, 2.7 V \leq V _b \leq 4.0 V, C _b = 50 pF, R _b = 2.7 k Ω | | 400 ^{Note 1} | kHz |
| | | 2.7 V \leq EV _{DD0} < 4.0 V, 2.3 V \leq V _b \leq 2.7 V, C _b = 50 pF, R _b = 2.7 k Ω | | 400 ^{Note 1} | kHz |
| | | 4.0 V \leq EV _{DD0} \leq 5.5 V, 2.7 V \leq V _b \leq 4.0 V, C _b = 100 pF, R _b = 2.8 k Ω | | 100 ^{Note 1} | kHz |
| | | 2.7 V \leq EV _{DD0} < 4.0 V, 2.3 V \leq V _b \leq 2.7 V, C _b = 100 pF, R _b = 2.7 k Ω | | 100 ^{Note 1} | kHz |
| | | 2.4 V \leq EV _{DD0} < 3.3 V, 1.6 V \leq V _b \leq 2.0 V, C _b = 100 pF, R _b = 5.5 k Ω | | 100 ^{Note 1} | kHz |
| Hold time when SCLr = "L" | t _{LOW} | 4.0 V \leq EV _{DD0} \leq 5.5 V, 2.7 V \leq V _b \leq 4.0 V, C _b = 50 pF, R _b = 2.7 k Ω | 1200 | | ns |
| | | 2.7 V \leq EV _{DD0} < 4.0 V, 2.3 V \leq V _b \leq 2.7 V, C _b = 50 pF, R _b = 2.7 k Ω | 1200 | | ns |
| | | 4.0 V \leq EV _{DD0} \leq 5.5 V, 2.7 V \leq V _b \leq 4.0 V, C _b = 100 pF, R _b = 2.8 k Ω | 4600 | | ns |
| | | 2.7 V \leq EV _{DD0} < 4.0 V, 2.3 V \leq V _b \leq 2.7 V, C _b = 100 pF, R _b = 2.7 k Ω | 4600 | | ns |
| | | 2.4 V \leq EV _{DD0} < 3.3 V, 1.6 V \leq V _b \leq 2.0 V, C _b = 100 pF, R _b = 5.5 k Ω | 4650 | | ns |
| Hold time when SCLr = "H" | t _{HIGH} | 4.0 V \leq EV _{DD0} \leq 5.5 V, 2.7 V \leq V _b \leq 4.0 V, C _b = 50 pF, R _b = 2.7 k Ω | 620 | | ns |
| | | 2.7 V \leq EV _{DD0} < 4.0 V, 2.3 V \leq V _b \leq 2.7 V, C _b = 50 pF, R _b = 2.7 k Ω | 500 | | ns |
| | | 4.0 V \leq EV _{DD0} \leq 5.5 V, 2.7 V \leq V _b \leq 4.0 V, C _b = 100 pF, R _b = 2.8 k Ω | 2700 | | ns |
| | | 2.7 V \leq EV _{DD0} < 4.0 V, 2.3 V \leq V _b \leq 2.7 V, C _b = 100 pF, R _b = 2.7 k Ω | 2400 | | ns |
| | | 2.4 V \leq EV _{DD0} < 3.3 V, 1.6 V \leq V _b \leq 2.0 V, C _b = 100 pF, R _b = 5.5 k Ω | 1830 | | ns |

(Notes and Caution are listed on the next page, and Remarks are listed on the page after the next page.)

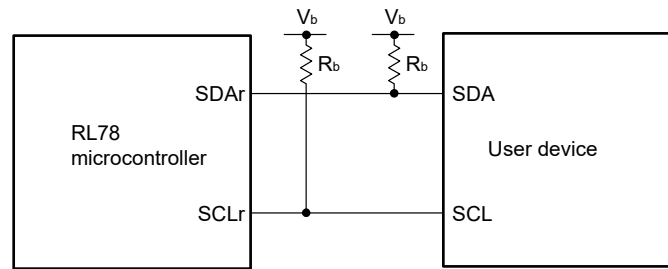
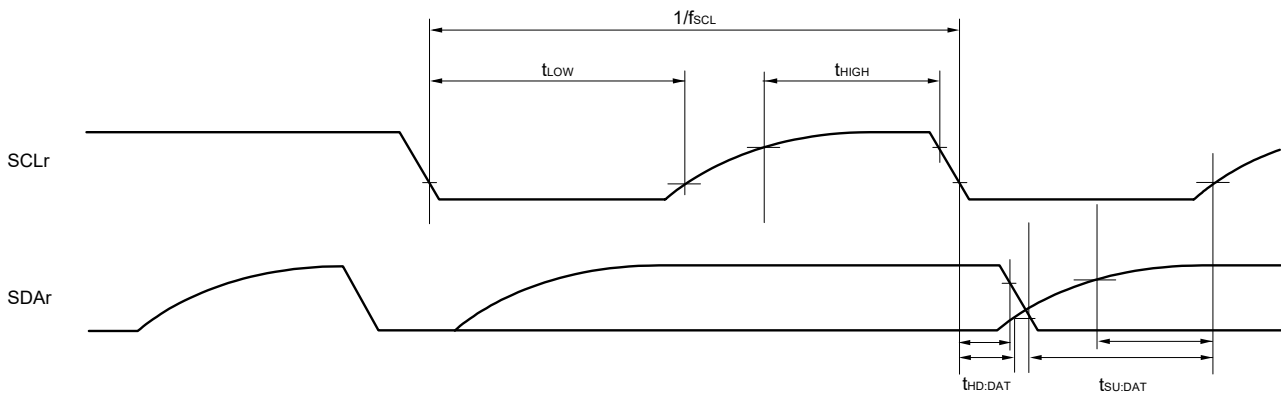
(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode) (2/2)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|-------------------------------|---------------------|--|------------------------------------|------|------|
| | | | MIN. | MAX. | |
| Data setup time (reception) | $t_{\text{SU:DAT}}$ | $4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | $1/f_{\text{MCK}} + 340$ Note 2 | | ns |
| | | $2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | $1/f_{\text{MCK}} + 340$ Note 2 | | ns |
| | | $4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.8\text{ k}\Omega$ | $1/f_{\text{MCK}} + 760$ Note 2 | | ns |
| | | $2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | $1/f_{\text{MCK}} + 760$ Note 2 | | ns |
| | | $2.4\text{ V} \leq \text{EV}_{\text{DD}0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5.5\text{ k}\Omega$ | $1/f_{\text{MCK}} + 570$ Note 2 | | ns |
| Data hold time (transmission) | $t_{\text{HD:DAT}}$ | $4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | 0 | 770 | ns |
| | | $2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | 0 | 770 | ns |
| | | $4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.8\text{ k}\Omega$ | 0 | 1420 | ns |
| | | $2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.7\text{ k}\Omega$ | 0 | 1420 | ns |
| | | $2.4\text{ V} \leq \text{EV}_{\text{DD}0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5.5\text{ k}\Omega$ | 0 | 1215 | ns |

Notes 1. The value must also be equal to or less than $f_{\text{MCK}}/4$.**2.** Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/ EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/ EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

Simplified I²C mode connection diagram (during communication at different potential)**Simplified I²C mode serial transfer timing (during communication at different potential)**

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/ EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/ EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

- Remarks**
- $R_b[\Omega]$: Communication line (SDAr, SCLr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance, $V_b[V]$: Communication line voltage
 - r: IIC number (r = 00, 01, 10, 20, 30, 31), g: PIM, POM number (g = 0, 1, 4, 5, 8, 14)
 - f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))

3.5.2 Serial interface IICA

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$)

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | | | Unit |
|---|---------------------|---|---------------------------|------|-----------|------|---------------|
| | | | Standard Mode | | Fast Mode | | |
| | | | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | f_{SCL} | Fast mode: $f_{\text{CLK}} \geq 3.5\text{ MHz}$ | – | – | 0 | 400 | kHz |
| | | Standard mode: $f_{\text{CLK}} \geq 1\text{ MHz}$ | 0 | 100 | – | – | kHz |
| Setup time of restart condition | $t_{\text{SU:STA}}$ | | 4.7 | | 0.6 | | μs |
| Hold time ^{Note 1} | $t_{\text{HD:STA}}$ | | 4.0 | | 0.6 | | μs |
| Hold time when SCLA0 = "L" | t_{LOW} | | 4.7 | | 1.3 | | μs |
| Hold time when SCLA0 = "H" | t_{HIGH} | | 4.0 | | 0.6 | | μs |
| Data setup time (reception) | $t_{\text{SU:DAT}}$ | | 250 | | 100 | | ns |
| Data hold time (transmission) ^{Note 2} | $t_{\text{HD:DAT}}$ | | 0 | 3.45 | 0 | 0.9 | μs |
| Setup time of stop condition | $t_{\text{SU:STO}}$ | | 4.0 | | 0.6 | | μs |
| Bus-free time | t_{BUF} | | 4.7 | | 1.3 | | μs |

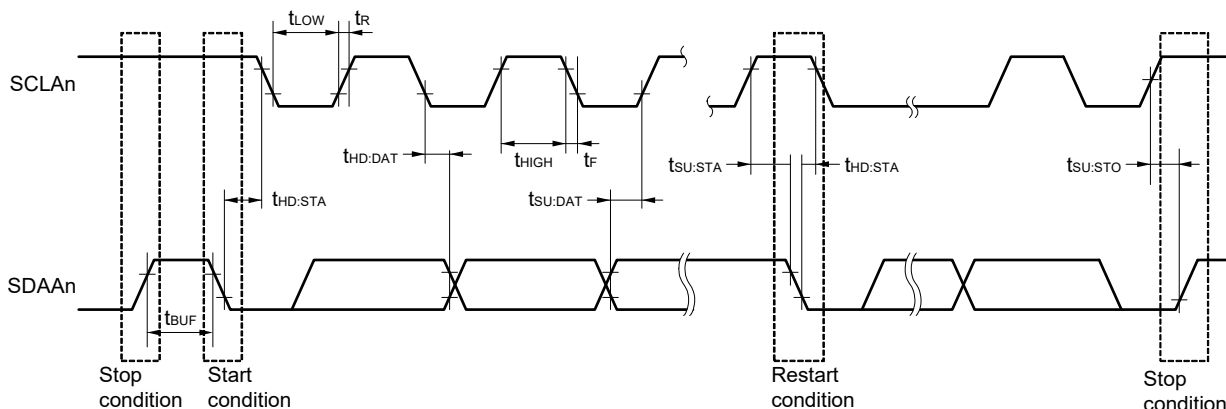
- Notes**
- The first clock pulse is generated after this period when the start/restart condition is detected.
 - The maximum value (MAX.) of $t_{\text{HD:DAT}}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1} , I_{OL1} , V_{OH1} , V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: $C_b = 400\text{ pF}$, $R_b = 2.7\text{ k}\Omega$
 Fast mode: $C_b = 320\text{ pF}$, $R_b = 1.1\text{ k}\Omega$

IICA serial transfer timing



Remark $n = 0, 1$

3.6 Analog Characteristics

3.6.1 A/D converter characteristics

Classification of A/D converter characteristics

| Input channel | Reference Voltage | | |
|--|--|--|--|
| | Reference voltage (+) = AV_{REFP} Reference voltage (-) = AV_{REFM} | Reference voltage (+) = V_{DD} Reference voltage (-) = V_{SS} | Reference voltage (+) = V_{BGR} Reference voltage (-) = AV_{REFM} |
| ANI0 to ANI14 | Refer to 3.6.1 (1) . | Refer to 3.6.1 (3) . | Refer to 3.6.1 (4) . |
| ANI16 to ANI26 | | | |
| Internal reference voltage Temperature sensor output voltage | Refer to 3.6.1 (1) . | | – |

(1) When reference voltage (+) = $AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), reference voltage (-) = $AV_{REFM}/ANI1$ ($ADREFM = 1$), target pin : ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|------------|---|---|--------|------|--------------------------------|---------------|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error ^{Note 1} | AINL | 10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3} | $2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ | | 1.2 | ± 3.5 | LSB |
| Conversion time | t_{CONV} | 10-bit resolution Target pin: ANI2 to ANI14 | $3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 2.125 | | 39 | μs |
| | | | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 3.1875 | | 39 | μs |
| | | | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 17 | | 39 | μs |
| | | 10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode) | $3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 2.375 | | 39 | μs |
| | | | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 3.5625 | | 39 | μs |
| | | | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 17 | | 39 | μs |
| Zero-scale error ^{Notes 1, 2} | E_{ZS} | 10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3} | $2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ | | | ± 0.25 | %FSR |
| Full-scale error ^{Notes 1, 2} | E_{FS} | 10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3} | $2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ | | | ± 0.25 | %FSR |
| Integral linearity error ^{Note 1} | ILE | 10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3} | $2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ | | | ± 2.5 | LSB |
| Differential linearity error ^{Note 1} | DLE | 10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3} | $2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ | | | ± 1.5 | LSB |
| Analog input voltage | V_{AIN} | ANI2 to ANI14 | | 0 | | AV_{REFP} | V |
| | | Internal reference voltage output ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode) | | | | V_{BGR} ^{Note 4} | V |
| | | Temperature sensor output voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode) | | | | V_{TMPS25} ^{Note 4} | V |

(Notes are listed on the next page.)

- Notes**
1. Excludes quantization error ($\pm 1/2$ LSB).
 2. This value is indicated as a ratio (%FSR) to the full-scale value.
 3. When $AV_{REFP} < V_{DD}$, the MAX. values are as follows.
Overall error: Add ± 1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.
Zero-scale error/Full-scale error: Add $\pm 0.05\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.
Integral linearity error/ Differential linearity error: Add ± 0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.
 4. Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

(2) When reference voltage (+) = $AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), reference voltage (-) = $AV_{REFM}/ANI1$ ($ADREFM = 1$), target pin : ANI16 to ANI26

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $2.4\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--|------------------|--|---|--------|-------------------------------|---------------|
| Resolution | RES | | 8 | | 10 | bit |
| Overall error ^{Note 1} | AINL | 10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4 | $2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ | 1.2 | ± 5.0 | LSB |
| Conversion time | t_{CONV} | 10-bit resolution Target pin : ANI16 to ANI26 | $3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 2.125 | 39 | μs |
| | | | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 3.1875 | 39 | μs |
| | | | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 17 | 39 | μs |
| Zero-scale error ^{Notes 1, 2} | E _{ZS} | 10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4 | $2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ | | ± 0.35 | %FSR |
| Full-scale error ^{Notes 1, 2} | E _{FS} | 10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4 | $2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ | | ± 0.35 | %FSR |
| Integral linearity error ^{Note 1} | ILE | 10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4 | $2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ | | ± 3.5 | LSB |
| Differential linearity error ^{Note 1} | DLE | 10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4 | $2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ | | ± 2.0 | LSB |
| Analog input voltage | V _{AIN} | ANI16 to ANI26 | 0 | | AV_{REFP} and EV_{DD0} | V |

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When $AV_{REFP} < V_{DD}$, the MAX. values are as follows.

Overall error: Add ± 1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Zero-scale error/Full-scale error: Add $\pm 0.05\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.

Integral linearity error/ Differential linearity error: Add ± 0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

4. When $AV_{REFP} < EV_{DD0} \leq V_{DD}$, the MAX. values are as follows.

Overall error: Add ± 4.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Zero-scale error/Full-scale error: Add $\pm 0.20\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.

Integral linearity error/ Differential linearity error: Add ± 2.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

(3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = V_{SS} (ADREFM = 0), target pin : ANI0 to ANI14, ANI16 to ANI26, internal reference voltage, and temperature sensor output voltage

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$, Reference voltage (+) = V_{DD} , Reference voltage (-) = V_{SS})

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit | |
|--|-----------------|---|--|--------------------------------|------|------------|---------------|---|
| Resolution | RES | | | 8 | | 10 | bit | |
| Overall error ^{Note 1} | AINL | 10-bit resolution | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | 1.2 | ± 7.0 | LSB | |
| Conversion time | t_{CONV} | 10-bit resolution Target pin: ANI0 to ANI14, ANI16 to ANI26 | $3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 2.125 | | 39 | μs | |
| | | | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 3.1875 | | 39 | μs | |
| | | | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 17 | | 39 | μs | |
| | | 10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode) | $3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 2.375 | | 39 | μs | |
| | | | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 3.5625 | | 39 | μs | |
| | | | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 17 | | 39 | μs | |
| Zero-scale error ^{Notes 1, 2} | E _{ZS} | 10-bit resolution | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | | ± 0.60 | %FSR | |
| Full-scale error ^{Notes 1, 2} | E _{FS} | 10-bit resolution | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | | ± 0.60 | %FSR | |
| Integral linearity error ^{Note 1} | ILE | 10-bit resolution | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | | ± 4.0 | LSB | |
| Differential linearity error Note 1 | DLE | 10-bit resolution | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | | ± 2.0 | LSB | |
| Analog input voltage | V_{AIN} | ANI0 to ANI14 | | 0 | | V_{DD} | V | |
| | | ANI16 to ANI26 | | 0 | | EV_{DD0} | V | |
| | | Internal reference voltage output ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode) | | V_{BGR} ^{Note 3} | | | | V |
| | | Temperature sensor output voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode) | | V_{TMPS25} ^{Note 3} | | | | V |

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = $AV_{REFM}/ANI1$ (ADREFM = 1), target pin : ANI0, ANI2 to ANI14, ANI16 to ANI26

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$, Reference voltage (+) = V_{BGR} ^{Note 3}, Reference voltage (-) = AV_{REFM} ^{Note 4} = 0 V, HS (high-speed main) mode)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|--|------------|------------------|--|------|------|-----------------------------|---------------|
| Resolution | RES | | | 8 | | | bit |
| Conversion time | t_{CONV} | 8-bit resolution | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 17 | | 39 | μs |
| Zero-scale error ^{Notes 1, 2} | E_{ZS} | 8-bit resolution | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | | ± 0.60 | %FSR |
| Integral linearity error ^{Note 1} | ILE | 8-bit resolution | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | | ± 2.0 | LSB |
| Differential linearity error ^{Note 1} | DLE | 8-bit resolution | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | | ± 1.0 | LSB |
| Analog input voltage | V_{AIN} | | | 0 | | V_{BGR} ^{Note 3} | V |

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

4. When reference voltage (-) = V_{SS} , the MAX. values are as follows.

Zero-scale error: Add $\pm 0.35\%$ FSR to the MAX. value when reference voltage (-) = AV_{REFM} .

Integral linearity error: Add ± 0.5 LSB to the MAX. value when reference voltage (-) = AV_{REFM} .

Differential linearity error: Add ± 0.2 LSB to the MAX. value when reference voltage (-) = AV_{REFM} .

3.6.2 Temperature sensor/internal reference voltage characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, HS (high-speed main) mode)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-----------------------------------|--------------|---|------|------|------|----------------------|
| Temperature sensor output voltage | V_{TMPS25} | Setting ADS register = 80H, $T_A = +25^\circ\text{C}$ | | 1.05 | | V |
| Internal reference voltage | V_{BGR} | Setting ADS register = 81H | 1.38 | 1.45 | 1.5 | V |
| Temperature coefficient | F_{VTMPS} | Temperature sensor that depends on the temperature | | -3.6 | | mV/ $^\circ\text{C}$ |
| Operation stabilization wait time | t_{AMP} | | 5 | | | μs |

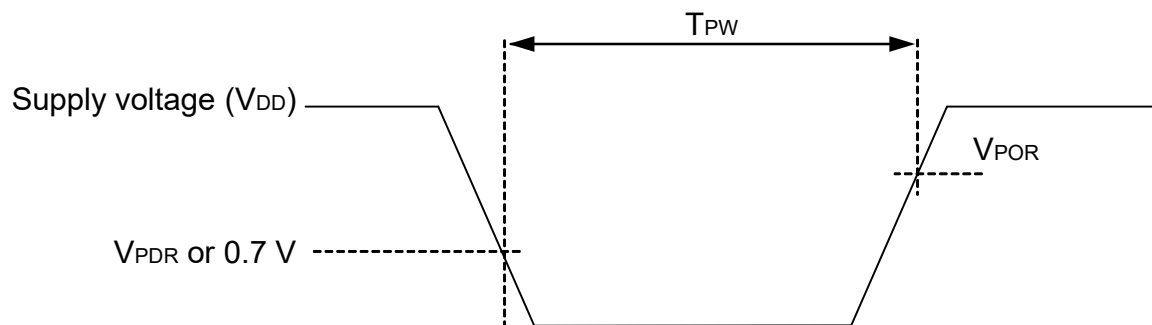
3.6.3 POR circuit characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $V_{SS} = 0\text{ V}$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-------------------------------------|-----------|------------------------|------|------|------|---------------|
| Detection voltage | V_{POR} | Power supply rise time | 1.45 | 1.51 | 1.57 | V |
| | V_{PDR} | Power supply fall time | 1.44 | 1.50 | 1.56 | V |
| Minimum pulse width ^{Note} | T_{PW} | | 300 | | | μs |

<R>

Note Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR} . This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7 V to when V_{DD} exceeds V_{POR} while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



3.6.4 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode

 $(T_A = -40$ to $+105^\circ\text{C}$, $V_{PDR} \leq V_{DD} \leq 5.5$ V, $V_{SS} = 0$ V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|-------------------|----------------------|------------------------|------------------------|------|------|------|---------------|
| Detection voltage | Supply voltage level | V_{LVD0} | Power supply rise time | 3.90 | 4.06 | 4.22 | V |
| | | | Power supply fall time | 3.83 | 3.98 | 4.13 | V |
| | V_{LVD1} | Power supply rise time | 3.60 | 3.75 | 3.90 | V | |
| | | Power supply fall time | 3.53 | 3.67 | 3.81 | V | |
| | V_{LVD2} | Power supply rise time | 3.01 | 3.13 | 3.25 | V | |
| | | Power supply fall time | 2.94 | 3.06 | 3.18 | V | |
| | V_{LVD3} | Power supply rise time | 2.90 | 3.02 | 3.14 | V | |
| | | Power supply fall time | 2.85 | 2.96 | 3.07 | V | |
| | V_{LVD4} | Power supply rise time | 2.81 | 2.92 | 3.03 | V | |
| | | Power supply fall time | 2.75 | 2.86 | 2.97 | V | |
| | V_{LVD5} | Power supply rise time | 2.70 | 2.81 | 2.92 | V | |
| | | Power supply fall time | 2.64 | 2.75 | 2.86 | V | |
| | V_{LVD6} | Power supply rise time | 2.61 | 2.71 | 2.81 | V | |
| | | Power supply fall time | 2.55 | 2.65 | 2.75 | V | |
| | V_{LVD7} | Power supply rise time | 2.51 | 2.61 | 2.71 | V | |
| | | Power supply fall time | 2.45 | 2.55 | 2.65 | V | |
| | Minimum pulse width | t_{LW} | | 300 | | | μs |
| | Detection delay time | | | | | 300 | μs |

LVD Detection Voltage of Interrupt & Reset Mode

 $(T_A = -40$ to $+105^\circ\text{C}$, $V_{PDR} \leq V_{DD} \leq 5.5$ V, $V_{SS} = 0$ V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|--------------------------|-------------|--|------------------------------|------|------|------|---|
| Interrupt and reset mode | V_{LVDD0} | $V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 1$, falling reset voltage | 2.64 | 2.75 | 2.86 | V | |
| | V_{LVDD1} | LVIS1, LVIS0 = 1, 0 | Rising release reset voltage | 2.81 | 2.92 | 3.03 | V |
| | | | Falling interrupt voltage | 2.75 | 2.86 | 2.97 | V |
| | V_{LVDD2} | LVIS1, LVIS0 = 0, 1 | Rising release reset voltage | 2.90 | 3.02 | 3.14 | V |
| | | | Falling interrupt voltage | 2.85 | 2.96 | 3.07 | V |
| | V_{LVDD3} | LVIS1, LVIS0 = 0, 0 | Rising release reset voltage | 3.90 | 4.06 | 4.22 | V |
| | | | Falling interrupt voltage | 3.83 | 3.98 | 4.13 | V |

3.6.5 Power supply voltage rising slope characteristics

 $(T_A = -40$ to $+105^\circ\text{C}$, $V_{SS} = 0$ V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-----------------------------------|-----------|------------|------|------|------|------|
| Power supply voltage rising slope | S_{VDD} | | | | 54 | V/ms |

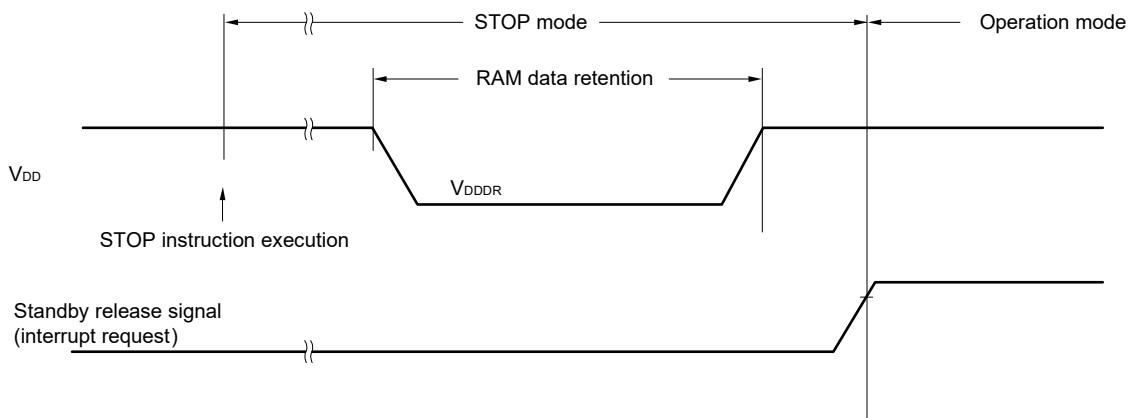
Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 3.4 AC Characteristics.

3.7 RAM Data Retention Characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $V_{SS} = 0$ V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-------------------------------|------------|------------|----------------------|------|------|------|
| Data retention supply voltage | V_{DDDR} | | 1.44 ^{Note} | | 5.5 | V |

Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



3.8 Flash Memory Programming Characteristics

($T_A = -40$ to $+105^\circ\text{C}$, 2.4 V $\leq V_{DD} \leq 5.5$ V, $V_{SS} = 0$ V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|------------|---|---------|-----------|------|-------|
| CPU/peripheral hardware clock frequency | f_{CLK} | 2.4 V $\leq V_{DD} \leq 5.5$ V | 1 | | 32 | MHz |
| Number of code flash rewrites <small>Notes 1, 2, 3</small> | C_{enwr} | Retained for 20 years $T_A = 85^\circ\text{C}$ ^{Note 4} | 1,000 | | | Times |
| Number of data flash rewrites <small>Notes 1, 2, 3</small> | | Retained for 1 years $T_A = 25^\circ\text{C}$ | | 1,000,000 | | |
| | | Retained for 5 years $T_A = 85^\circ\text{C}$ ^{Note 4} | 100,000 | | | |
| | | Retained for 20 years $T_A = 85^\circ\text{C}$ ^{Note 4} | 10,000 | | | |

- Notes**
- 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.
 2. When using flash memory programmer and Renesas Electronics self programming library.
 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.
 4. This temperature is the average value at which data are retained.

3.9 Dedicated Flash Memory Programmer Communication (UART)

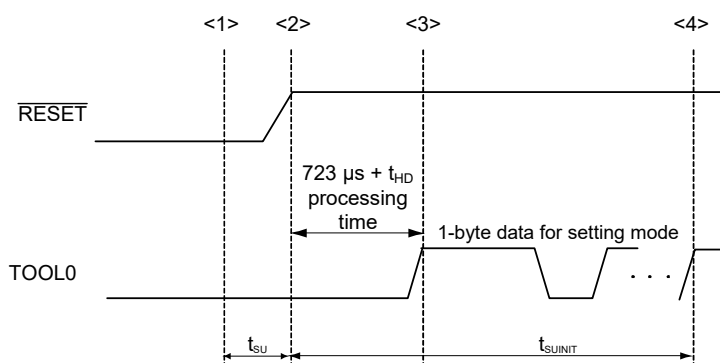
($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---------------|--------|---------------------------|---------|------|-----------|------|
| Transfer rate | | During serial programming | 115,200 | | 1,000,000 | bps |

3.10 Timing of Entry to Flash Memory Programming Modes

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--|--------------------|---|------|------|------|---------------|
| Time to complete the communication for the initial setting after the external reset is released | t_{SUNIT} | POR and LVD reset must be released before the external reset is released. | | | 100 | ms |
| Time to release the external reset after the TOOL0 pin is set to the low level | t_{SU} | POR and LVD reset must be released before the external reset is released. | 10 | | | μs |
| Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory) | t_{HD} | POR and LVD reset must be released before the external reset is released. | 1 | | | ms |



- <1> The low level is input to the TOOL0 pin.
- <2> The external reset is released (POR and LVD reset must be released before the external reset is released.).
- <3> The TOOL0 pin is set to the high level.
- <4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUNIT} : Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

t_{SU} : Time to release the external reset after the TOOL0 pin is set to the low level

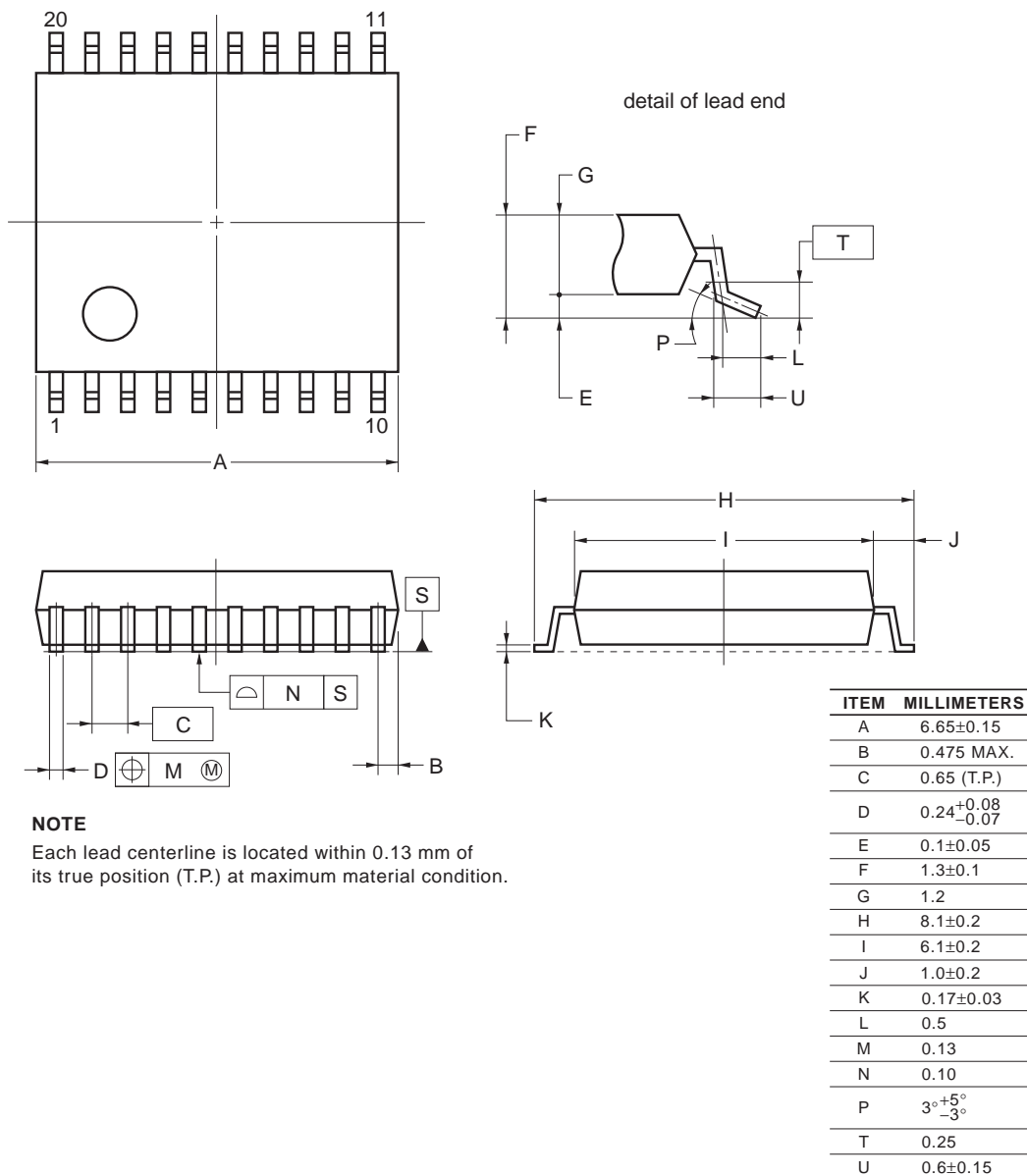
t_{HD} : Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

4. PACKAGE DRAWINGS

4.1 20-pin Products

R5F1006AASP, R5F1006CASP, R5F1006DASP, R5F1006EASP
 R5F1016AASP, R5F1016CASP, R5F1016DASP, R5F1016EASP
 R5F1006ADSP, R5F1006CDSP, R5F1006DDSP, R5F1006EDSP
 R5F1016ADSP, R5F1016CDSP, R5F1016DDSP, R5F1016EDSP
 R5F1006AGSP, R5F1006CGSP, R5F1006DGSP, R5F1006EGSP

| | | | |
|---------------------|--------------|----------------|-----------------|
| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
| P-LSSOP20-0300-0.65 | PLSP0020JC-A | S20MC-65-5A4-3 | 0.12 |

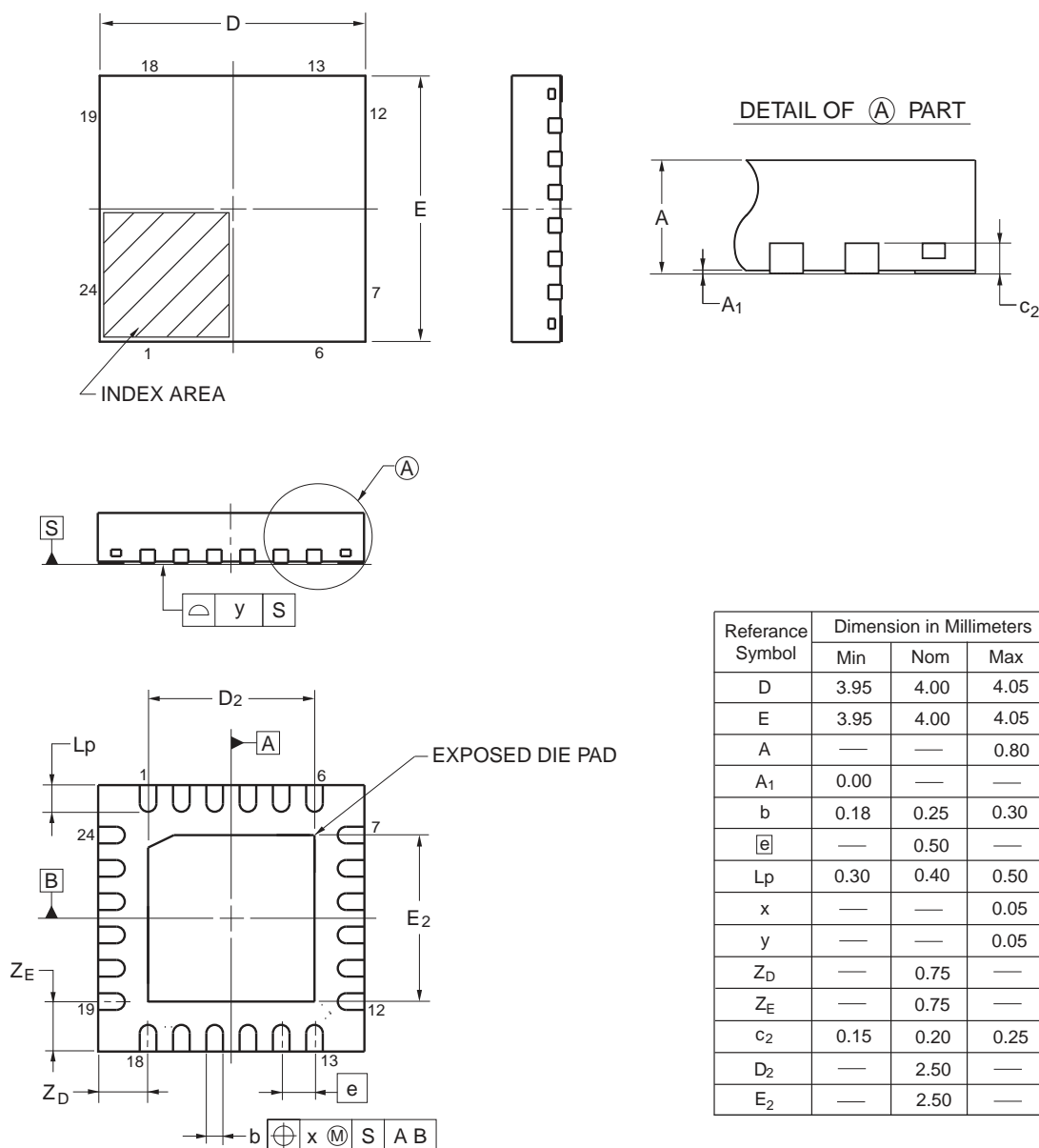


NOTE
 Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

4.2 24-pin Products

R5F1007AANA, R5F1007CANA, R5F1007DANA, R5F1007EANA
 R5F1017AANA, R5F1017CANA, R5F1017DANA, R5F1017EANA
 R5F1007ADNA, R5F1007CDNA, R5F1007DDNA, R5F1007EDNA
 R5F1017ADNA, R5F1017CDNA, R5F1017DDNA, R5F1017EDNA
 R5F1007AGNA, R5F1007CGNA, R5F1007DGNA, R5F1007EGNA

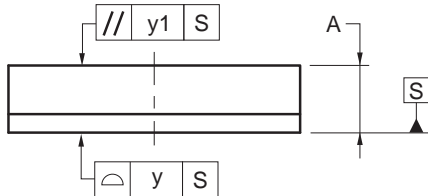
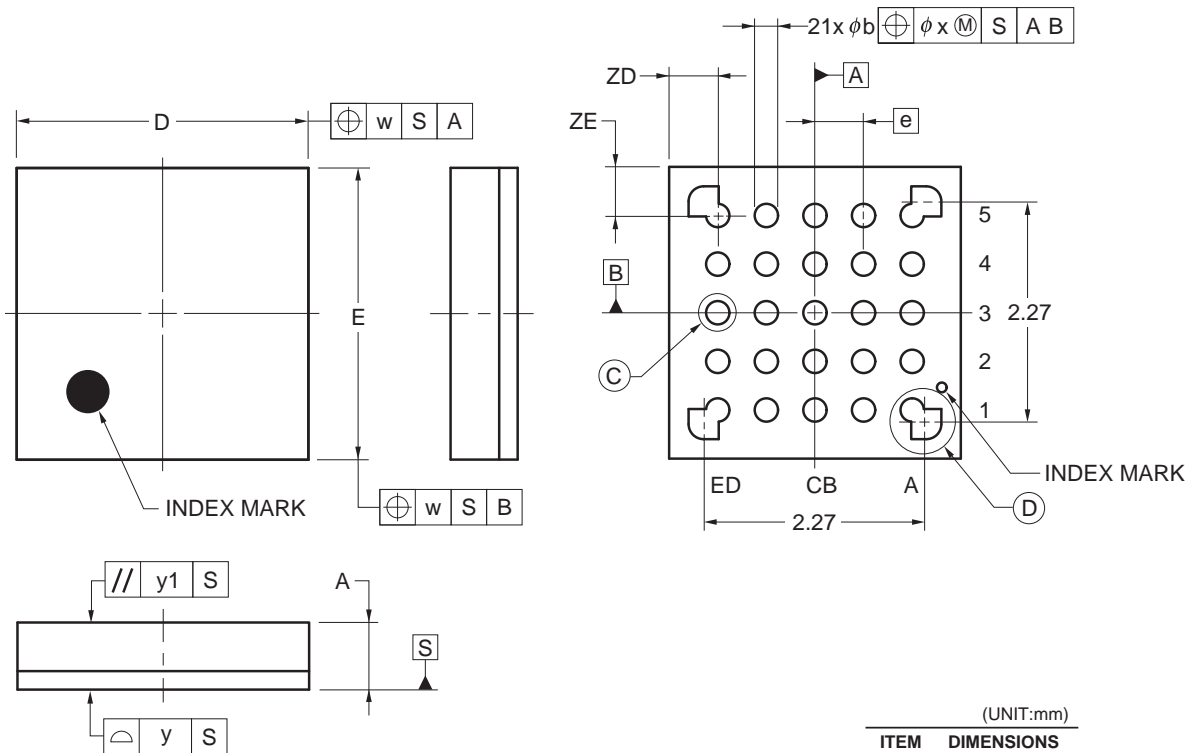
| JEITA Package code | RENESAS code | Previous code | MASS(TYP.)[g] |
|--------------------|--------------|----------------|---------------|
| P-HWQFN24-4x4-0.50 | PWQN0024KE-A | P24K8-50-CAB-3 | 0.04 |



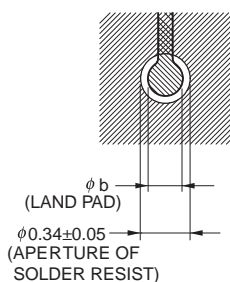
4.3 25-pin Products

R5F1008AALA, R5F1008CALA, R5F1008DALA, R5F1008EALA
 R5F1018AALA, R5F1018CALA, R5F1018DALA, R5F1018EALA
 R5F1008AGLA, R5F1008CGLA, R5F1008DGLA, R5F1008EGLA

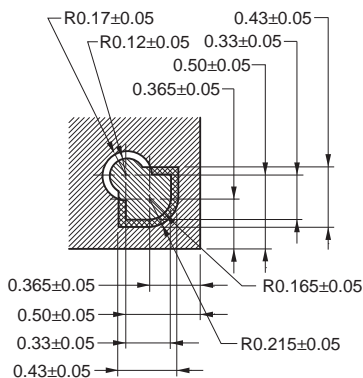
| | | | |
|--------------------|--------------|----------------|-----------------|
| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
| P-WFLGA25-3x3-0.50 | PWLG0025KA-A | P25FC-50-2N2-2 | 0.01 |



DETAIL OF © PART



DETAIL OF © PART



(UNIT:mm)

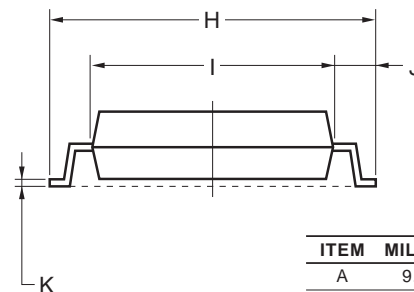
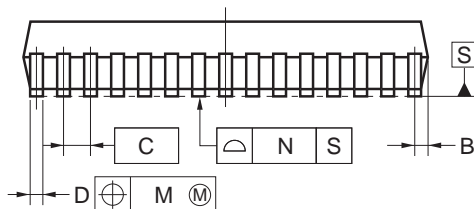
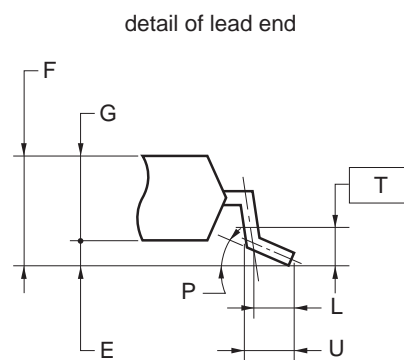
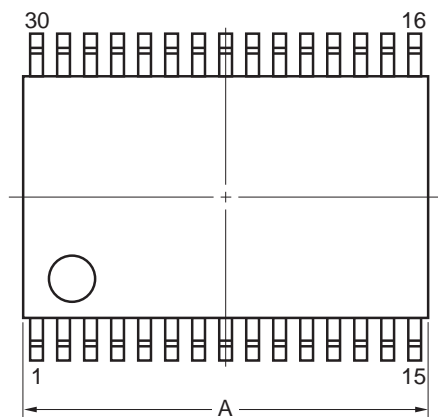
| ITEM | DIMENSIONS |
|------|-------------|
| D | 3.00 ± 0.10 |
| E | 3.00 ± 0.10 |
| w | 0.20 |
| e | 0.50 |
| A | 0.69 ± 0.07 |
| b | 0.24 ± 0.05 |
| x | 0.05 |
| y | 0.08 |
| y1 | 0.20 |
| ZD | 0.50 |
| ZE | 0.50 |

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4.4 30-pin Products

R5F100AAASP, R5F100ACASP, R5F100ADASP, R5F100AEASP, R5F100AFASP, R5F100AGASP
 R5F101AAASP, R5F101ACASP, R5F101ADASP, R5F101AEASP, R5F101AFASP, R5F101AGASP
 R5F100AADSP, R5F100ACDSP, R5F100ADDSP, R5F100AEDSP, R5F100AFDSP, R5F100AGDSP
 R5F101AADSP, R5F101ACDSP, R5F101ADDSP, R5F101AEDSP, R5F101AFDSP, R5F101AGDSP
 R5F100AAGSP, R5F100ACGSP, R5F100ADGSP, R5F100AEGSP, R5F100AFGSP, R5F100AGGSP

| | | | |
|---------------------|--------------|----------------|-----------------|
| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
| P-LSSOP30-0300-0.65 | PLSP0030JB-B | S30MC-65-5A4-3 | 0.18 |



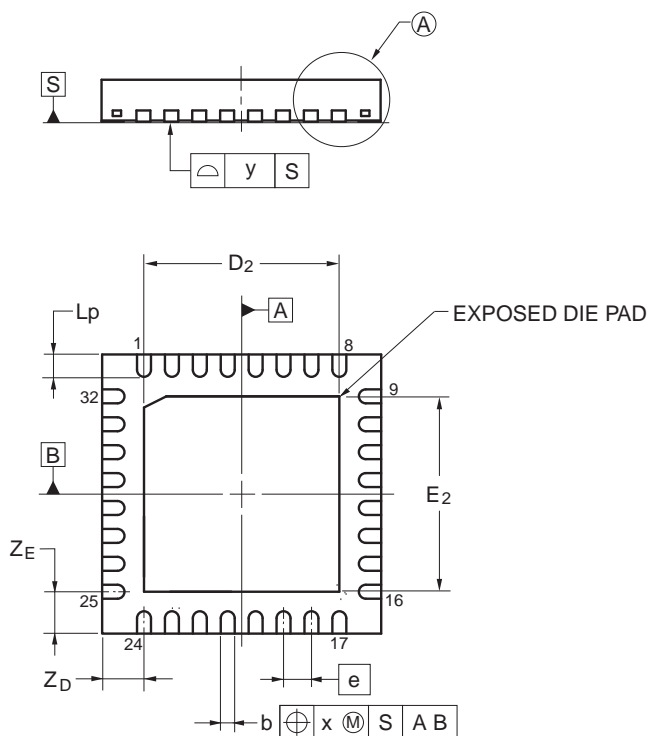
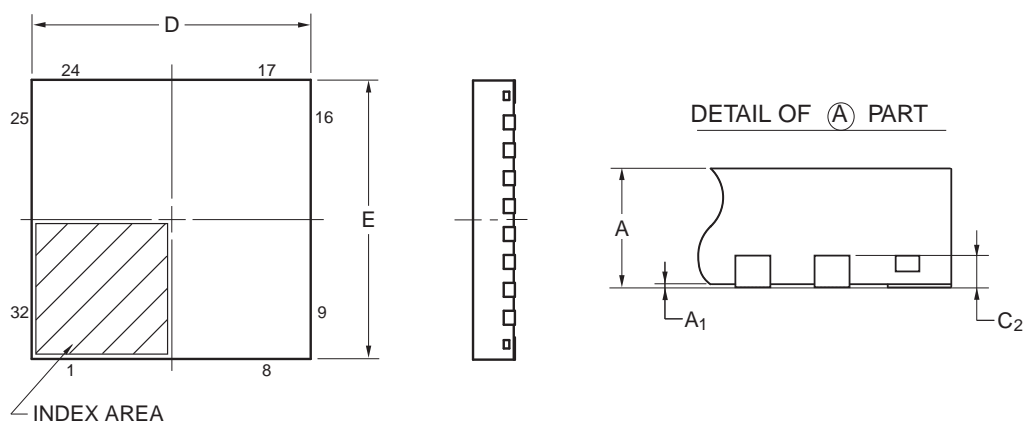
NOTE
 Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS |
|------|--|
| A | 9.85±0.15 |
| B | 0.45 MAX. |
| C | 0.65 (T.P.) |
| D | 0.24 ^{+0.08} _{-0.07} |
| E | 0.1±0.05 |
| F | 1.3±0.1 |
| G | 1.2 |
| H | 8.1±0.2 |
| I | 6.1±0.2 |
| J | 1.0±0.2 |
| K | 0.17±0.03 |
| L | 0.5 |
| M | 0.13 |
| N | 0.10 |
| P | 3° ^{+5°} _{-3°} |
| T | 0.25 |
| U | 0.6±0.15 |

4.5 32-pin Products

R5F100BAANA, R5F100BCANA, R5F100BDANA, R5F100BEANA, R5F100BFANA, R5F100BGANA
 R5F101BAANA, R5F101BCANA, R5F101BDANA, R5F101BEANA, R5F101BFANA, R5F101BGANA
 R5F100BADNA, R5F100BCDNA, R5F100BDDNA, R5F100BEDNA, R5F100BFDNA, R5F100BGDNA
 R5F101BADNA, R5F101BCDNA, R5F101BDDNA, R5F101BEDNA, R5F101BFDNA, R5F101BGDNA
 R5F100BAGNA, R5F100BCGNA, R5F100BDGNA, R5F100BEGNA, R5F100BFGNA, R5F100BGGNA

| | | | |
|--------------------|--------------|----------------|----------------|
| JEITA Package code | RENESAS code | Previous code | MASS (TYP.)[g] |
| P-HWQFN32-5x5-0.50 | PWQN0032KB-A | P32K8-50-3B4-5 | 0.06 |



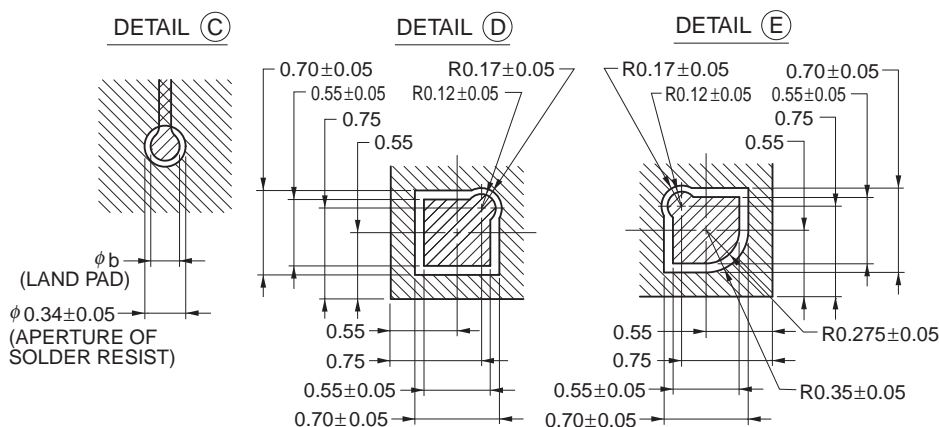
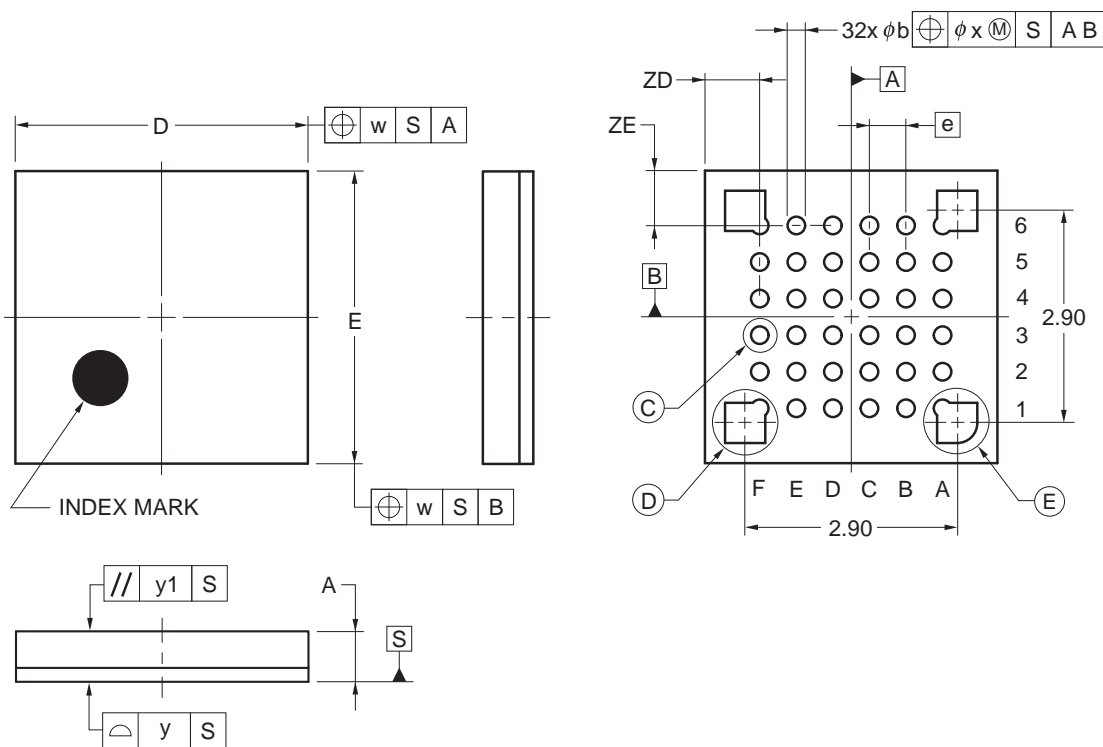
| Reference Symbol | Dimension in Millimeters | | |
|------------------|--------------------------|------|------|
| | Min | Nom | Max |
| D | 4.95 | 5.00 | 5.05 |
| E | 4.95 | 5.00 | 5.05 |
| A | — | — | 0.80 |
| A ₁ | 0.00 | — | — |
| b | 0.18 | 0.25 | 0.30 |
| e | — | 0.50 | — |
| L _p | 0.30 | 0.40 | 0.50 |
| x | — | — | 0.05 |
| y | — | — | 0.05 |
| Z _D | — | 0.75 | — |
| Z _E | — | 0.75 | — |
| c ₂ | 0.15 | 0.20 | 0.25 |
| D ₂ | — | 3.50 | — |
| E ₂ | — | 3.50 | — |

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4.6 36-pin Products

R5F100CAALA, R5F100CCALA, R5F100CDALA, R5F100CEALA, R5F100CFALA, R5F100CGALA
 R5F101CAALA, R5F101CCALA, R5F101CDALA, R5F101CEALA, R5F101CFALA, R5F101CGALA
 R5F100CAGLA, R5F100CCGLA, R5F100CDGLA, R5F100CEGLA, R5F100CFGLA, R5F100CGGLA

| | | | |
|--------------------|--------------|----------------|-----------------|
| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
| P-WFLGA36-4x4-0.50 | PWLG0036KA-A | P36FC-50-AA4-2 | 0.023 |



(UNIT:mm)

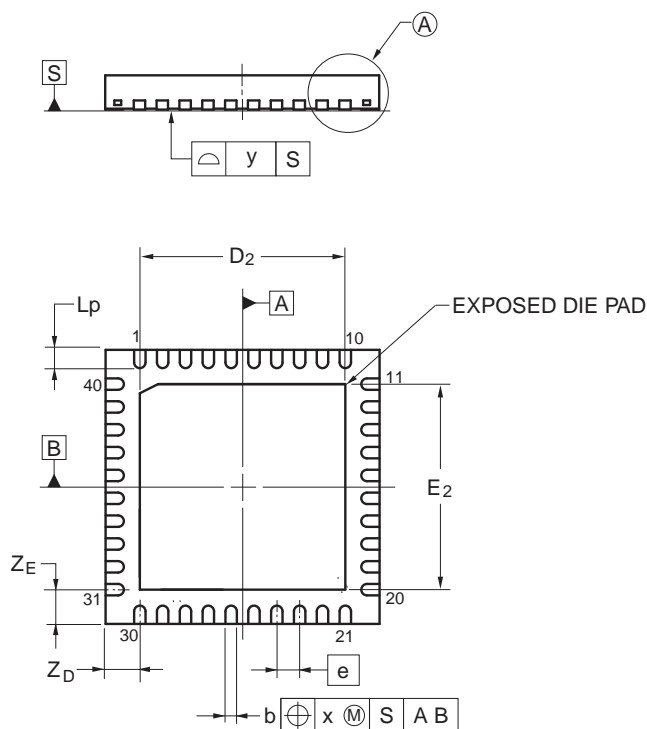
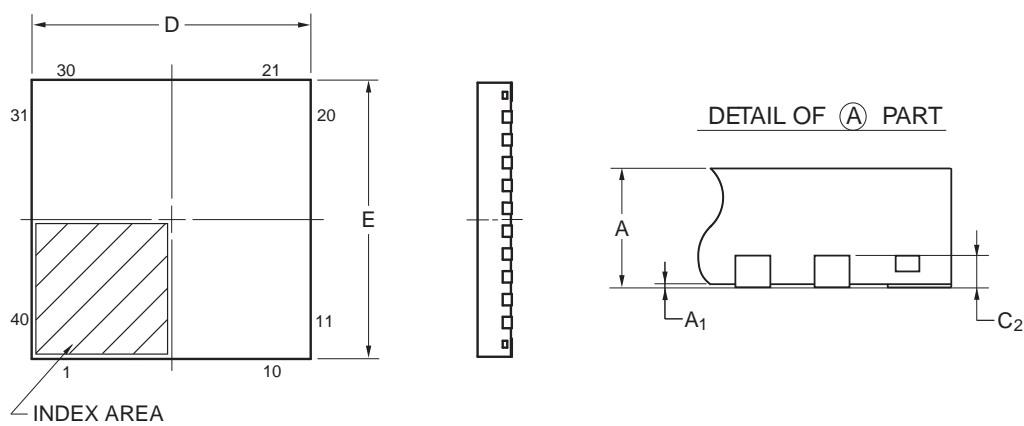
| ITEM | DIMENSIONS |
|------|------------|
| D | 4.00±0.10 |
| E | 4.00±0.10 |
| w | 0.20 |
| e | 0.50 |
| A | 0.69±0.07 |
| b | 0.24±0.05 |
| x | 0.05 |
| y | 0.08 |
| y1 | 0.20 |
| ZD | 0.75 |
| ZE | 0.75 |

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4.7 40-pin Products

R5F100EAANA, R5F100ECANA, R5F100EDANA, R5F100EEANA, R5F100EFANA, R5F100EGANA, R5F100EHANA
 R5F101EAANA, R5F101ECANA, R5F101EDANA, R5F101EEANA, R5F101EFANA, R5F101EGANA, R5F101EHANA
 R5F100EADNA, R5F100ECDNA, R5F100EDDNA, R5F100EEDNA, R5F100EFDNA, R5F100EGDNA, R5F100EHDNA
 R5F101EADNA, R5F101ECDNA, R5F101EDDNA, R5F101EEDNA, R5F101EFDNA, R5F101EGDNA, R5F101EHDNA
 R5F100EAGNA, R5F100ECGNA, R5F100EDGNA, R5F100EEGNA, R5F100EFGNA, R5F100EGGNA, R5F100EHGNA

| JEITA Package code | RENESAS code | Previous code | MASS (TYP) [g] |
|--------------------|--------------|----------------|----------------|
| P-HWQFN40-6x6-0.50 | PWQN0040KC-A | P40K8-50-4B4-5 | 0.09 |



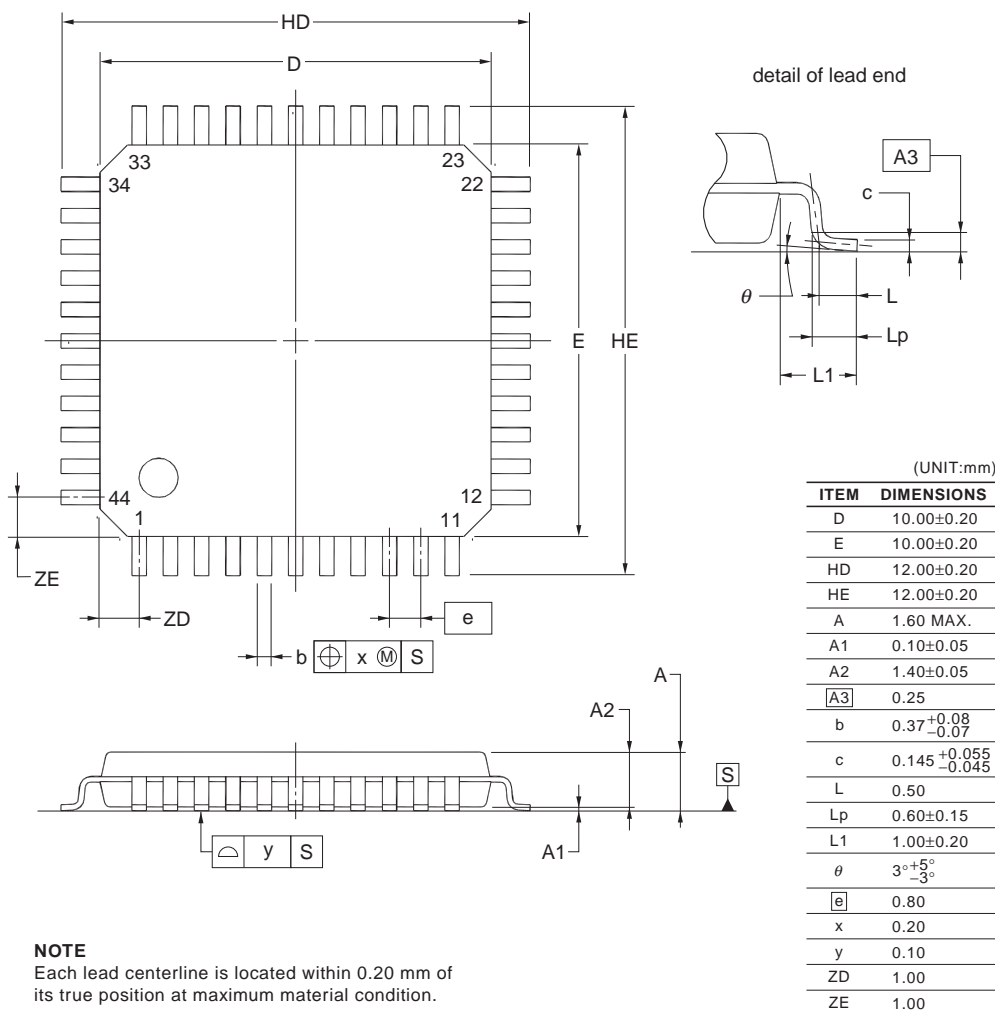
| Reference Symbol | Dimension in Millimeters | | |
|------------------|--------------------------|------|------|
| | Min | Nom | Max |
| D | 5.95 | 6.00 | 6.05 |
| E | 5.95 | 6.00 | 6.05 |
| A | — | — | 0.80 |
| A ₁ | 0.00 | — | — |
| b | 0.18 | 0.25 | 0.30 |
| e | — | 0.50 | — |
| L _p | 0.30 | 0.40 | 0.50 |
| x | — | — | 0.05 |
| y | — | — | 0.05 |
| Z _D | — | 0.75 | — |
| Z _E | — | 0.75 | — |
| c ₂ | 0.15 | 0.20 | 0.25 |
| D ₂ | — | 4.50 | — |
| E ₂ | — | 4.50 | — |

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4.8 44-pin Products

R5F100FAAFP, R5F100FCAFP, R5F100FDAFP, R5F100FEAFP, R5F100FFAFP, R5F100FGAFP, R5F100FHAFP, R5F100FJAFP, R5F100FKAFP, R5F100FLAFP
 R5F101FAAFP, R5F101FCAFP, R5F101FDAFP, R5F101FEAFP, R5F101FFAFP, R5F101FGAFP, R5F101FHAFP, R5F101FJAFP, R5F101FKAFP, R5F101FLAFP
 R5F100FADFP, R5F100FCDFP, R5F100FDDFP, R5F100FEDFP, R5F100FFDFP, R5F100FGDFP, R5F100FHDFP, R5F100FJDFP, R5F100FKDFP, R5F100FLDFP
 R5F101FADFP, R5F101FCDFP, R5F101FDDFP, R5F101FEDFP, R5F101FFDFP, R5F101FGDFP, R5F101FHDFP, R5F101FJDFP, R5F101FKDFP, R5F101FLDFP
 R5F100FAGFP, R5F100FCGFP, R5F100FDGFP, R5F100FEGFP, R5F100FFGFP, R5F100FGGFP, R5F100FHGFP, R5F100FJGFP

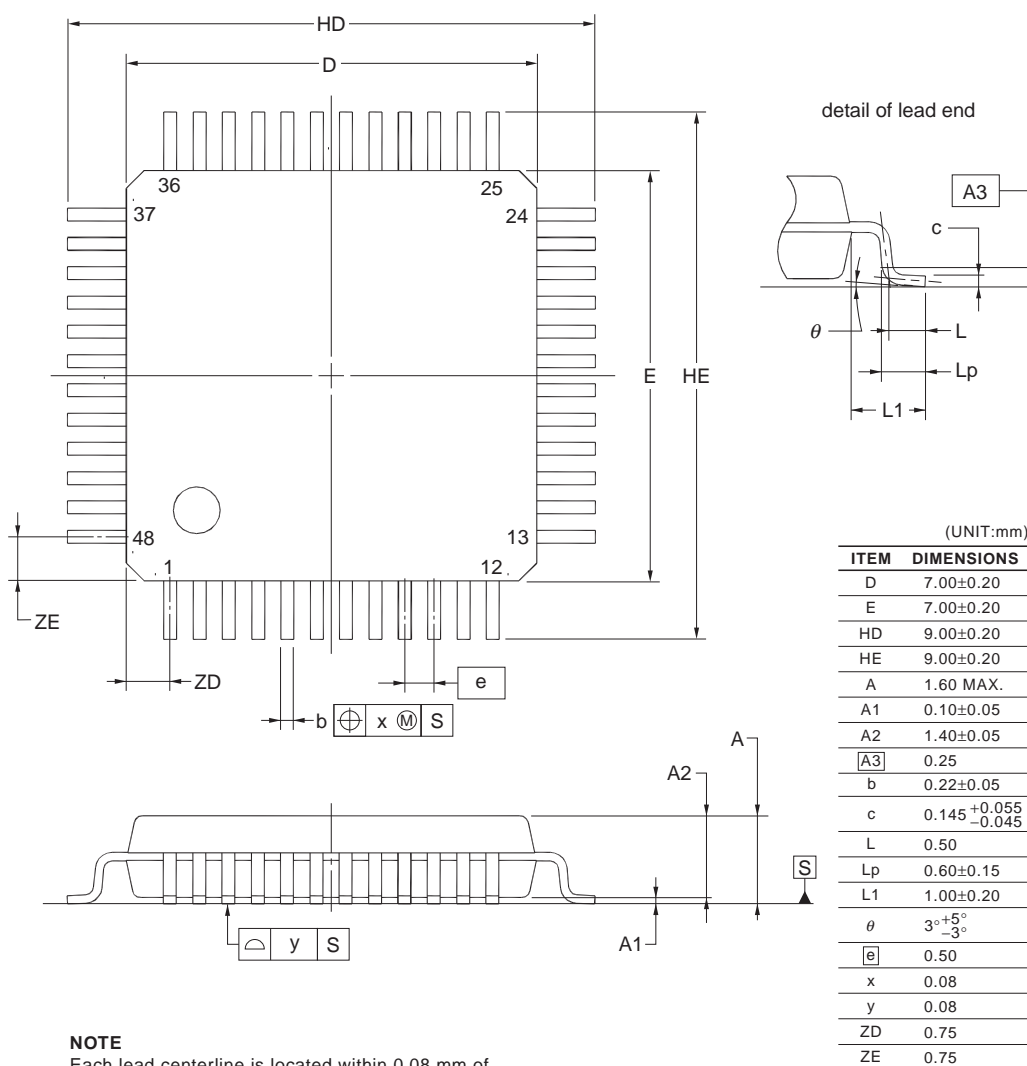
| | | | |
|---------------------|--------------|----------------|-----------------|
| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
| P-LQFP44-10x10-0.80 | PLQP0044GC-A | P44GB-80-UES-2 | 0.36 |



4.9 48-pin Products

R5F100GAAFB, R5F100GCAFB, R5F100GDAFB, R5F100GEAFB, R5F100GFAFB, R5F100GGAFB, R5F100GHAFB, R5F100GJAFB, R5F100GKAFB, R5F100GLAFB
 R5F101GAAFB, R5F101GCAFB, R5F101GDAFB, R5F101GEAFB, R5F101GFAFB, R5F101GGAFB, R5F101GHAFB, R5F101GJAFB, R5F101GKAFB, R5F101GLAFB
 R5F100GADFB, R5F100GCDFB, R5F100GDDFB, R5F100GEDFB, R5F100GFDFB, R5F100GGDFB, R5F100GHDFB, R5F100GJDFB, R5F100GKDFB, R5F100GLDFB
 R5F101GADFB, R5F101GCDFB, R5F101GDDFB, R5F101GEDFB, R5F101GFDFB, R5F101GGDFB, R5F101GHDFB, R5F101GJDFB, R5F101GKDFB, R5F101GLDFB
 R5F100GAGFB, R5F100GCGFB, R5F100GDGFB, R5F100GEGFB, R5F100GFGFB, R5F100GGGFB, R5F100GHGFB, R5F100GJGFB

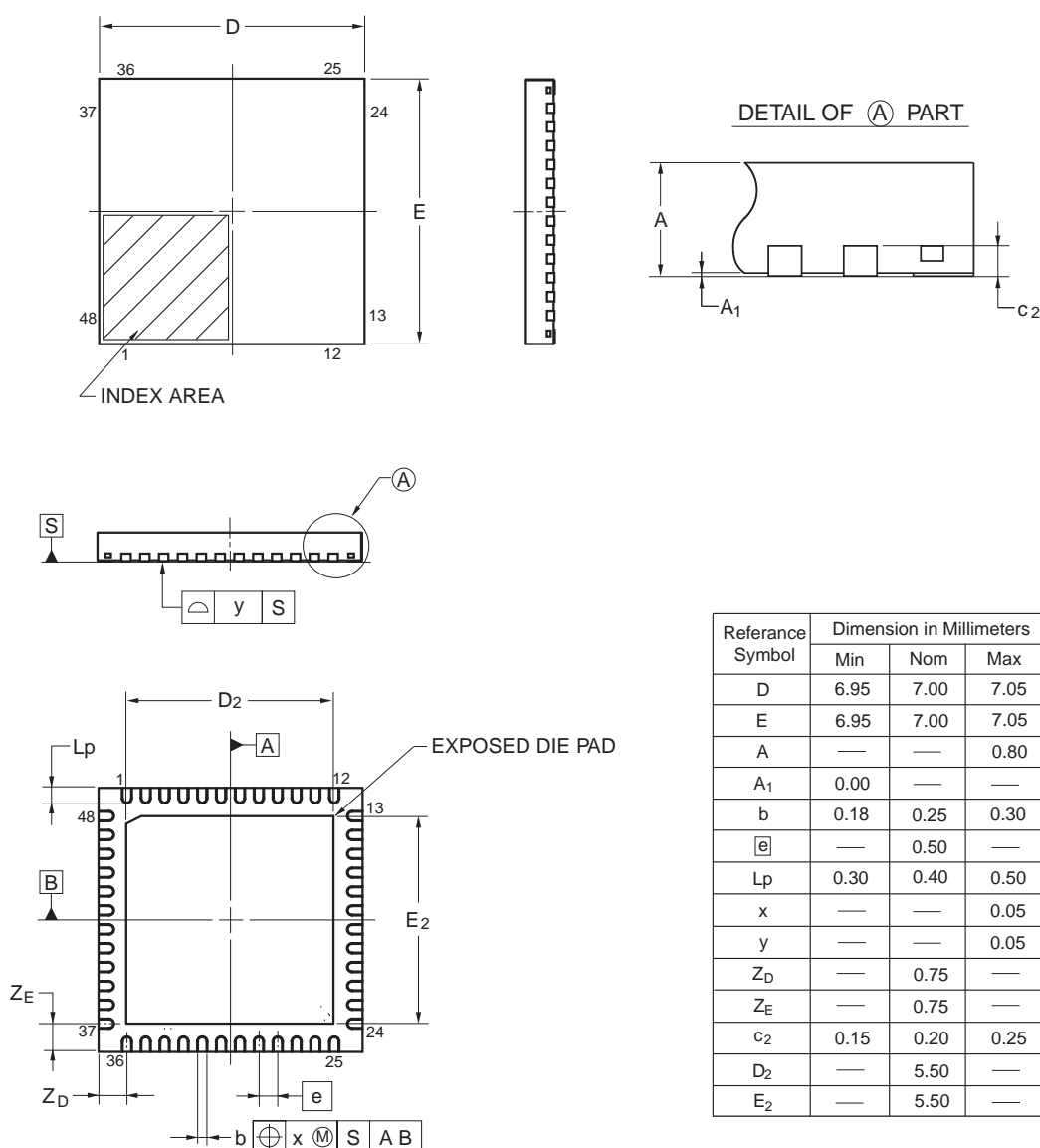
| | | | |
|--------------------|--------------|----------------|-----------------|
| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
| P-LFQFP48-7x7-0.50 | PLQP0048KF-A | P48GA-50-8EU-1 | 0.16 |



NOTE
 Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

R5F100GAANA, R5F100GCANA, R5F100GDANA, R5F100GEANA, R5F100GFANA, R5F100GGANA,
 R5F100GHANA, R5F100GJANA, R5F100GKANA, R5F100GLANA
 R5F101GAANA, R5F101GCANA, R5F101GDANA, R5F101GEANA, R5F101GFANA, R5F101GGANA,
 R5F101GHANA, R5F101GJANA, R5F101GKANA, R5F101GLANA
 R5F100GADNA, R5F100GCDNA, R5F100GDDNA, R5F100GEDNA, R5F100GFDNA, R5F100GGDNA,
 R5F100GHDNA, R5F100GJDNA, R5F100GKDNA, R5F100GLDNA
 R5F101GADNA, R5F101GCDNA, R5F101GDDNA, R5F101GEDNA, R5F101GFDNA, R5F101GGDNA,
 R5F101GHDNA, R5F101GJDNA, R5F101GKDNA, R5F101GLDNA
 R5F100GAGNA, R5F100GCGNA, R5F100GDGNA, R5F100GEGNA, R5F100GFGNA, R5F100GGGNA,
 R5F100GHGNA, R5F100GJGNA

| JEITA Package code | RENESAS code | Previous code | MASS(TYP.)[g] |
|--------------------|--------------|---------------------------|---------------|
| P-HWQFN48-7x7-0.50 | PWQN0048KB-A | 48PJN-A P48K8-50-5B4-6 | 0.13 |

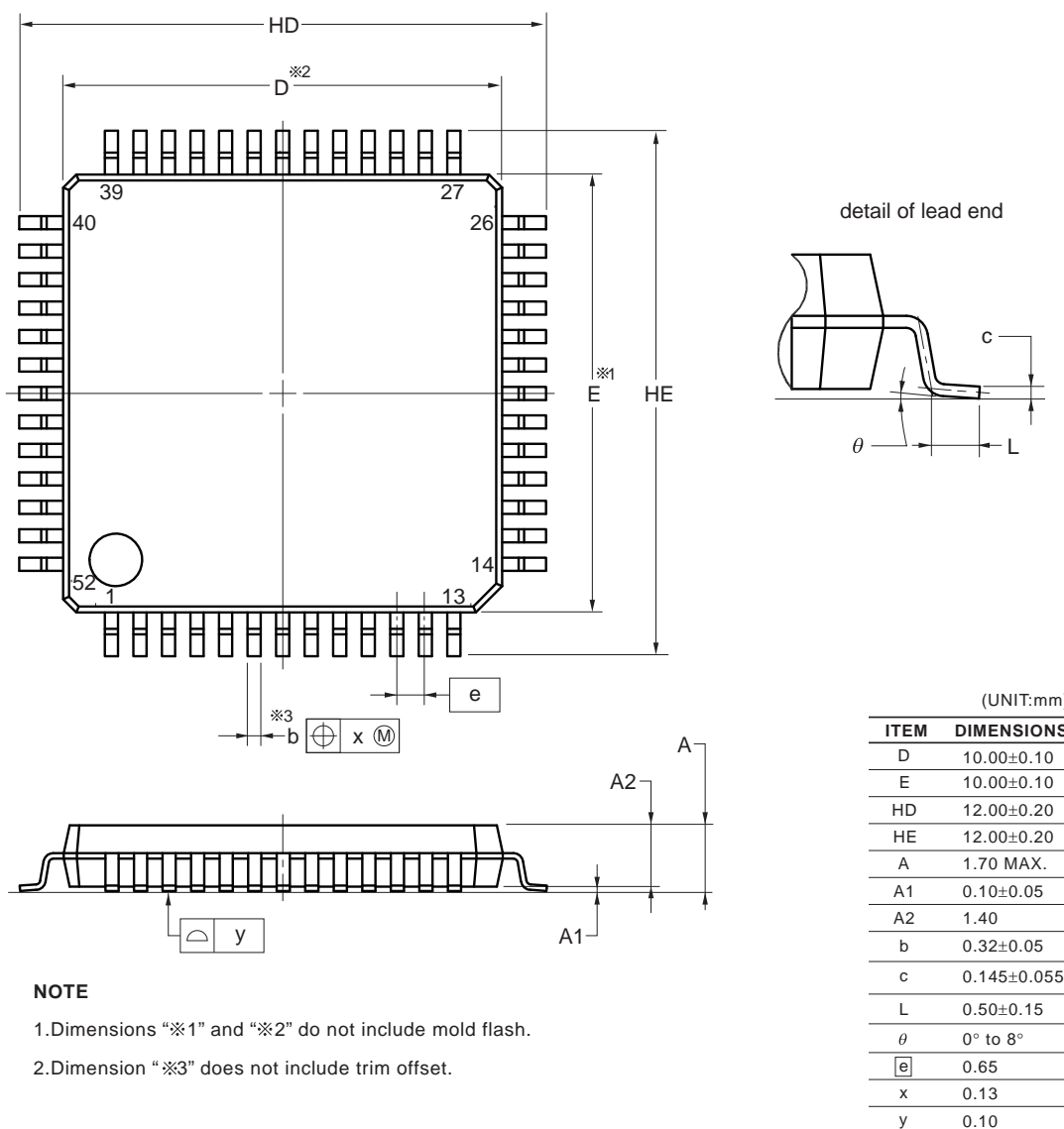


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4.10 52-pin Products

R5F100JCAFA, R5F100JDAFA, R5F100JEAFA, R5F100JFAFA, R5F100JGAFA, R5F100JHAFA, R5F100JJFAFA,
 R5F100JKFAFA, R5F100JLAFA
 R5F101JCAFA, R5F101JDAFA, R5F101JEAFA, R5F101JFAFA, R5F101JGAFA, R5F101JHAFA, R5F101JJFAFA,
 R5F101JKFAFA, R5F101JLAFA
 R5F100JCDFA, R5F100JDDFA, R5F100JEDFA, R5F100JFDFA, R5F100JGDFA, R5F100JHDFA, R5F100JJDFA,
 R5F100JKDFA, R5F100JLDFA
 R5F101JCDFA, R5F101JDDFA, R5F101JEDFA, R5F101JFDFA, R5F101JGDFA, R5F101JHDFA, R5F101JJDFA,
 R5F101JKDFA, R5F101JLDFA
 R5F100JCGFA, R5F100JDGFA, R5F100JEGFA, R5F100JFGFA, R5F100JGGFA, R5F100JHGFA, R5F100JJGFA

| | | | |
|---------------------|--------------|----------------|-----------------|
| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
| P-LQFP52-10x10-0.65 | PLQP0052JA-A | P52GB-65-GBS-1 | 0.3 |



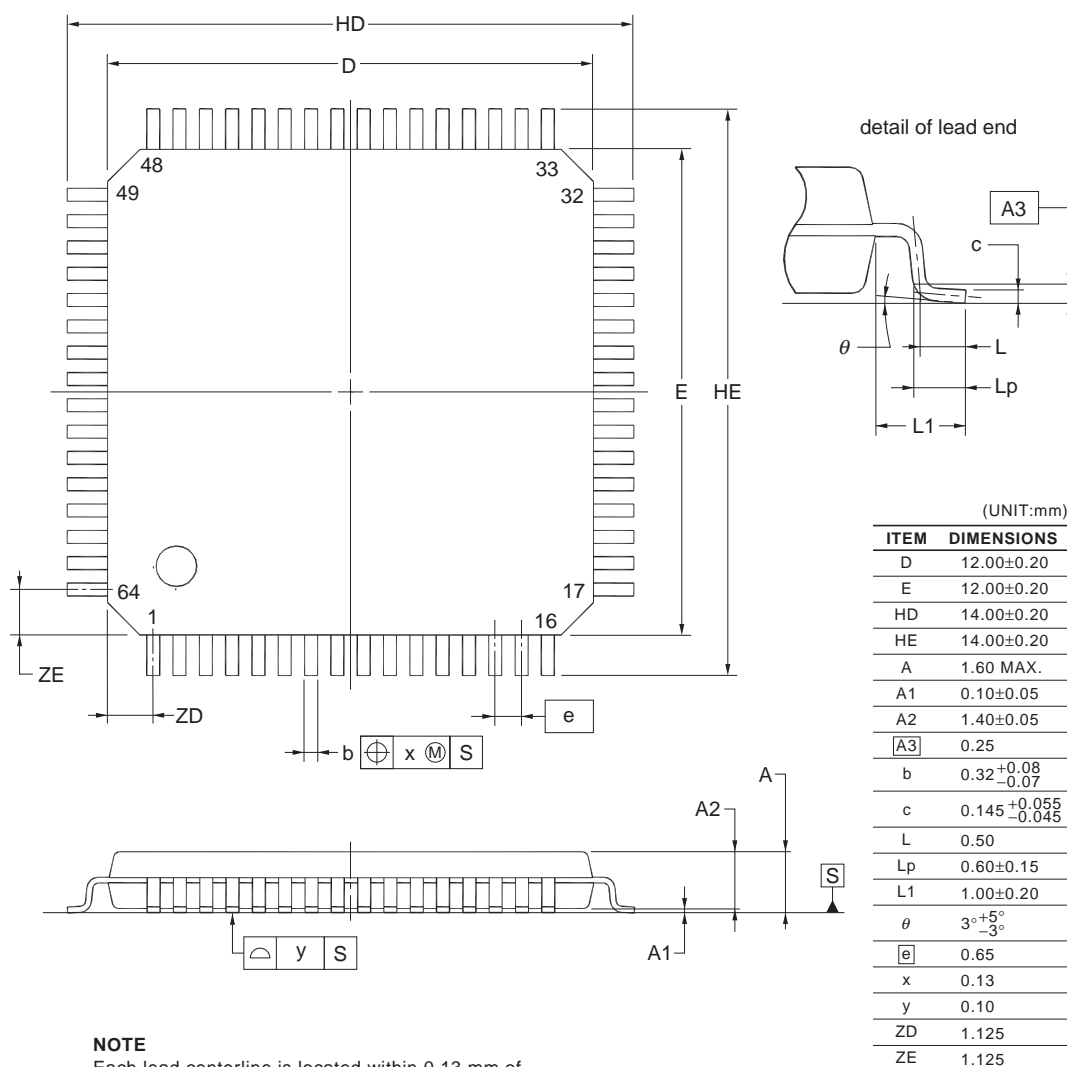
NOTE

1. Dimensions “*1” and “*2” do not include mold flash.
2. Dimension “*3” does not include trim offset.

4.11 64-pin Products

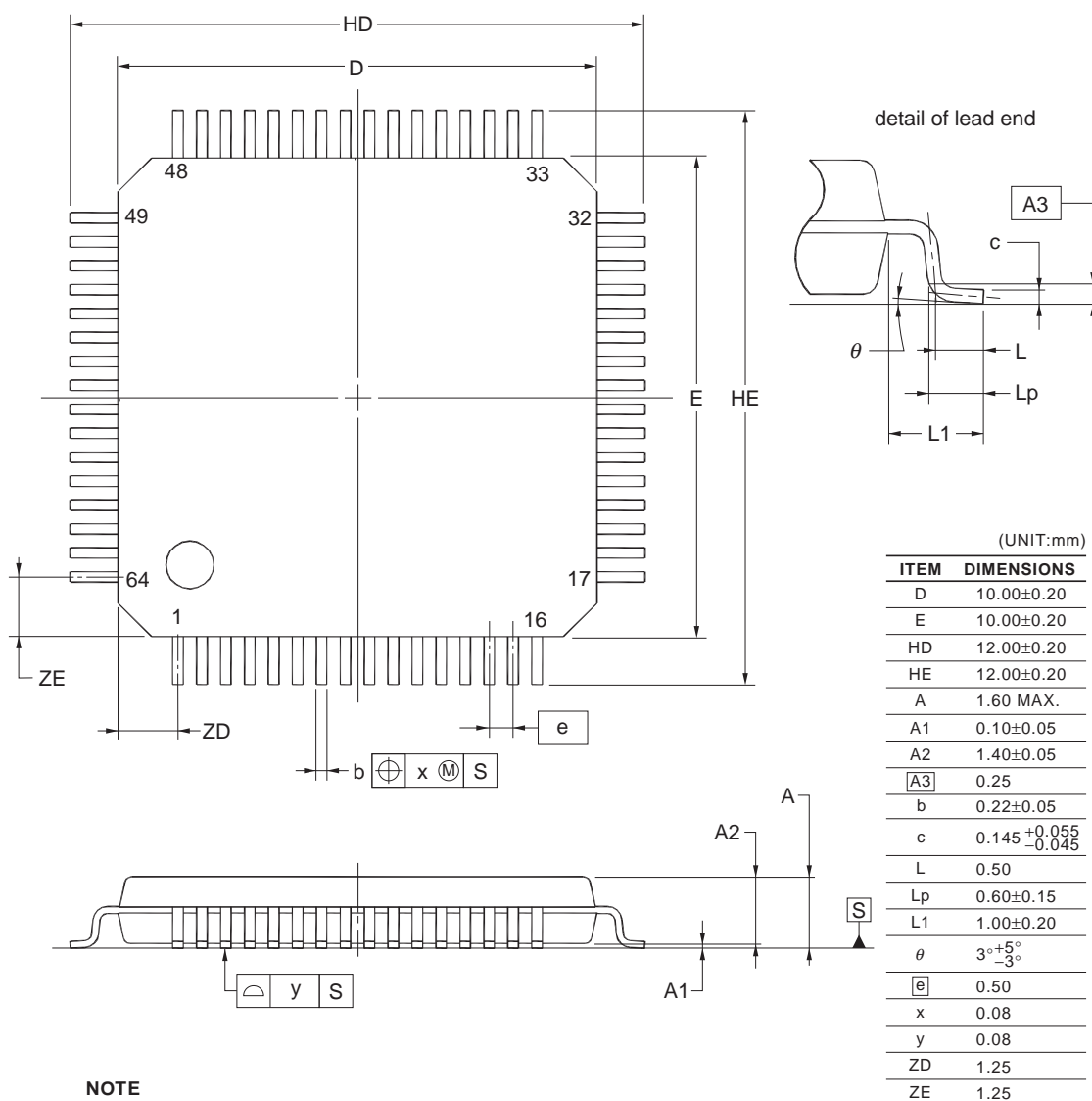
R5F100LCAFA, R5F100LDAFA, R5F100LEAFA, R5F100LFAFA, R5F100LGAFA, R5F100LHAFA, R5F100LJafa,
 R5F100LKafa, R5F100LLafa
 R5F101LCAFA, R5F101LDAFA, R5F101LEAFA, R5F101LFAFA, R5F101LGAFA, R5F101LHAFA, R5F101LJafa,
 R5F101LKafa, R5F101LLafa
 R5F100LCDFa, R5F100LDDFa, R5F100LEDFa, R5F100LFDfA, R5F100LGDfA, R5F100LHDfA, R5F100LJDfA,
 R5F100LKDFa, R5F100LLDFa
 R5F101LCDFa, R5F101LDDFa, R5F101LEDFa, R5F101LFDfA, R5F101LGDfA, R5F101LHDfA, R5F101LJDfA,
 R5F101LKDFa, R5F101LLDFa
 R5F100LCGFa, R5F100LDGFa, R5F100LEGFa, R5F100LFGfA, R5F100LGGfA, R5F100LHGfA, R5F100LJGfA

| | | | |
|---------------------|--------------|----------------|-----------------|
| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
| P-LQFP64-12x12-0.65 | PLQP0064JA-A | P64GK-65-UET-2 | 0.51 |



R5F100LCAFB, R5F100LDAFB, R5F100LEAFB, R5F100LFAFB, R5F100LGAFB, R5F100LHAFB, R5F100LJAFB,
 R5F100LKAFB, R5F100LLAFB
 R5F101LCAFB, R5F101LDAFB, R5F101LEAFB, R5F101LFAFB, R5F101LGAFB, R5F101LHAFB, R5F101LJAFB,
 R5F101LKAFB, R5F101LLAFB
 R5F100LCDFB, R5F100LDDFB, R5F100LEDFB, R5F100LDFDB, R5F100LGDFB, R5F100LHDFB, R5F100LJDFB,
 R5F100LKDFB, R5F100LLDFB
 R5F101LCDFB, R5F101LDDFB, R5F101LEDFB, R5F101LDFDB, R5F101LGDFB, R5F101LHDFB, R5F101LJDFB,
 R5F101LKDFB, R5F101LLDFB
 R5F100LCGFB, R5F100LDGFB, R5F100LEGFB, R5F100LFGFB, R5F100LGGFB, R5F100LHGFB, R5F100LJGFB

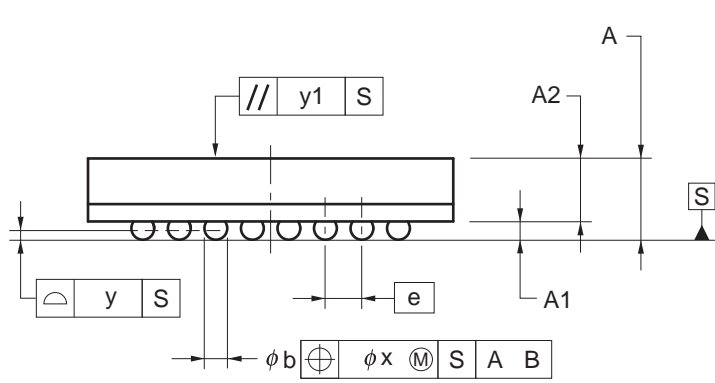
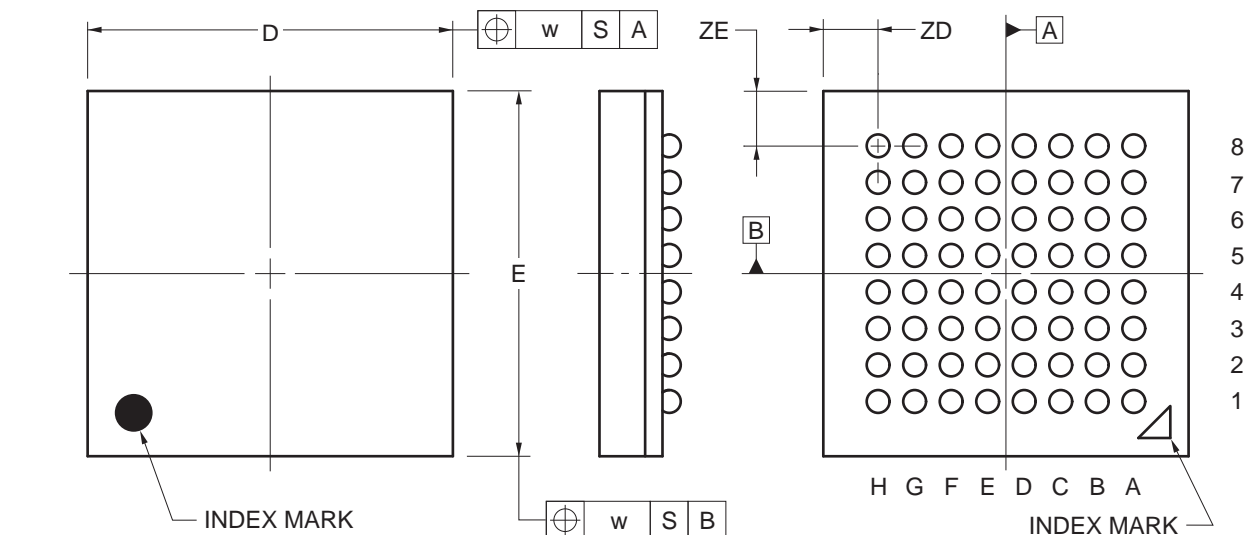
| | | | |
|----------------------|--------------|----------------|-----------------|
| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
| P-LFQFP64-10x10-0.50 | PLQP0064KF-A | P64GB-50-UEU-2 | 0.35 |



NOTE
 Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

R5F100LCABG, R5F100LDABG, R5F100LEABG, R5F100LFABG, R5F100LGABG, R5F100LHABG, R5F100LJABG
 R5F101LCABG, R5F101LDABG, R5F101LEABG, R5F101LFABG, R5F101LGABG, R5F101LHABG, R5F101LJABG
 R5F100LCGBG, R5F100LDGBG, R5F100LEGBG, R5F100LFGBG, R5F100LGGBG, R5F100LHGBG, R5F100LJGBG

| | | | |
|--------------------|--------------|----------------|-----------------|
| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
| P-VFBGA64-4x4-0.40 | PVBG0064LA-A | P64F1-40-AA2-2 | 0.03 |



(UNIT:mm)

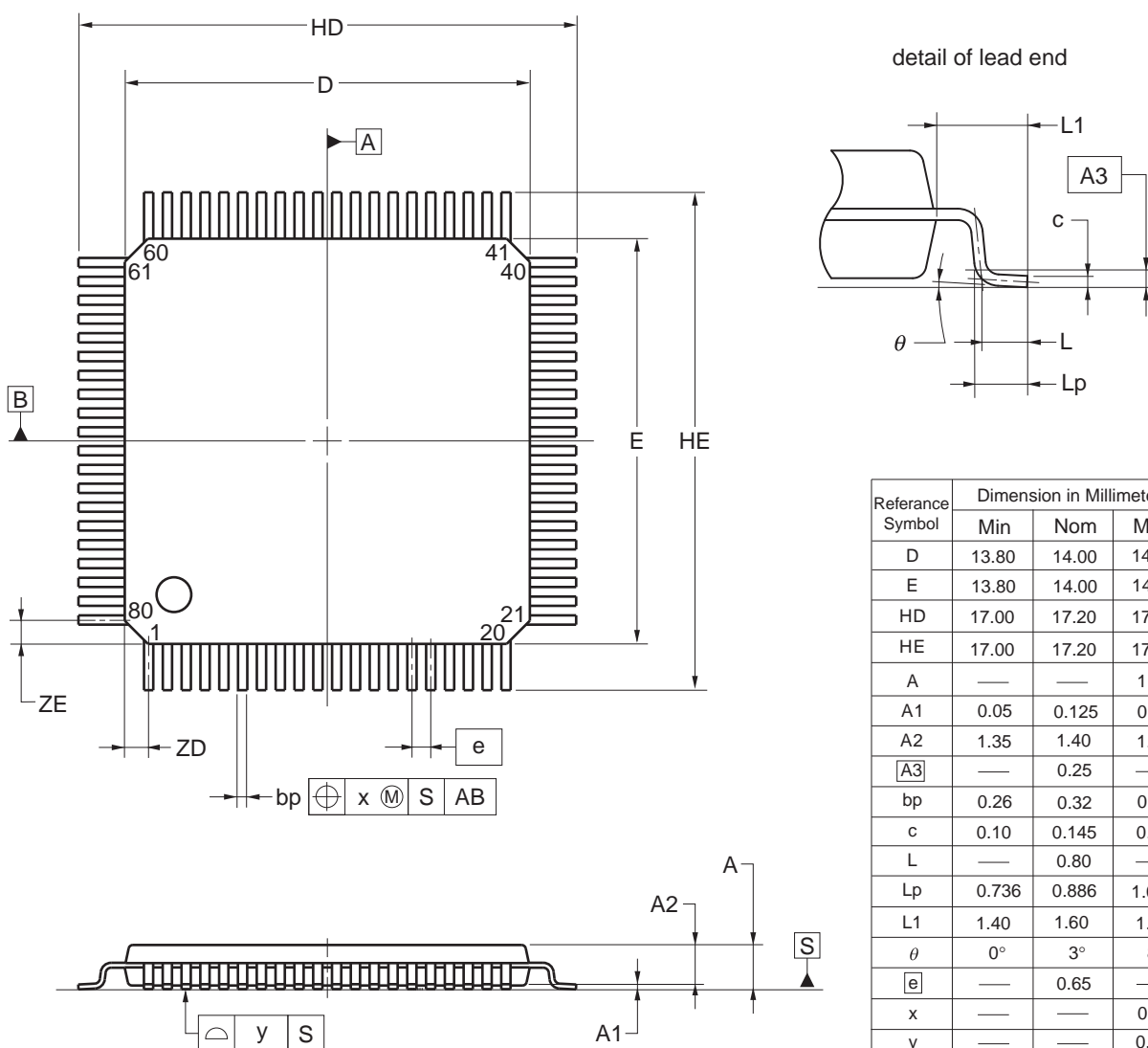
| ITEM | DIMENSIONS |
|------|------------|
| D | 4.00±0.10 |
| E | 4.00±0.10 |
| w | 0.15 |
| A | 0.89±0.10 |
| A1 | 0.20±0.05 |
| A2 | 0.69 |
| e | 0.40 |
| b | 0.25±0.05 |
| x | 0.05 |
| y | 0.08 |
| y1 | 0.20 |
| ZD | 0.60 |
| ZE | 0.60 |

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4.12 80-pin Products

R5F100MFAFA, R5F100MGafa, R5F100MHafa, R5F100MJafa, R5F100MKafa, R5F100MLafa
 R5F101MFAFA, R5F101MGafa, R5F101MHafa, R5F101MJafa, R5F101MKafa, R5F101MLafa
 R5F100MFDFA, R5F100MGDFA, R5F100MHDFA, R5F100MJDFA, R5F100MKDFA, R5F100MLDFA
 R5F101MFDFA, R5F101MGDFA, R5F101MHDFA, R5F101MJDFA, R5F101MKDFA, R5F101MLDFA
 R5F100MFGFA, R5F100MGGFA, R5F100MHGFA, R5F100MJGFA

| | | | |
|---------------------|--------------|----------------|----------------|
| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP) [g] |
| P-LQFP80-14x14-0.65 | PLQP0080JB-E | P80GC-65-UBT-2 | 0.69 |

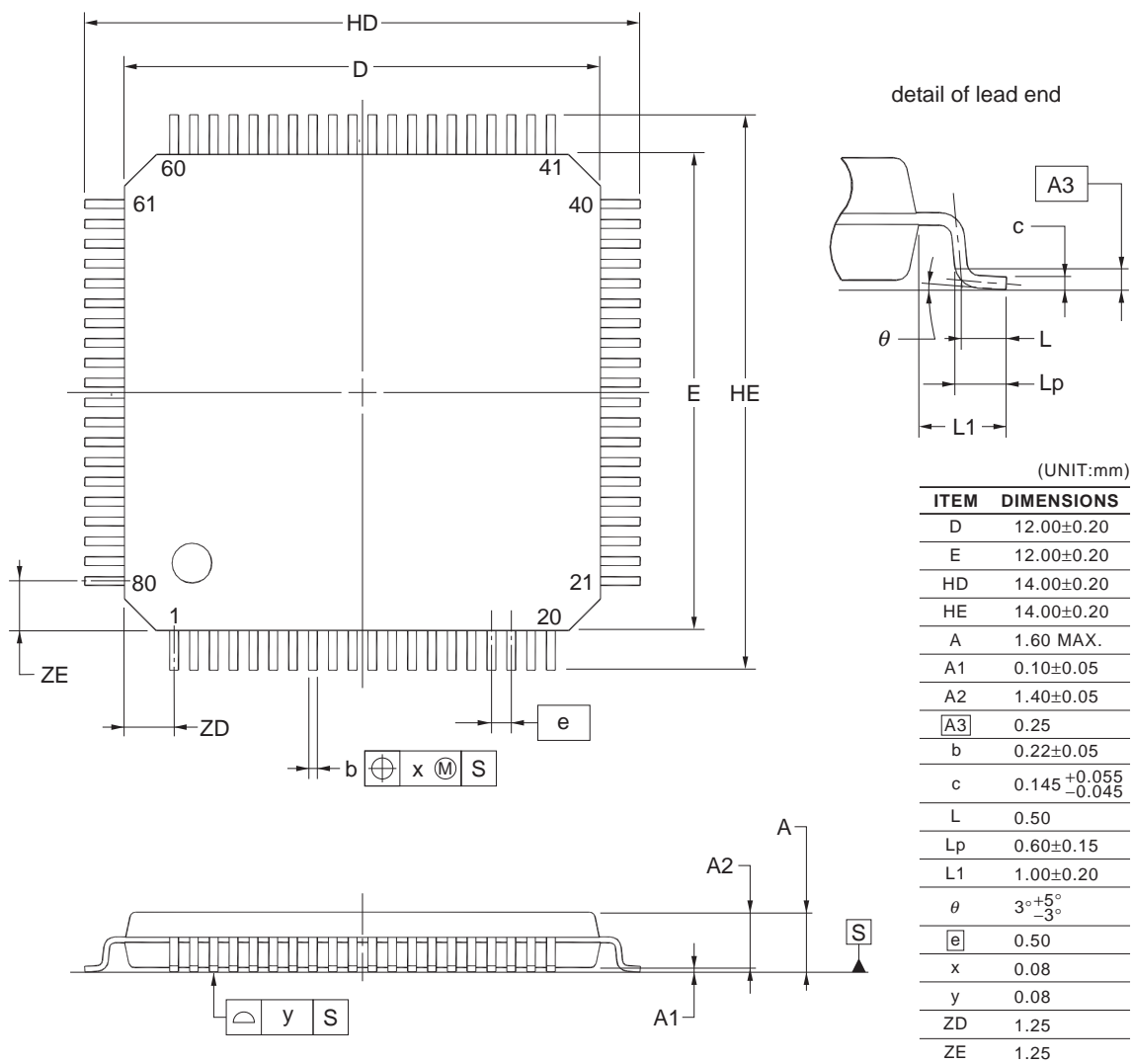


| Reference Symbol | Dimension in Millimeters | | |
|------------------|--------------------------|-------|-------|
| | Min | Nom | Max |
| D | 13.80 | 14.00 | 14.20 |
| E | 13.80 | 14.00 | 14.20 |
| HD | 17.00 | 17.20 | 17.40 |
| HE | 17.00 | 17.20 | 17.40 |
| A | — | — | 1.70 |
| A1 | 0.05 | 0.125 | 0.20 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | — | 0.25 | — |
| bp | 0.26 | 0.32 | 0.38 |
| c | 0.10 | 0.145 | 0.20 |
| L | — | 0.80 | — |
| Lp | 0.736 | 0.886 | 1.036 |
| L1 | 1.40 | 1.60 | 1.80 |
| theta | 0° | 3° | 8° |
| e | — | 0.65 | — |
| x | — | — | 0.13 |
| y | — | — | 0.10 |
| ZD | — | 0.825 | — |
| ZE | — | 0.825 | — |

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R5F100MFAFB, R5F100MGAFB, R5F100MHAFB, R5F100MJAFB, R5F100MKAFB, R5F100MLAFB
 R5F101MFAFB, R5F101MGAFB, R5F101MHAFB, R5F101MJAFB, R5F101MKAFB, R5F101MLAFB
 R5F100MDFB, R5F100MGDFB, R5F100MHDFB, R5F100MJDFB, R5F100MKDFB, R5F100MLDFB
 R5F101MDFB, R5F101MGDFB, R5F101MHDFB, R5F101MJDFB, R5F101MKDFB, R5F101MLDFB
 R5F100MFGFB, R5F100MGGFB, R5F100MHGFB, R5F100MJGFB

| | | | |
|----------------------|--------------|----------------|-----------------|
| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
| P-LFQFP80-12x12-0.50 | PLQP0080KE-A | P80GK-50-8EU-2 | 0.53 |

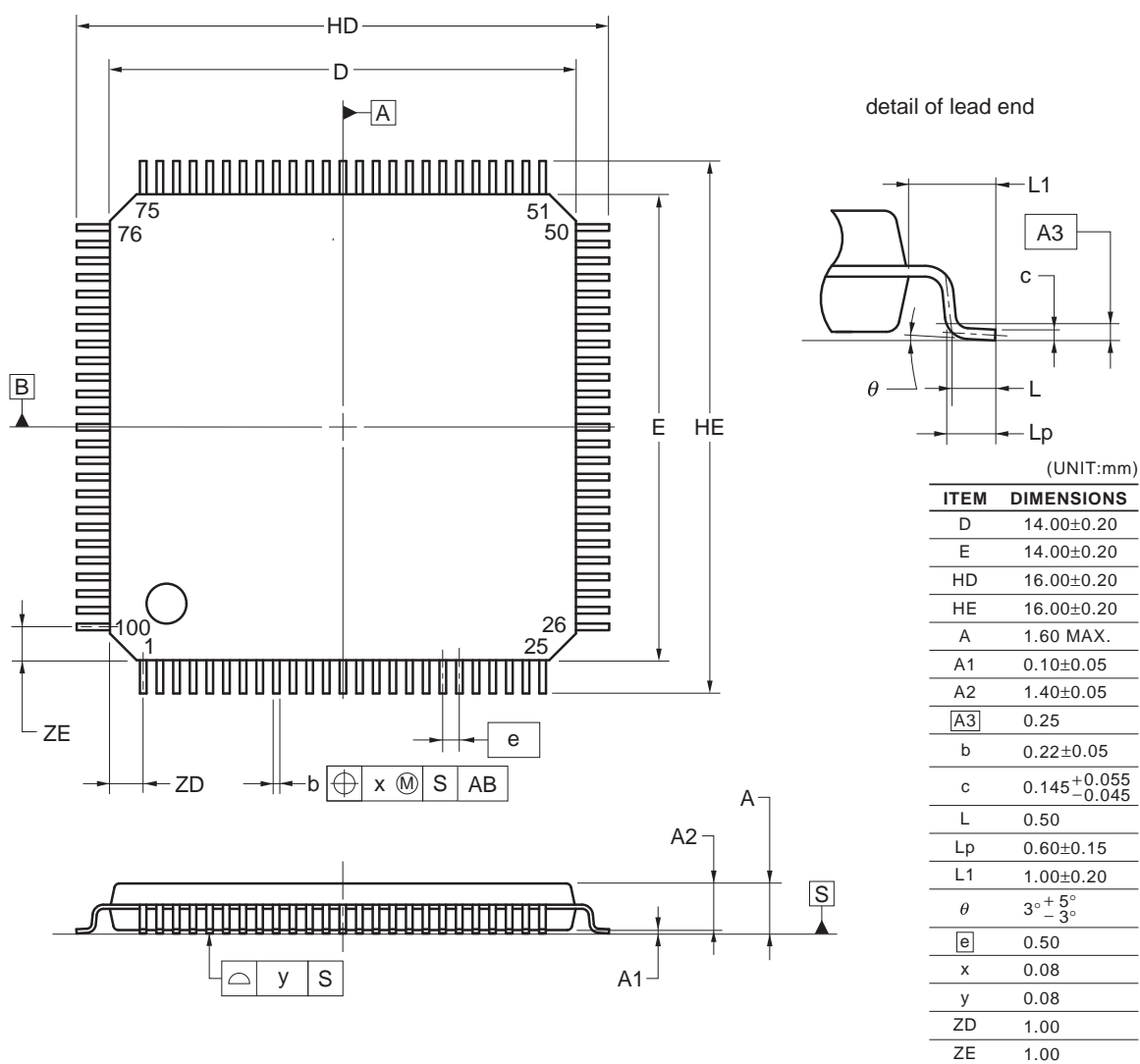


NOTE
 Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

4.13 100-pin Products

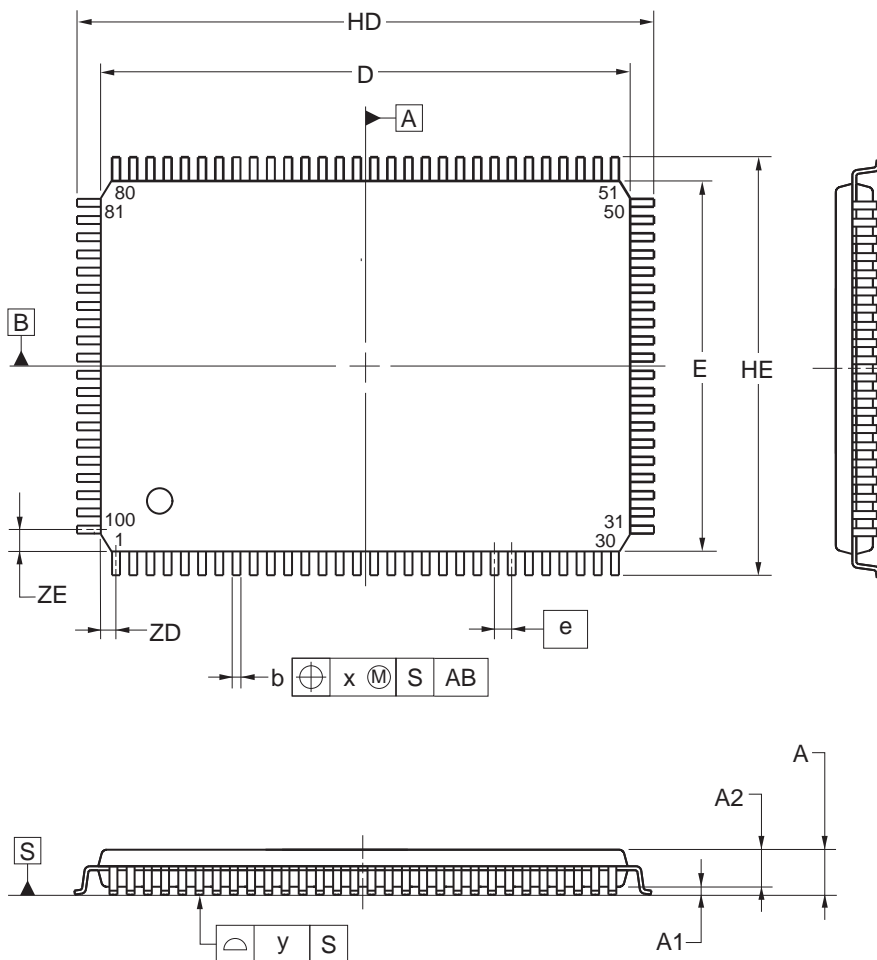
R5F100PFAFB, R5F100PGAFA, R5F100PHAFA, R5F100PJAFB, R5F100PKAFB, R5F100PLAFB
 R5F101PFAFB, R5F101PGAFA, R5F101PHAFA, R5F101PJAFB, R5F101PKAFB, R5F101PLAFB
 R5F100PFDFA, R5F100PGDFA, R5F100PHDFA, R5F100PJDFB, R5F100PKDFA, R5F100PLDFA
 R5F101PFDFA, R5F101PGDFA, R5F101PHDFA, R5F101PJDFB, R5F101PKDFA, R5F101PLDFA
 R5F100PFGFB, R5F100PGGFB, R5F100PHGFB, R5F100PJGFB

| | | | |
|-----------------------|--------------|-----------------|-----------------|
| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
| P-LFQFP100-14x14-0.50 | PLQP0100KE-A | P100GC-50-GBR-1 | 0.69 |



R5F100PFAFA, R5F100PGAFA, R5F100PHAFA, R5F100PJAF A, R5F100PKAFA, R5F100PLAFA
 R5F101PFAFA, R5F101PGAFA, R5F101PHAFA, R5F101PJAF A, R5F101PKAFA, R5F101PLAFA
 R5F100PFDFA, R5F100PGDFA, R5F100PHDFA, R5F100PJDFA, R5F100PKDFA, R5F100PLDFA
 R5F101PFDFA, R5F101PGDFA, R5F101PHDFA, R5F101PJDFA, R5F101PKDFA, R5F101PLDFA
 R5F100PGGFA, R5F100PHGFA, R5F100PJGFA

| | | | |
|----------------------|--------------|-----------------|-----------------|
| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
| P-LQFP100-14x20-0.65 | PLQP0100JC-A | P100GF-65-GBN-1 | 0.92 |



detail of lead end

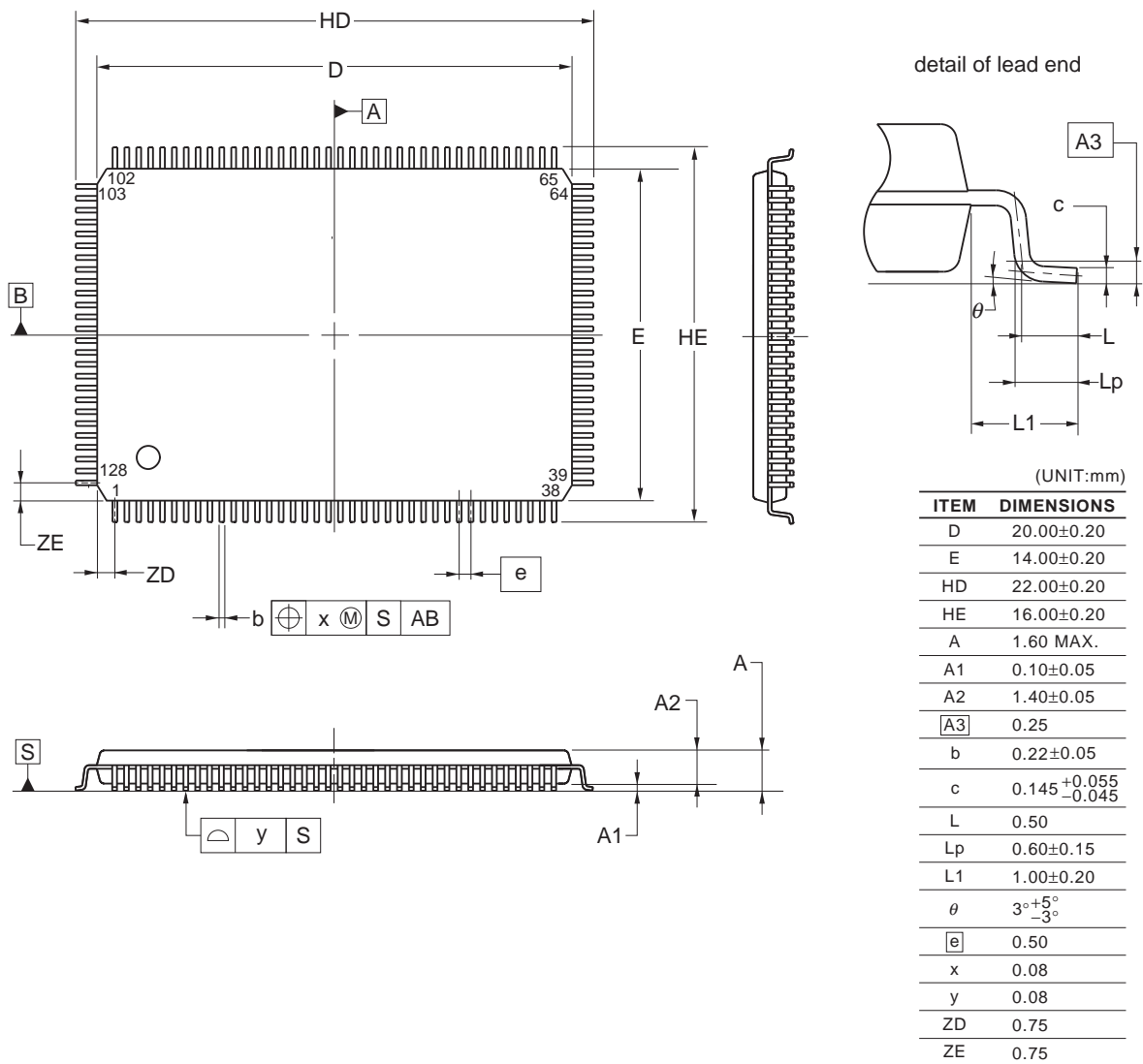
(UNIT:mm)

| ITEM | DIMENSIONS |
|------|---|
| D | 20.00±0.20 |
| E | 14.00±0.20 |
| HD | 22.00±0.20 |
| HE | 16.00±0.20 |
| A | 1.60 MAX. |
| A1 | 0.10±0.05 |
| A2 | 1.40±0.05 |
| A3 | 0.25 |
| b | 0.32 ^{+0.08} _{-0.07} |
| c | 0.145 ^{+0.055} _{-0.045} |
| L | 0.50 |
| Lp | 0.60±0.15 |
| L1 | 1.00±0.20 |
| θ | 3° ^{+5°} _{-3°} |
| e | 0.65 |
| x | 0.13 |
| y | 0.10 |
| ZD | 0.575 |
| ZE | 0.825 |

4.14 128-pin Products

R5F100SHAFB, R5F100SJAFB, R5F100SKAFB, R5F100SLAFB
 R5F101SHAFB, R5F101SJAFB, R5F101SKAFB, R5F101SLAFB
 R5F100SHDFB, R5F100SJDFB, R5F100SKDFB, R5F100SLDFB
 R5F101SHDFB, R5F101SJDFB, R5F101SKDFB, R5F101SLDFB

| | | | |
|-----------------------|--------------|-----------------|-----------------|
| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
| P-LFQFP128-14x20-0.50 | PLQP0128KD-A | P128GF-50-GBP-1 | 0.92 |



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| | |
|-------------------------|---------------------------|
| Revision History | RL78/G13 Datasheet |
|-------------------------|---------------------------|

| Rev. | Date | Description | |
|--------|---|-------------|--|
| | | Page | Summary |
| 1.00 | Feb 29, 2012 | - | First Edition issued |
| 2.00 | Oct 12, 2012 | 7 | Figure 1-1. Part Number, Memory Size, and Package of RL78/G13: Pin count corrected. |
| | | 25 | 1.4 Pin Identification: Description of pins INTP0 to INTP11 corrected. |
| | | 40, 42, 44 | 1.6 Outline of Functions: Descriptions of Subsystem clock, Low-speed on-chip oscillator, and General-purpose register corrected. |
| | | 41, 43, 45 | 1.6 Outline of Functions: Lists of Descriptions changed. |
| | | 59, 63, 67 | Descriptions of Note 8 in a table corrected. |
| | | 68 | (4) Common to RL78/G13 all products: Descriptions of Notes corrected. |
| | | 69 | 2.4 AC Characteristics: Symbol of external system clock frequency corrected. |
| | | 96 to 98 | 2.6.1 A/D converter characteristics: Notes of overall error corrected. |
| | | 100 | 2.6.2 Temperature sensor characteristics: Parameter name corrected. |
| | | 104 | 2.8 Flash Memory Programming Characteristics: Incorrect descriptions corrected. |
| | | 116 | 3.10 52-pin products: Package drawings of 52-pin products corrected. |
| | | 120 | 3.12 80-pin products: Package drawings of 80-pin products corrected. |
| 3.00 | Aug 02, 2013 | 1 | Modification of 1.1 Features |
| | | 3 | Modification of 1.2 List of Part Numbers |
| | | 4 to 15 | Modification of Table 1-1. List of Ordering Part Numbers, note, and caution |
| | | 16 to 32 | Modification of package type in 1.3.1 to 1.3.14 |
| | | 33 | Modification of description in 1.4 Pin Identification |
| | | 48, 50, 52 | Modification of caution, table, and note in 1.6 Outline of Functions |
| | | 55 | Modification of description in table of Absolute Maximum Ratings ($T_A = 25^{\circ}\text{C}$) |
| | | 57 | Modification of table, note, caution, and remark in 2.2.1 X1, XT1 oscillator characteristics |
| | | 57 | Modification of table in 2.2.2 On-chip oscillator characteristics |
| | | 58 | Modification of note 3 of table (1/5) in 2.3.1 Pin characteristics |
| | | 59 | Modification of note 3 of table (2/5) in 2.3.1 Pin characteristics |
| | | 63 | Modification of table in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products |
| | | 64 | Modification of notes 1 and 4 in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products |
| | | 65 | Modification of table in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products |
| | | 66 | Modification of notes 1, 5, and 6 in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products |
| | | 68 | Modification of notes 1 and 4 in (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products |
| | | 70 | Modification of notes 1, 5, and 6 in (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products |
| | | 72 | Modification of notes 1 and 4 in (3) Flash ROM: 384 to 512 KB of 44- to 100-pin products |
| | | 74 | Modification of notes 1, 5, and 6 in (3) Flash ROM: 384 to 512 KB of 44- to 100-pin products |
| | | 75 | Modification of (4) Peripheral Functions (Common to all products) |
| 77 | Modification of table in 2.4 AC Characteristics | | |
| 78, 79 | Addition of Minimum Instruction Execution Time during Main System Clock Operation | | |
| 80 | Modification of figures of AC Timing Test Points and External System Clock Timing | | |

| Rev. | Date | Description | |
|------|--|-------------|--|
| | | Page | Summary |
| 3.00 | Aug 02, 2013 | 81 | Modification of figure of AC Timing Test Points |
| | | 81 | Modification of description and note 3 in (1) During communication at same potential (UART mode) |
| | | 83 | Modification of description in (2) During communication at same potential (CSI mode) |
| | | 84 | Modification of description in (3) During communication at same potential (CSI mode) |
| | | 85 | Modification of description in (4) During communication at same potential (CSI mode) (1/2) |
| | | 86 | Modification of description in (4) During communication at same potential (CSI mode) (2/2) |
| | | 88 | Modification of table in (5) During communication at same potential (simplified I ² C mode) (1/2) |
| | | 89 | Modification of table and caution in (5) During communication at same potential (simplified I ² C mode) (2/2) |
| | | 91 | Modification of table and notes 1 and 4 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2) |
| | | 92, 93 | Modification of table and notes 2 to 7 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2) |
| | | 94 | Modification of remarks 1 to 4 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2) |
| | | 95 | Modification of table in (7) Communication at different potential (2.5 V, 3 V) (CSI mode) (1/2) |
| | | 96 | Modification of table and caution in (7) Communication at different potential (2.5 V, 3 V) (CSI mode) (2/2) |
| | | 97 | Modification of table in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/3) |
| | | 98 | Modification of table, note 1, and caution in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/3) |
| | | 99 | Modification of table, note 1, and caution in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (3/3) |
| | | 100 | Modification of remarks 3 and 4 in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (3/3) |
| | | 102 | Modification of table in (9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/2) |
| | | 103 | Modification of table and caution in (9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/2) |
| | | 106 | Modification of table in (10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I ² C mode) (1/2) |
| | | 107 | Modification of table, note 1, and caution in (10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I ² C mode) (2/2) |
| | | 109 | Addition of (1) I ² C standard mode |
| | | 111 | Addition of (2) I ² C fast mode |
| | | 112 | Addition of (3) I ² C fast mode plus |
| | | 112 | Modification of IICA serial transfer timing |
| | | 113 | Addition of table in 2.6.1 A/D converter characteristics |
| | | 113 | Modification of description in 2.6.1 (1) |
| 114 | Modification of notes 3 to 5 in 2.6.1 (1) | | |
| 115 | Modification of description and notes 2, 4, and 5 in 2.6.1 (2) | | |
| 116 | Modification of description and notes 3 and 4 in 2.6.1 (3) | | |
| 117 | Modification of description and notes 3 and 4 in 2.6.1 (4) | | |

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| | | Page | Summary |
| 3.00 | Aug 02, 2013 | 118 | Modification of table in 2.6.2 Temperature sensor/internal reference voltage characteristics |
| | | 118 | Modification of table and note in 2.6.3 POR circuit characteristics |
| | | 119 | Modification of table in 2.6.4 LVD circuit characteristics |
| | | 120 | Modification of table of LVD Detection Voltage of Interrupt & Reset Mode |
| | | 120 | Renamed to 2.6.5 Power supply voltage rising slope characteristics |
| | | 122 | Modification of table, figure, and remark in 2.10 Timing Specs for Switching Flash Memory Programming Modes |
| | | 123 | Modification of caution 1 and description |
| | | 124 | Modification of table and remark 3 in Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$) |
| | | 126 | Modification of table, note, caution, and remark in 3.2.1 X1, XT1 oscillator characteristics |
| | | 126 | Modification of table in 3.2.2 On-chip oscillator characteristics |
| | | 127 | Modification of note 3 in 3.3.1 Pin characteristics (1/5) |
| | | 128 | Modification of note 3 in 3.3.1 Pin characteristics (2/5) |
| | | 133 | Modification of notes 1 and 4 in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products (1/2) |
| | | 135 | Modification of notes 1, 5, and 6 in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products (2/2) |
| | | 137 | Modification of notes 1 and 4 in (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products (1/2) |
| | | 139 | Modification of notes 1, 5, and 6 in (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products (2/2) |
| | | 140 | Modification of (3) Peripheral Functions (Common to all products) |
| | | 142 | Modification of table in 3.4 AC Characteristics |
| | | 143 | Addition of Minimum Instruction Execution Time during Main System Clock Operation |
| | | 143 | Modification of figure of AC Timing Test Points |
| | | 143 | Modification of figure of External System Clock Timing |
| | | 145 | Modification of figure of AC Timing Test Points |
| | | 145 | Modification of description, note 1, and caution in (1) During communication at same potential (UART mode) |
| | | 146 | Modification of description in (2) During communication at same potential (CSI mode) |
| | | 147 | Modification of description in (3) During communication at same potential (CSI mode) |
| | | 149 | Modification of table, note 1, and caution in (4) During communication at same potential (simplified I ² C mode) |
| | | 151 | Modification of table, note 1, and caution in (5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2) |
| | | 152 to 154 | Modification of table, notes 2 to 6, caution, and remarks 1 to 4 in (5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2) |
| | | 155 | Modification of table in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/3) |
| | | 156 | Modification of table and caution in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/3) |
| 157, 158 | Modification of table, caution, and remarks 3 and 4 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (3/3) | | |
| 160, 161 | Modification of table and caution in (7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) | | |

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| | | Page | Summary |
| 3.00 | Aug 02, 2013 | 163 | Modification of table in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I ² C mode) (1/2) |
| | | 164, 165 | Modification of table, note 1, and caution in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I ² C mode) (2/2) |
| | | 166 | Modification of table in 3.5.2 Serial interface IICA |
| | | 166 | Modification of IICA serial transfer timing |
| | | 167 | Addition of table in 3.6.1 A/D converter characteristics |
| | | 167, 168 | Modification of table and notes 3 and 4 in 3.6.1 (1) |
| | | 169 | Modification of description in 3.6.1 (2) |
| | | 170 | Modification of description and note 3 in 3.6.1 (3) |
| | | 171 | Modification of description and notes 3 and 4 in 3.6.1 (4) |
| | | 172 | Modification of table and note in 3.6.3 POR circuit characteristics |
| | | 173 | Modification of table of LVD Detection Voltage of Interrupt & Reset Mode |
| | | 173 | Modification from Supply Voltage Rise Time to 3.6.5 Power supply voltage rising slope characteristics |
| | | 174 | Modification of 3.9 Dedicated Flash Memory Programmer Communication (UART) |
| | | 175 | Modification of table, figure, and remark in 3.10 Timing Specs for Switching Flash Memory Programming Modes |
| 3.10 | Nov 15, 2013 | 123 | Caution 4 added. |
| | | 125 | Note for operating ambient temperature in 3.1 Absolute Maximum Ratings deleted. |
| 3.30 | Mar 31, 2016 | 18 | Modification of the position of the index mark in 25-pin plastic WFLGA (3 × 3 mm, 0.50 mm pitch) of 1.3.3 25-pin products |
| | | 49 | Modification of power supply voltage in 1.6 Outline of Functions [20-pin, 24-pin, 25-pin, 30-pin, 32-pin, 36-pin products] |
| | | 51 | Modification of power supply voltage in 1.6 Outline of Functions [40-pin, 44-pin, 48-pin, 52-pin, 64-pin products] |
| | | 53 | Modification of power supply voltage in 1.6 Outline of Functions [80-pin, 100-pin, 128-pin products] |
| | | 110 to 112, 167 | $\overline{\text{ACK}}$ corrected to ACK |
| 3.40 | May 31, 2018 | 172 | Addition of note in 3.6.3 POR circuit characteristics |

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NOTES FOR CMOS DEVICES

- (1) **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN:** Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).
- (2) **HANDLING OF UNUSED INPUT PINS:** Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
- (3) **PRECAUTION AGAINST ESD:** A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
- (4) **STATUS BEFORE INITIALIZATION:** Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
- (5) **POWER ON/OFF SEQUENCE:** In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
- (6) **INPUT OF SIGNAL DURING POWER OFF STATE :** Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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