

# K1295-VB Datasheet N-Channel 100-V (D-S) MOSFET

PRODUCT	SUMMARY	
V <sub>(BR)DSS</sub> (V)	r <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)
100	0.034 at V <sub>GS</sub> = 10 V	50 <sup>a</sup>

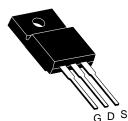
## FEATURES

- Trench Power MOSFET
- 175 °C Junction Temperature
- Low Thermal Resistance Package
- 100 % R<sub>g</sub> Tested

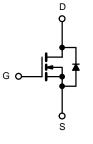
### **APPLICATIONS**

• Isolated DC/DC Converters





TO-220 FULLPAK



N-Channel MOSFET

<b>ABSOLUTE MAXIMUM RATINGS</b>	T <sub>C</sub> = 25 °C, unless oth	erwise noted		
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V <sub>DS</sub>	100	V
Gate-Source Voltage		V <sub>GS</sub>	± 20	v
Continuous Drain Current (T <sub>1</sub> = 175 °C)	T <sub>C</sub> = 25 °C	1-	50 <sup>a</sup>	
Continuous Drain Current (1) = 175 C)	T <sub>C</sub> = 125 °C	I <sub>D</sub>	28 <sup>a</sup>	A
Pulsed Drain Current		I <sub>DM</sub>	120	A
Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	31	
Single Pulse Avalanche Energy <sup>b</sup>	L = 0.11111	E <sub>AS</sub>	61	mJ
	T <sub>C</sub> = 25 °C	р	360 <sup>c</sup>	14/
Maximum Power Dissipation <sup>b</sup>	T <sub>A</sub> = 25 °C <sup>d</sup>	– P <sub>D</sub> –	3.70	W
Operating Junction and Storage Temperature Ra	ange	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 175	°C

THERMAL RESISTANCE R	ATINGS			
Parameter		Symbol	Limit	Unit
Junction-to-Ambient	PCB Mount (TO-263) <sup>d</sup>	R <sub>thJA</sub>	40	°C/W
Junction-to-Case (Drain)		R <sub>thJC</sub>	0.4	C/W

Notes:

a. Package limited.

b. Duty cycle  $\leq$  1 %.

c. See SOA curve for voltage derating.

d. When Mounted on 1" square PCB (FR-4 material).

Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static	-				1	I
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{DS} = 0 \text{ V}, \text{ I}_{D} = 250 \mu\text{A}$	100			V
Gate-Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	1.5		2.5	v
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA
		$V_{DS} = 100 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$			1	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = 100 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 125 ^{\circ}\text{C}$			50	μA
		$V_{DS} = 100 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 175 \text{ °C}$			250	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 V$ , $V_{GS} = 10 V$	120			А
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 30 A		0.034		Ω
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	$V_{GS}$ = 10 V, I <sub>D</sub> = 30 A, T <sub>J</sub> = 125 °C		0.063		
		$V_{GS}$ = 10 V, I <sub>D</sub> = 30 A, T <sub>J</sub> = 175 °C		0.084		
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 30 A	25			S
Dynamic <sup>b</sup>	•					
Input Capacitance	C <sub>iss</sub>			5100		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1 MHz		480		
Reverse Transfer Capacitance	C <sub>rss</sub>			210		
Total Gate Charge <sup>c</sup>	Qg			90	130	
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	$V_{\text{DS}}$ = 100 V, $V_{\text{GS}}$ = 10 V, $I_{\text{D}}$ = 65 A		23		nC
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			34		
Gate Resistance	Rg		0.5	1.7	3.3	Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			24	35	
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD}$ = 100 V, R <sub>L</sub> = 1.5 $\Omega$		220	330	ns
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>	$\rm I_D \cong 65$ A, $\rm V_{GEN}$ = 10 V, $\rm R_g$ = 2.5 $\Omega$		45	70	
Fall Time <sup>c</sup>	t <sub>f</sub>			200	300	
Source-Drain Diode Ratings and Cha	aracteristics 7	$\Gamma_{\rm C} = 25 \ ^{\circ}{\rm C}^{\rm b}$				
Continuous Current	ا <sub>S</sub>			50		٨
Pulsed Current	I <sub>SM</sub>			120		A
Forward Voltage <sup>a</sup>	V <sub>SD</sub>	$I_{F} = 65 \text{ A}, \text{ V}_{GS} = 0 \text{ V}$		1.0	1.5	V
Reverse Recovery Time	t <sub>rr</sub>			130	200	ns
Peak Reverse Recovery Current	I <sub>RM(REC)</sub>	I <sub>F</sub> = 50 A, di/dt = 100 A/µs		8	12	А
Reverse Recovery Charge	Q <sub>rr</sub>			0.52	1.2	μC

Notes:

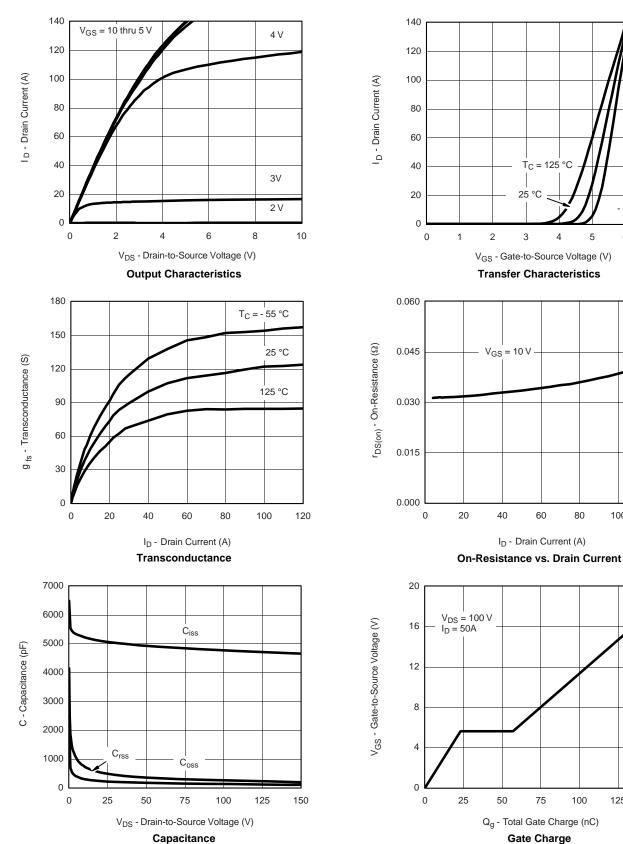
a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %. b. Guaranteed by design, not subject to production testing. c. Independent of operating temperature.

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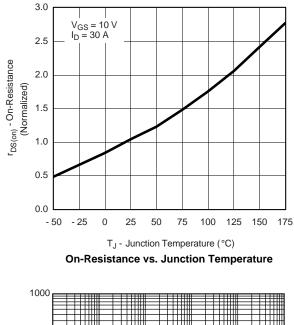
- 55 °C

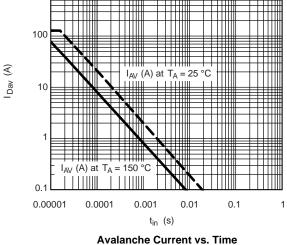


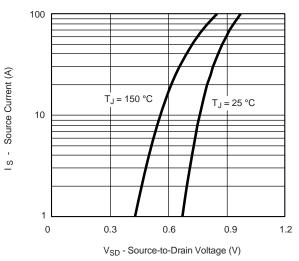
### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



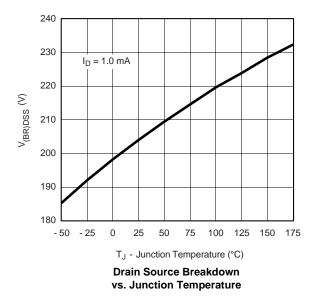
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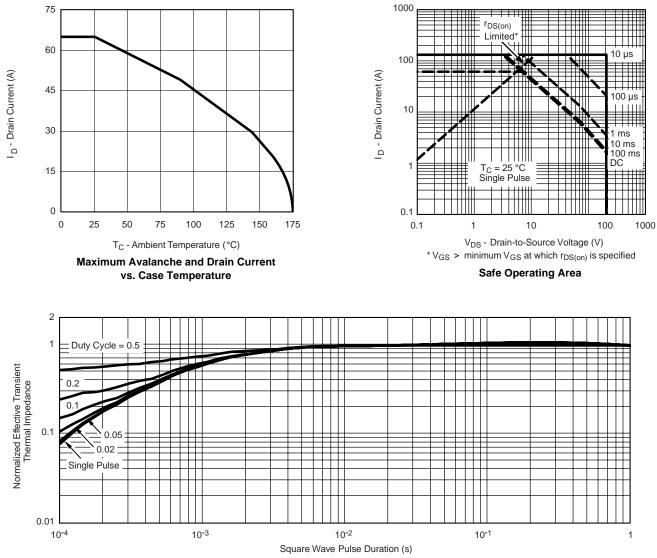


Source-Drain Diode Forward Voltage





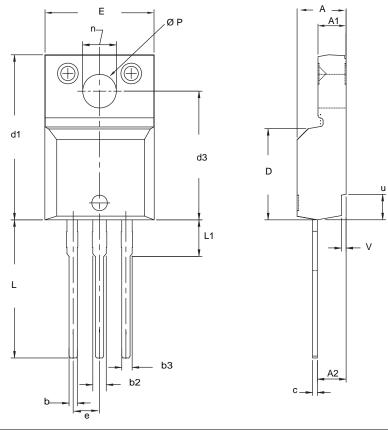
### THERMAL RATINGS



Normalized Thermal Transient Impedance, Junction-to-Case



## **TO-220 FULLPAK (HIGH VOLTAGE)**



DIM.	MILLI	METERS	INC	HES
	MIN.	MAX.	MIN.	MAX.
А	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
С	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
е	2.54	BSC	0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
ØP	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
V	0.400	0.500	0.016	0.020

Notes

1. To be used only for process drawing. 2. These dimensions apply to all TO-220, FULLPAK leadframe versions 3 leads. 3. All critical dimensions should C meet  $C_{pk} > 1.33$ . 4. All dimensions include burrs and plating thickness. 5. No chipping or package damage.



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