











SN74LVCC3245A

SCAS585P - NOVEMBER 1996-REVISED DECEMBER 2015

# SN74LVCC3245A Octal Bus Transceiver With Adjustable Output Voltage and 3-State Outputs

#### **Features**

- **Bidirectional Voltage Translator**
- 2.3 V to 3.6 V on A Port and 3 V to 5.5 V on B Port
- Control Inputs VIH and VIL Levels Are Referenced to V<sub>CCA</sub> Voltage
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

## **Applications**

- Level translation
- **USB**
- Interfacing
- Analog and Digital Applications

## 3 Description

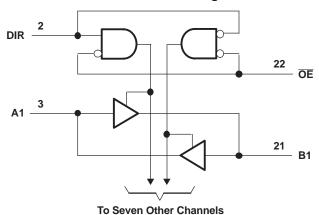
The SN74LVCC3245A device is 8-bit (octal) noninverting bus transceiver contains two separate supply rails. The B port is designed to track V<sub>CCB</sub>, which accepts voltages from 3 V to 5.5 V, and the A port is designed to track V<sub>CCA</sub>, which operates at 2.3 V to 3.6 V. This allows for translation from a 3.3-V to a 5-V system environment and vice versa, from a 2.5-V to a 3.3-V system environment and vice versa.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVCC3245ADBQ	SSOP (24)	8.65 mm × 3.90 mm
SN74LVCC3245ADW	SOIC (24)	15.40 mm × 7.50 mm
SN74LVCC3245ADB	SSOP (24)	8.20 mm × 5.30 mm
SN74LVCC3245ANS	SO (24)	15.00 mm × 5.30 mm
SN74LVCC3245APW	TSSOP (24)	7.80 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### **Functional Block Diagram**





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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

#### Changes from Revision O (March 2005) to Revision P

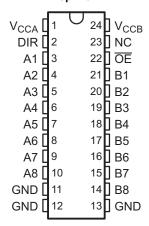
**Page** 

Added Applications section, Device Information table, ESD Ratings table, Feature Description section, Device
Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout
section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section...... 1
 Removed Ordering Information table.



## 5 Pin Configuration and Functions

DB, DBQ, DW, NS, or PW Package 24-Pin SSOP, SOIC, SO, or TSSOP Top View



NC - No internal connection

See Mechanical, Packaging, and Orderable Information for dimensions.

#### **Pin Functions**

F	PIN	1/0	DECORPORTION
NAME	NO.	I/O	DESCRIPTION
A1	3	I/O	A1 port
A2	4	I/O	A2 port
A3	5	I/O	A3 port
A4	6	I/O	A4 port
A5	7	I/O	A5 port
A6	8	I/O	A6 port
A7	9	I/O	A7 port
A8	10	I/O	A8 port
B1	21	I/O	B1 port
B2	20	I/O	B2 port
B3	19	I/O	B3 port
B4	18	I/O	B4 port
B5	17	I/O	B5 port
B6	16	I/O	B6 port
B7	15	I/O	B7 port
B8	14	I/O	B8 port
DIR	2	I	Dir input
	11		
GND	12		Ground
	13		
NC	23		Unconnected
ŌE	22	I	Output Enable active low
$V_{CCA}$	1		A port power
$V_{CCB}$	24		B port power

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## 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
$V_{CCA} V_{CCB}$	Supply voltage		-0.5	6	V
		All A ports <sup>(2)</sup>	-0.5	V <sub>CCA</sub> + 0.5	
$V_{I}$	Input voltage	All B ports <sup>(3)</sup>	-0.5	V <sub>CCB</sub> + 0.5	V
		Except I/O ports (2)	-0.5	V <sub>CCA</sub> + 0.5	
1/	Outrot calls as (3)	All A ports	-0.5	V <sub>CCA</sub> + 0.5	).5 V
V <sub>O</sub>	Output voltage <sup>(3)</sup>	All B ports	-0.5	V <sub>CCB</sub> + 0.5	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-50	mA
l <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50	mA
lo	Continuous output current			±50	mA
	Continuous current through V <sub>CCA</sub> , V <sub>CCA</sub>	CCB, or GND		±100	mA
T <sub>J</sub>	Junction temperature			150	°C
T <sub>stg</sub>	Storage temperature		-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### 6.2 ESD Ratings

			VALUE	UNIT
\/	Flactrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
V <sub>(ESD)</sub>	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	V

<sup>(1)</sup> JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions<sup>(1)</sup>

		V <sub>CCA</sub>	V <sub>CCB</sub>	MIN	NOM	MAX	UNIT
$V_{CCA}$	Supply voltage			2.3	3.3	3.6	V
$V_{CCB}$	Supply voltage			3	5	5.5	V
		2.3 V	3 V	1.7			
\/	High level input voltage	2.7 V	3 V	2			V
$V_{IHA}$	High-level input voltage	3 V	3.6 V	2			V
		3.6 V	5.5 V	2			
		2.3 V	3 V	2			
\ <u>\</u>	High level input voltage	2.7 V	3 V	2			V
$V_{IHB}$	High-level input voltage	3 V	3.6 V	2			V
		3.6 V	5.5 V	3.85			
		2.3 V	3 V			0.7	
.,	Low-level input voltage	2.7 V	3 V			8.0	V
$V_{ILA}$		3 V	3.6 V			0.8	
		3.6 V	5.5 V			0.8	

<sup>(2)</sup> This value is limited to 4.6 V maximum.

<sup>(3)</sup> This value is limited to 6 V maximum.

<sup>(2)</sup> JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

<sup>(1)</sup> All unused inputs of the device must be held at the associated V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.



## Recommended Operating Conditions<sup>(1)</sup> (continued)

		V <sub>CCA</sub>	V <sub>CCB</sub>	MIN	NOM	MAX	UNIT
		2.3 V	3 V			0.8	
17	Low level input veltage	2.7 V	3 V			8.0	V
$V_{ILB}$	Low-level input voltage	3 V	3.6 V			0.8	V
		3.6 V	5.5 V			1.65	
		2.3 V	3 V	1.7			
.,	High-level input voltage (control terminals)	2.7 V	3 V	2			
$V_{\text{IH}}$	(referenced to V <sub>CCA</sub> )	3 V	3.6 V	2			V
		3.6 V	5.5 V	2			
		2.3 V	3 V			0.7	
	Low-level input voltage (control terminals)	2.7 V	3 V			0.8	
$V_{IL}$	(referenced to V <sub>CCA</sub> )	3 V	3.6 V			0.8	V
		3.6 V	5.5 V			0.8	
V <sub>IA</sub>	Input voltage			0		$V_{CCA}$	V
V <sub>IB</sub>	Input voltage			0		V <sub>CCB</sub>	V
V <sub>OA</sub>	Output voltage			0		V <sub>CCA</sub>	V
V <sub>OB</sub>	Output voltage			0		V <sub>CCB</sub>	V
- 02		2.3 V	3 V			-8	
		2.7 V	3 V			-12	
I <sub>OHA</sub>	High-level output current	3 V	3 V			-24	mA
		2.7 V	4.5 V			-24	
		2.3 V	3 V			-12	
		2.7 V	3 V			-12	
I <sub>OHB</sub>	High-level output current	3 V	3 V			-24	mA
		2.7 V	4.5 V			-24	
		2.3 V	3 V			8	
		2.7 V	3 V			12	
$I_{OLA}$	Low-level output current	3 V	3 V			24	mA
		2.7 V	4.5 V			24	
		2.3 V	3 V			12	
		2.7 V	3 V			12	
$I_{OLB}$	Low-level output current	3 V	3 V			24	mA
		2.7 V	4.5 V			24	-
Δt/Δν	Input transition rise or fall rate					10	ns/V
T <sub>A</sub>	Operating free-air temperature			-40		85	°C

## 6.4 Thermal Information

			SN	174LVCC3245	A		
THERMAL METRIC <sup>(1)(2)</sup>		DB (SSOP)	DBQ (SSOP)	DW (SOIC)	NS (SO)	PW (TSSOP)	UNIT
		24 PINS	24 PINS	24 PINS	24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63	61	46	65	88	°C/W

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

<sup>(2)</sup> The package thermal impedance is calculated in accordance with JESD 51-7.



#### 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	V <sub>CCA</sub>	V <sub>CCB</sub>	MIN	TYP	MAX	UNIT
		$I_{OH} = -100 \mu A$	3 V	3 V	2.9	3		
		$I_{OH} = -8 \text{ mA}$	2.3 V	3 V	2			
		1040		3 V	2.2	2.5		V
$V_{OHA}$		$I_{OH} = -12 \text{ mA}$	3 V	3 V	2.4	2.8		V
		1 - 24 mA	3 V	3 V	2.2	2.6		
		$I_{OH} = -24 \text{ mA}$	2.7 V	4.5 V	2	2.3		
		$I_{OH} = -100 \mu A$	3 V	3 V	2.9	3		
		I <sub>OH</sub> = -12 mA	2.3 V	3 V	2.4			
$V_{OHB}$		10H = -12 111A	2.7 V	3 V	2.4	2.8		V
		L <sub>0.1</sub> = -24 mΔ	3 V	3 V	2.2	2.6		
		$I_{OH} = -24 \text{ mA}$		4.5 V	3.2	4.2		
		I <sub>OL</sub> = 100 μA	3 V	3 V			0.1	
		I <sub>OL</sub> = 8 mA	2.3 V	3 V			0.6	
$V_{OLA}$		$I_{OL} = 12 \text{ mA}$	2.7 V	3 V		0.1	0.5	V
		L <sub>2</sub> = 24 mΛ	3 V	3 V		0.2	0.5	
		I <sub>OL</sub> = 24 mA	2.7 V	4.5 V		0.2	0.5	
		I <sub>OL</sub> = 100 μA	3 V	3 V			0.1	
\/		I <sub>OL</sub> = 12 mA	2.3 V	3 V			0.4	V
$V_{OLB}$		I <sub>OL</sub> = 24 mA	3 V	3 V		0.2	0.5	V
		10L - 24 IIIA	2.7 V	4.5 V		0.2	0.5	
I.	Control inputs	V <sub>I</sub> = V <sub>CCA</sub> or GND	3.6 V	3.6 V		±0.1	±1	μA
I <sub>I</sub>	Control inputs	VI = VCCA OF GIVE	3.0 V	5.5 V		±0.1	±1	μΛ
I <sub>OZ</sub> <sup>(1)</sup>	A or B ports	$V_O = V_{CCA/B}$ or GND, $V_I = V_{IL}$ or $V_{IH}$	3.6 V	3.6 V		±0.5	±5	μΑ
		A port = $V_{CCA}$ or GND, $I_O = 0$	3.6 V	Open		5	50	
$I_{CCA}$	B to A	B port = $V_{CCB}$ or GND, $I_O = 0$	3.6 V	3.6 V		5	50	μΑ
		D port = VCCB of GIAD,	3.0 V	5.5 V		5	50	
laas	A to B	A port = $V_{CCA}$ or GND, $I_O = 0$	3.6 V	3.6 V		5	50	μA
ICCB	7.10 5	A port = VCCA of GND, 10 = 0	3.0 V	5.5 V		8	80	μΛ
	A port	$V_L$ = $V_{CCA}$ – 0.6 V, Other inputs at $V_{CCA}$ or GND, OE at GND and DIR at $V_{CCA}$	3.6 V	3.6 V		0.35	0.5	
$\Delta I_{\text{CCA}}^{(2)}$	ŌĒ	$V_{I} = V_{CCA} - 0.6 \text{ V}$ , Other inputs at $V_{CCA}$ or GND, DIR at $V_{CCA}$	3.6 V	3.6 V		0.35	0.5	mA
	DIR	$\frac{V_{L}}{OE} = V_{CCA} - 0.6 \text{ V}$ , Other inputs at $V_{CCA}$ or GND, $OE$ at GND	3.6 V	3.6 V		0.35	0.5	
$\Delta I_{CCB}^{(2)}$	B port	$V_L = V_{CCB} - 2.1 \text{ V}$ , Other inputs at $V_{CCB}$ or GND, OE at GND and DIR at GND	3.6 V	5.5 V		1	1.5	mA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CCA</sub> or GND	Open	Open		4		pF
C <sub>io</sub>	A or B ports	$V_O = V_{CCA/B}$ or GND	3.3 V	5 V		18.5		pF

 <sup>(1)</sup> For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.
 (2) This is the increase in supply current for each input that is at one of the specified voltage levels, rather than 0 V or the associated V<sub>CC</sub>.



## 6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2 through Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CCA,</sub> V <sub>CCB</sub>	MIN	MAX	UNIT
			$V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}, V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1	9.4	
t <sub>PHL</sub>	Α	В	V <sub>CCA</sub> = 2.7 V TO 3.6 V, V <sub>CCB</sub> = 5 V ± 0.5 V	1	6	ns
			$V_{CCA} = 2.7 \text{ V TO } 3.6 \text{ V}, V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1	7.1	
			$V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}, V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1	9.1	
t <sub>PLH</sub>	Α	В	$V_{CCA}$ = 2.7 V TO 3.6 V, $V_{CCB}$ = 5 V ± 0.5 V	1	5.3	ns
			$V_{CCA}$ = 2.7 V TO 3.6 V, $V_{CCB}$ = 3.3 V ± 0.3 V	1	7.2	
			$V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}, V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1	11.2	
t <sub>PHL</sub>	В	Α	$V_{CCA} = 2.7 \text{ V TO } 3.6 \text{ V}, V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$	1	5.8	ns
			$V_{CCA}$ = 2.7 V TO 3.6 V, $V_{CCB}$ = 3.3 V ± 0.3 V	1	6.4	
			$V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}, V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1	9.9	
t <sub>PLH</sub>	В	А	$V_{CCA}$ = 2.7 V TO 3.6 V, $V_{CCB}$ = 5 V ± 0.5 V	1	7	ns
			$V_{CCA}$ = 2.7 V TO 3.6 V, $V_{CCB}$ = 3.3 V ± 0.3 V	1	7.6	
			$V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}, V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1	14.5	
t <sub>PZL</sub>	ŌĒ	Α	$V_{CCA}$ = 2.7 V TO 3.6 V, $V_{CCB}$ = 5 V ± 0.5 V	1	9.2	ns
			$V_{CCA}$ = 2.7 V TO 3.6 V, $V_{CCB}$ = 3.3 V ± 0.3 V	1	9.7	
			$V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}, V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1	12.9	
t <sub>PZH</sub>	ŌĒ	Α	$V_{CCA}$ = 2.7 V TO 3.6 V, $V_{CCB}$ = 5 V ± 0.5 V	1	9.5	ns
			$V_{CCA}$ = 2.7 V TO 3.6 V, $V_{CCB}$ = 3.3 V ± 0.3 V	1	9.5	
			$V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}, V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1	13	
t <sub>PZL</sub>	ŌĒ	В	$V_{CCA}$ = 2.7 V TO 3.6 V, $V_{CCB}$ = 5 V ± 0.5 V	1	8.1	ns
			$V_{CCA}$ = 2.7 V TO 3.6 V, $V_{CCB}$ = 3.3 V ± 0.3 V	1	9.2	
			$V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}, V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1	12.8	
t <sub>PZH</sub>	ŌĒ	В	$V_{CCA}$ = 2.7 V TO 3.6 V, $V_{CCB}$ = 5 V ± 0.5 V	1	8.4	ns
			$V_{CCA} = 2.7 \text{ V TO } 3.6 \text{ V}, V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1	9.9	
			$V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}, V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1	7.1	
t <sub>PLZ</sub>	ŌĒ	Α	$V_{CCA}$ = 2.7 V TO 3.6 V, $V_{CCB}$ = 5 V ± 0.5 V	1	7	ns
			$V_{CCA}$ = 2.7 V TO 3.6 V, $V_{CCB}$ = 3.3 V ± 0.3 V	1	6.6	



## **Switching Characteristics (continued)**

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2 through Figure 5)

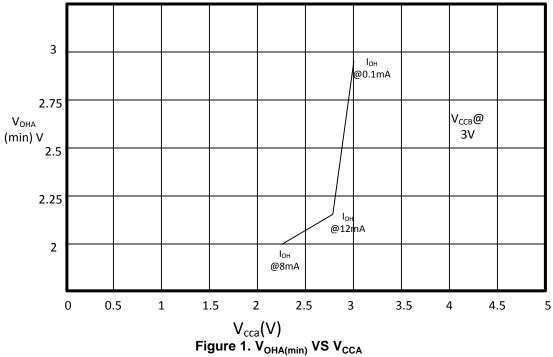
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CCA</sub> , V <sub>CCB</sub>	MIN	MAX	UNIT
			$V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}, V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1	6.9	
t <sub>PHZ</sub>	ŌĒ	А	$V_{CCA}$ = 2.7 V TO 3.6 V, $V_{CCB}$ = 5 V ± 0.5 V	1	7.8	ns
			$V_{CCA}$ = 2.7 V TO 3.6 V, $V_{CCB}$ = 3.3 V $\pm$ 0.3 V	1	6.9	
			$V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}, V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1	8.8	
$t_{PLZ}$	ŌĒ	В	$V_{CCA}$ = 2.7 V TO 3.6 V, $V_{CCB}$ = 5 V ± 0.5 V	1	7.3	ns
			$V_{CCA}$ = 2.7 V TO 3.6 V, $V_{CCB}$ = 3.3 V $\pm$ 0.3 V	1	7.5	
			$V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}, V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1	8.9	
t <sub>PHZ</sub>	ŌĒ	В	$V_{CCA}$ = 2.7 V TO 3.6 V, $V_{CCB}$ = 5 V ± 0.5 V	1	7	ns
			$V_{CCA}$ = 2.7 V TO 3.6 V, $V_{CCB}$ = 3.3 V $\pm$ 0.3 V	1	7.9	

## 6.7 Operating Characteristics

 $V_{CCA} = 3.3 \text{ V}, V_{CCB} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$ 

	PARAMETER			NDITIONS	TYP	UNIT
C	Dower dissination conscitance per transcriver	Outputs enabled	$C_1 = 50.$	f = 10 MHz	38	nE
$C_{pd}$	Power dissipation capacitance per transceiver	Outputs disabled	$C_L = 50$ ,	I = IU WINZ	4.5	рг

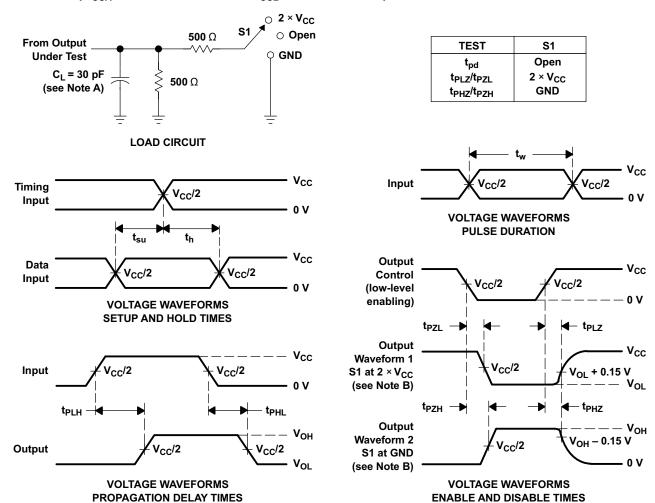
## 6.8 Typical Characteristics





#### 7 Parameter Measurement Information

## 7.1 A Port ( $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$ and $V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$ )

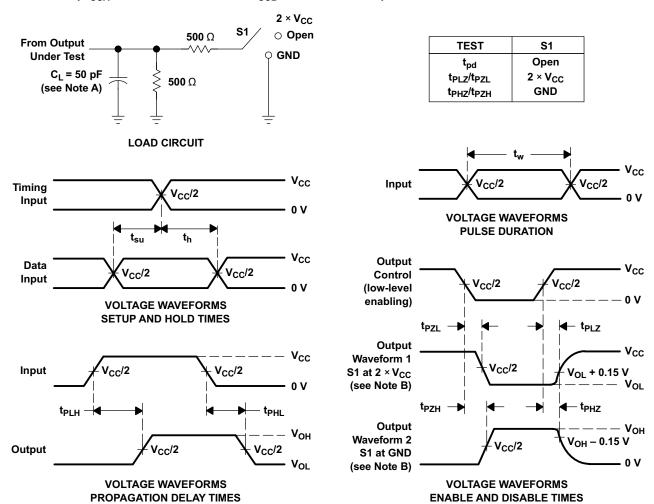


- C<sub>L</sub> includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
  - Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_f \leq$  2 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>
- F. t<sub>PZL</sub> and t<sub>PZH</sub>are the same as t<sub>en</sub>.
- G. t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd</sub>.
- H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms



## 7.2 B Port ( $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$ and $V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$ )

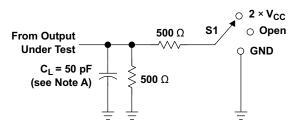


- A. C<sub>L</sub> includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
  - Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_f \leq$  2 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
- F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

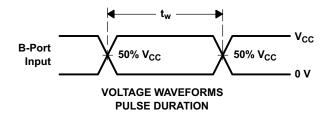
Figure 3. Load Circuit and Voltage Waveforms



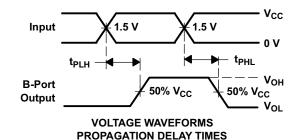
## 7.3 B Port ( $V_{CCA} = 3.6 \text{ V} \text{ and } V_{CCB} = 5.5 \text{ V}$ )



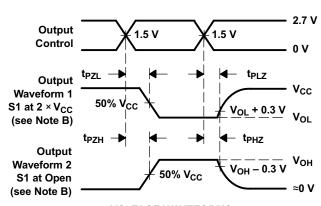
TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	2 × V <sub>CC</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	Open



LOAD CIRCUIT



**NONINVERTING OUTPUTS** 



**VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING** 

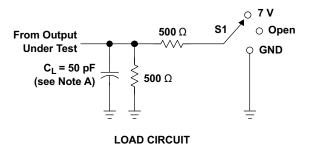
- C<sub>L</sub> includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output
  - Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r \leq$  2.5 ns,  $t_f \le 2.5 \text{ ns.}$
- The outputs are measured one at a time, with one transition per measurement.
- All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

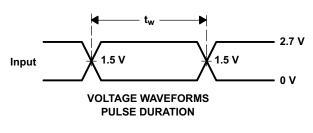
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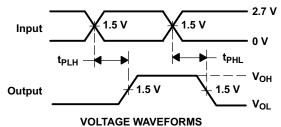


## 7.4 A and B Port ( $V_{CCA}$ and $V_{CCB} = 3.6 \text{ V}$ )

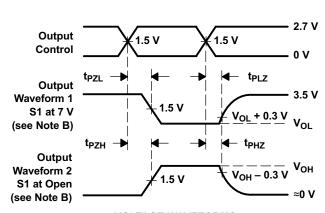


TEST	<b>S</b> 1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	7 V
t <sub>PHZ</sub> /t <sub>PZH</sub>	Open





PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- A. C<sub>L</sub> includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
  - Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq$  2.5 ns,  $t_f \leq$  2.5 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 5. Load Circuit and Voltage Waveforms

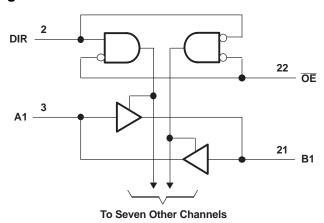


## 8 Detailed Description

#### 8.1 Overview

The SN74LVCC3245A device is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable  $(\overline{OE})$  input can be used to disable the device so the buses are effectively isolated. The control circuitry (DIR,  $\overline{OE}$ ) is powered by  $V_{CCA}$ .

#### 8.2 Functional Block Diagram



#### 8.3 Feature Description

This device is a bidirectional level translator designed to operate from 2.3 V to 3.6 V on Port A and 3 V to 5.5 V on B port. The control inputs recommended operating specifications are referenced with respect to  $V_{CCA}$  Voltage.

#### 8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74LVCC3245A.

Table 1. Function Table (Each Transceiver)

INP	UTS	OPERATION
ŌĒ	DIR	OPERATION
L	L	B data to A bus
L	Н	A data to B bus
Н	X	Isolation



## 9 Application and Implementation

#### **NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

#### 9.1 Application Information

The SN74LVCC3245A device is a bidirectional level translator designed to operate from 2.3 V to 3.6 V on Port A and 3 V to 5.5 V on B port and designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input.

## 9.2 Typical Application

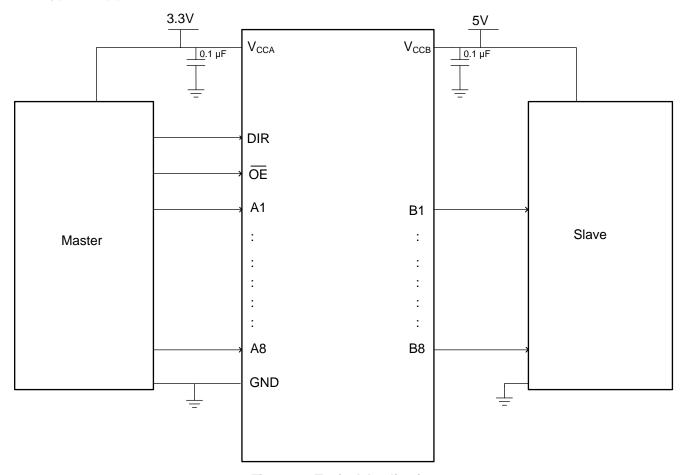


Figure 6. Typical Application

#### 9.2.1 Design Requirements

This device can be used as bidirectional level translator depending on the DIR pin. The application describes the level translation of Master with signals at 3.3 V to slave operating at 5 V. The OE pin is low and DIR pin is 3.3-V high.



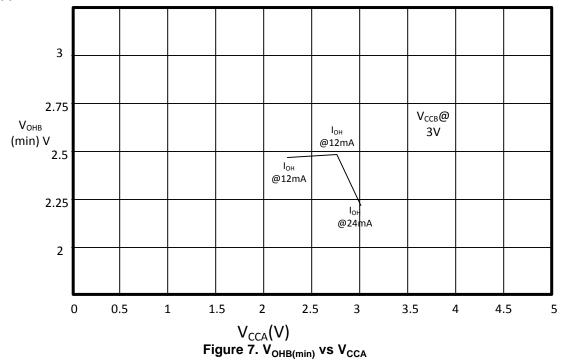
## **Typical Application (continued)**

#### 9.2.2 Detailed Design Procedure

Use the procedure that follows for the design:

- 1. Recommended Input Conditions
  - Rise time and fall time specs. See (Δt/ΔV) in the Recommended Operating Conditions table.
  - Specified high and low levels. See (V<sub>IH</sub> and V<sub>IL</sub>) in the Recommended Operating Conditions table.
  - Inputs are overvoltage tolerant allowing them to go as high as (V<sub>I</sub> max) in the Recommended Operating
     Conditions table at any valid V<sub>CC</sub>.
- 2. Absolute Maximum Output Conditions
  - Load currents should not exceed (I<sub>O</sub> max) per output and should not exceed total current (continuous current through V<sub>CC</sub> or GND) for the part. These limits are located in the *Absolute Maximum Ratings* table
  - All the voltages on A and B ports should not exceed above V<sub>CCA</sub> or V<sub>CCB</sub> to prevent the biasing of Electrostatic discharge (ESD) diodes.

#### 9.2.3 Application Curve



## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions* table.

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- $\mu$ F capacitor is recommended and if there are multiple  $V_{CC}$  pins then 0.01- $\mu$ F or 0.022- $\mu$ F capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

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## 11 Layout

#### 11.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V<sub>CC</sub> whichever make more sense or is more convenient.

### 11.2 Layout Example



Figure 8. Layout Example

## 11.3 Power-Up Considerations

TI level-translation devices offer an opportunity for successful mixed-voltage signal design. A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device terminals. To guard against such power-up problems, take these precautions:

- 1. Connect ground before any supply voltage is applied.
- 2. Power up the control side of the device (V<sub>CCA</sub> for all four of these devices).
- 3. Tie  $\overline{OE}$  to  $V_{CCA}$  with a pullup resistor so that it ramps with  $V_{CCA}$ .
- 4. Depending on the direction of the data path, DIR can be high or low. If DIR high is needed (A data to B bus), ramp it with V<sub>CCA</sub>. Otherwise, keep DIR low.

Refer to the TI application report, Texas Instruments Voltage-Level-Translation Devices, SCEA021.



## 12 Device and Documentation Support

## 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation, see the following:

- Implications of Slow or Floating CMOS Inputs, SCBA004
- Texas Instruments Voltage-Level-Translation Devices, SCEA021

#### 12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community T's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support TI's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

#### 12.3 Trademarks

E2E is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

## 12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

#### 12.5 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

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24-Aug-2018

## **PACKAGING INFORMATION**

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVCC3245ADBQR	ACTIVE	SSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVCC3245A	Samples
SN74LVCC3245ADBR	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	Samples
SN74LVCC3245ADBRE4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	Samples
SN74LVCC3245ADBRG4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	Samples
SN74LVCC3245ADW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	Samples
SN74LVCC3245ADWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	Samples
SN74LVCC3245ADWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	Samples
SN74LVCC3245ADWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	Samples
SN74LVCC3245ADWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	Samples
SN74LVCC3245ANSR	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	Samples
SN74LVCC3245ANSRE4	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	Samples
SN74LVCC3245ANSRG4	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	Samples
SN74LVCC3245APW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	Samples
SN74LVCC3245APWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	Samples
SN74LVCC3245APWRE4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	Samples
SN74LVCC3245APWRG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	Samples
SN74LVCC3245APWT	ACTIVE	TSSOP	PW	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	Samples



## PACKAGE OPTION ADDENDUM

24-Aug-2018

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
SN74LVCC3245APWTG4	ACTIVE	TSSOP	PW	24	250	Green (RoHS	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	Samalar.
						& no Sb/Br)					Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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#### OTHER QUALIFIED VERSIONS OF SN74LVCC3245A:

Enhanced Product: SN74LVCC3245A-EP





24-Aug-2018

NOTE: Qualified Version Definitions:

• Enhanced Product - Supports Defense, Aerospace and Medical Applications

## PACKAGE MATERIALS INFORMATION

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## TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVCC3245ADBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVCC3245ADBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74LVCC3245ADWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74LVCC3245ADWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74LVCC3245ADWRG4	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74LVCC3245ANSR	so	NS	24	2000	330.0	24.4	8.3	15.4	2.6	12.0	24.0	Q1
SN74LVCC3245APWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
SN74LVCC3245APWT	TSSOP	PW	24	250	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

www.ti.com 24-Jun-2019



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVCC3245ADBQR	SSOP	DBQ	24	2500	367.0	367.0	38.0
SN74LVCC3245ADBR	SSOP	DB	24	2000	367.0	367.0	38.0
SN74LVCC3245ADWR	SOIC	DW	24	2000	350.0	350.0	43.0
SN74LVCC3245ADWR	SOIC	DW	24	2000	364.0	364.0	27.0
SN74LVCC3245ADWRG4	SOIC	DW	24	2000	350.0	350.0	43.0
SN74LVCC3245ANSR	SO	NS	24	2000	367.0	367.0	45.0
SN74LVCC3245APWR	TSSOP	PW	24	2000	367.0	367.0	38.0
SN74LVCC3245APWT	TSSOP	PW	24	250	367.0	367.0	38.0

DW (R-PDSO-G24)

## PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AD.



DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

#### **28 PINS SHOWN**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

DBQ (R-PDSO-G24)

## PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
- D. Falls within JEDEC MO-137 variation AE.





SMALL OUTLINE PACKAGE



#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



## **MECHANICAL DATA**

## NS (R-PDSO-G\*\*)

# 14-PINS SHOWN

## PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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