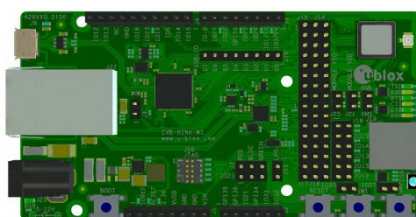


# EVK-NINA-W1/EVK-NINA-B2

## Evaluation Kit for NINA-W1 and NINA-B2 modules

### User Guide



### Abstract

This document describes how to set up the EVK-NINA-W1/EVK-NINA-B2 evaluation kits to evaluate NINA-W1 series and NINA-B2 series stand-alone modules. It also describes the different options for debugging and the development capabilities included in the evaluation board.

# Document Information

<b>Title</b>	EVK-NINA-W1/EVK-NINA-B2	
<b>Subtitle</b>	Evaluation Kit for NINA-W1 and NINA-B2 modules	
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<b>Disclosure Restriction</b>		

This document applies to the following products:

<b>Product name</b>	<b>Software version</b>	<b>PCN reference</b>
EVK-NINA-W101	N/A	-
EVK-NINA-W102	N/A	-
EVK-NINA-W131	N/A	-
EVK-NINA-W132	N/A	-
EVK-NINA-W151	N/A	-
EVK-NINA-W152	N/A	-
EVK-NINA-B221	N/A	-
EVK-NINA-B222	N/A	-

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# 1 Product description

## 1.1 Overview

The EVK-NINA-W1/EVK-NINA-B2 evaluation kit includes an evaluation board, which can be used as a reference design for the NINA-W1 or NINA-B2 series modules, a quick start guide, and a USB cable.

For the NINA-B221 and the NINA-W1x1 module, the evaluation board is prepared with a U.FL coaxial connector for connecting the external antenna. The NINA-B222 and the NINA-W1x2 module has an onboard antenna; thus the EVK-NINA-B222 and the EVK-NINA-W1x2 evaluation board does not have a U.FL connector.

The main features of the EVK-NINA-W1/EVK-NINA-B2 are:

- Available in several variants:
  - NINA-B221 and NINA-B222
  - NINA-W101 and NINA-W102
  - NINA-W131 and NINA-W132
  - NINA-W151 and NINA-W152
- All of the module pins are available at connectors or jumpers
- Can be powered through USB (J8) or external power supply (J23)
- Equipped with a Quad High Speed USB to Multipurpose UART/MPSSE IC (FT4232) that allows serial communication and flashing over USB.

The EVK-NINA-W1/EVK-NINA-B2 evaluation kits are available in the following variants, depending on the NINA module that is mounted on the EVK:

- EVK-NINA-B221 – Evaluation kit for NINA-B221 module, RF port available on U.FL connector (J21)
- EVK-NINA-B222 – Evaluation kit for NINA-B222 module with onboard antenna
- EVK-NINA-W101 – Evaluation kit for NINA-W101 module, RF port available on U.FL connector (J21)
- EVK-NINA-W102 – Evaluation kit for NINA-W102 module with onboard antenna
- EVK-NINA-W131 – Evaluation kit for NINA-W131 module, RF port available on U.FL connector (J21)
- EVK-NINA-W132 – Evaluation kit for NINA-W132 module with onboard antenna
- EVK-NINA-W151 – Evaluation kit for NINA-W151 module, RF port available on U.FL connector (J21)
- EVK-NINA-W152 – Evaluation kit for NINA-W152 module with onboard antenna

This section describes the main connectors and settings that are required to get started. Figure 1 and Figure 2 show the two different antenna variants of the EVK-NINA-W1/EVK-NINA-B2 evaluation board.

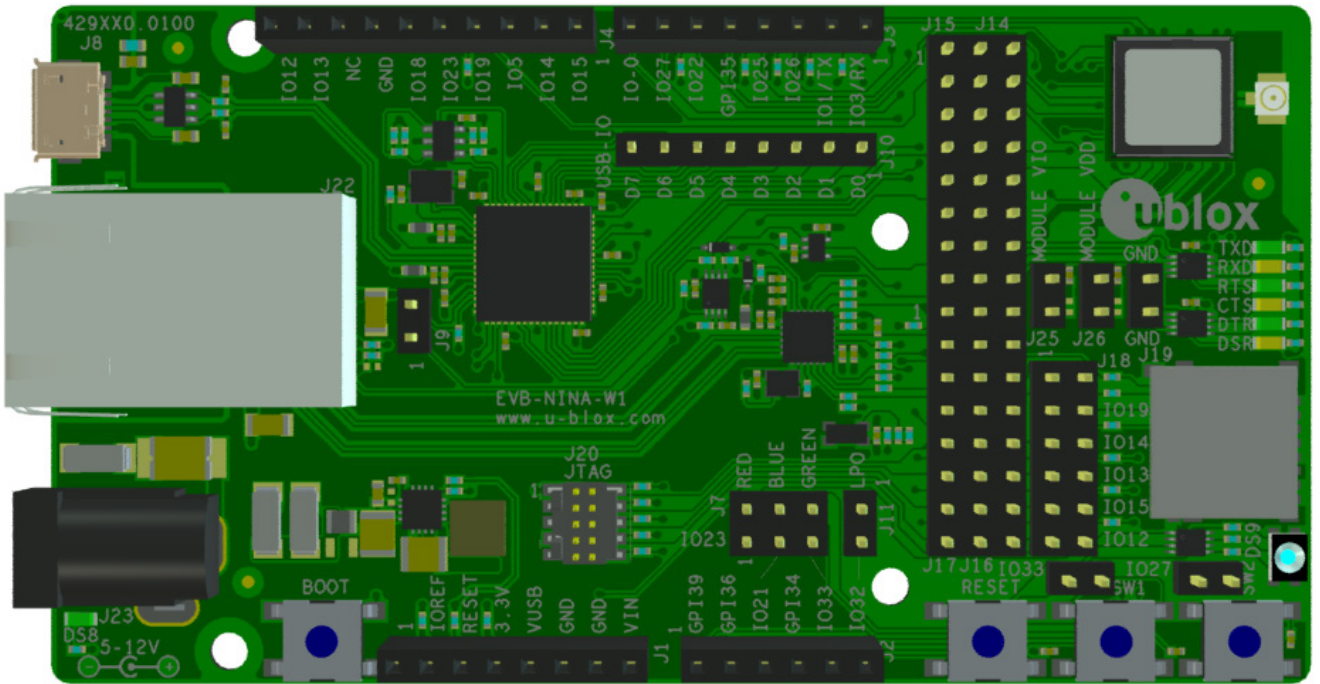


Figure 1: EVK-NINA-W1/EVK-NINA-B2 evaluation board with U.FL connector for external antenna

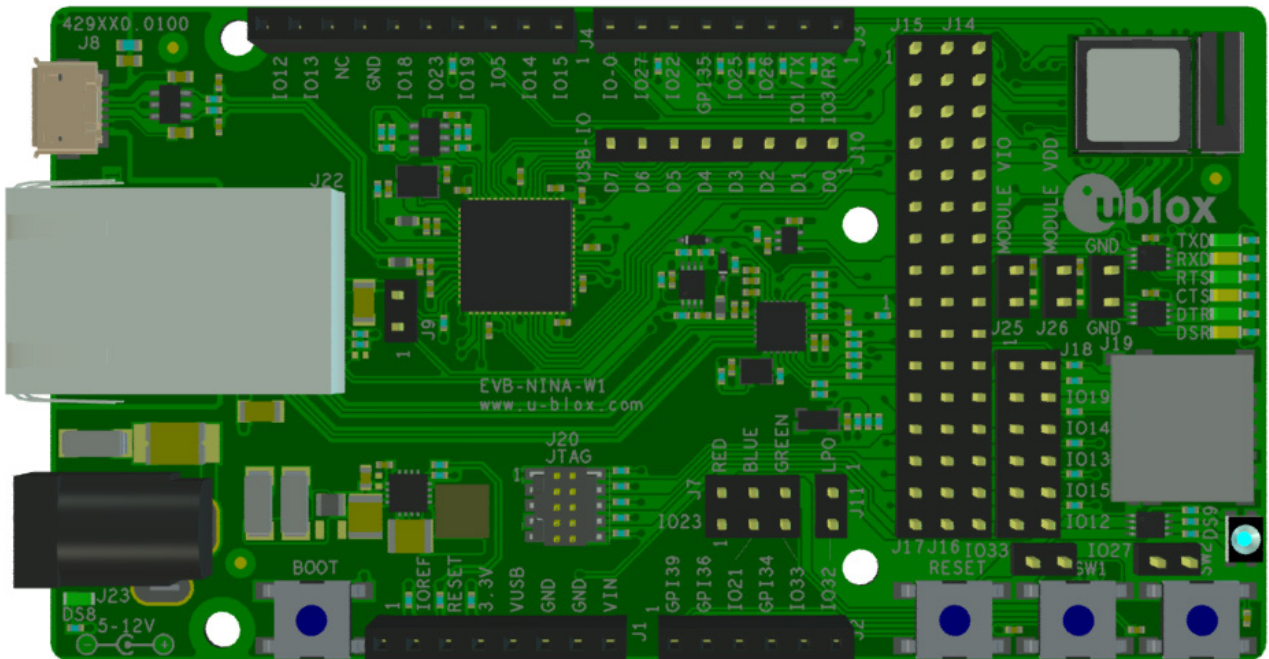



Figure 2: EVK-NINA-W1/EVK-NINA-B2 evaluation board with internal antenna

-  Take care while handling the EVK-NINA-B222 and EVK-NINA-W1x2. Applying force to the NINA module might damage the internal antenna.

## 1.2 Kit includes

### 1.2.1 EVK-NINA-B221 and EVK-NINA-W1x1

The EVK-NINA-B221 and EVK-NINA-W1x1 evaluation kits include the following:

- EVK-NINA-B221 or EVK-NINA-W1x1 evaluation board
- 2.4 GHz foldable antenna (Ex-It 2400) with reverse polarity SMA connector
- RP-SMA - U.FL cable assembly, 100 mm length
- USB cable
- Quick Start guide

### 1.2.2 EVK-NINA-B222 and EVK-NINA-W1x2

The EVK-NINA-B222 and EVK-NINA-W1x2 evaluation kits include the following:

- EVK-NINA-B222 and EVK-NINA-W1x2
- USB cable
- Quick Start guide

## 1.3 I/O allocation

The block diagram in Figure 3 provides a better understanding of how I/O signals from the module are made available at connectors and/or interfaces of the EVK.

Sixteen (16) I/O signals are available at the middle row of the I/O allocator. These signals can be distributed to connectors and/or interfaces on the EVK by use of jumpers to connect the associated middle and outer row pin(s).

The signals IO-12, IO-13, IO-14 and IO-15 can be disconnected from the J4 connector by not populating the corresponding jumpers at J18. This can be useful if the SDIO signals D2, D3, CLK, and CMD are directed to the SD card reader (J19).

Eight signals are connected directly between the module and the J2 or J3 connector.

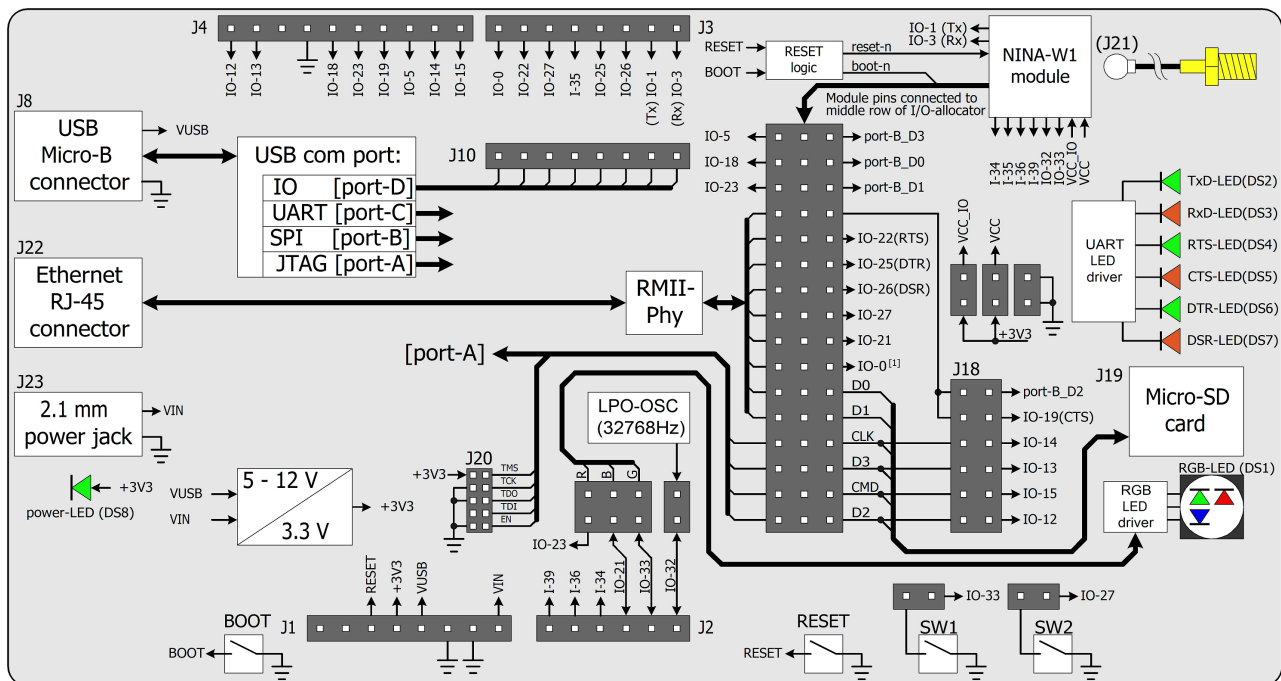


Figure 3: Block diagram of EVK-NINA-W10

When reset-n is released, the module pin 27 is read as boot-n. When IO-0 is connected to the module, it must be held high during start up.

## 1.4 Jumper description

Parameter	Description	Name	Default
Enable SW1	Jumper at J5-1_J5-2 connects switch 1 to module pin-7	J5	<input checked="" type="checkbox"/>
Enable SW2	Jumper at J6-1_J6-2 connects switch 2 to IO-27 (Jumper at J14-15_J14-16 must be populated to connect IO27 to module pin-18)	J6	<input checked="" type="checkbox"/>
Enable RGB-LED	Jumper at J7-1_J7-2 connects RED LED to IO-23 (Jumper at J15-3_J14-5 must be populated to connect IO23 to module pin-1)	J7-RED	<input checked="" type="checkbox"/>
	Jumper at J7-3_J7-4 connects BLUE LED to IO-21 (Jumper at J16-1_J16-2 must be populated to connect IO21 to module pin-8)	J7-BLUE	<input checked="" type="checkbox"/>
	Jumper at J7-5_J7-6 connects GREEN LED to IO-33	J7-GREEN	<input checked="" type="checkbox"/>
IO/Interface select	Module pin to IO/Interface distribution	J14	See Table 3
IO/Interface select	Module pin to IO/Interface distribution	J15	See Table 3
IO/Interface select	Module pin to IO/Interface distribution	J16	See Table 3
IO/Interface select	Module pin to IO/Interface distribution	J17	See Table 3
IO/Interface select	Module pin to IO/Interface distribution	J18	See Table 3
Enable VCC_IO	Connects EVK internal 3.3 V to module pin-9 to supply module VCC_IO	J25	<input checked="" type="checkbox"/>
Enable VCC	Connects EVK internal 3.3 V to module pin-10 to supply module VCC	J26	<input checked="" type="checkbox"/>

Table 1: EVK-NINA-W1/EVK-NINA-B2 jumper descriptions

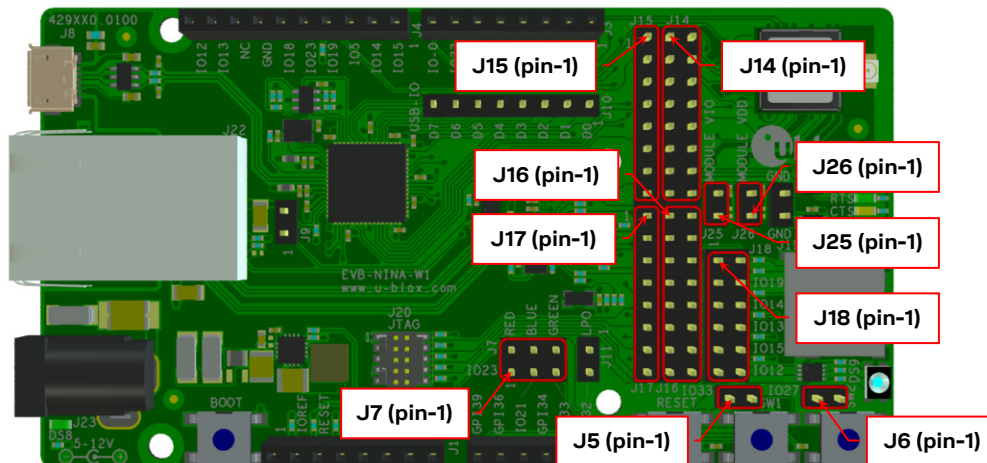


Figure 4: Jumper positions on the EVK

Middle row jumper pin	Connected to
J14-1	Module pin-28
J14-3	Module pin-29
J14-5	Module pin-1
J14-7	Module pin-21
J14-9	Module pin-20
J14-11	Module pin-16

Middle row jumper pin	Connected to
J14-13	Module pin-17
J14-15	Module pin-18
J16-1	Module pin-8
J16-3	Module pin-27
J16-5	Module pin-25
J16-7	Module pin-24
J16-9	Module pin-31
J16-11	Module pin-35
J16-13	Module pin-32
J16-15	Module pin-36

**Table 2: Available module pins at the middle row of jumpers J14 and J16**

Connected to	Left row jumper pin	Middle row jumper pin	Right row jumper pin	Connected to	Default
IO-5, J4 pin-3	J15-1	J14-1	J14-2	SPI_CS, U5-PB-3	[ J15-1_J14-1 ]
IO-18, J4 pin-6	J15-2	J14-3	J14-4	SPI_CLK, U5-PB-0	[ J15-2_J14-3 ]
IO-23, J4 pin-5	J15-3	J14-5	J14-6	SPI_MOSI, U5-PB-1	[ J15-3_J14-5 ]
reserved	J15-4	J14-7	J14-8	J18 pin-1_3	[ J14-7_J14-8 ]
reserved	J15-5	J14-9	J14-10	IO-22, J3 pin-6 (RTS)	[ J14-9_J14-10 ]
reserved	J15-6	J14-11	J14-12	IO-25, J3 pin-4 (DTR)	[ J14-11_J14-12 ]
reserved	J15-7	J14-13	J14-14	IO-26, J3 pin-3 (DSR)	[ J14-13_J14-14 ]
reserved	J15-8	J14-15	J14-16	IO-27, J3 pin-7	[ J14-15_J14-16 ]
reserved	J17-1	J16-1	J16-2	IO-21, J2 pin-3	[ J16-1_J16-2 ]
reserved	J17-2	J16-3	J16-4	IO-0, J3 pin-8	[ J16-3_J16-4 ]
reserved	J17-3	J16-5	J16-6	reserved	
reserved	J17-4	J16-7	J16-8	reserved	
Reserved	J17-5	J16-9	J16-10	J18 pin-5	[ J16-9_J16-10 ]
Reserved	J17-6	J16-11	J16-12	J18 pin-7	[ J16-11_J16-12 ]
Reserved	J17-7	J16-13	J16-14	J18 pin-9	[ J16-13_J16-14 ]
Reserved	J17-8	J16-15	J16-16	J18 pin-11	[ J16-15_J16-16 ]

**Table 3: IO-allocation via jumpers J14, J15, J16, and J17**

Connected to	Left row jumper pin	Right row jumper pin	Connected to	Default
J14-8	J18-1	J18-2	SPI_MISO, U5-PB-2	
J14-8	J18-3	J18-4	IO-19, J4 pin-4 (CTS)	[ J18-3_J18-4 ]
J16-10	J18-5	J18-6	IO-14, J4 pin-2	[ J18-5_J18-6 ]
J16-12	J18-7	J18-8	IO-13, J4 pin-9	[ J18-7_J18-8 ]
J16-14	J18-9	J18-10	IO-15, J4 pin-1	[ J18-9_J18-10 ]
J16-16	J18-11	J18-12	IO-12, J4 pin-10	[ J18-11_J18-12 ]

**Table 4: IO-allocation via jumper J18**



### 1.4.1 Default jumper configuration

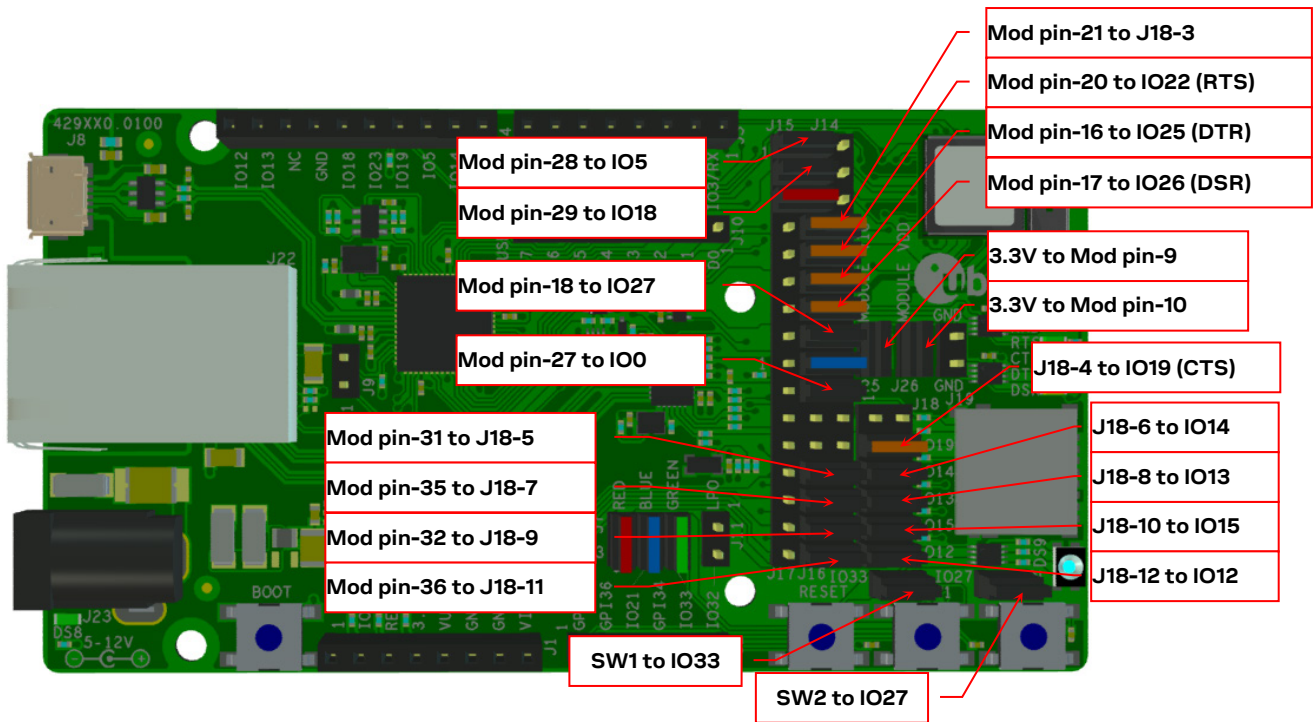


Figure 5: Jumper configuration to enable UART, IOs, and switches 1 and 2

### 1.4.2 RMII to PHY jumper configuration

The jumpers shown in Figure 6 must be inserted to connect the 10Base-T/100Base-TX PHY with the associated module RMII interface pins.

When the RMII PHY is connected to the module, the “BLUE-LED” is not available at IO-21.

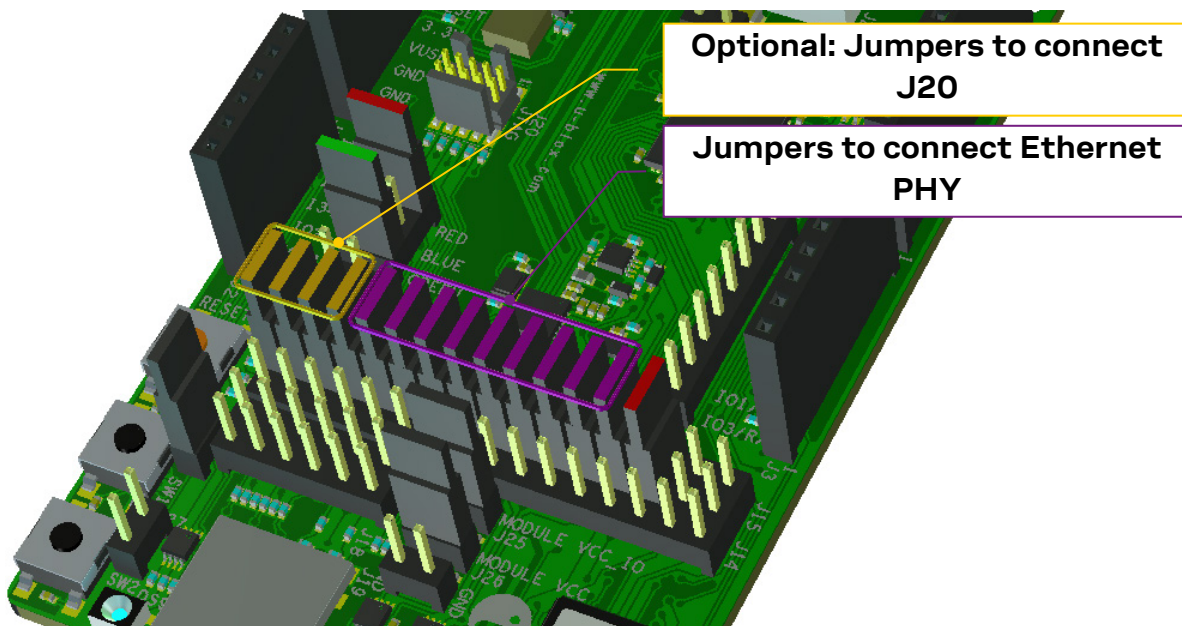


Figure 6: RMII to PHY jumper configuration

## 1.5 LEDs

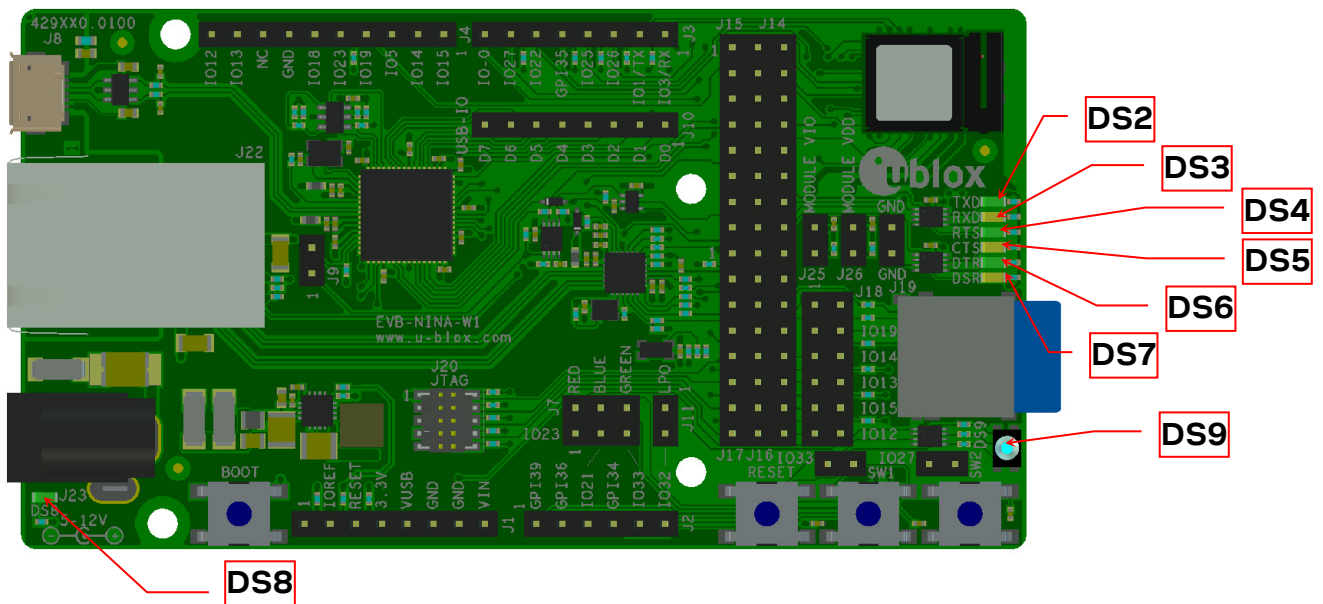


Figure 7: Position of LEDs on EVK-NINA-W1/EVK-NINA-B2

Function	Description	Name	Color
Power LED	Supplied from the EVK 3.3 V DC/DC converter	DS8	Green
UART TxD	Flashing LED indicates UART Tx activity (output from the module)	DS2	Green
UART RxD	Flashing LED indicates UART Rx activity (input to the module)	DS3	Amber
UART RTS	LED indicates UART RTS status (output from the module)	DS4 <sup>[1]</sup>	Green
UART CTS	LED indicates UART CTS status (input to the module)	DS5 <sup>[1]</sup>	Amber
UART DTR	LED indicates UART DTR status (output from the module)	DS6 <sup>[1]</sup>	Green
UART DSR	LED indicates UART DSR status (input to the module)	DS7 <sup>[1]</sup>	Amber
status	RGB LED to present module status	DS9 <sup>[1]</sup>	RGB

Table 5: EVK-NINA-W1/EVK-NINA-B2 LEDs description

[1] To control the LEDs, the corresponding signal jumper(s) must be populated.

### 1.5.1 RGB-LED Jumper configuration

The jumpers shown in Figure 8 must be inserted to connect the RGB-LED driver with the associated module pins.

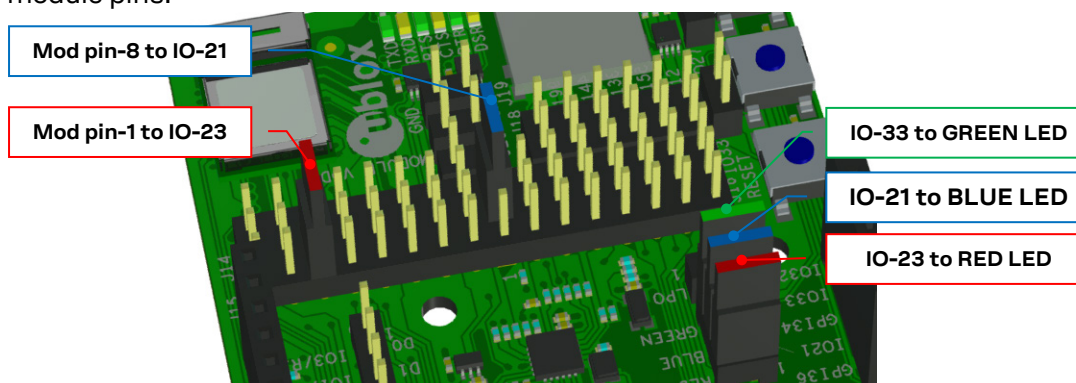


Figure 8: RGB-LED to IO signals jumpers

## 1.6 Connectors

The available connectors on the EVK-NINA-W1/EVK-NINA-B2 board are shown in Figure 9.

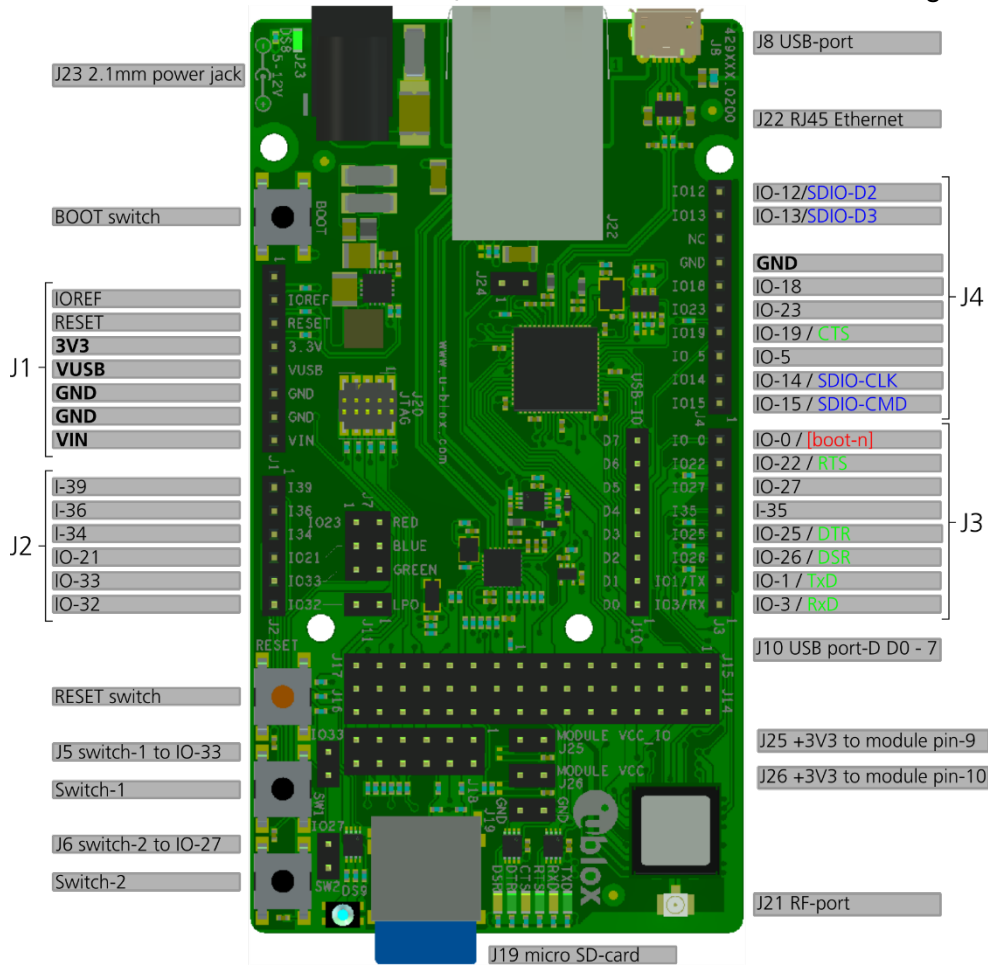


Figure 9: EVK-NINA-W1/EVK-NINA-B2 connectors

Connector	Description
J1, J2, J3, J4	Connectors for accessing the NINA-W1 IO signals (GPIO)
J8	USB connector; type Micro-B
J10	Reserved
J21	RF-port at U.FL coaxial connector for external antenna (not used on EVK-NINA-B221 or EVK-NINA-W1x2)
J22	RJ45 connector, RMII to PHY
J23	2.1 mm Power jack, positive center pin, 5 – 12 V

Table 6: EVK-NINA-W1/EVK-NINA-B2 connector descriptions

## 1.7 Buttons

The EVK-NINA-W1/EVK-NINA-B2 evaluation board has four buttons as explained in Table 7. Two of them can be connected to NINA pins via jumper configuration.



Button	Description
RESET	Reset button, triggers the reset logic that pulls module pin-19 low
BOOT	If reset is asserted pressing BOOT-switch will pull module pin-27 low
SW1	General function button connected to jumper J5 pin-2
SW2	General function button connected to jumper J6 pin-2

Table 7: EVK-NINA-W1/EVK-NINA-B2 buttons descriptions

## 1.8 Configuration options


Module pin number	IO- signal	Primary function	Accessible at Jumper/Connector	Module pin number	IO- signal	Primary function	Accessible at Jumper/Connector
1	GPIO-23		J14-5, [J4-5, J7-1] <sup>(1)</sup>	20	GPIO-22	UART_RTS	J14-9, [J3-7] <sup>(1)</sup>
2	GPI-34		J2-3	21	GPIO-19	UART_CTS	J14-7, [J4-4] <sup>(1)(2)</sup>
3	GPI-39		J2-1	22	GPIO-1	UART_TXD	J3-2
4	GPI-36		J2-2	23	GPIO-3	UART_RXD	J3-1
5	GPIO-32		J2-6, J11-2	24	GPIO-4		J16-7
6,12, 14	GND		J1-6,-7, J4-7, J12-1,-2	25	GPIO-2		J16-5
7	GPIO-33		J2-5, J5-1, J7-5	26, 30	GND		J1-6,-7, J4-7, J12-1,-2
8	GPIO-21		J16-1, [J2-4, J7-3] <sup>(1)</sup>	27	GPIO-0		J16-3, [J3-8] <sup>(1)</sup>
9	VCC_IO		J25-2	28	GPIO-5		J14-1, [J4-3] <sup>(1)</sup>
10	VCC		J26-2	29	GPIO-18		J14-3, [J4-6] <sup>(1)</sup>
13	RF-port	Antenna	J21	31	GPIO-14		J16-9, [J4-2] <sup>(1)(2)</sup>
16	GPIO-25	UART_DTR	J14-11, [J3-4] <sup>(1)</sup>	32	GPIO-15		J16-13, [J4-1] <sup>(1)(2)</sup>
17	GPIO-26	UART_DSR	J14-13, [J3-3] <sup>(1)</sup>	34	GPI-35		J3-5
18	GPIO-27		J14-15, [J3-6, J6-1] <sup>(1)</sup>	35	GPIO-13		J16-11, [J4-9] <sup>(1)(2)</sup>
19	RESET-N	RESET	(J1-3 via logic)	36	GPIO-12		J16-15, [J4-10] <sup>(1)(2)</sup>

**Table 8: Module pin to IO signal conversion**

-  (1) Connector/jumper placed inside the brackets indicates that a jumper must be positioned at the corresponding position of the IO distribution jumpers J14 – J17 if the IO-signal is to be presented at the designated connector/jumper as mentioned in Table 3.
-  (2) These IO signals require a second jumper to be positioned at the IO distribution jumper J18 as mentioned in Table 4.

### 1.8.1 Power supply

The supply voltage to the EVK-NINA-W1/EVK-NINA-B2 evaluation board can be sourced from the following connectors:

- USB (J8)
-  Depending on your USB source, the USB supply current may be insufficient.
- External power supply (J23): The external supply voltage must be in the range 5 – 12 V

## 2 Setting up the evaluation board

The EVK-NINA-W10 is delivered without any software (open CPU) and the software must be developed by the user.

The EVK-NINA-B2, EVK-NINA-W13 and the EVK-NINA-W15 is delivered with the ublox connectivity software pre-flashed on the module.

- ⚠ The module is designed to be used only with the applicable software and only compatible software can be flashed on the module.

Before connecting the module, download and install the latest u-blox s-center evaluation software from the u-blox website.

Plug in external supply power at connector J23 or connect J8 (USB type Micro B) to a USB host using the USB cable. The status light (DS8) will turn green, indicating that the internal EVK 3.3 V is on.

- ⚠ When using the evaluation board with external antenna, before powering up the EVK, ensure that you have connected the 2.4 GHz antenna with the U.FL antenna connector (J21). Failing to do so may cause undesired operation.
- ⚠ Be careful to check polarity before connecting external power supply to the evaluation board. Center conductor is positive (+) and the ring is negative (-).
- ⚠ The current consumption during startup of the evaluation board can be high.

The operating system will install the correct COM port drivers automatically. The drivers will need to be installed only when you connect the unit to a new computer for the first time. For more information about the COM ports and their configuration, see the FTDI FT4232H Datasheet [6].

One COM port will automatically be assigned to the unit by the Windows OS. To view the assigned COM ports on Windows 7, follow the steps mentioned below:

- Open the **Control Panel** and click **Hardware and Sound**.
- Click **Device Manager** in **Devices and Printers**. This will open the Device Manager window where you can view the assigned COM ports.

### 2.1 EVK without software (open CPU)

The chapter is applicable to the following EVKs.

- EVK-NINA-W101
- EVK-NINA-W102

When using the NINA-W10 open CPU variant, it is not possible to download the u-blox connectivity software. Use the software developed and compiled using the Espressif SDK on this variant.

Information on how to build and FLASH the module when using Espressif SDK is available at the following URL - <http://esp-idf.readthedocs.io/en/latest/get-started/index.html>.

This URL webpage provides information on how to set up the software environment using the hardware based on the Espressif ESP32 such as NINA-W10 and also how to use the ESP-IDF (Espressif IoT Development Framework).

The following steps must be performed to compile, flash, and execute a program on NINA-W10:

- **Set up the Toolchain**
  - Windows, Mac, and Linux is supported
- **Get the ESP-IDF**

- Download the GIT repository provided by Espressif
- **Setup Path to ESP-IDF**
  - The tool chain program can access the ESP-IDF using the IDF\_PATH environment variable
- **Build and Flash**
  - Start a Project, Connect, Configure, Build and Flash a program

More information about this is available at <http://esp-idf.readthedocs.io/en/latest/index.html>

More information on this topic can be found in the NINA-W1 System Integration Manual [7].

## 2.2 EVK with u-blox connectivity software

This section is applicable for the following EVKs:

- EVK-NINA-B221
- EVK-NINA-B222
- EVK-NINA-W131
- EVK-NINA-W132
- EVK-NINA-W151
- EVK-NINA-W152

### 2.2.1 Starting up

Perform the following steps to enable communication with the module:

1. Start the u-blox s-center evaluation software.
2. Use the default baud rate 115200, 8N1 with flow control. Now, it is possible to communicate with the module through AT commands.

For a list of available AT commands, see the u-blox Short Range AT Commands Manual [5].

### 2.2.2 Getting the latest software

Go to the u-blox support web page to obtain the latest available software. Instructions on reflashing the evaluation board can be found in the Software section of the NINA-B2 System Integration Manual [8] or the NINA-W1 System Integration Manual [7].

# Appendix

## A Layouts

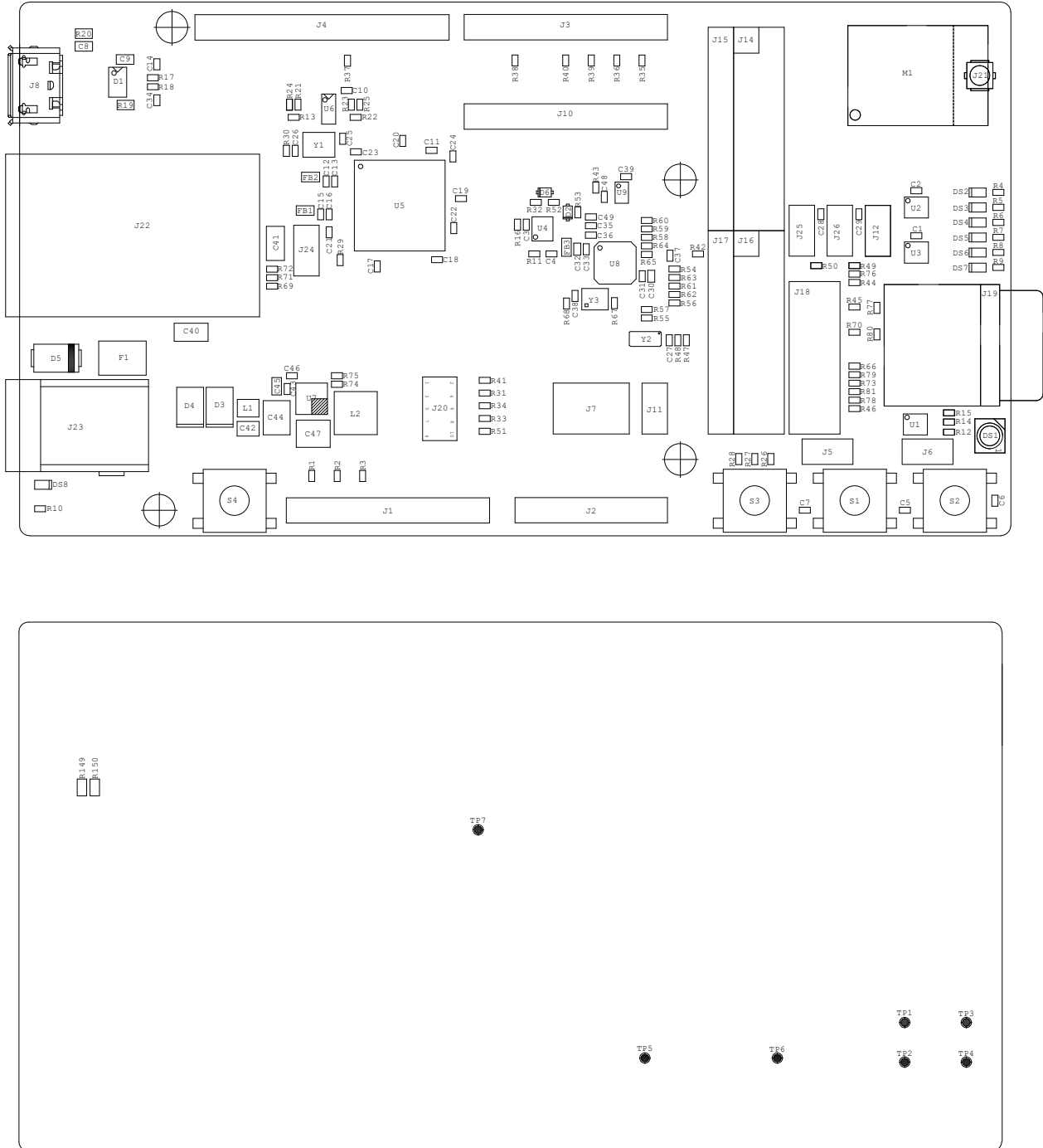
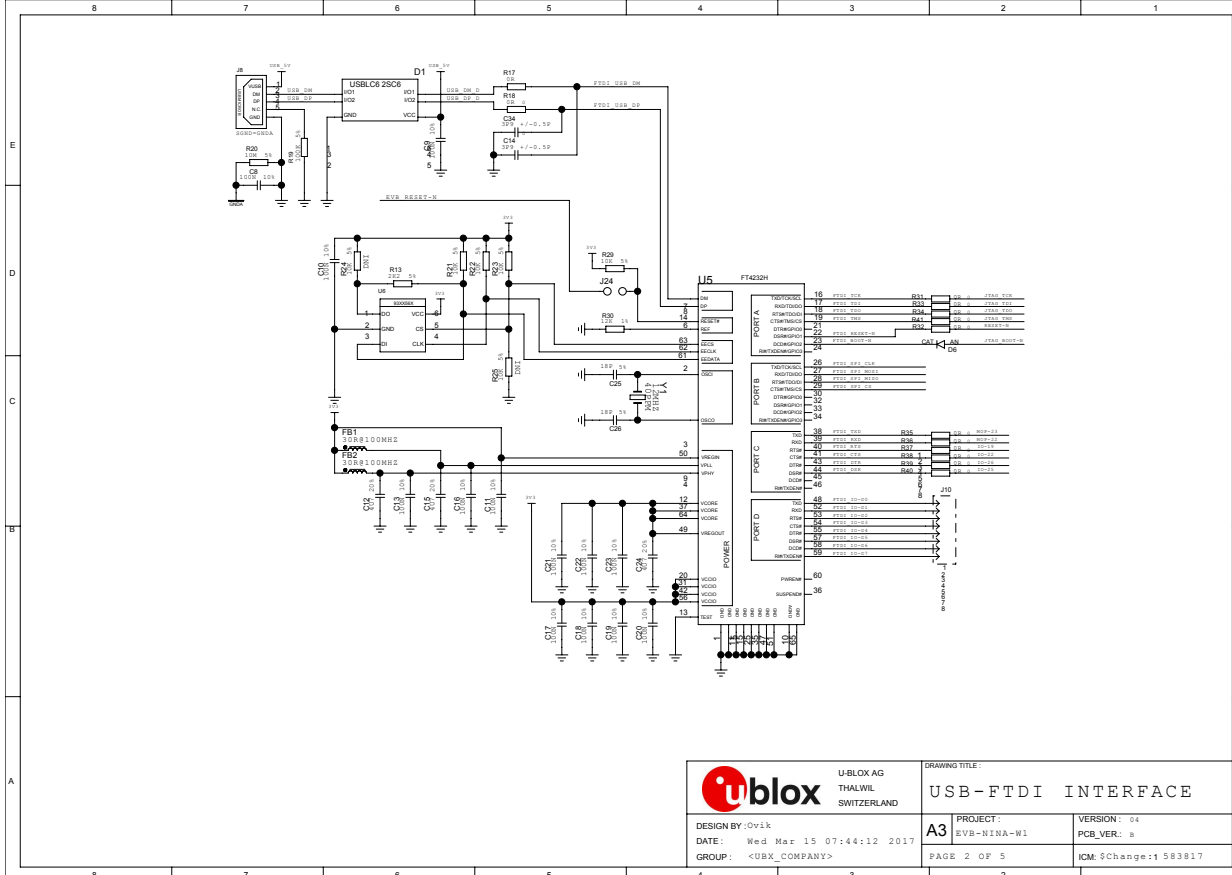
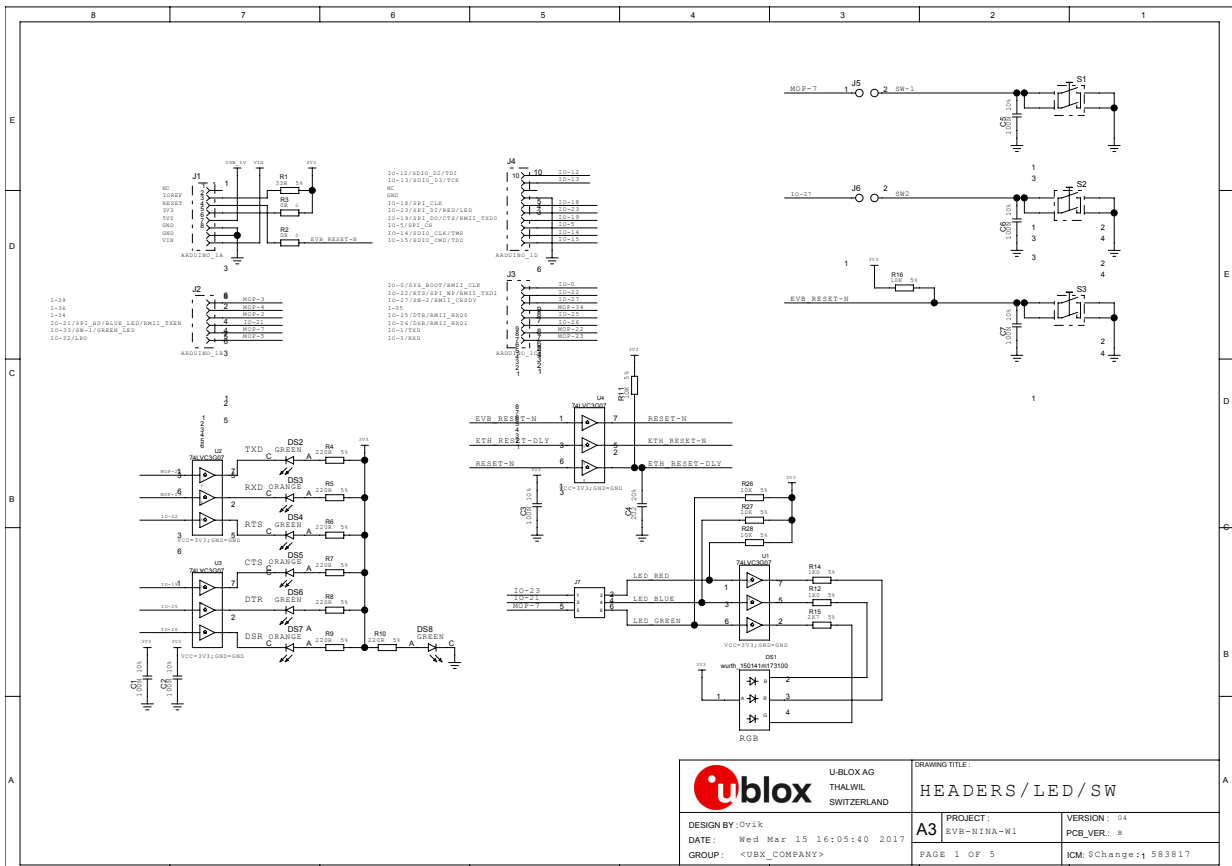
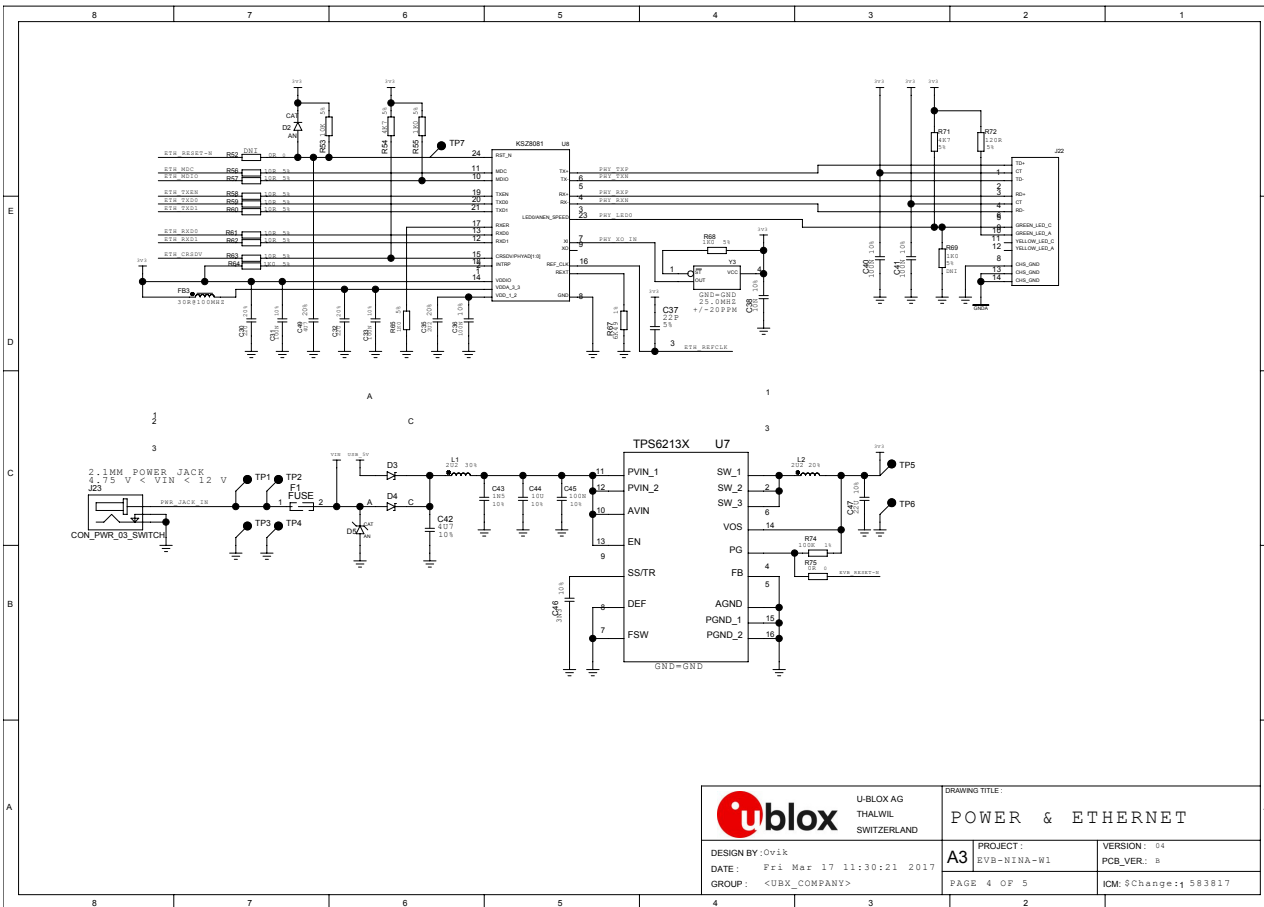
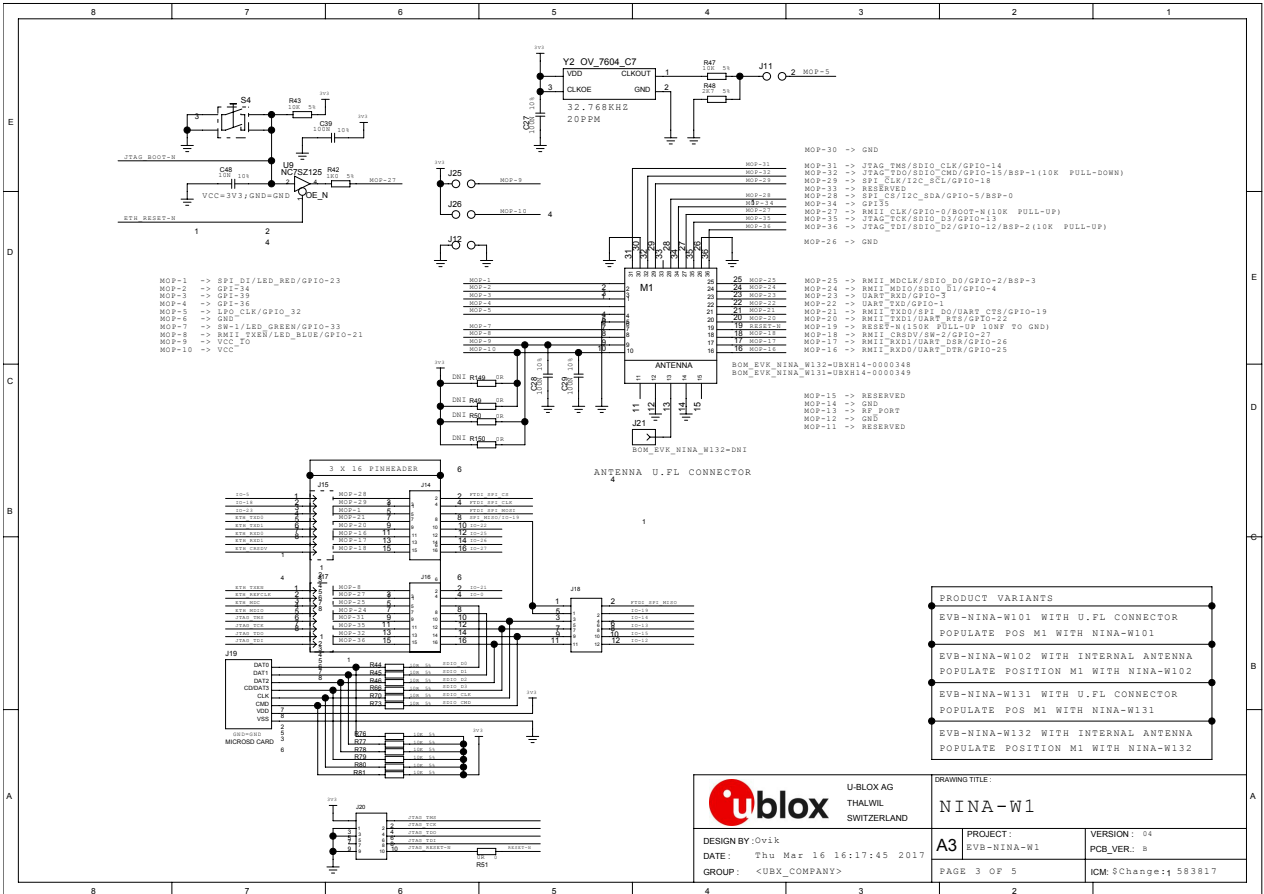


Figure 10: Primary and secondary side layouts of EVK-NINA-W1/EVK-NINA-B2

## B Schematic drawings







REVISION HISTORY			
REV	SHEET	DESCRIPTION	DATE/DESIGNER
01	ALL	FIRST VERSION OF EVK-NINA-W1	OVIK
02	ALL	REVISED AFTER REVISION MEETING 2016-10-18 OF EVB-NINA-W1	2016-10-21 OVIK
03	ALL	SHEET-1, PINSWOP ON U1 AND U4 SHEET-2, PIN SWOP OF SIGNALS "FTDI_BOOT-N" AND "FTDI_RESET-N", REMOVED J9 R33 R34 R41 SHEET-3, REPLACED J12 WITH 3X2-PIN JUMPERS, REDUCED NUMBER OF PINS ON J28, REMOVED TP7-TP19 SHEET-4, ADDED TP1-TP7	2016-11-02 OVIK
04	ALL	SHEET-1, PINSWOP ON J7 FIN 2 AND 4, J3 FIN 2 AND 3, ADDED 3 X 50-RESISTOR ON U1 SHEET-2, CHANGED J5 TO ROLEX 133017-0001 MICRO USB B SURFACE MOUNT WITH 2H SOLDER TABS SHEET-3, ADDED 5 X 50-RESISTORS ON J19, REMOVED R46 AND CHANGED VALUE ON R88 SHEET-4, REMOVED "DNI" ON C12 AND C13 (NEEDED TO REDUCE CONDUCTED EMISSIONS)	2017-03-15 OVIK

U-BLOX AG THALWIL SWITZERLAND	DRAWING TITLE: <b>REVISION HISTORY</b>	
	DESIGN BY: Ovik DATE: Thu Mar 16 16:19:13 2017 GROUP: <UBX_COMPANY>	A3 PROJECT: EVB-NINA-W1 PAGE 5 OF 5


## C Glossary

Name	Definition
COM	Communication
CTS	Clear To Send
DSR	Data Set Ready
DTR	Data Terminal Ready
EVK	Evaluation Kit
GND	Ground
GPI	General Purpose Input
GPIO	General Purpose Input/Output
IO	Input-Output
LED	Light-Emitting Diode
PHY	Physical layer
U.FL	Miniature coaxial RF connector
USB	Universal Serial Bus
RF	Radio frequency
RMII	Reduced Media-Independent Interface
RTS	Request To Send
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
VCC	IC power-supply pin

**Table 9: Explanation of abbreviations used**

## Related documents

- [1] NINA-W10 Data Sheet, document number UBX-17065507
- [2] NINA-W13 Data Sheet, document number UBX-17006694
- [3] NINA-W15 Data Sheet, document number UBX-18006647
- [4] NINA-B2 Data Sheet, document number UBX-18006649
- [5] u-blox Short Range AT Commands Manual, document number UBX-14044127
- [6] FTDI FT4232H QUAD HIGH SPEED USB TO MULTIPURPOSE UART/MPSSSE IC Datasheet - [http://www.ftdichip.com/Support/Documents/DataSheets/ICs/DS\\_FT4232H.pdf](http://www.ftdichip.com/Support/Documents/DataSheets/ICs/DS_FT4232H.pdf)
- [7] NINA-W1 System Integration Manual, document number UBX-17005730
- [8] NINA-B2 System Integration Manual, document number UBX-18011096

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## Revision history

Revision	Date	Name	Comments
R01	22-May-2017	ovik, kgom	Initial release.
R02	04-Jul-2017	ovik, mwej	Updated Figure 9 and Table 8 due to pin swap on connectors J2 and J3. Updated Figure 10 and schematic drawing (Appendix B). Updated assigned COM ports in section 2.1.
R03	09-Nov-2017	kgom	Renamed this document as EVK-NINA-W13 User Guide and updated the content due to the availability of a separate user guide for the EVK-NINA-W10x evaluation kits (UBX-17057549).
R04	12-Mar-2018	cmag	Updated the software version to 1.0.0 in the last table on page 2 and the "Related documents and links" section.
R05	29-Nov-2018	fbro, kgom	Renamed this document. Restructured the information to include support for EVK-NINA-W1 and EVK-NINA-B2.

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