4.0mΩ, 100V, N-Channel Power MOSFET SRT10N040L

General Description

The Sanrise SRT10N040L is a low voltage power MOSFET, fabricated using advanced split gate trench technology. The resulting device has extremely low on resistance, low gate charge and fast switching time, making it especially suitable for applications which require superior power density and synchronous rectification.

The SRT10N040L break down voltage is 100V and it has a high rugged avalanche characteristics. The SRT10N040L is available in PDFN5*6 package.

Symbol

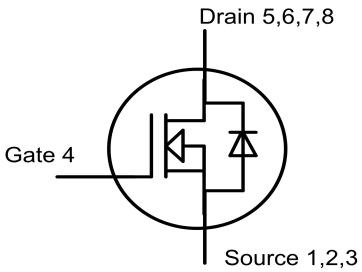


Figure 1 Symbol of SRT10N040L

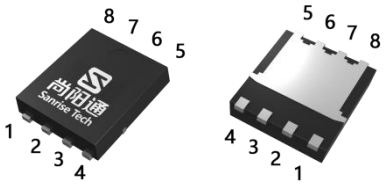
Features

- Ultra Low

$R_{DS(ON)\_TYP}$ = 3.3mΩ @V_{GS} = 10V.

- Ultra Low Gate Charge, Qg=68nC typ.
- Fast switching capability
- Robust design with better EAS performance
- Non-automotive Qualified

Package Type



PDFN5*6

Figure 2 Package Type of SRT10N040L

Application

- PD
- Charger/Adapter
- E-Tools
- BMS

Ordering Information

SRT10N040L□□–□

Circuit Type

Package

D56: PDFN5*6

E: Lead Free

G: Green

Blank: Tube

TR: Tape & Reel

Package	Part Number	Marking ID	Packing Type
PDFN5*6	SRT10N040LD56TR-G	SRT10N040LD56G	Tape & Reel

4.0mΩ, 100V, N-Channel Power MOSFET SRT10N040L

Absolute Maximum Ratings

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DSS}	100	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current, Package Limited	T_C=25ºC	I_D	100	A
	T_C=100ºC		82	
Continuous Drain Current, Silicon	T_C=25ºC		129	
Pulsed Drain Current (Note 2)		I_{DM}	300	A
Power Dissipation (T_C = 25°C)		P_D	131	W
Avalanche Destructive Energy, Single Pulse (Note 4)		E_{AS_Limit}	361	mJ
Avalanche Energy, Single Pulse (Note 3)		E_{AS}	64	mJ
Avalanche Energy, Repetitive (Note 2)		E_{AR}	0.1	mJ
Avalanche Current, Repetitive (Note 2)		I_{AR}	16.0	A
Continuous Diode Forward Current		I_S	100	A
Diode Pulse Current		$I_{S.PULSE}$	300	A
Operating Junction Temperature		T_J	150	ºC
Storage Temperature		T_{STG}	-55 to 150	ºC
Lead Temperature (Soldering, 10 sec)		T_{LEAD}	260	ºC

Note:

1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Repetitive Rating: Pulse width limited by maximum junction temperature
3. I_{AS}= 16.0A, V_{DD}= 50V, R_G= 25Ω, Starting T_J= 25°C
4. I_{AS_Limit}= 38A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C

Thermal Resistance

Parameter	Symbol	Min	Typ	Max	Unit
Thermal Resistance，Junction-to-Case	R_{thJC}			0.95	ºC/W
Thermal Resistance，Junction-to-Ambient	R_{thJA}			50	

Electrical Characteristics

T_J = 25℃, unless otherwise specified.

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Statistic Characteristics							
Drain-Source Breakdown Voltage		BV_{DSS}	V_{GS}=0V, I_D=250uA	100			V
Zero Gate Voltage Drain Current		I_{DSS}	V_{DS}=100V, V_{GS}=0V			1	uA
Gate-Body Leakage Current	Forward	I_{GSSF}	V_{GS}=20V, V_{DS}=0V			100	nA
	Reverse	I_{GSSR}	V_{GS}=-20V, V_{DS}=0V			-100	
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=0.25mA	1.2	1.8	2.4	V
Static Drain-Source On-Resistance		$R_{DS(ON)}$	V_{GS}=4.5V, I_D=20A		4.2	6.0	mΩ
Static Drain-Source On-Resistance		$R_{DS(ON)}$	V_{GS}=10V, I_D=20A		3.3	4.0	mΩ
Gate Resistance		R_G	f=1MHz, Open Drain		1.0		Ω
Dynamic Characteristics							
Input Capacitance		C_{ISS}	V_{DS}=50V, V_{GS}=0V, f=1MHz		4.4		nF
Output Capacitance		C_{OSS}			1.3		nF
Reverse Transfer Capacitance		C_{RSS}			23		pF
Effective output capacitance, energy related NOTE5		$C_{O(er)}$	V_{GS}=0V, V_{DS}=0…60V		1.7		nF
Effective output capacitance, time related NOTE6		$C_{O(tr)}$			2.0		
Turn-on Delay Time		$t_{d(on)}$	V_{DD}=50V, I_D=20A R_G=3.0Ω, V_{GS}=10V		15		nS
Rise Time		t_r			8		
Turn-off Delay Time		$t_{d(off)}$			39		
Fall Time		t_f			12		
Gate Charge Characteristics							
Gate to Source Charge		Q_{gs}	V_{DD}=50V, I_D=20A V_{GS}=0 to 4.5V		15		nC
Gate to Drain Charge		Q_{gd}			12		
Gate Charge Total		Q_g			34		
Gate Charge Total		Q_g	V_{DD}=50V, I_D=20A V_{GS}=0 to 10V		68		nC
Gate Charge Total, sync FET		Q_g	V_{DD}=0.1V, V_{GS}=0 to 10V		61		nC
Reverse Diode Characteristics							
Drain-Source Diode Forward Voltage		V_{SD}	V_{GS}=0V, I_{SD}=20A		0.81	1.1	V
Reverse Recovery Time		t_{rr}	V_R=50V, I_F=20A dI$_F$/dt=100A/us		49		nS
Reverse Recovery Charge		Q_{rr}			74		nC
Peak Reverse Recovery Current		I_{rrm}			3		A

Note:

5. $C_{O(er)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 60V
6. $C_{O(tr)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 60 V

Typical Performance Characteristics

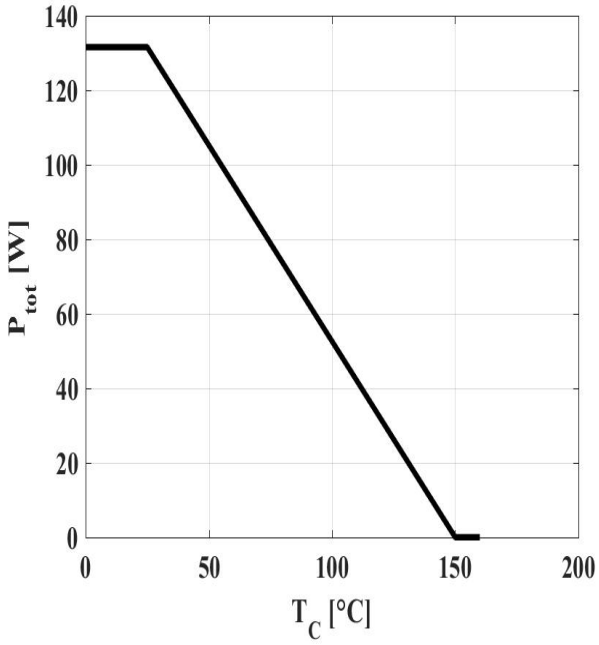
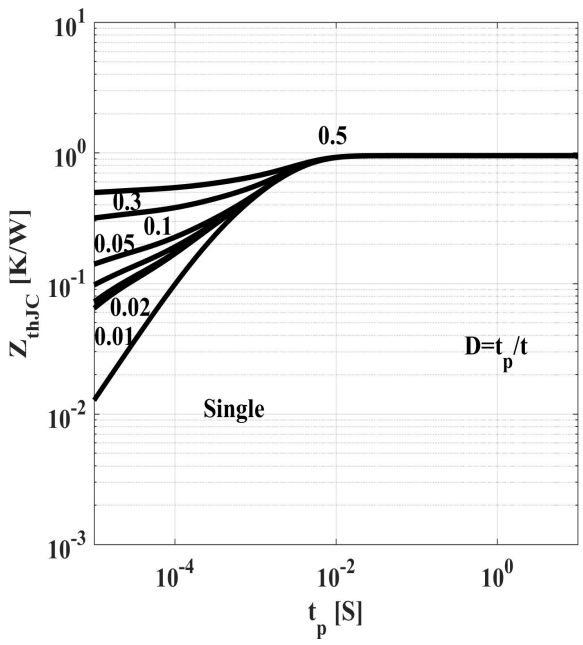
Figure 3A: Power Dissipation	Figure 4: Max. Transient Thermal Impedance
	
$P_{tot}=f(T_c)$	$Z_{(thJC)}=f(t_p)$;parameter:$D=t_p/T$

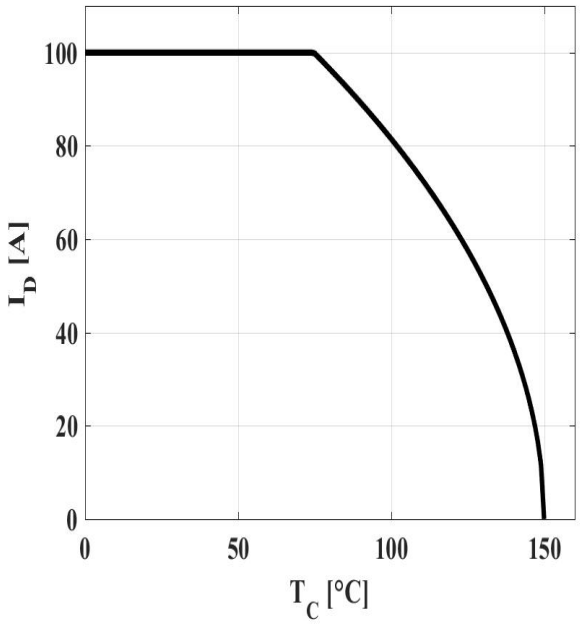
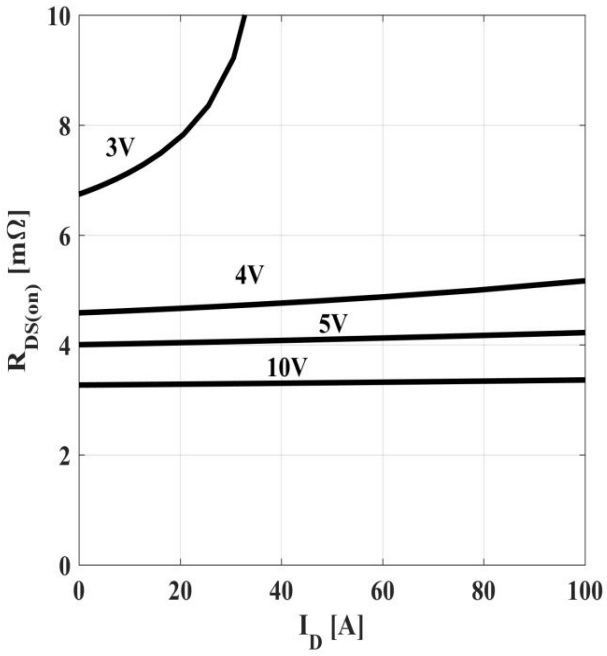
Figure5: Drain Current	Figure6: Typ. Drain-Source On-State
	
$I_D=f(T_C)$;$V_{GS}\geq 10V$	$R_{DS(ON)}=f(I_D)$;$T_j=25°C$; parameter:V_{GS}

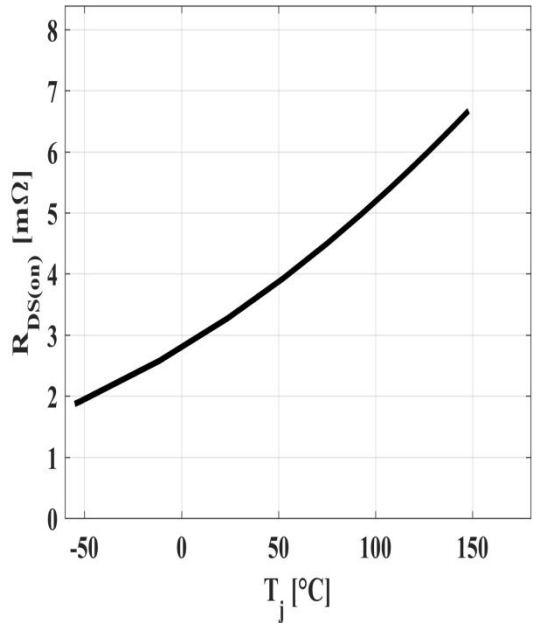
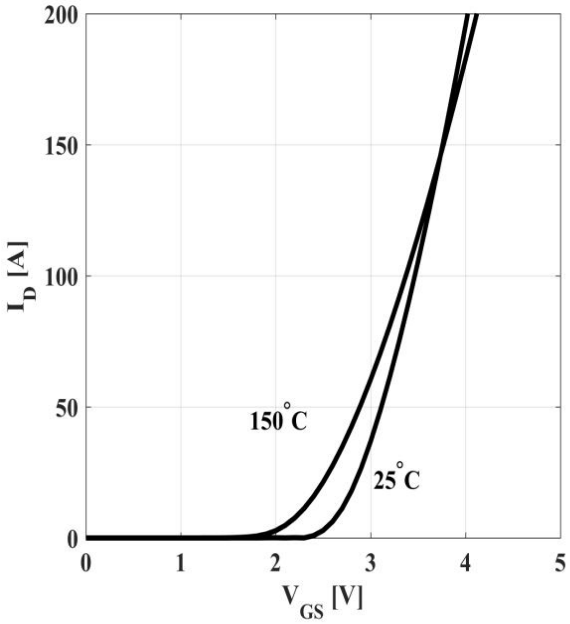
Figure7: Typ. Drain-Source On-State	Figure8: Typ. Transfer Characteristics
	
$R_{DS(ON)}$=f(T_j);I_D=20A;V_{GS}=10V	I_D=f(V_{GS}); |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

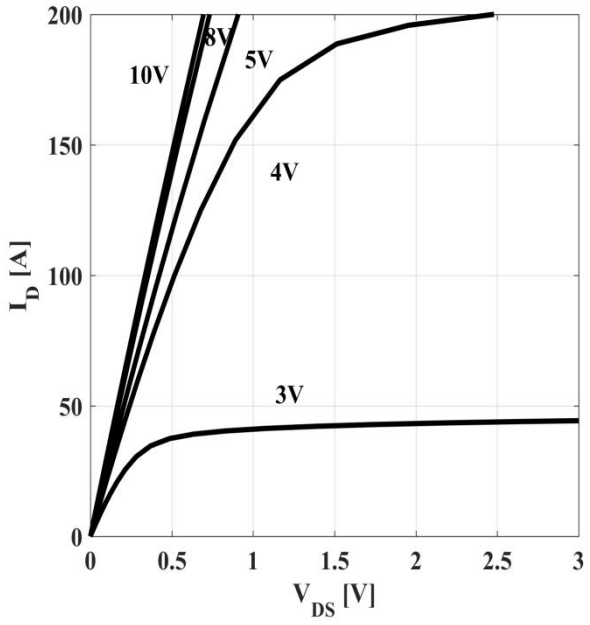
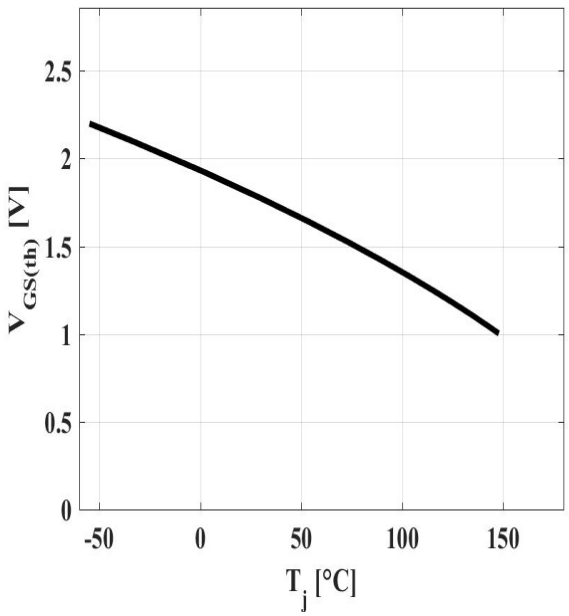
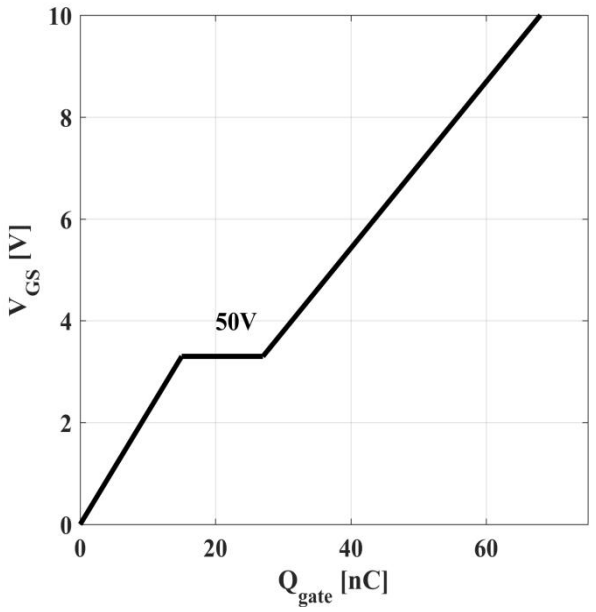
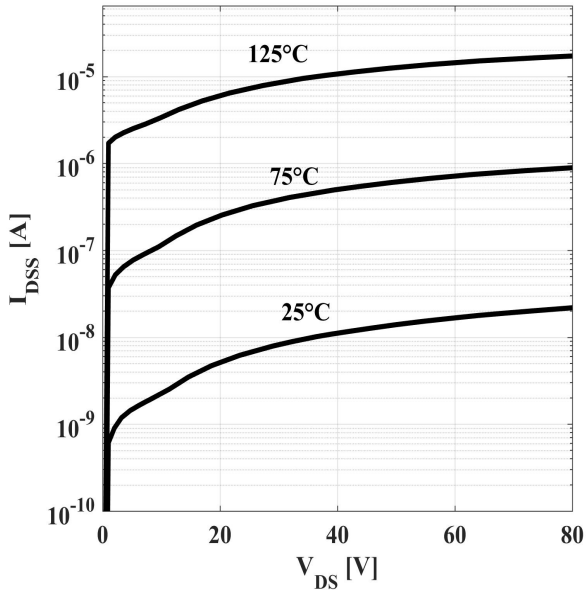
Figure9: Typ. Output Characteristics	Figure10: Typ.Gate Threshold Voltage
	
I_D=f(V_{DS});Tj=25ºC; parameter:V_{GS}	$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}; I_{DS}=250μA

Figure 11: Typ. Gate Charge



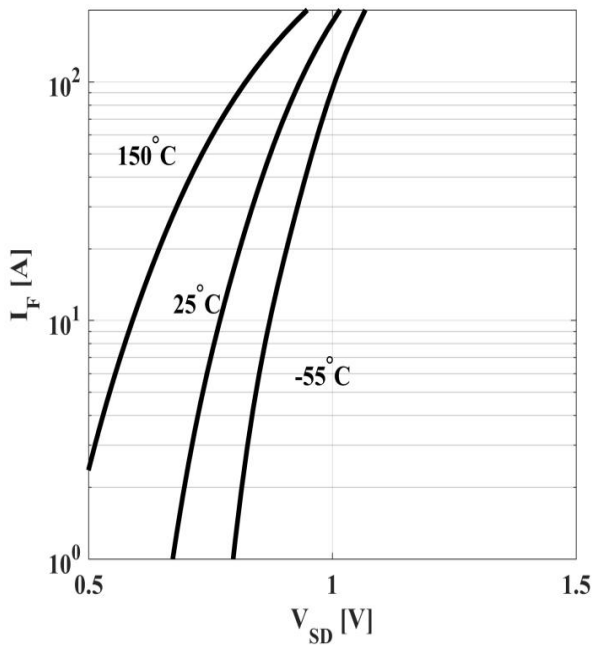
V_{GS}= f(Q_{gate}), I_D=20A pulsed

Figure 12: Drain-Source Leakage Current



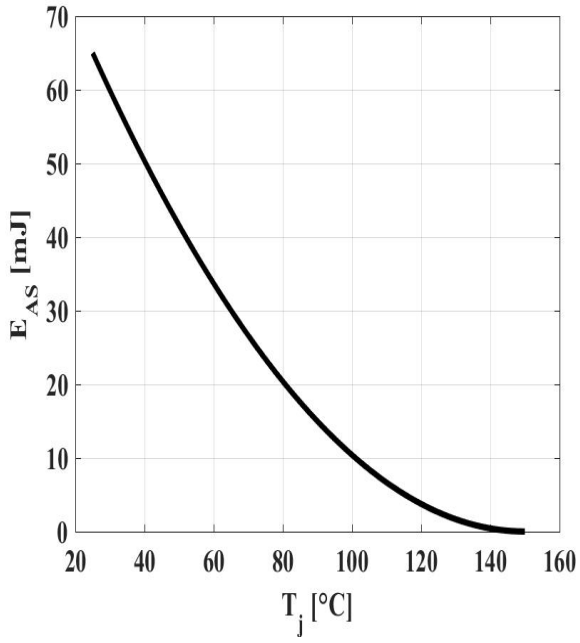
I_{DSS}=f(V_{DS}); V_{GS}=0V; parameter: T_j

Figure 13: Forward Characteristics of Reverse Diode



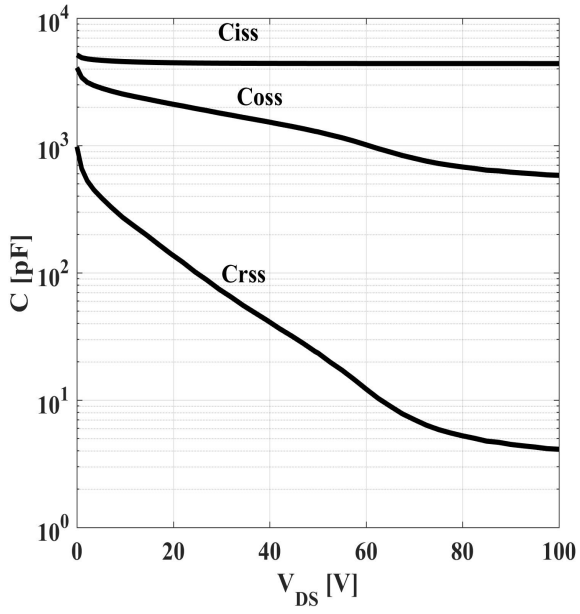
I_F=f(V_{SD}); parameter: T_j

Figure 14: Avalanche Energy



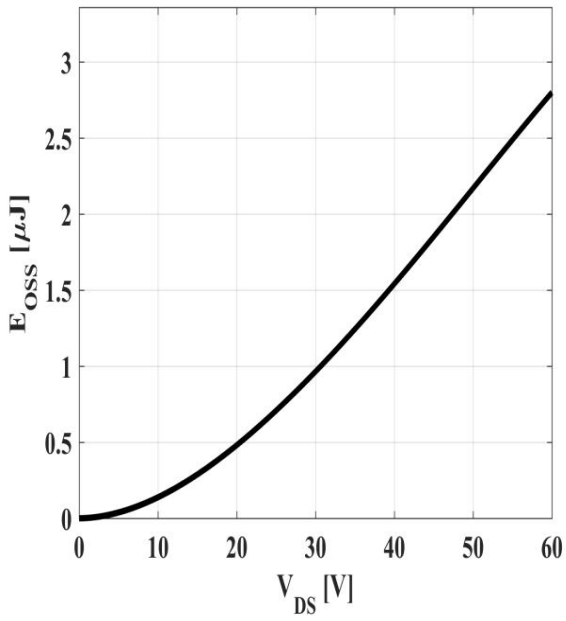
E_{AS}=f(T_j);I_D=10.0A; V_{DD}=50V

Figure 15: Typ. Capacitances



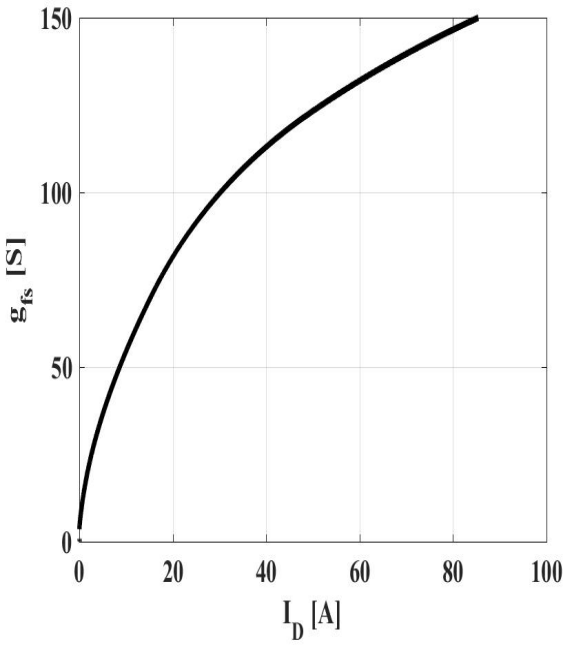
$C=f(V_{DS})$; $V_{GS}=0$; f=1MHz

Figure 16: C_{OSS} Stored Energy



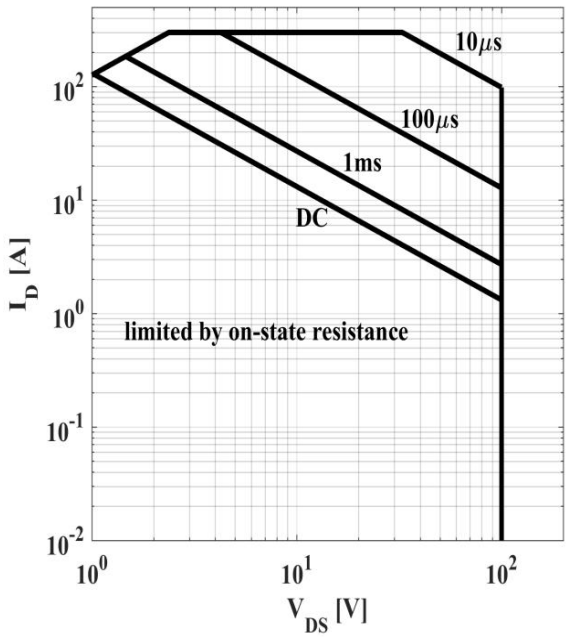
$E_{OSS}=f(V_{DS})$

Figure17: Typ. Forward Trans conductance



$g_{fs}=f(I_D)$; T_j=25°C

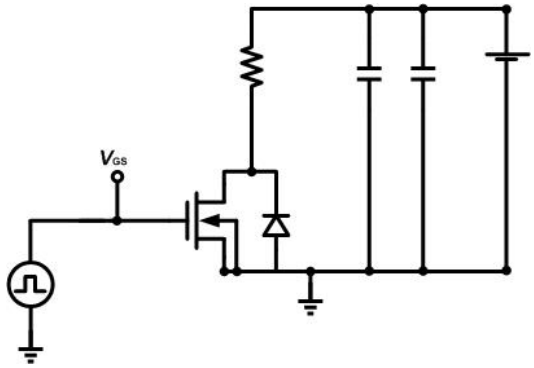
Figure 18: Safe Operating Area

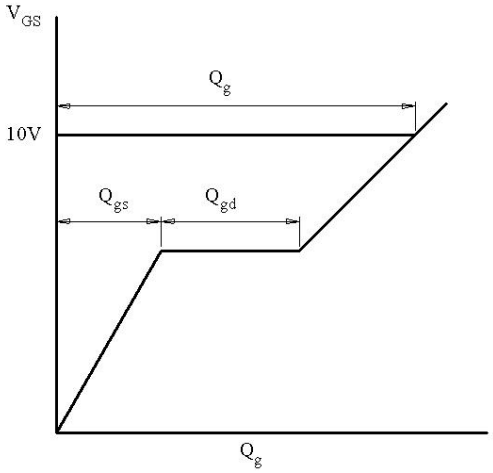


$I_D = f(V_{DS})$; T_c= 25ºC; V_{GS}>7V; parameter t_p

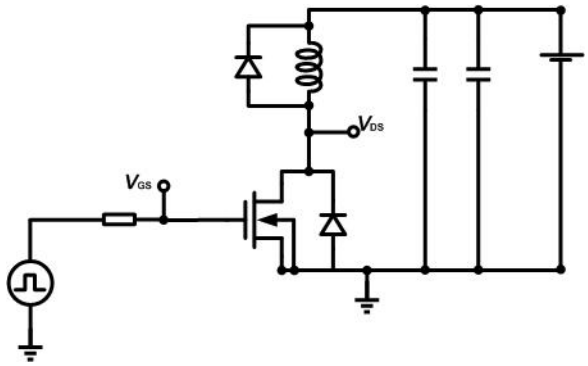
Test Circuits

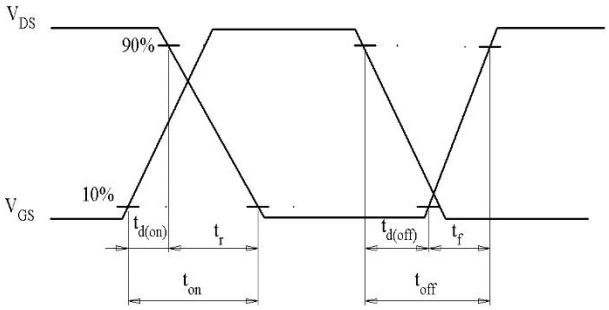
1. Gate Charge Test Circuit & Waveform



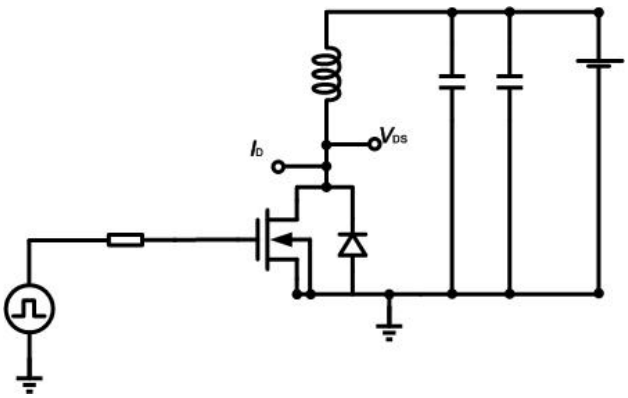


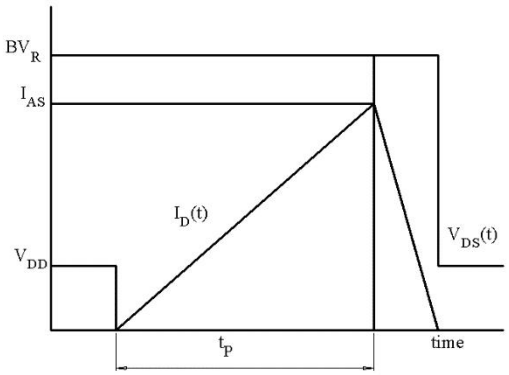
2. Switch Time Test Circuit



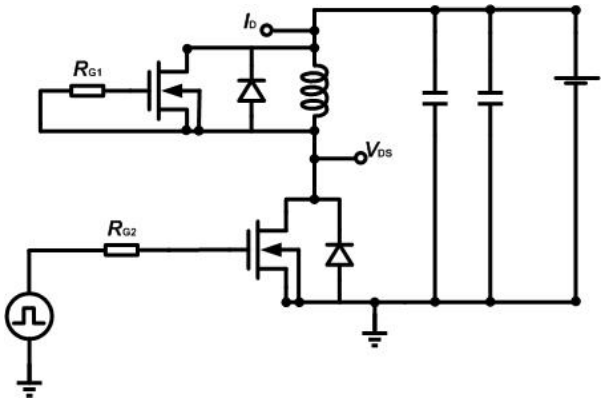


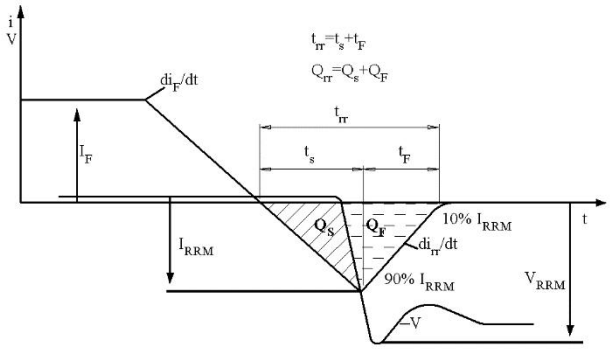
3. Unclamped Inductive Switching Test Circuit & Waveforms





4. Test Circuit and Waveform for Diode Characteristics

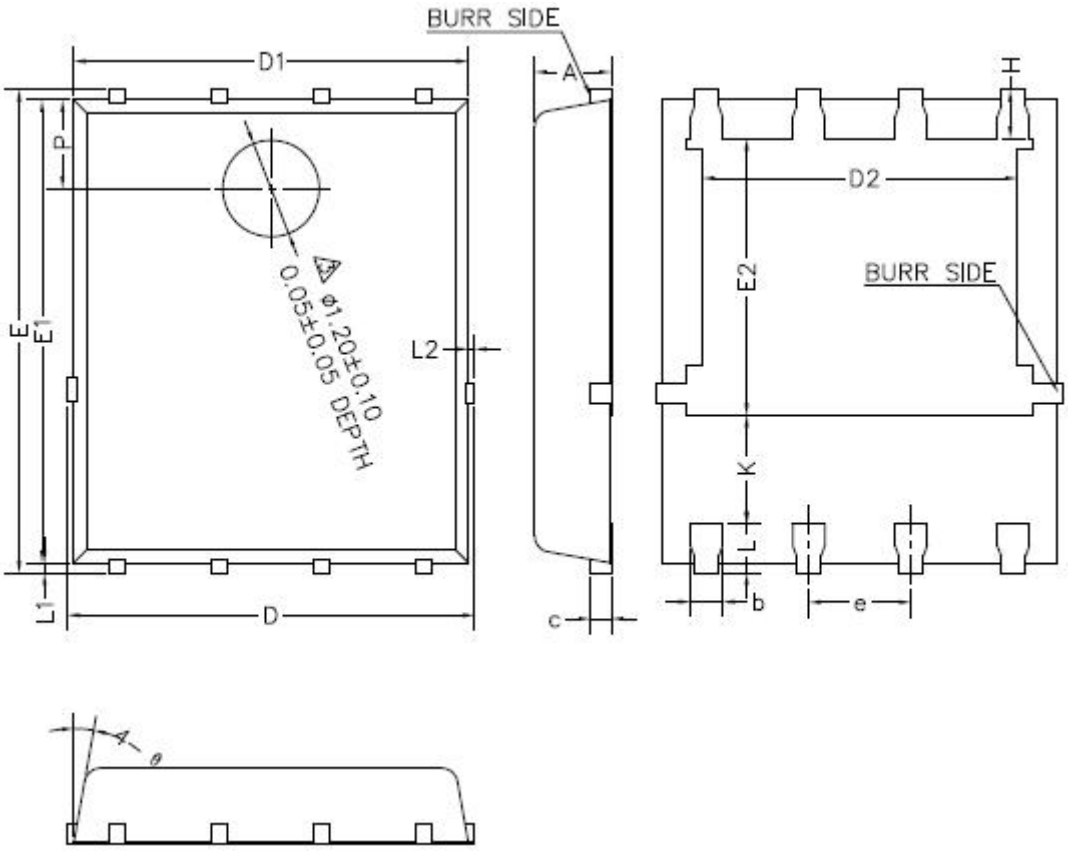




4.0mΩ, 100V, N-Channel Power MOSFET SRT10N040L

Mechanical Dimensions

PDFN5*6 **Unit: mm**



Symbol	Dimensions(mm)		
	Min.	Typ.	Max.
A	0.90	1.10	1.20
b	0.35	0.40	0.45
c	0.21	0.25	0.34
D			5.10
D1	4,80	4.90	5.00
D2	3.91	4.01	4.11
e	1.17	1.27	1.37
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.34	3.44	3.54
H	0.51	0.61	0.71
K	1.10		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
L2			0.10
P	1.00	1.10	1.20
θ	8°	10°	12°

4.0mΩ, 100V, N-Channel Power MOSFET SRT10N040L

Sanrise Technology Limited Company

http://www.sanrise-tech.com

IMPORTANT NOTICE

Shenzhen Sanrise Technology Co., LTD. reserves the right to make changes without further notice to any products or specifications herein. Shenzhen Sanrise Technology Co., LTD. does not assume any responsibility for use of any its products for any particular purpose, nor does Shenzhen Sanrise Technology Co., LTD. assume any liability arising out of the application or use of any its products or circuits. Shenzhen Sanrise Technology Co., LTD. does not convey any license under its patent rights or other rights nor the rights of others.

Main Site:

- Headquarter

Shenzhen Sanrise Technology Co., LTD.

A1206, Skyworth building, No. 008, gaoxinnan 1st Road, Gaoxin District, Yuehai street,, Nanshan District, ShenZhen, P.R.China

Tel: +86-755-22953335

Fax: +86-755-22916878

- Shanghai Office

Sanrise Technology Limited Company

Rm.401, Building B, No. 666, Zhangheng Road, Zhangjiang Hi-Tech Park, Shanghai, P.R.China

Tel: +86-21-68825918