DATASHEET

ISL28136

5MHz, Single Precision Rail-to-Rail Input-Output (RRIO) Op Amp

FN6153
Rev 6.00
January 16, 2014

The ISL28136 is a low-power single operational amplifier optimized for single supply operation from 2.4V to 5.5V, allowing operation from one lithium cell or two Ni-Cd batteries. This device features a gain-bandwidth product of 5MHz and is unity-gain stable with a -3dB bandwidth of 13MHz.

This device features an Input Range Enhancement Circuit (IREC), which enables it to maintain CMRR performance for input voltages greater than the positive supply. The input signal is capable of swinging 0.25V above the positive supply and to the negative supply with only a slight degradation of the CMRR performance. The output operation is rail-to-rail.

The part typically draws less than 1mA supply current while meeting excellent DC accuracy, AC performance, noise and output drive specifications. Operation is guaranteed over -40°C to +125°C temperature range.

Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	PACKAGE (Pb-Free)	PKG. DWG. #
ISL28136FHZ-T7 (Note 1)	GABP (Note 4)	6 Ld SOT-23	P6.064A
ISL28136FHZ-T7A (Note 1)	GABP (Note 4)	6 Ld SOT-23	P6.064A
ISL28136FBZ	28136 FBZ	8 Ld SOIC	M8.15E
ISL28136FBZ-T7 (Note 1)	28136 FBZ	8 Ld SOIC	M8.15E
ISL28136EVAL1Z	Evaluation Board		

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL28136. For more information on MSL please see techbrief TB363.
4. The part marking is located on the bottom of the parts.

Features

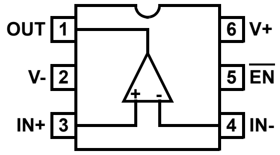
- 5MHz Gain bandwidth product @ A_V = 100
- 13MHz -3dB unity gain bandwidth
- 900µA typical supply current
- 150µV maximum offset voltage (8 Ld SOIC)
- 5nA typical input bias current
- Down to 2.4V single supply voltage range
- Rail-to-rail input and output
- Enable pin
- -40°C to +125°C operation
- Pb-free (RoHS compliant)

Applications

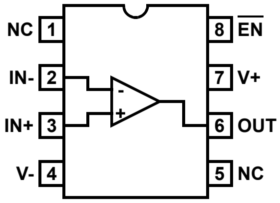
- Low-end audio
- 4mA to 20mA current loops
- Medical devices
- Sensor amplifiers
- ADC buffers
- DAC output amplifiers

Pinouts

ISL28136
(6 LD SOT-23)
TOP VIEW



ISL28136
(8 LD SOIC)
TOP VIEW



Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage	5.75V
Supply Turn-on Voltage Slew Rate	1V/µs
Differential Input Current	5mA
Differential Input Voltage	0.5V
Input Voltage	V- - 0.5V to V+ + 0.5V
ESD Rating	
Human Body Model	3kV
Machine Model	300V

Thermal Information

Thermal Resistance (Typical)	θJA (°C/W)	θJC (°C/W)
6 Ld SOT-23 Package (Note 5)	230	N/A
8 Ld SOIC Package (Notes 5, 6)	125	71

Ambient Operating Temperature Range	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Operating Junction Temperature	+125°C
Pb-free reflow profile	see link below

http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely affect product reliability and result in failures not covered by warranty.

NOTES:

5. θJA is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
6. For θJC, the "case temp" location is taken at the package top center.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L = Open, T_A = +25°C unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C.** Temperature data established by characterization.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
DC SPECIFICATIONS						
V_{OS}	Input Offset Voltage	8 Ld SOIC	-150	±10	150	µV
			-270		**270**	
		6 Ld SOT-23	-400	±10	400	µV
			-450		**450**	
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage vs Temperature			0.4		µV/°C
I_{OS}	Input Offset Current	T_A = -40°C to +85°C	-10	0	10	nA
			-15		15	
I_B	Input Bias Current	T_A = -40°C to +85°C	-35	5	35	nA
			-40		40	
V_{CM}	Common-Mode Voltage Range	Guaranteed by CMRR	0		5	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0V to 5V	90	114		dB
			85			
PSRR	Power Supply Rejection Ratio	V_+ = 2.4V to 5.5V	90	99		dB
			85			
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5V to 4V, R_L = 100kΩ to V_{CM}	600	1770		V/mV
			500			
		V_O = 0.5V to 4V, R_L = 1kΩ to V_{CM}		140		V/mV
V_{OUT}	Maximum Output Voltage Swing	Output low, R_L = 100kΩ to V_{CM}		3	6	mV
					10	
		Output low, R_L = 1kΩ to V_{CM}		70	90	mV
					110	
		Output high, R_L = 100kΩ to V_{CM}	4.99	4.994		V
			4.98			
		Output high, R_L = 1kΩ to V_{CM}	4.92	4.94		V
			4.89			
$I_{S,ON}$	Supply Current, Enabled	Per Amp	0.8	0.9	1.1	mA
					1.4	

Electrical Specifications V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L = Open, T_A = +25°C unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C.** Temperature data established by characterization. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
$I_{S,OFF}$	Supply Current, Disabled			10	14	µA
					16	
I_O+	Short-Circuit Output Source Current	R_L = 10Ω to V_{CM}	48	56		mA
			45			
I_O-	Short-Circuit Output Sink Current	R_L = 10Ω to V_{CM}	50	55		mA
			45			
V_{SUPPLY}	Supply Operating Range	V_+ to V_-	2.4		5.5	V
$V_{\overline{EN}H}$	$\overline{EN}$ Pin High Level		**2**			V
$V_{\overline{EN}L}$	$\overline{EN}$ Pin Low Level				**0.8**	V
$I_{\overline{EN}H}$	$\overline{EN}$ Pin Input High Current	$V_{\overline{EN}} = V_+$		1	1.5	µA
					1.6	
$I_{\overline{EN}L}$	$\overline{EN}$ Pin Input Low Current	$V_{\overline{EN}} = V_-$		16	25	nA
					30	
AC SPECIFICATIONS						
GBW	Gain Bandwidth Product	A_V = 100, R_F = 100kΩ, R_G = 1kΩ to V_{CM}		5		MHz
Unity Gain Bandwidth	-3dB Bandwidth	A_V = 1, R_F = 0Ω, R_L = 10kΩ to V_{CM}, V_{OUT} = 10mV_{P-P}		13		MHz
e_N	Input Noise Voltage Peak-to-Peak	f = 0.1Hz to 10Hz, R_L = 10kΩ to V_{CM}		0.4		µV_{P-P}
	Input Noise Voltage Density	f_O = 1kHz, R_L = 10kΩ to V_{CM}		15		nV/√Hz
i_N	Input Noise Current Density	f_O = 10kHz, R_L = 10kΩ to V_{CM}		0.35		pA/√Hz
CMRR	Input Common Mode Rejection Ratio	f_O = to 120Hz; V_{CM} = 1V_{P-P}, R_L = 1kΩ to V_{CM}		-90		dB
PSRR+ to 120Hz	Power Supply Rejection Ratio (V_+)	V_+, V_- = ±1.2V and ±2.5V, V_{SOURCE} = 1V_{P-P}, R_L = 1kΩ to V_{CM}		-88		dB
PSRR- to 120Hz	Power Supply Rejection Ratio (V_-)	V_+, V_- = ±1.2V and ±2.5V V_{SOURCE} = 1V_{P-P}, R_L = 1kΩ to V_{CM}		-105		dB
TRANSIENT RESPONSE						
SR	Slew Rate	V_{OUT} = ±1.5V; R_f = 50kΩ, R_G = 50kΩ to V_{CM}		±1.9		V/µs
t_r, t_f, Large Signal	Rise Time, 10% to 90%, V_{OUT}	A_V = +2, V_{OUT} = 2V_{P-P}, R_g = R_f = R_L = 1kΩ to V_{CM}		0.6		µs
	Fall Time, 90% to 10%, V_{OUT}	A_V = +2, V_{OUT} = 2V_{P-P}, R_g = R_f = R_L = 1kΩ to V_{CM}		0.5		µs
t_r, t_f, Small Signal	Rise Time, 10% to 90%, V_{OUT}	A_V = +2, V_{OUT} = 10mV_{P-P}, R_g = R_f = R_L = 1kΩ to V_{CM}		65		ns
	Fall Time, 90% to 10%, V_{OUT}	A_V = +2, V_{OUT} = 10mV_{P-P}, R_g = R_f = R_L = 1kΩ to V_{CM}		62		ns
$t_{\overline{EN}}$	Enable to Output Turn-on Delay Time, 10% $\overline{EN}$ to 10% V_{OUT}	$V_{\overline{EN}}$ = 5V to 0V, A_V = +2, R_g = R_f = R_L = 1kΩ to V_{CM}		5		µs
	Enable to Output Turn-off Delay Time, 10% $\overline{EN}$ to 10% V_{OUT}	$V_{\overline{EN}}$ = 0V to 5V, A_V = +2, R_g = R_f = R_L = 1kΩ to V_{CM}		0.3		µs

NOTE:

7. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Typical Performance Curves $V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L = \text{Open}$

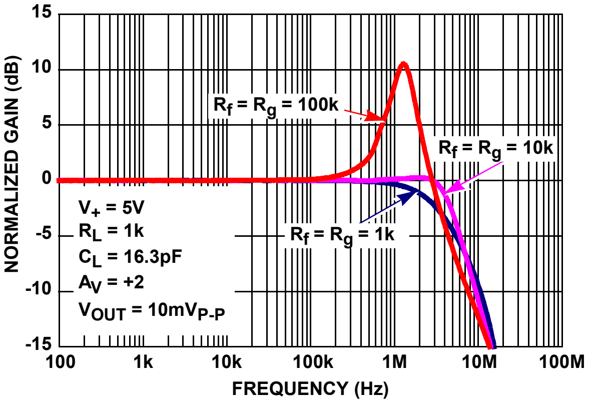


FIGURE 1. GAIN vs FREQUENCY vs FEEDBACK RESISTOR VALUES R_f/R_g

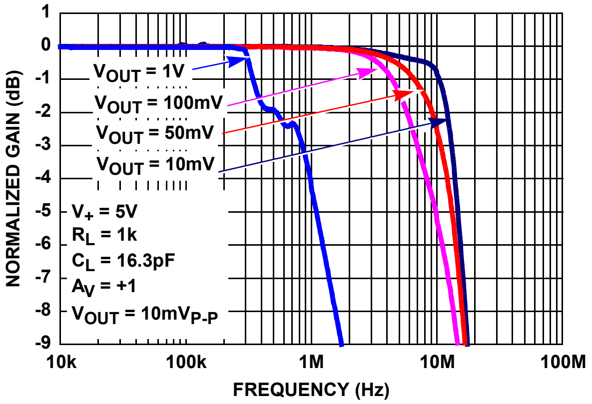


FIGURE 2. GAIN vs FREQUENCY vs V_{OUT}, R_L = 1k

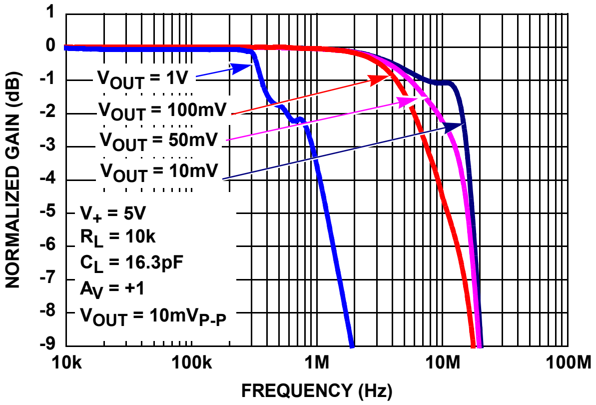


FIGURE 3. GAIN vs FREQUENCY vs V_{OUT}, R_L = 10k

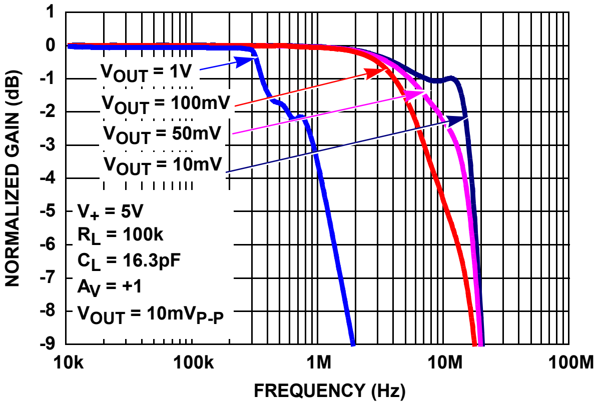


FIGURE 4. GAIN vs FREQUENCY vs V_{OUT}, R_L = 100k

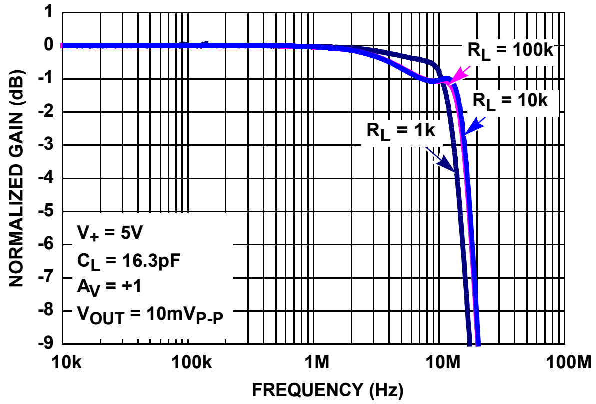


FIGURE 5. GAIN vs FREQUENCY vs R_L

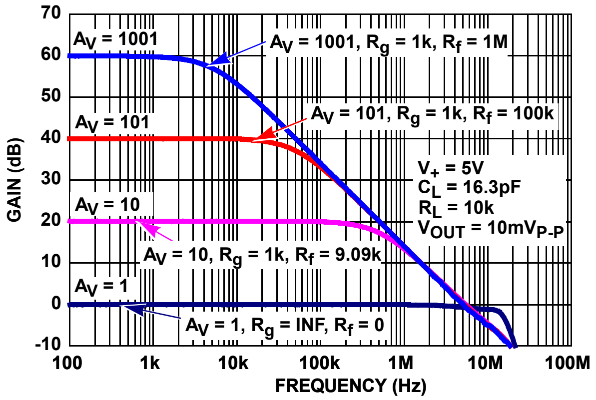


FIGURE 6. FREQUENCY RESPONSE vs CLOSED LOOP GAIN

Typical Performance Curves V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L = Open **(Continued)**

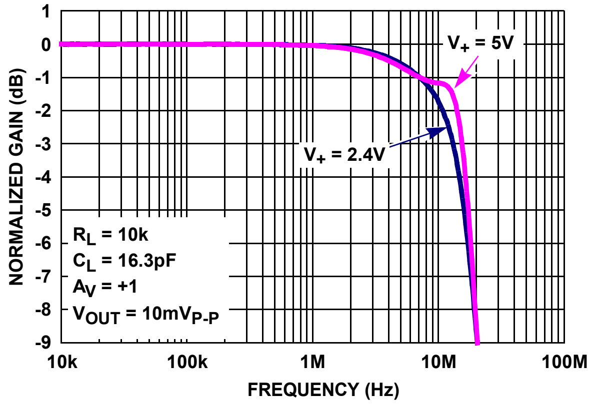


FIGURE 7. GAIN vs FREQUENCY vs SUPPLY VOLTAGE

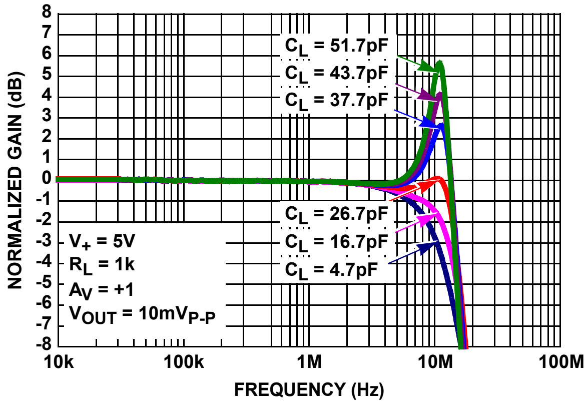


FIGURE 8. GAIN vs FREQUENCY vs C_L

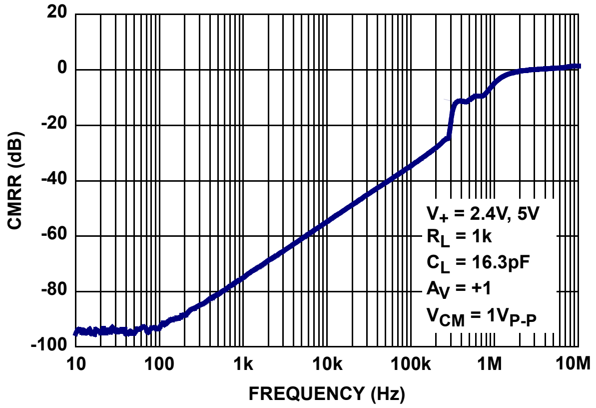


FIGURE 9. CMRR vs FREQUENCY; V_+ = 2.4V AND 5V

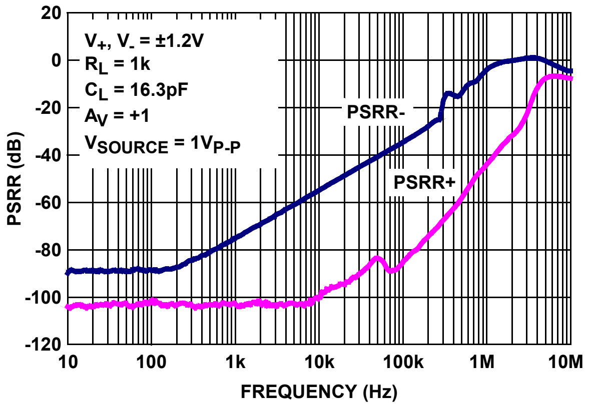


FIGURE 10. PSRR vs FREQUENCY, V_+, V_- = ±1.2V

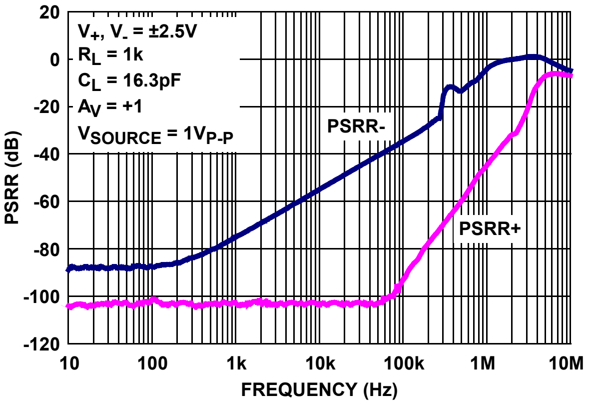


FIGURE 11. PSRR vs FREQUENCY, V_+, V_- = ±2.5V

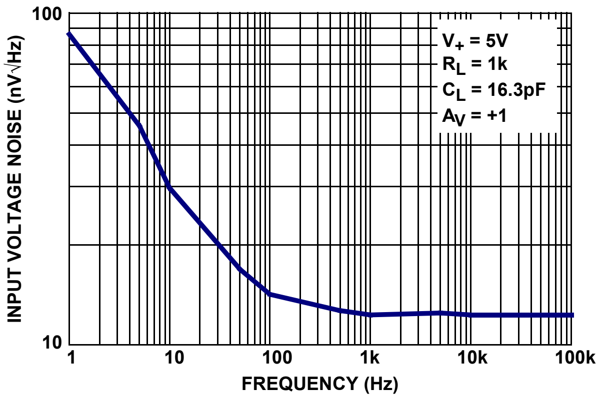


FIGURE 12. INPUT VOLTAGE NOISE DENSITY vs FREQUENCY

Typical Performance Curves V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L = Open **(Continued)**

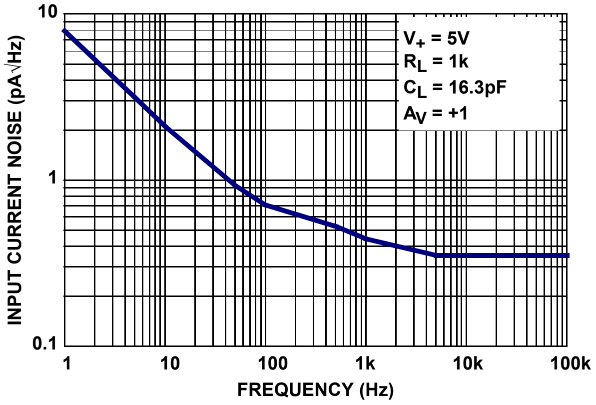


FIGURE 13. INPUT CURRENT NOISE DENSITY vs FREQUENCY

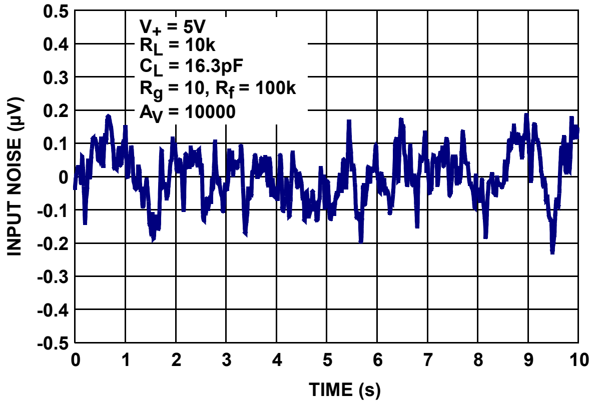


FIGURE 14. INPUT VOLTAGE NOISE 0.1Hz TO 10Hz

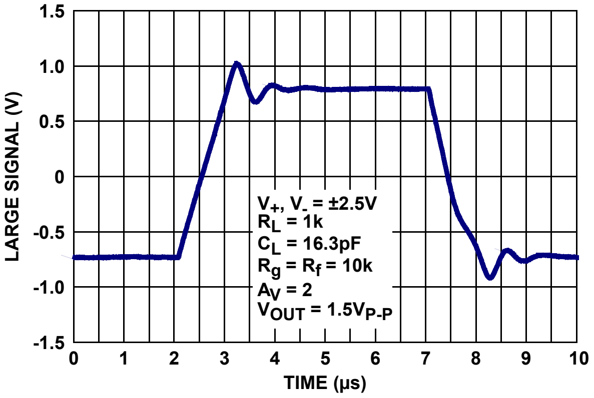


FIGURE 15. LARGE SIGNAL STEP RESPONSE

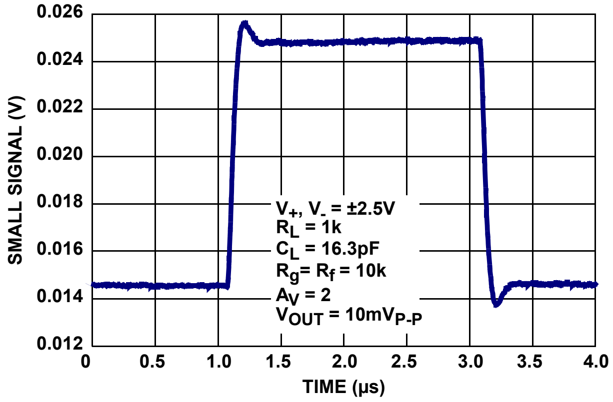


FIGURE 16. SMALL SIGNAL STEP RESPONSE

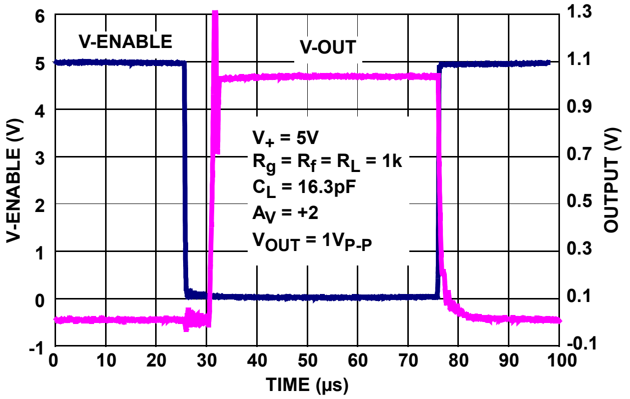


FIGURE 17. ENABLE TO OUTPUT RESPONSE

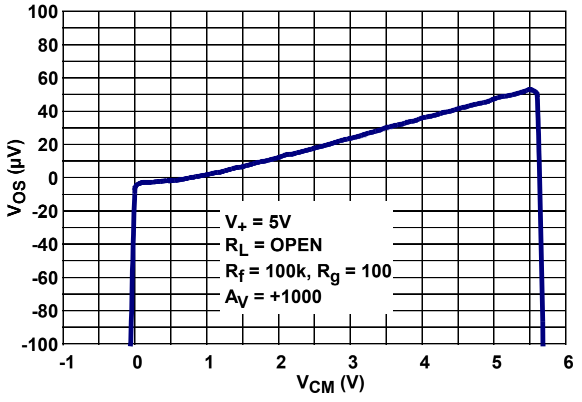


FIGURE 18. INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

Typical Performance Curves V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L = Open **(Continued)**

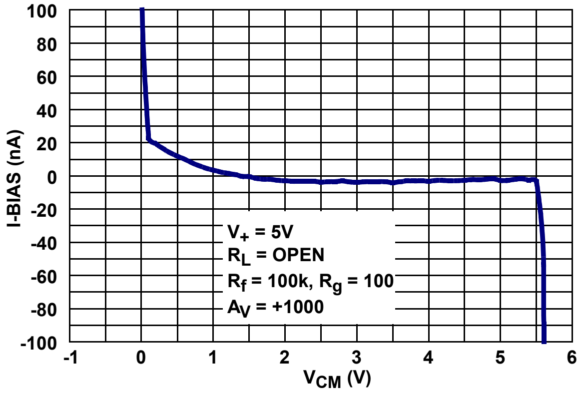


FIGURE 19. INPUT OFFSET CURRENT vs COMMON-MODE INPUT VOLTAGE

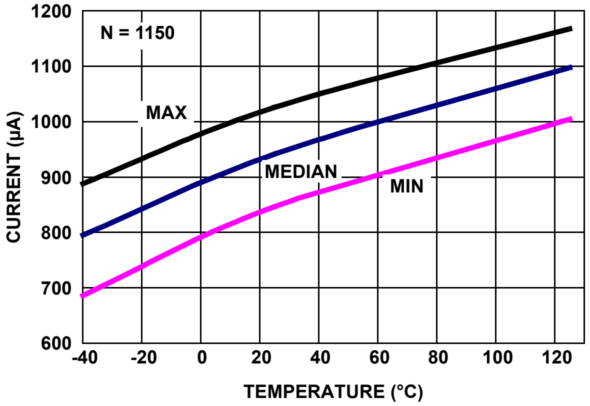


FIGURE 20. SUPPLY CURRENT ENABLED vs TEMPERATURE, V_+, V_- = ±2.5V

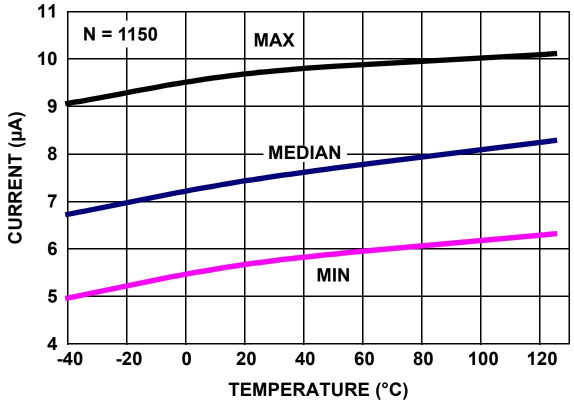


FIGURE 21. SUPPLY CURRENT DISABLED vs TEMPERATURE, V_+, V_- = ±2.5V

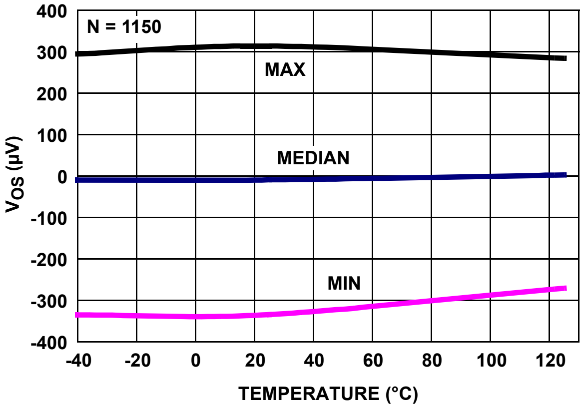


FIGURE 22. V_{OS} vs TEMPERATURE, V_+, V_- = ±2.5V, SOT PACKAGE

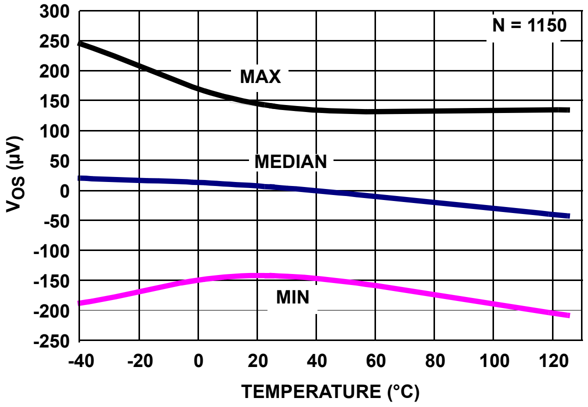


FIGURE 23. V_{OS} vs TEMPERATURE, V_+, V_- = ±2.5V, SOIC PACKAGE

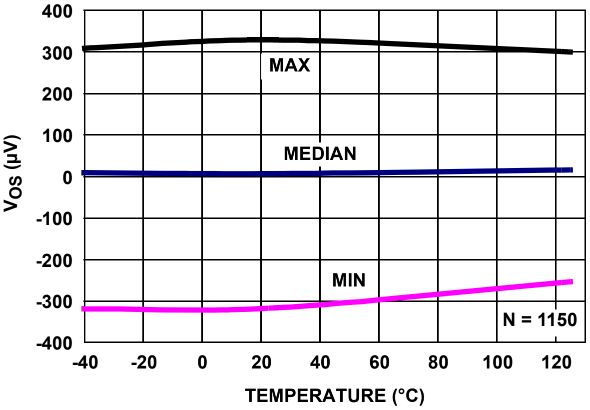


FIGURE 24. V_{OS} vs TEMPERATURE, V_+, V_- = ±1.2V, SOT PACKAGE

Typical Performance Curves $V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L = Open$ **(Continued)**

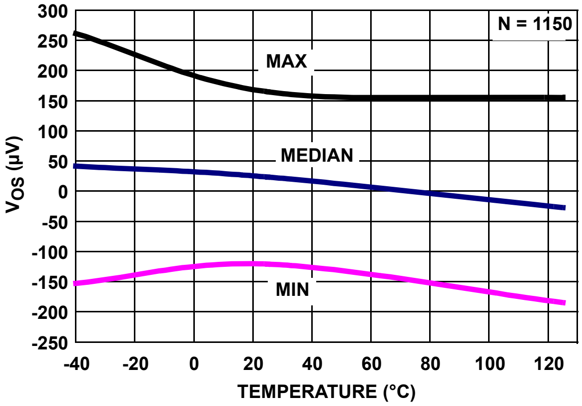


FIGURE 25. V_{OS} vs TEMPERATURE, V_+, $V_- = ±1.2V$SOIC PACKAGE

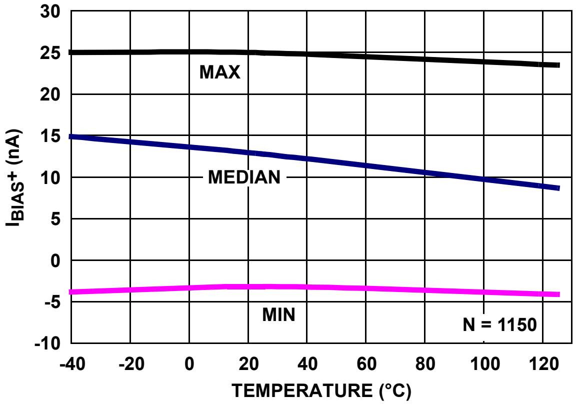


FIGURE 26. I_{BIAS}+ vs TEMPERATURE, V_+, $V_- = ±2.5V$

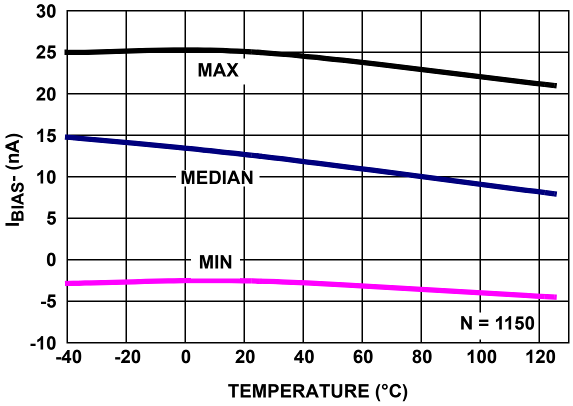


FIGURE 27. I_{BIAS}- vs TEMPERATURE, V_+, $V_- = ±2.5V$

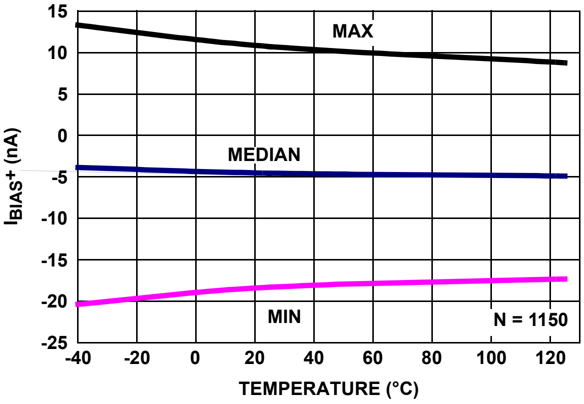


FIGURE 28. I_{BIAS}+ vs TEMPERATURE, V_+, $V_- = ±1.2V$

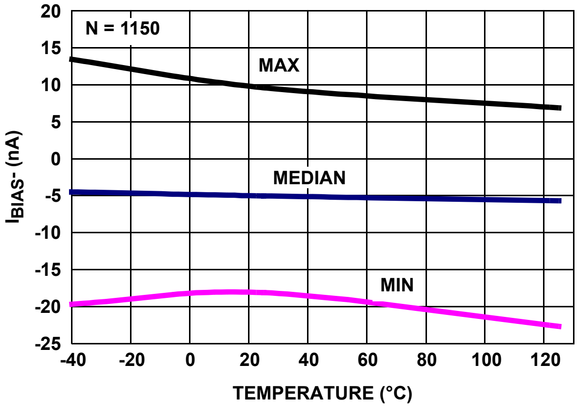


FIGURE 29. I_{BIAS}- vs TEMPERATURE, V_+, $V_- = ±1.2V$

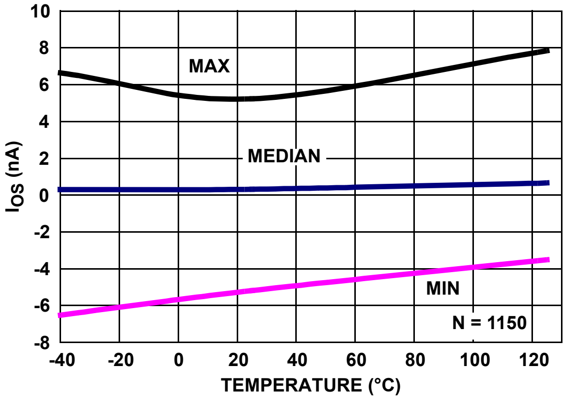


FIGURE 30. I_{OS} vs TEMPERATURE, V_+, $V_- = ±2.5V$

Typical Performance Curves $V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L = Open$ **(Continued)**

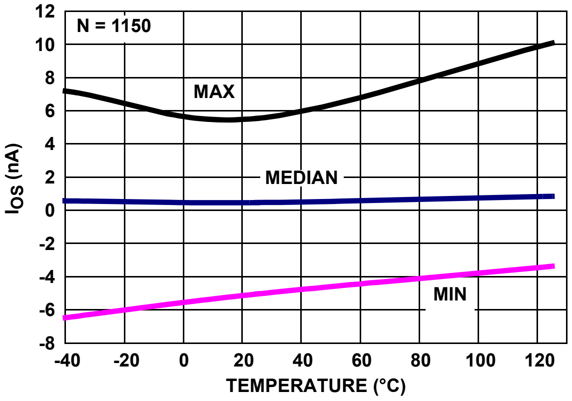


FIGURE 31. I_{OS} vs TEMPERATURE, $V_+, V_- = \pm1.2V$

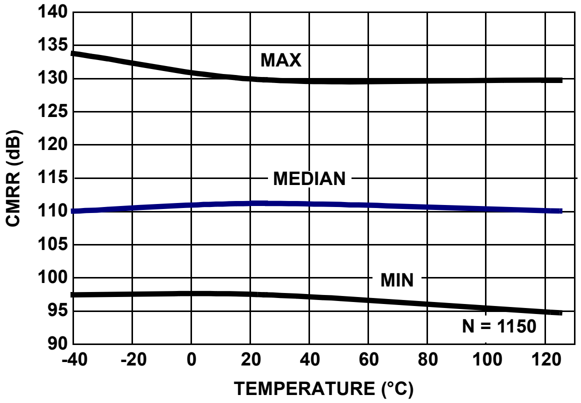


FIGURE 32. CMRR vs TEMPERATURE, $V_{CM} = -2.5V$ TO $+2.5V$, $V_+, V_- = \pm2.5V$

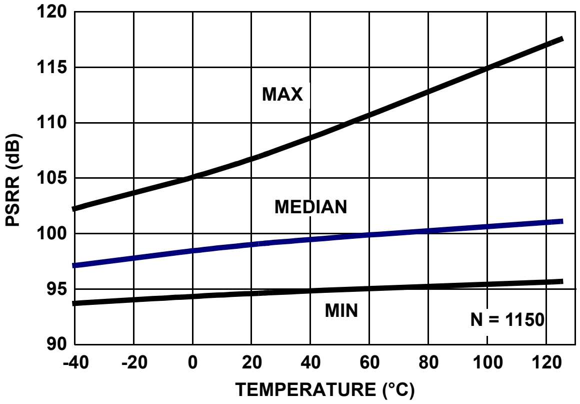


FIGURE 33. PSRR vs TEMPERATURE, $V_+, V_- = \pm1.2V$ TO $\pm2.75V$

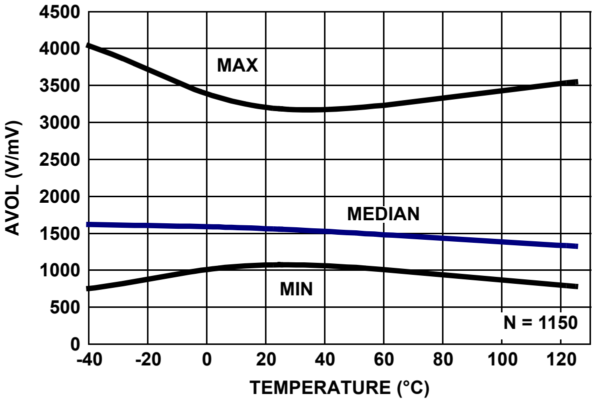


FIGURE 34. AVOL vs TEMPERATURE, $V_+, V_- = \pm2.5V$, $V_O = -2V$ TO $+2V$, $R_L = 100k$

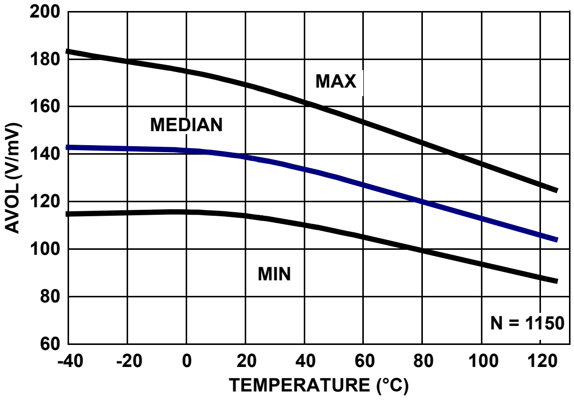


FIGURE 35. AVOL vs TEMPERATURE, $V_+, V_- = \pm2.5V$, $V_O = -2V$ TO $+2V$, $R_L = 1k$

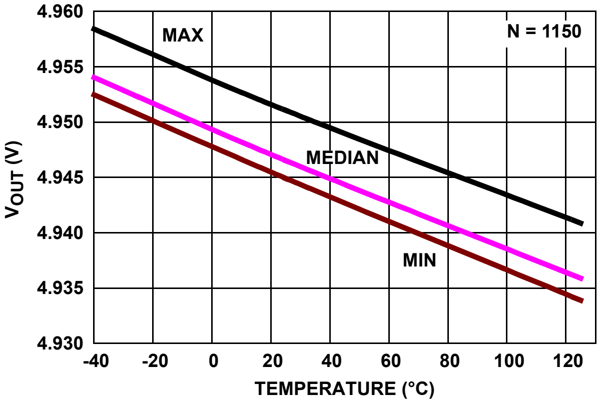


FIGURE 36. V_{OUT} HIGH vs TEMPERATURE, $V_+, V_- = \pm2.5V$, $R_L = 1k$

Typical Performance Curves $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, R_L = Open **(Continued)**

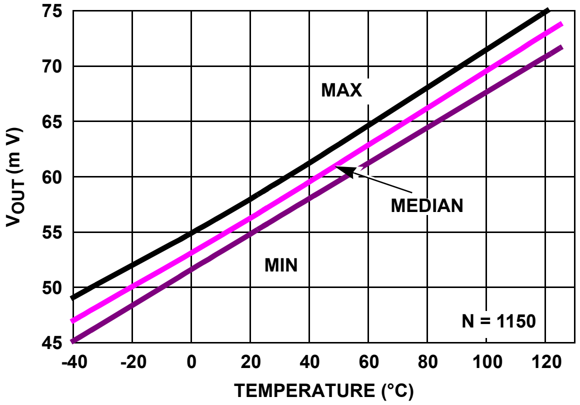
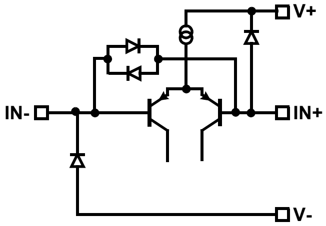
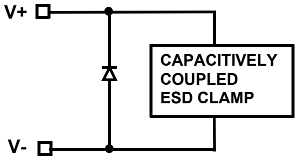
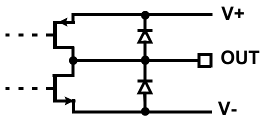
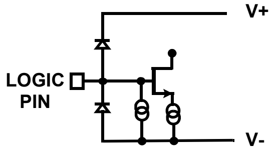


FIGURE 37. V_{OUT} LOW vs TEMPERATURE, V_+, V_- = ±2.5V, R_L = 1k

Pin Descriptions

ISL28136 (6 Ld SOT-23)	ISL28136 (8 Ld SOIC)	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT
	1, 5	NC	Not connected	
4	2	IN-	inverting input	 **Circuit 1**
3	3	IN+	Non-inverting input	**See Circuit 1**
2	4	V-	Negative supply	 **Circuit 2**
1	6	OUT	Output	 **Circuit 3**
6	7	V+	Positive supply	**See Circuit 2**
5	8	$\overline{EN}$	Chip enable	 **Circuit 3**

Applications Information

Introduction

The ISL28136 is a single channel Bi-CMOS rail-to-rail input, output (RRIO) micropower precision operational amplifier. The part is designed to operate from a single supply 2.4V to 5.5V. The part has an input common mode range that extends 0.25V above the positive rail and down to the negative supply rail. The output operation can swing within about 3mV of the supply rails with a 100kΩ load.

Rail-to-Rail Input

Many rail-to-rail input stages use two differential input pairs; a long-tail PNP (or PFET) and an NPN (or NFET). Severe penalties have to be paid for this circuit topology. As the input signal moves from one supply rail to another, the operational amplifier switches from one input pair to the other causing drastic changes in input offset voltage and an undesired change in magnitude and polarity of input offset current.

The ISL28136 achieves input rail-to-rail operation without sacrificing important precision specifications and degrading distortion performance. The device's input offset voltage exhibits a smooth behavior throughout the entire common-mode input range. The input bias current versus the common-mode voltage range gives an undistorted behavior from typically down to the negative rail to 0.25V higher than the positive rail.

Rail-to-Rail Output

The output stage uses drain-connected N and P-channel MOSFETs to achieve rail-to-rail output swing. The P-channel device sources current to swing the output in the positive direction and the N-channel sinks current to swing the output in the negative direction. The ISL28136 with a 100kΩ load will swing to within 3mV of the positive supply rail and within 3mV of the negative supply rail.

Results of Over-Driving the Output

Caution should be used when over-driving the output for long periods of time. Over-driving the output can occur in two ways. 1) The input voltage times the gain of the amplifier exceeds the supply voltage by a large value or, 2) the output current required is higher than the output stage can deliver. These conditions can result in a shift in the Input Offset Voltage (V_{OS}) as much as 1µV/hr. of exposure under these conditions.

IN+ and IN- Input Protection

All input terminals have internal ESD protection diodes to both positive and negative supply rails, limiting the input voltage to within one diode beyond the supply rails. They also contain back-to-back diodes across the input terminals (see "Pin Descriptions" on page 10 - Circuit 1). For applications where the input differential voltage is expected to exceed 0.5V, an external series resistor must be used to ensure the input currents never exceed 5mA (Figure 38).

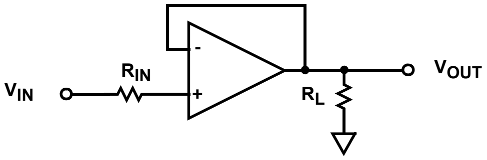


FIGURE 38. INPUT CURRENT LIMITING

Enable/Disable Feature

The ISL28136 offers an $\overline{EN}$ pin that disables the device when pulled up to at least 2.0V. In the disabled state (output in a high impedance state), the part consumes typically 10µA at room temperature. By disabling the part, multiple ISL28136 parts can be connected together as a MUX. In this configuration, the outputs are tied together in parallel and a channel can be selected by the $\overline{EN}$ pin. The loading effects of the feedback resistors of the disabled amplifier must be considered when multiple amplifier outputs are connected together. Note that feed through from the IN+ to IN- pins occurs on any Mux Amp disabled channel where the input differential voltage exceeds 0.5V (e.g., active channel V_{OUT} = 1V, while disabled channel V_{IN} = GND), so the mux implementation is best suited for small signal applications. If large signals are required, use series IN+ resistors, or a large value R_F, to keep the feed through current low enough to minimize the impact on the active channel. See"Limitations of the Differential Input Protection" on page 11 for more details.

To disable the part, the user needs to supply the 1.5µA required to pull the $\overline{EN}$ pin to the V_+ rail. If left open, the $\overline{EN}$ pin will pull to the negative rail and the device will be enabled by default. If the $\overline{EN}$ function is not required (no need to turn the part off), as a precaution, it is recommended that the user tie the $\overline{EN}$ pin to the V_- pin.

Limitations of the Differential Input Protection

If the input differential voltage is expected to exceed 0.5V, an external current limiting resistor must be used to ensure the input current never exceeds 5mA. For non-inverting unity gain applications, the current limiting can be via a series IN+ resistor, or via a feedback resistor of appropriate value. For other gain configurations, the series IN+ resistor is the best choice, unless the feedback (R_F) and gain setting (R_G) resistors are both sufficiently large to limit the input current to 5mA.

Large differential input voltages can arise from several sources:

1. During open loop (comparator) operation. Used this way, the IN+ and IN- voltages don't track, so differentials arise.
2. When the amplifier is disabled but an input signal is still present. An R_L or R_G to GND keeps the IN- at GND, while the varying IN+ signal creates a differential voltage. Mux Amp applications are similar, except that the active channel V_{OUT} determines the voltage on the IN- terminal.

3. When the slew rate of the input pulse is considerably faster than the op amp's slew rate. If the V_{OUT} can't keep up with the IN+ signal, a differential voltage results, and visible distortion occurs on the input and output signals. To avoid this issue, keep the input slew rate below 1.9V/µs, or use appropriate current limiting resistors.

Large (>2V) differential input voltages can also cause an increase in disabled I_{CC}.

Current Limiting

These devices have no internal current-limiting circuitry. If the output is shorted, it is possible to exceed the Absolute Maximum Rating for output current or power dissipation, potentially resulting in the destruction of the device.

Power Dissipation

It is possible to exceed the +125°C maximum junction temperatures under certain load and power-supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related in Equation 1:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} x PD_{MAXTOTAL}) \qquad \text{(EQ. 1)}$$

where:

- $P_{DMAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})
- PD_{MAX} for each amplifier can be calculated using Equation 2:

$$PD_{MAX} = 2{*}V_S \times I_{SMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \qquad \text{(EQ. 2)}$$

where:

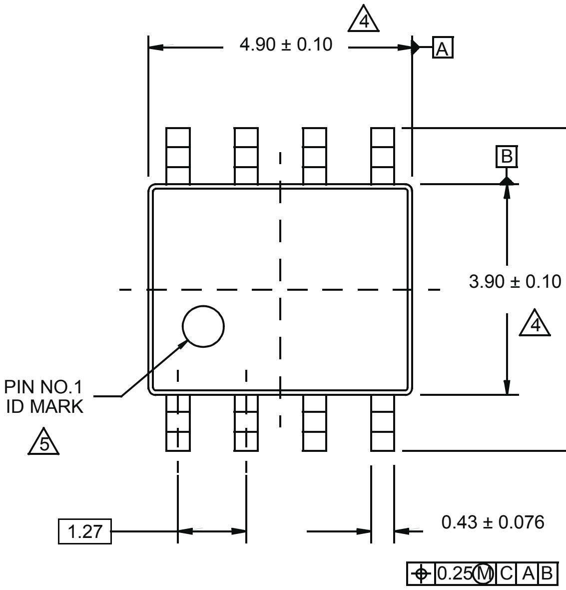
- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of 1 amplifier
- V_S = Supply voltage (Magnitude of V_+ and V_-)
- I_{MAX} = Maximum supply current of 1 amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application
- R_L = Load resistance

Package Outline Drawing

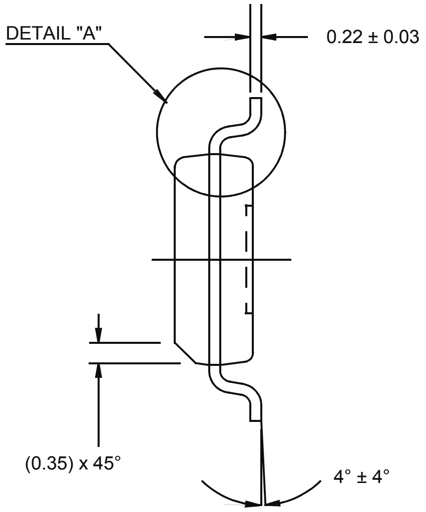
M8.15E

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

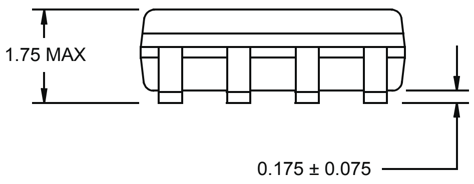
Rev 0, 08/09



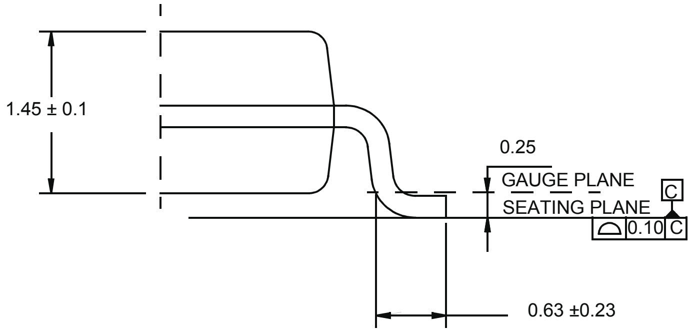
TOP VIEW



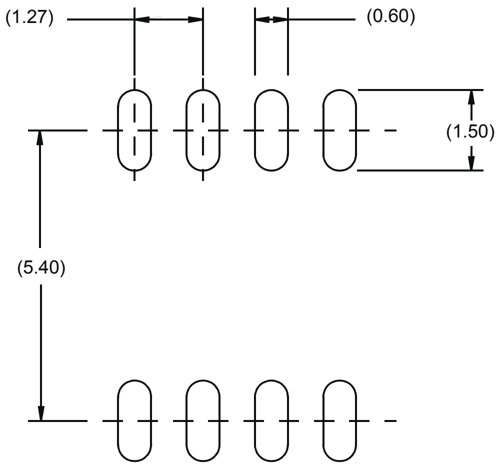
SIDE VIEW “B”



SIDE VIEW “A



DETAIL "A"



TYPICAL RECOMMENDED LAND PATTERN

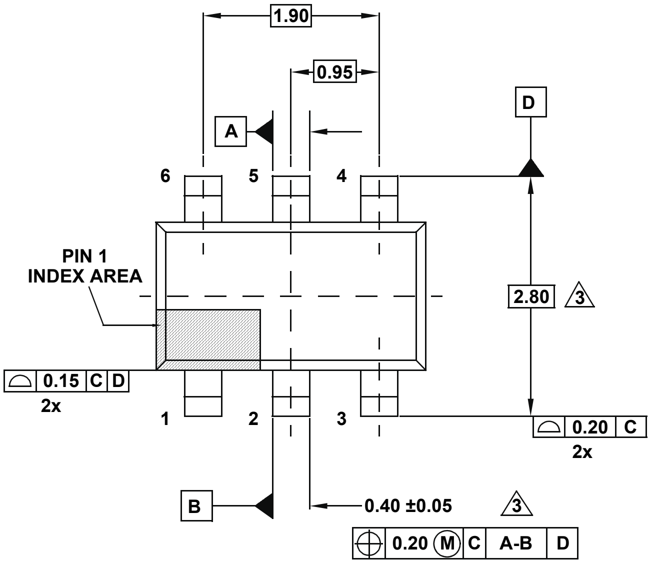
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.

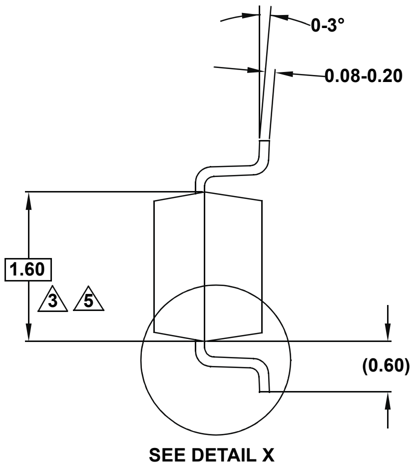
Package Outline Drawing

P6.064A

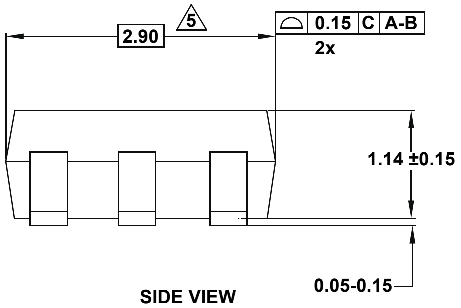
6 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE
Rev 0, 2/10



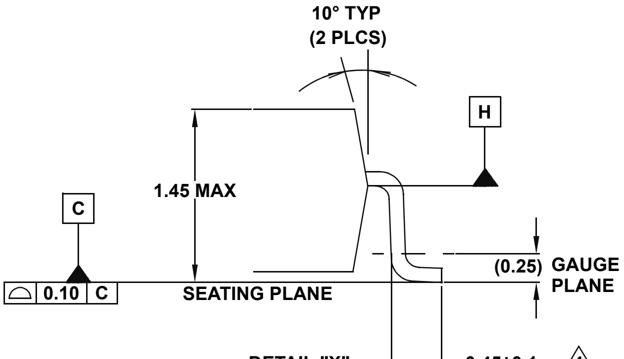
TOP VIEW



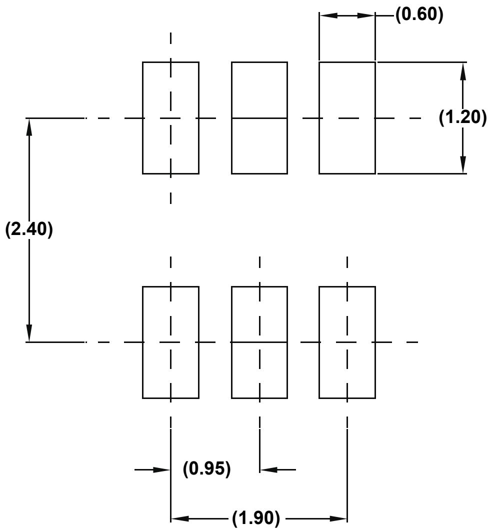
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. Dimension is exclusive of mold flash, protrusions or gate burrs.
4. Foot length is measured at reference to guage plane.
5. This dimension is measured at Datum “H”.
6. Package conforms to JEDEC MO-178AA.