

# **WAS3157D**

**5.5Ω, 400MHz Bandwidth, SPDT Analog Switch**

<https://www.ovt.com>

## **Descriptions**

The WAS3157D is a high performance, single pole double throw (SPDT) CMOS analog switch for bus switching or audio switching applications. It features high bandwidth up to 400MHz at -3dB and low on-resistance (5.5Ω Typ.).

The SEL pin has overvoltage protection that allows voltages above VCC, up to 7.0V to be present on the pin without damage or disruption of operation of the part, regardless of the operating voltage. The WAS3157D is also featured with smart circuitry to minimize VCC leakage current even when SEL control voltage is lower than VCC supply voltage. In other word, there is no need of additional device to shift SEL level to be the same as that of VCC in real application.

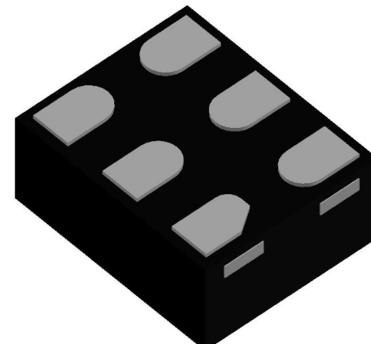
The WAS3157D is available in standard DFN1109-6L package. Standard product is Pb-Free and halogen-Free.

## **Features**

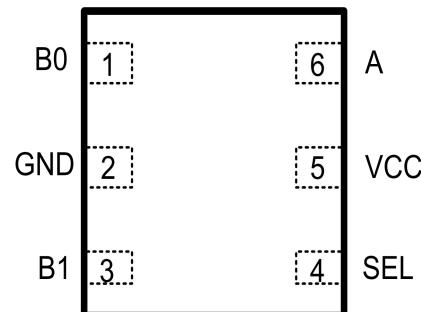
- Supply voltage : 1.5 ~ 5.5V
- On-Resistance : 5.5Ω @ VCC=4.5V
- -3dB Bandwidth : 400MHz @ CL=5pF
- Off isolation : -69dB @ 10MHz
- Low quiescent current : <1uA
- Break-before-make function
- ESD protection
  - HBM : ±8000V
  - MM : ±600V

## **Applications**

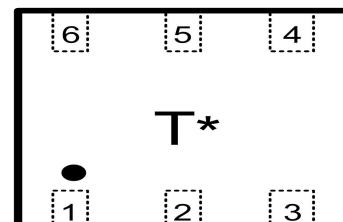
- Cell phones
- MID
- Other portable equipments



**DFN1109-6L (Bottom View)**



**Pin configuration (Top view)**



**Marking**

**T = Device code**

**\* = Month code**

## **Order information**

<b>Device</b>	<b>Package</b>	<b>Shipping</b>
WAS3157D-6/TR	DFN1109-6L	3000/Reel&Tape

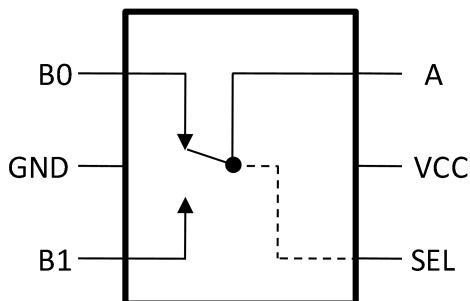
### Pin descriptions

Pin Number	Symbol	Descriptions
1	B0	Data 0 terminal, Normally closed
2	GND	Ground
3	B1	Data 1 terminal, Normally open
4	SEL	Switch select pin, Digit logic low or high
5	VCC	Power supply
6	A	Common Data terminal, Connect to B0 or B1 according to SEL logic

### Function descriptions

Logic Level (SEL pin, Pin 4)	Function
L	B0 connected to A
H	B1 connected to A

### Function Block



### Absolute maximum ratings

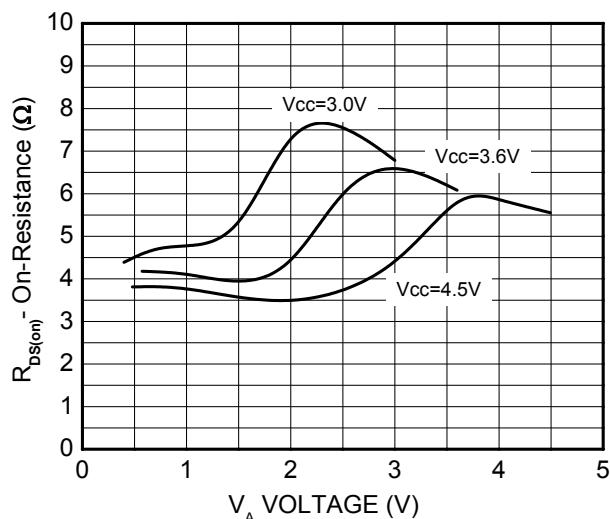
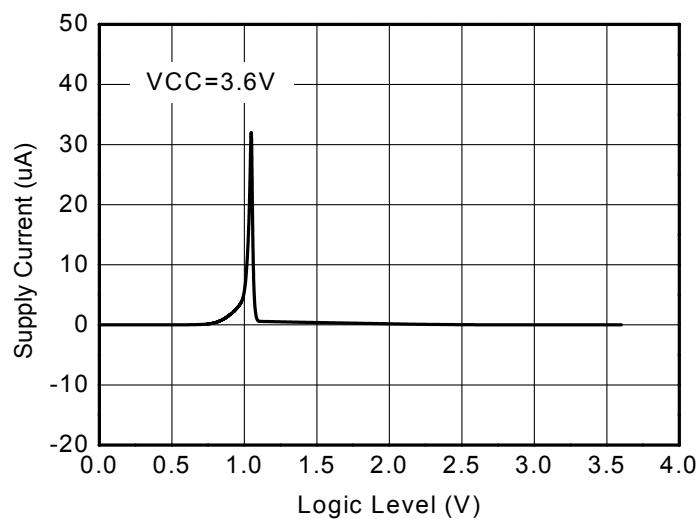
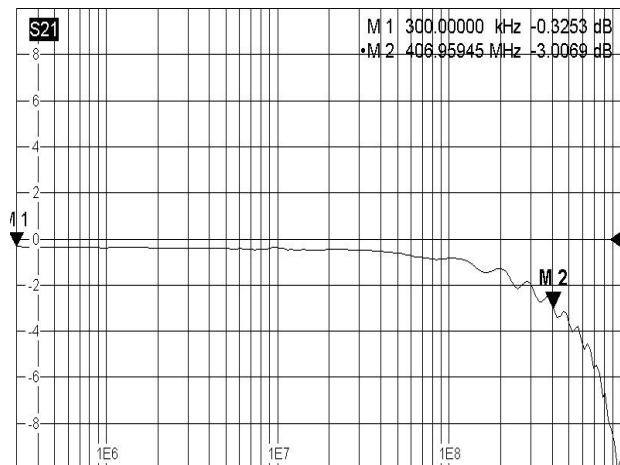
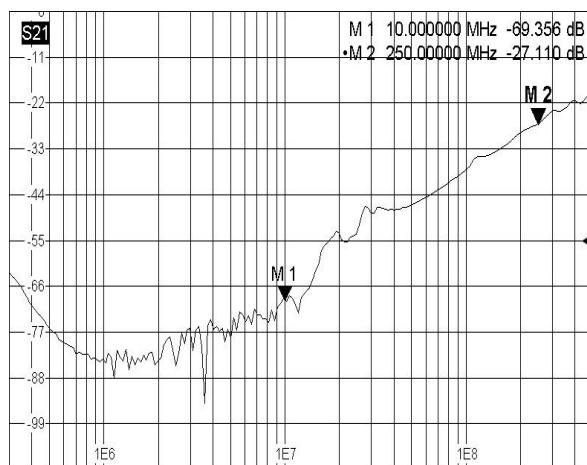
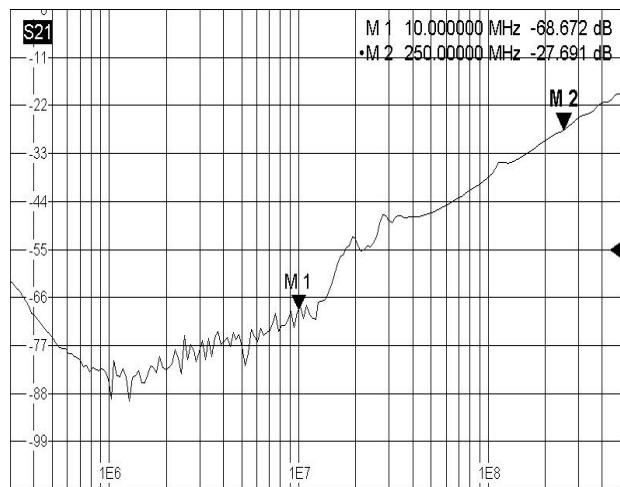
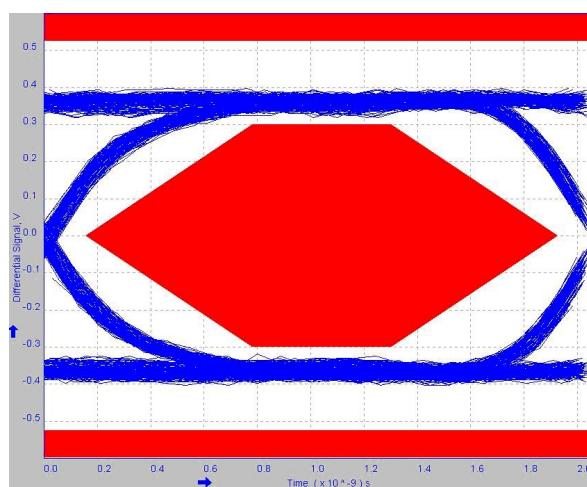
Parameter	Symbol	Value	Unit
Supply voltage range	VCC	-0.5 ~ 6.5	V
Data input/output voltage range	$V_{B0}, V_{B1}, V_A$	-0.5 ~ 6.5	V
Select input voltage range	$V_{SEL}$	-0.5 ~ 6.5	V
Continues current	$I_{B0}, I_{B1}, I_A$	$\pm 50$	mA
Junction temperature range	$T_J$	150	°C
Lead temperature range	$T_L$	260	°C
Storage temperature range	$T_{STG}$	-65 ~ 150	°C
Thermal resistance	$R_{\theta JA}$	350	°C/W

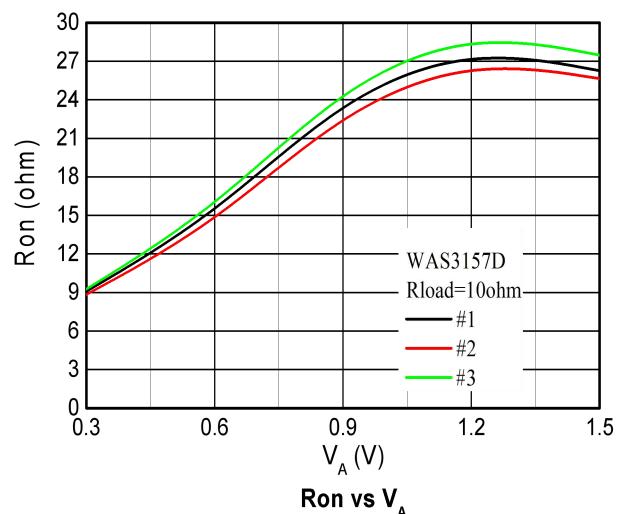
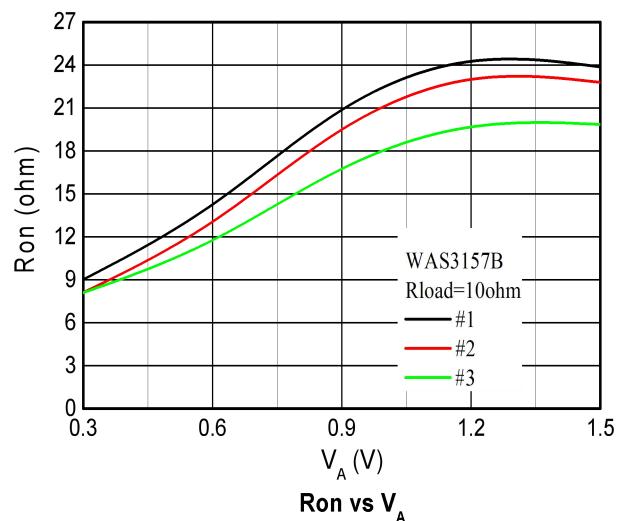
### Recommend operating ratings

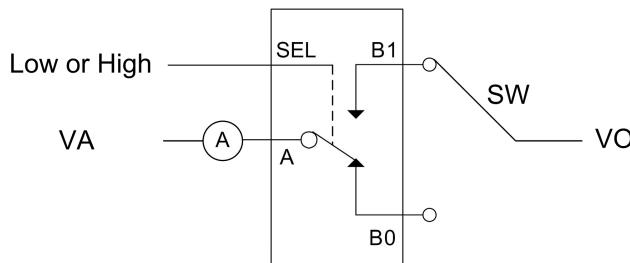
Parameter	Symbol	Value	Unit
Supply voltage range	VCC	1.5 ~ 5.5	V
Data input/output voltage range	$V_{B0}, V_{B1}, V_A$	0.0 ~ VCC	V
Select input voltage range	$V_I$	0.0 ~ VCC	V
Operating temperature range	$T_A$	-40 ~ 85	°C

**Electronics Characteristics (Ta=25°C, VCC=4.5V, unless otherwise noted)**

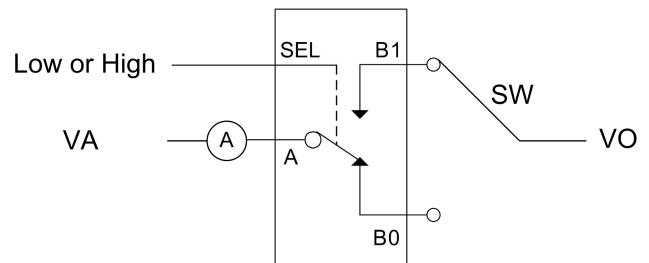
<b>Parameter</b>	<b>Symbol</b>	<b>Conditions</b>	<b>Min.</b>	<b>Typ.</b>	<b>Max.</b>	<b>Unit</b>
Select logic high level	$V_{IH}$	VCC=3.6~4.5V	1.5			V
		VCC=2.3~3.6V	1.3			V
Select logic low level	$V_{IL}$	VCC=3.6~4.5V			0.6	V
		VCC=2.3~3.6V			0.4	V
Quiescent current	$I_{CC}$	$I_{OUT}=0$			1.0	uA
Select input leakage current	$I_{SEL}$	$V_{SEL}=0 \sim VCC$			$\pm 0.1$	uA
Off state switch leakage current	$I_{OFF}$	See figure 1			$\pm 0.1$	uA
On state switch leakage current	$I_{ON}$	See figure 2			$\pm 0.1$	uA
On-Resistance (Channel B0 and Channel B1)	$R_{ON}$	VCC=4.5V, $V_A=4.5V$ , $I_{OUT}=30mA$ , See figure 3		5.5	12	$\Omega$
On-Resistance (Channel B0 or Channel B1)	$R_{ON}$	VCC=4.5V, $V_A=0V$ , $I_{OUT}=30mA$ , See figure 3		3.8	7.0	$\Omega$
On-Resistance (Channel B0 or Channel B1)	$R_{ON}$	VCC=3.6V, $V_A=3.6V$ , $I_{OUT}=30mA$ , See figure 3		6.5	13	$\Omega$
On-Resistance (Channel B0 or Channel B1)	$R_{ON}$	VCC=3.6V, $V_A=0V$ , $I_{OUT}=30mA$ , See figure 3		4.5	9.0	$\Omega$
Propagation delay time (A to Bn or Bn to A)	$T_{PLH} / T_{PHL}$	$C_L=50pF$ See figure 4, 5		0.3	1.2	ns
Select input to switch on time (A to Bn or Bn to A)	$T_{ON}$	$C_L=50pF$ See figure 5		80	120	ns
Select input to switch off time (A to Bn or Bn to A)	$T_{OFF}$	$C_L=50pF$ See figure 5		50	80	ns
Break-Before-Make time	$T_{BBM}$	Generated by design	0.5			ns
-3dB Bandwidth	BW	$R_L=50\Omega$ , $C_L=5pF$		400		MHz
Charge injection	$Q_g$	$C_L=0.1nF$ , $VCC=5V$		10		pC
Off isolation	OIRR	$R_L=50\Omega$ , $F=10MHz$		-69		dB
Crosstalk	Xtalk	$R_L=50\Omega$ , $F=10MHz$		-68		dB
Total harmonic distortion	THD	$R_L=600\Omega$ , $F=1KHz$ $V_A=0.5Vp-p$		0.03		%
Select pin input capacitance	$C_{IN}$	$VCC=0V$		5.5		pF
B port off capacitance	$C_{OFF}$			7.5		pF
A port on capacitance	$C_{ON}$			18.5		pF

**Typical Characteristics (Ta=25°C, VCC=4.5V, unless otherwise noted)**

**On-Resistance vs. VCC, VA voltage**

**Supply current vs. Select logic level**

**Bandwidth**

**Off isolation**

**Crosstalk**

**Eye Diagram (480Mbps)**

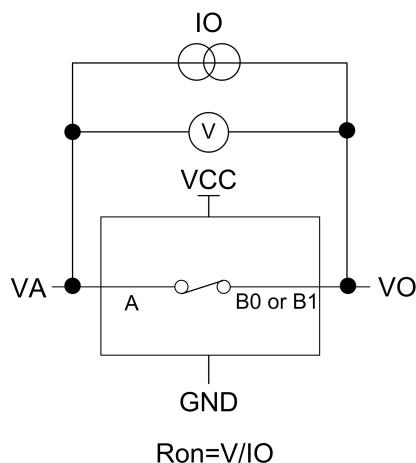
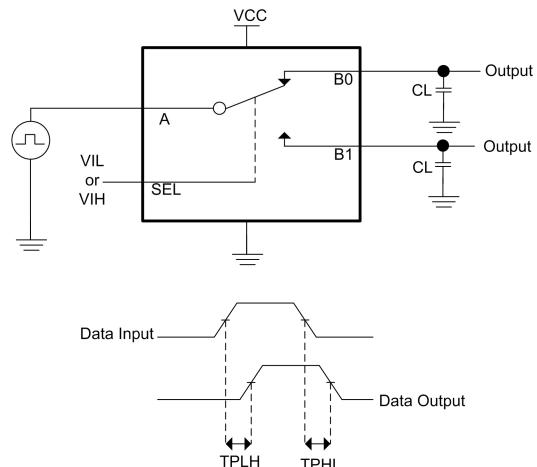
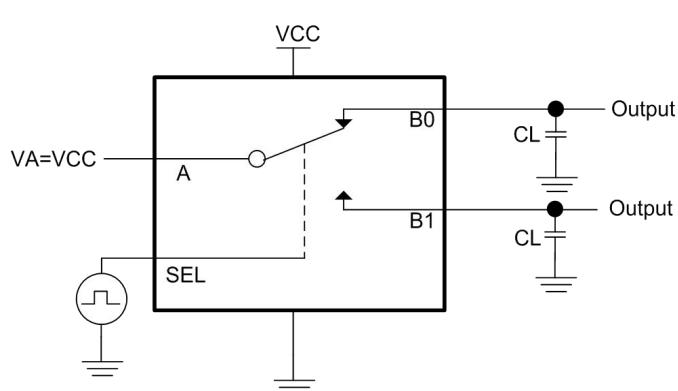


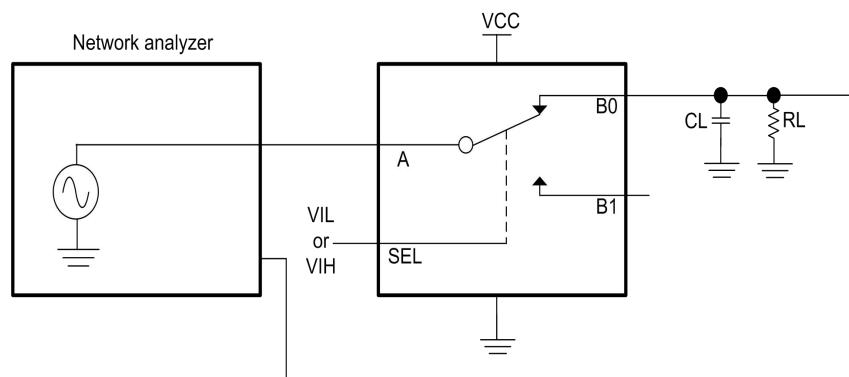
**Test Circuit**

**Conditions:**

- 1: SEL=Low, SW=B1, VA=5.5V, VO=GND
- 3: SEL=High, SW=B0, VA=5.5V, VO=GND

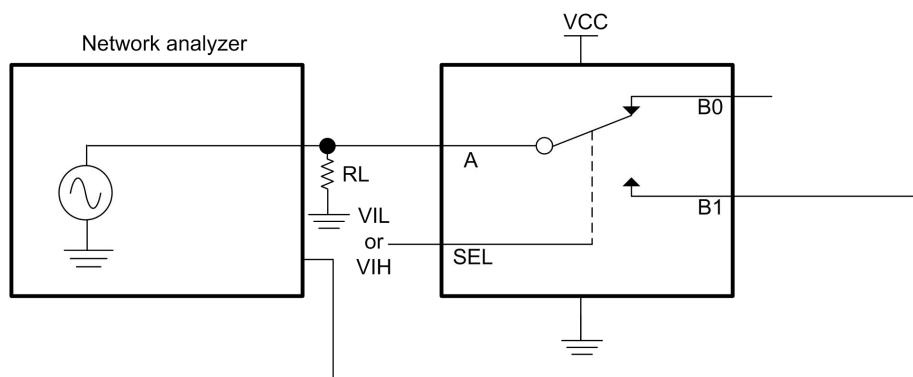

**Conditions:**

- 1: SEL=Low, SW=B0, VA=5.5V, VO=Open
- 3: SEL=High, SW=B1, VA=5.5V, VO=Open

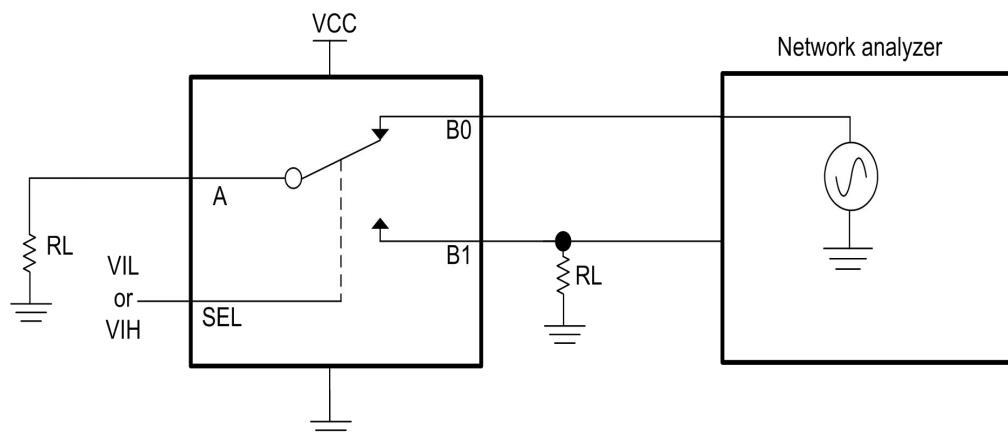
**Figure 1: Off state switch leakage current**
**Figure 2: On state switch leakage current**

**Figure 3: On-Resistance**

**Figure 4: Propagation delay time**

**Figure 5: Select input to switch on/off time**



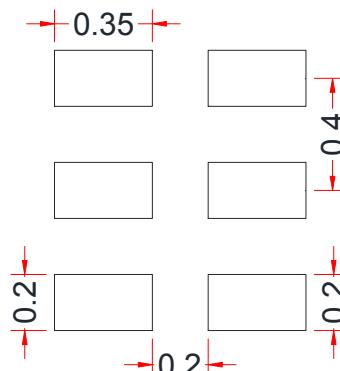
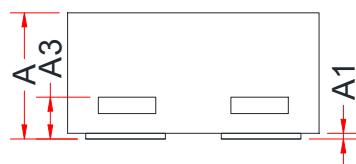
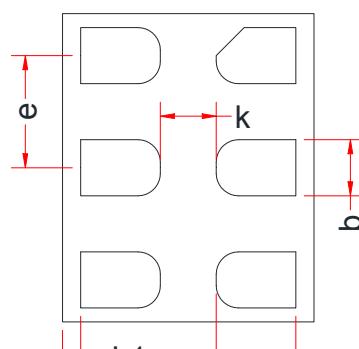
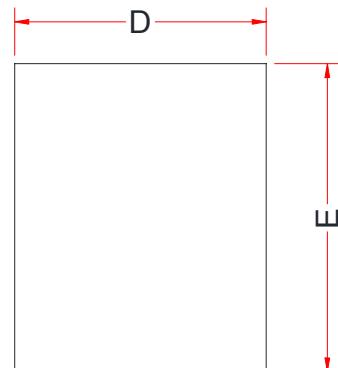
### Bandwidth (BW)



### Off isolation (OIRR)

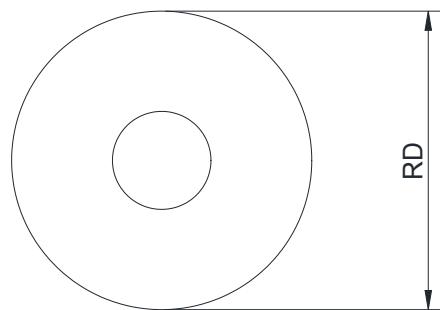
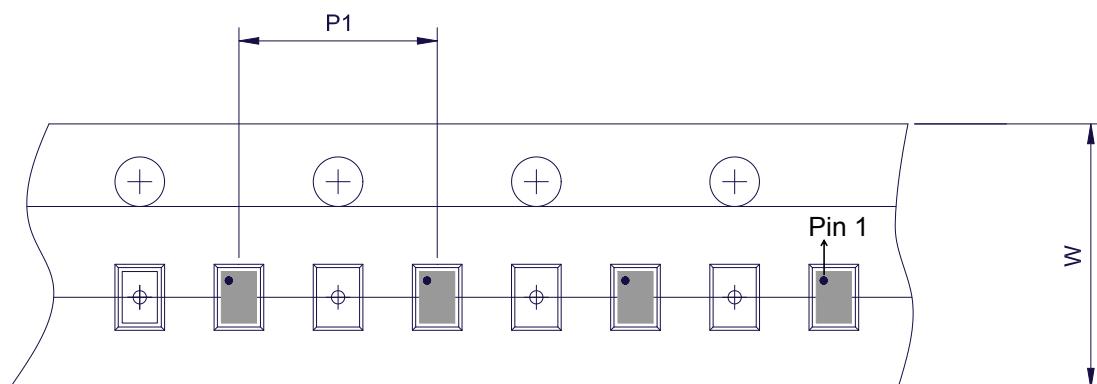
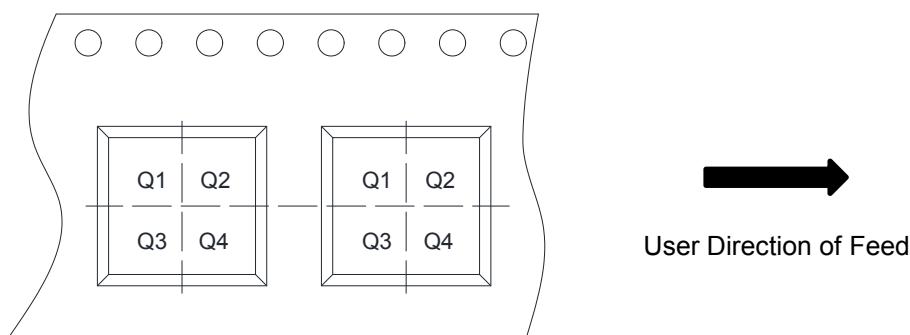


### Crosstalk (Xtalk)

**PACKAGE OUTLINE DIMENSIONS**
**DFN1109-6L**


RECOMMENDED LAND PATTERN (Unit:mm)

Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.40	0.45	0.50
A1	0.00	0.02	0.05
A3	0.15 Ref.		
b	0.15	0.20	0.25
D	0.80	0.90	1.00
E	1.00	1.10	1.20
e	0.40 BSC		
L	0.22	-	0.35
L1	0.05 Ref.		
k	0.20 Ref.		

**TAPE AND REEL INFORMATION**
**Reel Dimensions**

**Tape Dimensions**

**Quadrant Assignments For PIN1 Orientation In Tape**


RD	Reel Dimension	<input checked="" type="checkbox"/> 7inch <input type="checkbox"/> 13inch
W	Overall width of the carrier tape	<input checked="" type="checkbox"/> 8mm <input type="checkbox"/> 12mm <input type="checkbox"/> 16mm
P1	Pitch between successive cavity centers	<input type="checkbox"/> 2mm <input checked="" type="checkbox"/> 4mm <input type="checkbox"/> 8mm
Pin1	Pin1 Quadrant	<input checked="" type="checkbox"/> Q1 <input type="checkbox"/> Q2 <input type="checkbox"/> Q3 <input type="checkbox"/> Q4