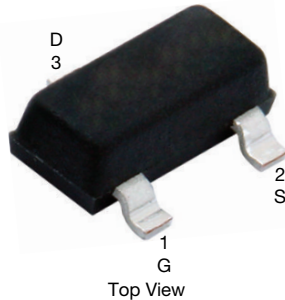


N-Channel 100 V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω) MAX.	I _D (A) ^a	Q _g (TYP.)
100	0.126 at V _{GS} = 10 V	3.1	2.9 nC
	0.144 at V _{GS} = 6 V	2.9	
	0.189 at V _{GS} = 4.5 V	2.6	

SOT-23 (TO-236)


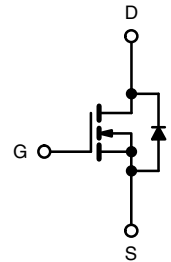
FEATURES

- TrenchFET® power MOSFET
- 100 % R_g and UIS tested
- Material categorization:
For definitions of compliance please see www.vishay.com/doc?99912


RoHS
 COMPLIANT
 HALOGEN
FREE

APPLICATIONS

- DC/DC converters / boost converters
- Load switch
- LED backlighting in LCD TVs
- Power management for mobile computing



N-Channel MOSFET

Marking Code: G2

Ordering Information:

Si2392ADS-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	V _{DS}	100	V	
Gate-Source Voltage	V _{GS}	± 20		
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	3.1	A
		T _C = 70 °C	2.5	
		T _A = 25 °C	2.2 ^{b, c}	
		T _A = 70 °C	1.8 ^{b, c}	
Pulsed Drain Current (t = 300 μs)	I _{DM}	8		
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	2.1	
		T _A = 25 °C	1 ^{b, c}	
Single Pulse Avalanche Current	I _{AS}	3		
Single Pulse Avalanche Energy	E _{AS}	0.45	mJ	
Maximum Power Dissipation	P _D	T _C = 25 °C	2.5	W
		T _C = 70 °C	1.6	
		T _A = 25 °C	1.25 ^{b, c}	
		T _A = 70 °C	0.8 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150	°C	

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT	
Maximum Junction-to-Ambient ^{b, d}	R _{thJA}	75	100	°C/W	
Maximum Junction-to-Foot (Drain)	R _{thJF}	40	50		

Notes

- Based on T_C = 25 °C.
- Surface mounted on 1" x 1" FR4 board.
- t = 5 s.
- Maximum under steady state conditions is 166 °C/W.



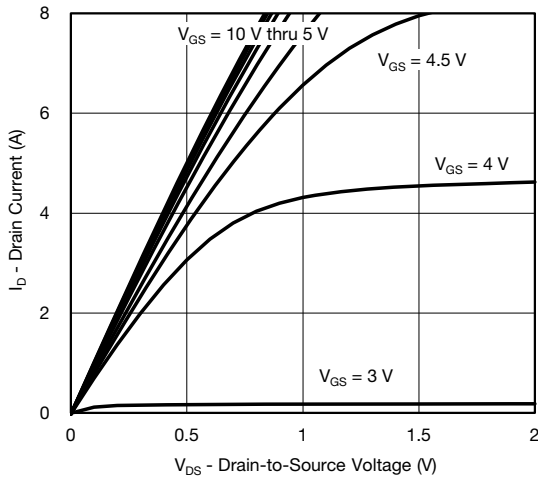
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	100	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA	-	59	-	mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J		-	-4.8	-	
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.2	-	3	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 100 V, V _{GS} = 0 V, T _J = 55 °C	-	-	10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	5	-	-	A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 2 A	-	0.102	0.126	Ω
		V _{GS} = 6 V, I _D = 1 A	-	0.120	0.144	
		V _{GS} = 4.5 V, I _D = 1 A	-	0.135	0.189	
Forward Transconductance ^a	g _{fs}	V _{DS} = 20 V, I _D = 2 A	-	5	-	S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = 50 V, V _{GS} = 0 V, f = 1 MHz	-	196	-	pF
Output Capacitance	C _{oss}		-	67	-	
Reverse Transfer Capacitance	C _{rss}		-	14	-	
Total Gate Charge	Q _g	V _{DS} = 50 V, V _{GS} = 10 V, I _D = 2.2 A	-	5.2	10.4	nC
Gate-Source Charge	Q _{gs}	V _{DS} = 50 V, V _{GS} = 4.5 V, I _D = 2.2 A	-	2.9	5.8	
Gate-Drain Charge	Q _{gd}		-	1	-	
Gate Resistance	R _g	f = 1 MHz	0.9	4.3	8.6	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 50 V, R _L = 27.7 Ω I _D = 1.8 A, V _{GEN} = 4.5 V, R _g = 1 Ω	-	40	60	ns
Rise Time	t _r		-	68	102	
Turn-Off Delay Time	t _{d(off)}		-	14	21	
Fall Time	t _f		-	20	30	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 50 V, R _L = 27.7 Ω I _D = 1.8 A, V _{GEN} = 10 V, R _g = 1 Ω	-	8	16	
Rise Time	t _r		-	10	20	
Turn-Off Delay Time	t _{d(off)}		-	10	20	
Fall Time	t _f		-	7	14	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	-	-	2.1	A
Pulse Diode Forward Current ^a	I _{SM}		-	-	8	
Body Diode Voltage	V _{SD}	I _S = 1.8 A	-	0.8	1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 1.8 A, dI/dt = 100 A/μs, T _J = 25 °C	-	23	35	ns
Body Diode Reverse Recovery Charge	Q _{rr}		-	21	32	nC
Reverse Recovery Fall Time	t _a		-	17	-	ns
Reverse Recovery Rise Time	t _b		-	6	-	

Notes

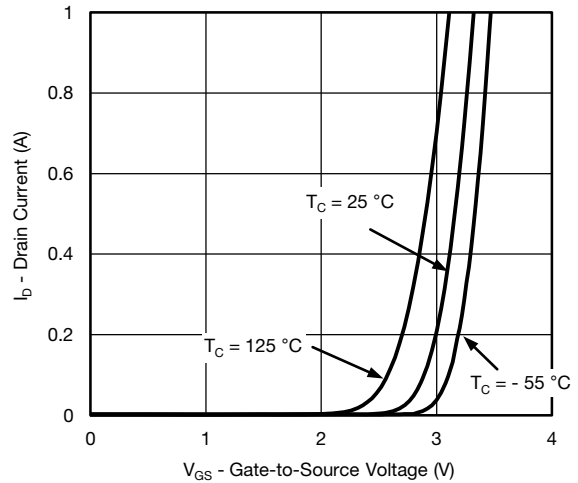
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

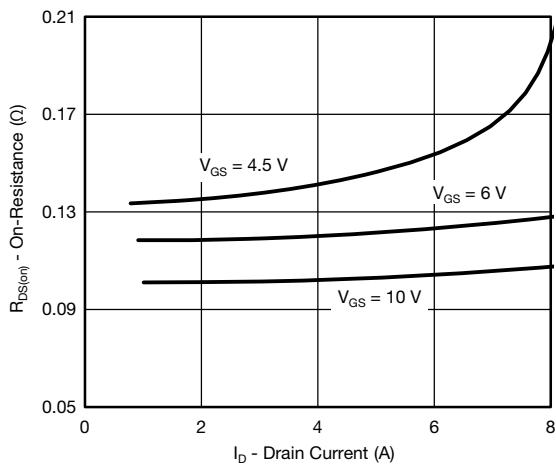
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



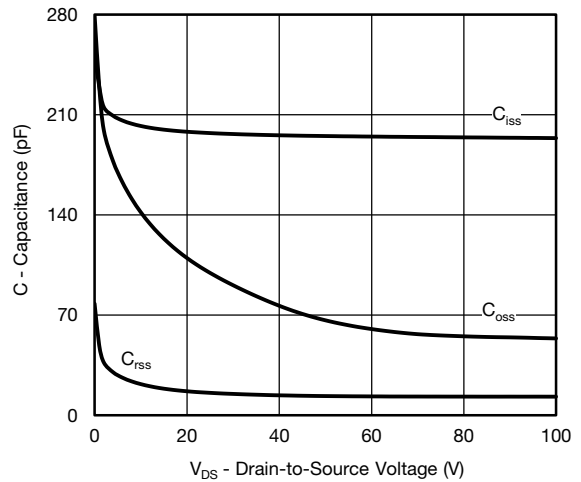
Output Characteristics



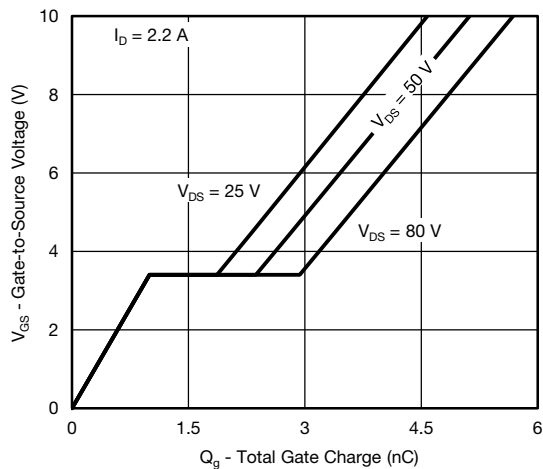
Transfer Characteristics



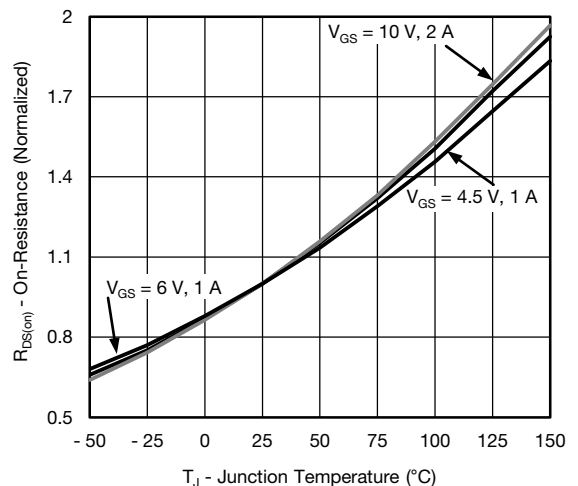
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



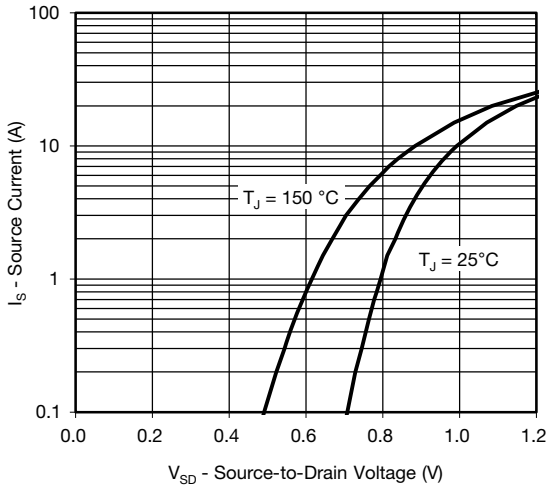
Gate Charge



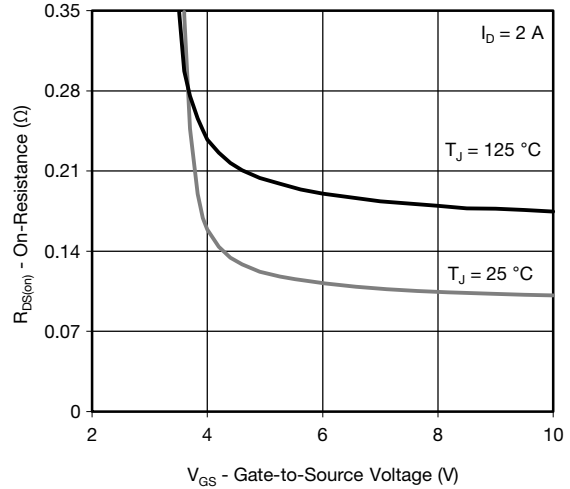
On-Resistance vs. Junction Temperature



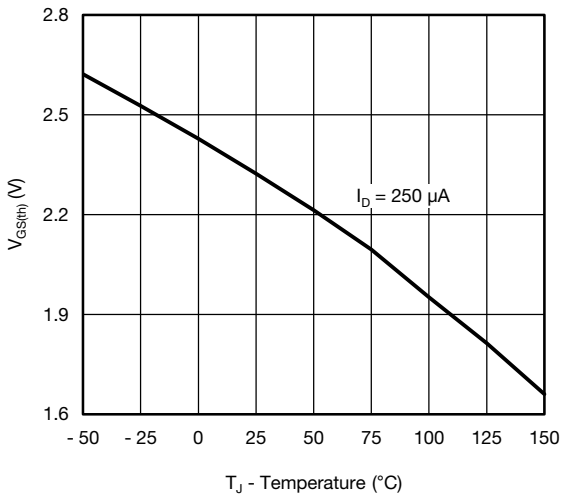
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



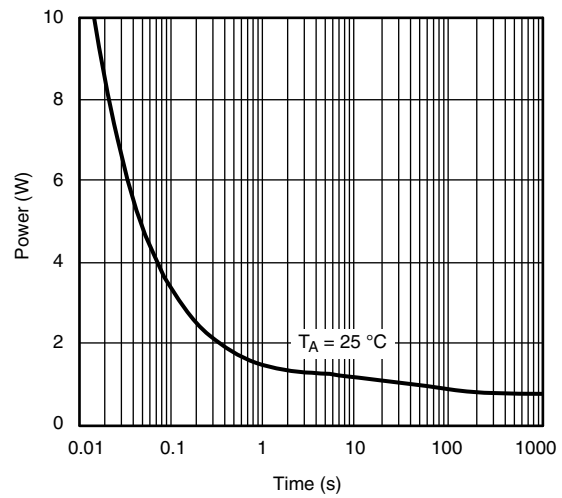
Source-Drain Diode Forward Voltage



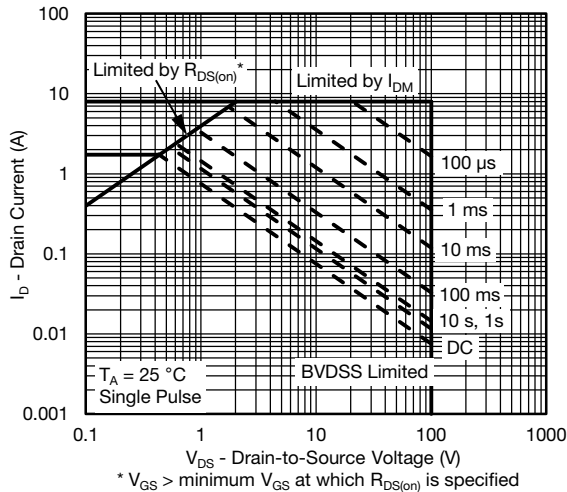
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



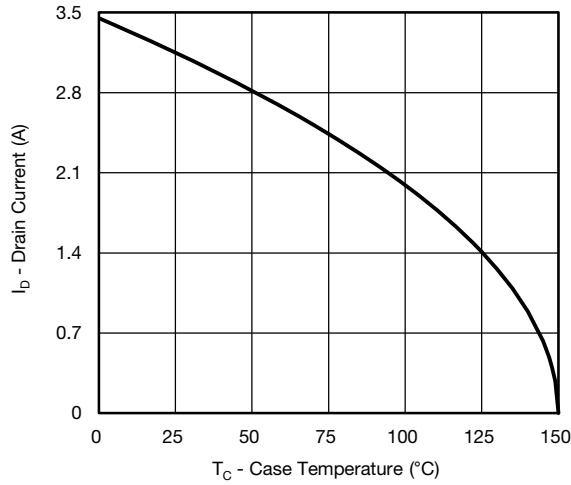
Single Pulse Power



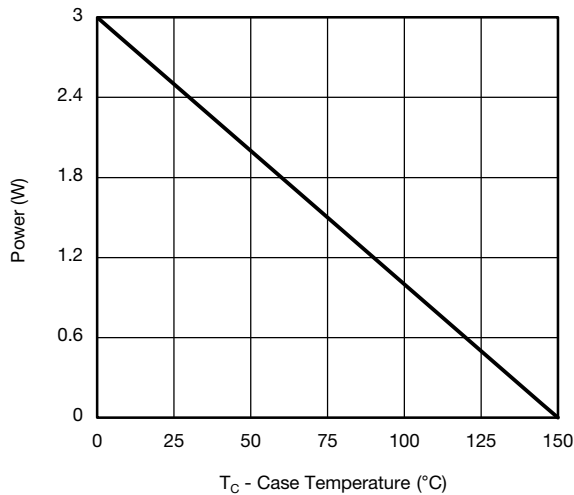
Safe Operating Area



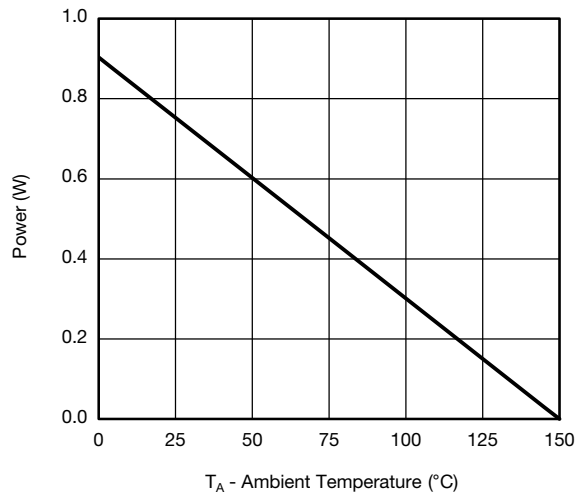
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*



Power, Junction-to-Foot

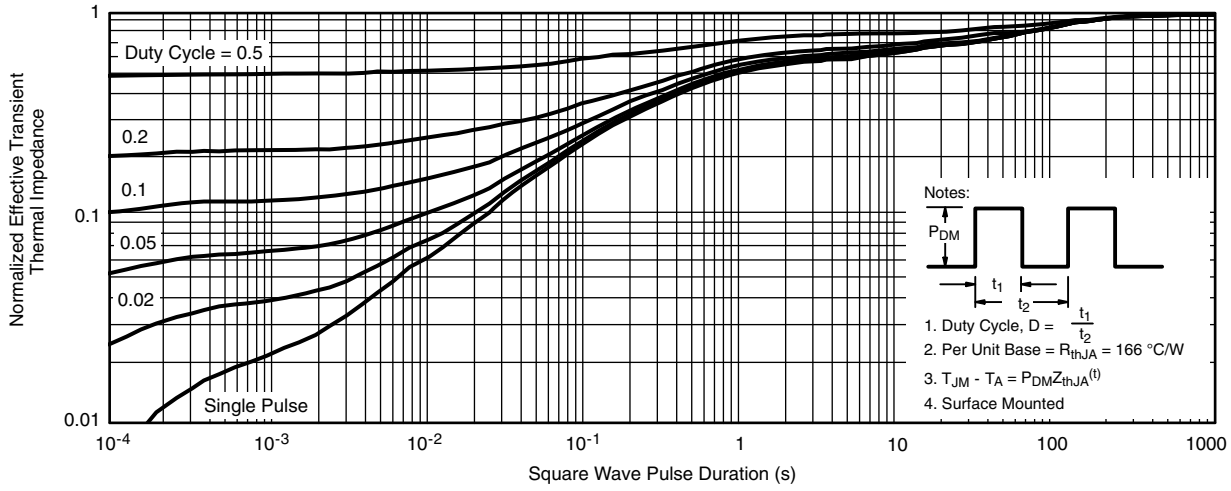


Power, Junction-to-Ambient

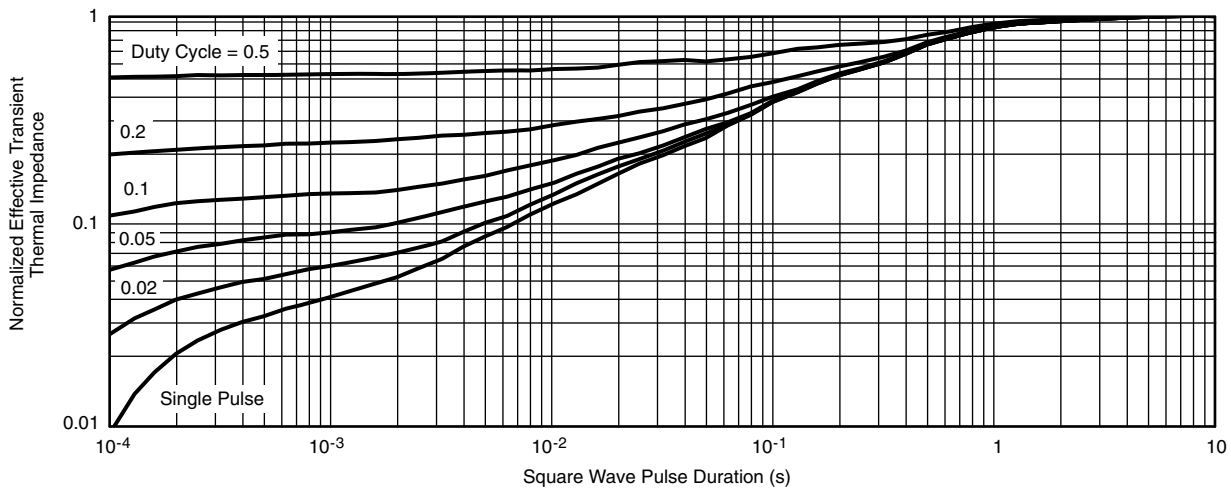
* The power dissipation P_D is based on T_{J(max)} = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62960.

SOT-23 (TO-236): 3-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	0.89	1.12	0.035	0.044
A ₁	0.01	0.10	0.0004	0.004
A ₂	0.88	1.02	0.0346	0.040
b	0.35	0.50	0.014	0.020
c	0.085	0.18	0.003	0.007
D	2.80	3.04	0.110	0.120
E	2.10	2.64	0.083	0.104
E ₁	1.20	1.40	0.047	0.055
e	0.95 BSC		0.0374 Ref	
e ₁	1.90 BSC		0.0748 Ref	
L	0.40	0.60	0.016	0.024
L ₁	0.64 Ref		0.025 Ref	
S	0.50 Ref		0.020 Ref	
q	3°	8°	3°	8°

ECN: S-03946-Rev. K, 09-Jul-01
 DWG: 5479

Mounting LITTLE FOOT[®] SOT-23 Power MOSFETs

Wharton McDaniel

Surface-mounted LITTLE FOOT power MOSFETs use integrated circuit and small-signal packages which have been modified to provide the heat transfer capabilities required by power devices. Leadframe materials and design, molding compounds, and die attach materials have been changed, while the footprint of the packages remains the same.

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (<http://www.vishay.com/doc?72286>), for the basis of the pad design for a LITTLE FOOT SOT-23 power MOSFET footprint. In converting this footprint to the pad set for a power device, designers must make two connections: an electrical connection and a thermal connection, to draw heat away from the package.

The electrical connections for the SOT-23 are very simple. Pin 1 is the gate, pin 2 is the source, and pin 3 is the drain. As in the other LITTLE FOOT packages, the drain pin serves the additional function of providing the thermal connection from the package to the PC board. The total cross section of a copper trace connected to the drain may be adequate to carry the current required for the application, but it may be inadequate thermally. Also, heat spreads in a circular fashion from the heat source. In this case the drain pin is the heat source when looking at heat spread on the PC board.

Figure 1 shows the footprint with copper spreading for the SOT-23 package. This pattern shows the starting point for utilizing the board area available for the heat spreading copper. To create this pattern, a plane of copper overlies the drain pin and provides planar copper to draw heat from the drain lead and start the process of spreading the heat so it can be dissipated into the

ambient air. This pattern uses all the available area underneath the body for this purpose.

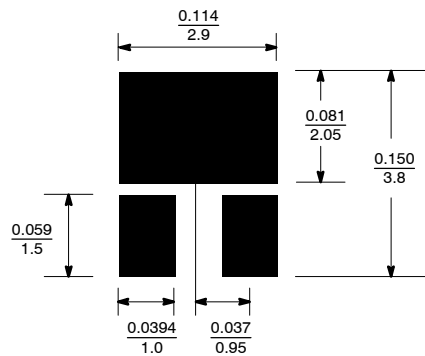


FIGURE 1. Footprint With Copper Spreading

Since surface-mounted packages are small, and reflow soldering is the most common way in which these are affixed to the PC board, “thermal” connections from the planar copper to the pads have not been used. Even if additional planar copper area is used, there should be no problems in the soldering process. The actual solder connections are defined by the solder mask openings. By combining the basic footprint with the copper plane on the drain pins, the solder mask generation occurs automatically.

A final item to keep in mind is the width of the power traces. The absolute minimum power trace width must be determined by the amount of current it has to carry. For thermal reasons, this minimum width should be at least 0.020 inches. The use of wide traces connected to the drain plane provides a low-impedance path for heat to move away from the device.

RECOMMENDED MINIMUM PADS FOR SOT-23



Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay's knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer's responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and / or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer's technical experts. Product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein.

Except as expressly indicated in writing, Vishay products are not designed for use in medical, life-saving, or life-sustaining applications or for any other application in which the failure of the Vishay product could result in personal injury or death. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.