NCP5201

Dual Output DDR Power Controller

The NCP5201 Dual DDR Power Controller is specifically designed as a total power solution for a high current DDR memory system. This IC combines the efficiency of a PWM controller for the VDDQ supply with the simplicity of a linear regulator for the VTT memory termination voltage. The secondary regulator (VTT) is designed to automatically track at half the primary regulator voltage (VDDQ). An internal power good voltage monitor tracks both VDDQ and VTT outputs and notifies the user in the event of a fault on either output. Protective features include soft−start circuitry and undervoltage monitoring of VCC and VSTBY. The IC is packaged in a 5 × 6 QFN−18.

Features

- Incorporates VDDQ, VTT Regulators
- Internal Switching Standby Regulator for VDDQ
- All External Power MOSFETs Are N−Channel
- Adjustable VDDQ
- VTT Tracks VDDQ/2
- Fixed Switching Frequency of 250 kHz for VDDQ in Normal Mode
- Doubled Switching Frequency (500 kHz) for Standby Mode
- Soft−Start Protection for VDDQ
- Undervoltage Monitor
- Short−Circuit Protection for Both VDDQ and VTT Outputs
- Housed in a space saving 5 × 6 QFN−18
- Pb−Free Packages are Available*

Typical Applications

- DDR Termination Voltage
- Active Termination Busses (SSTL−2, SSTL−3)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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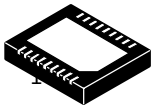
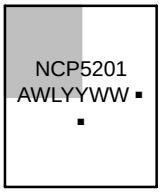
MARKING DIAGRAM

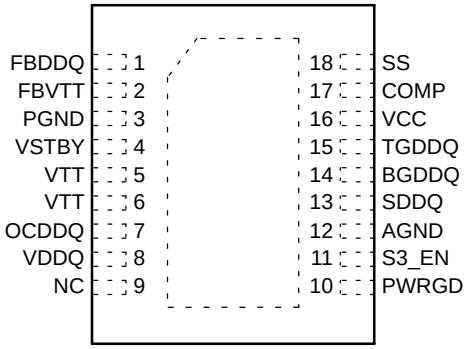


18−LEAD QFN, 5 x 6 mm
MN SUFFIX
CASE 505



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN CONNECTIONS



NOTE: Pin 19 is the thermal pad on the bottom of the device.

ORDERING INFORMATION

Device	Package	Shipping†
NCP5201MN	18−Lead QFN	61 Units / Rail
NCP5201MNG	18−Lead QFN (Pb−Free)	61 Units / Rail
NCP5201MNR2	18−Lead QFN	2500/Tape & Reel
NCP5201MNR2G	18−Lead QFN (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

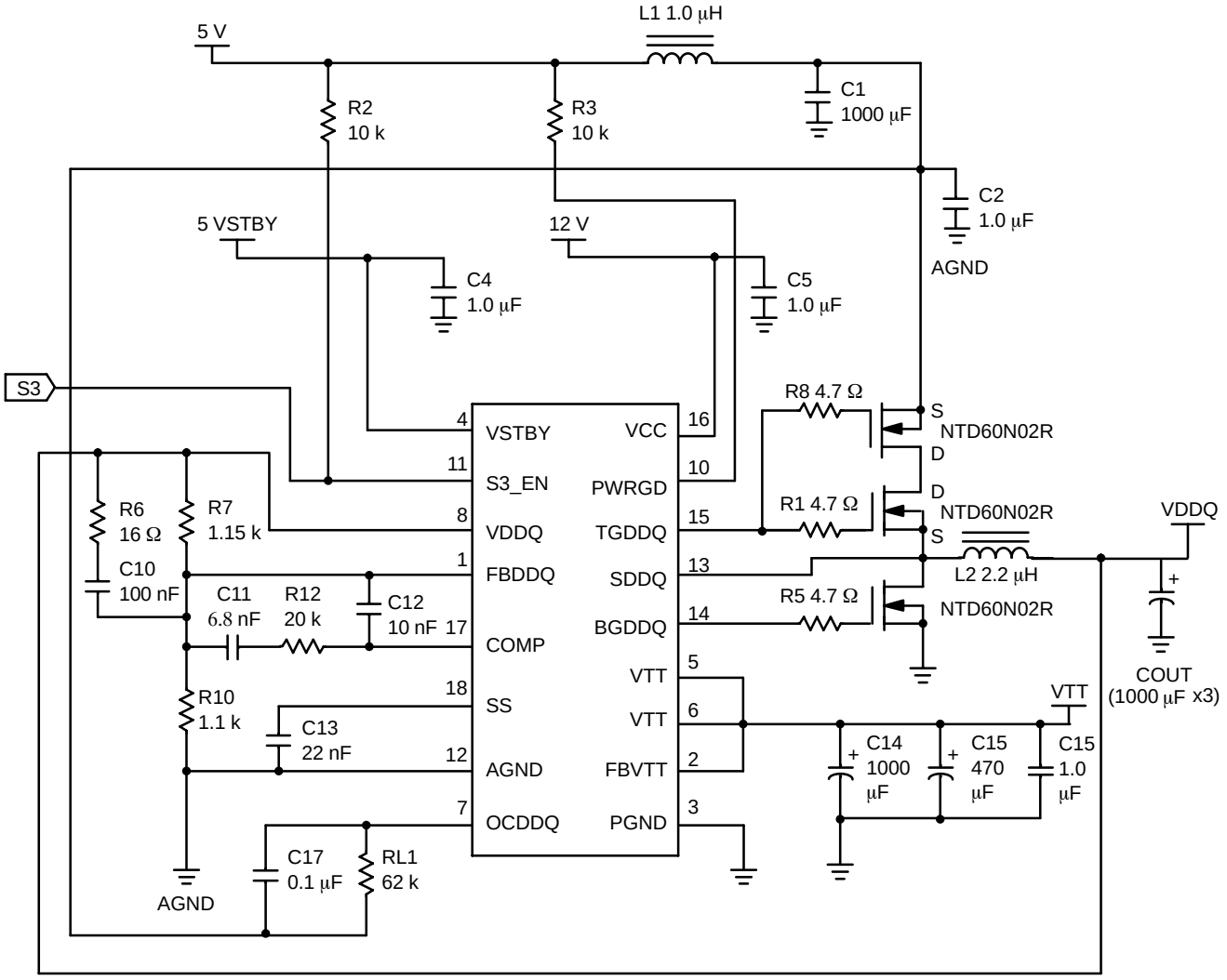


Figure 1. Application Diagram

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 4) to PGND (Pin 3) and GND (Pin 12)	VSTBY	−0.3, 6.0	V
Power Supply Voltage, VCC (Pin 16) to PGND (Pin 3) and GND (Pin 12)	VCC	−0.3, 14	V
Gate Drive Voltage (Pins 14, 15)	Vg	−0.3 DC, −4.0 for < 1.0 μs; 14	V
Input/Output Pins (Pins 1, 2, 5−11, 13, 17−18)	V_{IO}	−0.3, 6.0	V
Package Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	35	°C/W
Operating Junction Temperature Range	T_J	0 to +150	°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Moisture Sensitivity Level	MSL	2	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) ≤ 2.0 kV per JEDEC Standard JESD22−A114 except Pin 15 which is ≤ 1.5 kV.
   Machine Model (MM) ≤ 200 V per JEDEC Standard JESD22−A115 except Pin 14 which is ≤ 100 V.
2. Latchup Current Maximum Rating: ≤ 150 mA per JEDEC Standard JESD78.

ELECTRICAL CHARACTERISTICS (VSTBY = 5.0 V, VCC = 12 V, T_A = 0 to 70°C, L2 = 1.7 μH, COUT = 3770 μF, COUT2 = 220 μF, RL1 = 100 kΩ, R7 = 1.0 kΩ, R10 = 1.0 k, R12 = 20 kΩ, R6 = 16 Ω, C12 = 3.0 nF, C11 = 6.0 nF, C10 = 80 nF, for min/max values unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
SUPPLY CURRENT						
S0 Mode Supply Current from VSTBY	IST_S0	S3_EN = LOW, VCC = 12 V	−	−	8.0	mA
S3 Mode Supply Current from VSTBY	IST_S3	S3_EN = HIGH, VCC = 0 V	−	−	4.0	mA
S0 Mode Supply Current from VCC	ICC_S0	EN = HIGH, VCC = 12 V, 2.0 nF Capacitive Load to TGDDQ and BGDDQ	−	−	30	mA
UNDERVOLTAGE MONITOR						
VSTBY UVLO Lower Threshold	VSBUV−	−	−	4.25	−	V
Ratio of VSTBY UVLO Upper to Lower Threshold	VSBUV+/ VSBUV−	−	−	1.05	−	−
VCC UV Monitor Lower Threshold	VCCUV−	−	−	9.23	−	V
Ratio of VCC UV Monitor Upper to Lower Threshold	VCCUV+/ VCCUV−	−	−	1.14	−	−
VDDQ SWITCHING REGULATOR						
FBDDQ Feedback Voltage, Control Loop in Regulation	VFBQ	T_A = 25°C T_A = 0 to 70°C	1.271 1.264	1.300 −	1.326 1.333	V V
Feedback Input Current	Ifb	V(FBDDQ) = 1.3 V	−	−	0.5	μA
Oscillator Frequency in S0 Mode	F	−	225	250	275	kHz
OCDDQ Pin Current Sink	IOC	V(OCDDQ) = 4.0 V	6.0	10	14	μA
Minimum Duty Cycle	Dmin	−	0	−	−	%
Maximum Duty Cycle	Dmax	−	−	−	100	%
Soft−Start Timing	tss1	C_{SS} = 33 nF	10	16	−	ms
VDDQ STANDBY REGULATOR						
FBDDQ Feedback Voltage, Control Loop in Regulation	VFBQ	T_A = 25°C T_A = 0 to 70°C	1.281 1.274	1.300 −	1.319 1.326	V V
Load Regulation	LOADreg	ILOAD from 50 mA to 650 mA	−	0.4	−	%
Peak Current Limit	ILIMstbpk	−	−	2.0	−	A
Peak Current Limit Blanking Time	tbk	−	400	−	−	ns
Oscillator Frequency in S3 Mode	Fstb	−	−	500	−	kHz
VDDQ ERROR AMPLIFIER						
DC Gain	GAIN	−	−	70	−	dB
Unity Gain Bandwidth	Ft	COMP_GND = 200 nF, 1.0 Ω in series (Test circuit only)	−	2.0	−	MHz
Slew Rate	SR	COMP_GND = 10 pF	−	8.0	−	V/μs
VTT ACTIVE TERMINATOR						
VTT Tracking VDDQ/2 at S0 Mode	dVTT0	VDDQ/2 − VTT, IOUT = 1.8 A (Sink Current) IOUT = −1.8 A (Source Current)	 −30 −	 − −	 − 30	 mV mV
Source Current Limit	ILIMVTsrc	−	−	−2.3	−	A
Sink Current Limit	ILIMVTsnk	−	−	2.3	−	A

3. Guaranteed by design, not tested in production.

ELECTRICAL CHARACTERISTICS (VSTBY = 5.0 V, VCC = 12 V, T_A = 0 to 70°C, L2 = 1.7 μH, COUT = 3770 μF, COUT2 = 220 μF, RL1 = 100 kΩ, R7 = 1.0 kΩ, R10 = 1.0 k, R12 = 20 kΩ, R6 = 16 Ω, C12 = 3.0 nF, C11 = 6.0 nF, C10 = 80 nF, for min/max values unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
CONTROL SECTION						
S3_EN Pin Threshold HIGH	−	S3_EN_H	1.4	−	−	V
S3_EN Pin Threshold LOW	−	S3_EN_L	−	−	0.5	V
S3_EN Pin Input Current	−	IIN_EN	−	−	0.5	μA
PWRGD Pin ON Resistance	−	PWRGD_R	−	−	80	Ω
PWRGD Pin OFF Current	−	PWRGD_ LEAK	−	−	1.0	μA
PWRGD LOW−to−HIGH Hold Time, For S3 to S0 or S5 to S0	−	thold	−	−	200	μs
GATE DRIVERS						
TGDDQ Gate Pull−HIGH Resistance	VCC = 12 V, V(TGDDQ) = 11 V	RH_TG	−	3.0	−	Ω
TGDDQ Gate Pull−LOW Resistance	VCC = 12 V, V(TGDDQ) = 1.0 V	RL_TG	−	2.5	−	Ω
BGDDQ Gate Pull−HIGH Resistance	VCC = 12 V, V(BGDDQ) = 11 V	RH_BG	−	3.0	−	Ω
BGDDQ Gate Pull−LOW Resistance	VCC = 12 V, V(BGDDQ) = 1.0 V	RL_BG	−	1.3	−	Ω

PIN DESCRIPTION

Pin No.	Symbol	Description
1	FBDDQ	VDDQ feedback pin for closed loop regulation.
2	FBVTT	VTT regulator sense voltage.
3	PGND	Power ground.
4	VSTBY	5 V Standby input voltage.
5, 6	VTT	VTT regulator output.
7	OCDDQ	Overcurrent sense and program input for the VDDQ high−side FET.
8	VDDQ	Reference input and power stage input for VTT regulator.
9	NC	Not connected.
10	PWRGD	Open drain status output. High impedance when the product is operating in S0 state and both DDQ and VTT regulators are in compliance.
11	S3_EN	S3 mode enable input. High to enable.
12	AGND	Analog ground connection and remote ground sense.
13	SDDQ	Inductor driven node and current limit sense input.
14	BGDDQ	Gate driver output, VDDQ Low−Side N−Channel Power FET. Active during S0 mode.
15	TGDDQ	Gate driver output, VDDQ High−Side N−Channel Power FET. Active during S0 mode.
16	VCC	12 Volt input supply. This voltage is monitored by power good circuitry for mode selection.
17	COMP	VDDQ error amplifier compensation node.
18	SS	Soft−start capacitor connection to ground.
19	TH_PAD	Copper pad on bottom of IC used for heatsinking. This pin should be connected to the ground plane under the IC.

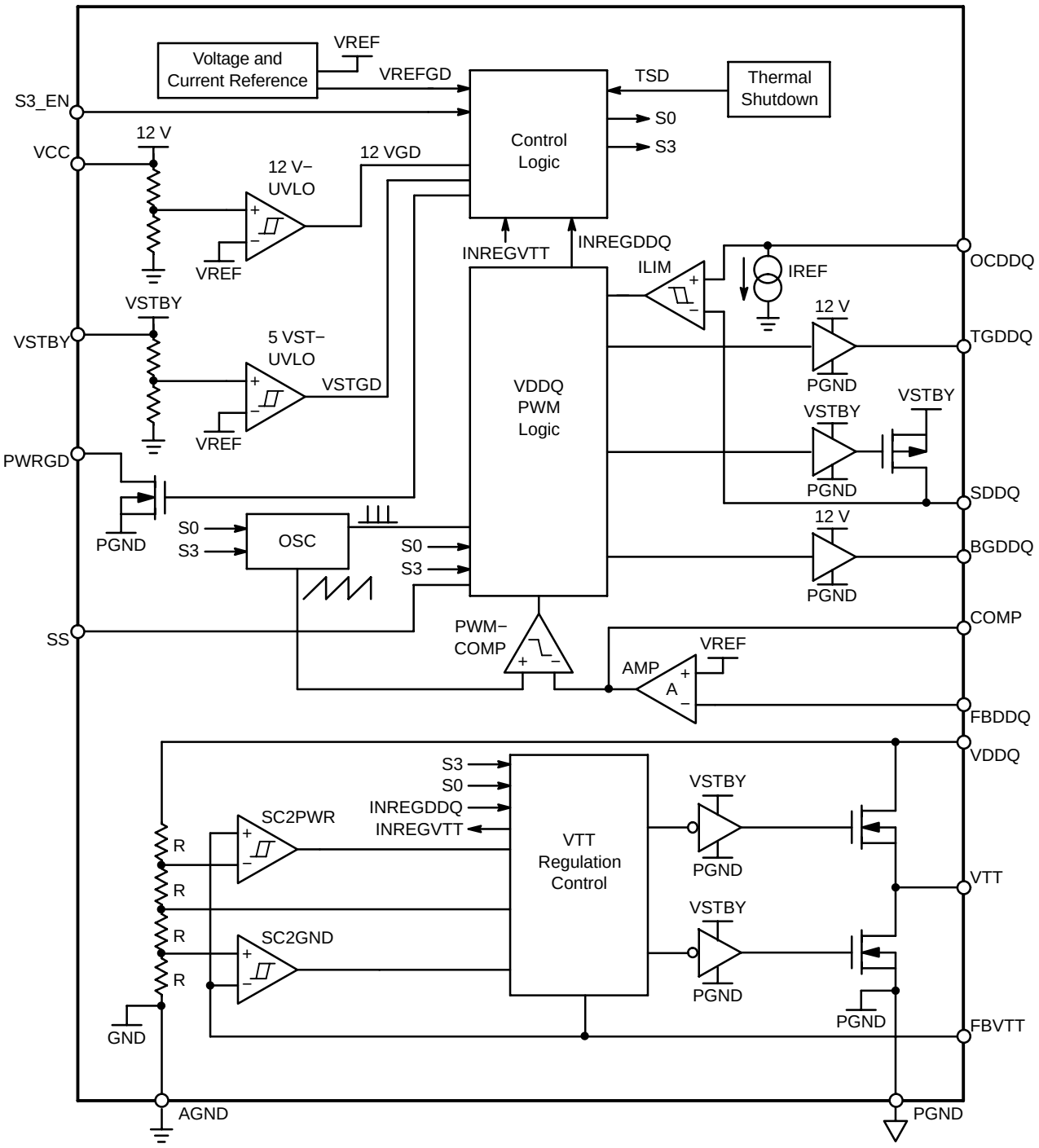


Figure 2. Internal Block Diagram

DETAILED OPERATION DESCRIPTIONS

General

The NCP5201 Dual DDR Power Controller combines the efficiency of a PWM controller for the VDDQ supply with the simplicity of a linear regulator for the VTT memory termination voltage. VTT is designed to automatically track at half VDDQ.

The inclusion of an internal PWM switching FET for VDDQ standby operation, both VDDQ and VTT power good voltage monitors, soft−start, undervoltage detection, and thermal shutdown, make this device a total power solution for high current DDR memory systems. The IC is packaged in 5×6 QFN−18.

IC Control States

The state decode logic and internal control functions are powered by 5.0 V VSTBY. An internal voltage reference and bias current block is enabled when VSTBY exceeds 3.8 V. Once VREF reaches its regulation voltage, internal signal _VREFGD will be asserted HIGH. This transition wakes up the voltage monitor block, which in turn detects whether the VSTBY and VCC voltages are within certain preset regulation levels. If they are, the voltage monitor generates an internal HIGH VSTGD and 12 VGD respectively.

There is an internal detection for 100% duty cycle of TGDDQ switching, if it occurs, an internal signal MAXDTY is asserted HIGH.

The logic control block accepts an external signal at the S3_EN pin and internal voltage monitor signals MXDTY, 12 VGD and VSTGD to decode the operating states in accordance with Table 1. PWRGD is an open−drain logic output that signifies VDDQ and VTT are both in regulation in the S0 mode.

Table 1. Control Logic State Truth Table

Input Conditions				Operation Mode	
VSTGD	**S3_EN**	**12 VGD**	**MAXDTY**	**Prev.**	**Next**
Low	X	X	X	X	S5
High	Low	Low	X	X	S5
High	Low	High	X	X	S0
High	High	High	Low	S0	S0
High	High	X	High	S0	S3
High	High	Low	X	S0	S3
High	High	X	X	S3	S3

VDDQ Regulator in Normal (SO) mode

The VDDQ regulator in S0 mode is a switching synchronous rectification buck controller directly driving two external N−Channel power FETs. An external resistor divider sets the nominal output voltage. The control architecture is voltage mode fixed frequency PWM with external compensation, and with switching frequency fixed at 250 kHz ±10%. As can be observed from Figure 1, the VDDQ output voltage is divided down and fed back to pin FBDDQ. This voltage connects to the inverting input of the internal error amplifier while the amplifier's noninverting input is connected to an internal voltage reference, VREF (= 1.3 V). The amplifier compares the feedback voltage to VREF and outputs an error signal to the PWM comparator. This error signal is compared with a fixed frequency RAMP waveform derived from the internal oscillator to generate a pulse−width−modulated signal. This PWM signal drives the external N−Channel Power FETs via the TGDDQ and BGDDQ pins. External inductor L and COUT1 filter the output waveform, which is subsequently fed back to FBDDQ via a resistor voltage divider to close the loop at VDDQ = VFBQ (1 + R2/R1). An adjustable soft−start is implemented, activated each time the IC exits state S5. When in normal mode, and regulation of VDDQ is detected, signal INREGDDQ will go HIGH to notify the Control Logic block.

Tolerance of VDDQ

The tolerance of VFBQ and the ratio of external resistor divider R7/R10 both impact the precision of VDDQ. With the control loop in regulation, VDDQ = (VFBQ) (1 + R7/R10). With a worst case (for all valid operating conditions) VFBQ tolerance of ±2%, a worst case range of ±2.5% for VDDQ will be assured if the ratio R7/R10 is specified as 0.9230 ±1%.

Synchronous Rectification

For enhanced efficiency, an active synchronous switch is used to eliminate the conduction loss contributed by the forward voltage of a diode or Schottky diode rectifier. Adaptive nonoverlap timing control of the complementary gate drive output signals is provided to reduce large shoot−through currents, which degrade efficiency.

VDDQ Regulator in Standby Mode (S3)

An internal P−Channel power FET switching at 500 kHz (doubled frequency), with peak current limit preset at 2.0 A, provides nonsynchronous switch−mode control while in the S3 state. In this mode, the internal P−Channel power FET derives its source from the 5 VSTBY pin. The 2.0 A peak current limit is designed to yield an average output current limit of 700 mA when using a 1.7 μH output inductor. When using this value inductor, the regulator will operate in discontinuous conduction mode (DCM) in the S3 state. And, switching in doubled frequency (500 kHz) is to reduce the peak conduction current. In this operating mode, the body diode of the external synchronous MOSFET acts as a flywheel diode and the MOSFET is never turned on. TGDDQ and BGDDQ are set Low to disable the external switches. Nominal output voltage and the PWM control scheme of Normal mode still apply.

Table 2. States, Operation and Output Pin Conditions

Operation Mode	Operating Conditions		Output Pin Conditions		
	VDDQ	VTT	TGDDQ	BGDDQ	PWRGD
S0	Normal	Normal	Normal	Normal	H−Z
S3	Standby	H−Z	Low	Low	Low
S5	H−Z	H−Z	Low	Low	Low

Fault Protection of VDDQ Regulator

During state S0, external resistor (RL1) sets current limit for the high−side switch. An internal 10 μA current sink at pin OCDDQ establishes the voltage drop across this resistor, which is compared to the voltage at the SDDQ pin when the high−side drive is high, and after a fixed period (500 ns) of blanking time to avoid false current limit triggering. When the voltage at SDDQ is lower than that at OCDDQ, an overcurrent condition occurs, both FETs are latched−off until the IC goes into S5 then S0, VDDQ will soft−start again. This protects against a short−to−ground condition on SDDQ or VDDQ.

During state S3, the internal P−Channel power FET is activated and switching. If the conduction current of the FET is higher than 2.0 A after a fixed period (~500 ns) of blanking time, an overcurrent condition occurs, and the FET is turned off for the remainder of that switching cycle.

Feedback Compensation of VDDQ Regulator

The compensation network is shown in Figure 1.

VTT Active Terminator in Normal Mode (S0)

The VTT regulator is a two−quadrant linear regulator with internal N−channel power FETs to provide transient current sink and source capability up to 1.8 A. This output is activated in normal mode in state S0 when VDDQ is in regulation. It is in standby mode in state S3. When in normal mode and VTT is in regulation, signal INREGVTT will go HIGH to notify the control logic block. The input power path is from VDDQ. Gate drive power is derived from VSTBY. VTT is stable with any value of output capacitor greater than 220 μF, and is insensitive to ESR value ranging 2 mΩ to 400 mΩ.

VTT Active Terminator in Standby Mode (S3)

VTT output is high−impedance in S3 mode.

Fault Protection of VTT Active Terminator

To provide protection for the internal FETs, bidirectional current limit is implemented, preset at 2.3 A magnitude.

Thermal Consideration of VTT Active Terminator

The VTT terminator is designed to handle large transient output currents. If large currents are required for very long durations, then care should be taken to ensure the maximum junction temperature is not exceeded. The 5×6 QFN−18 has a thermal resistance 35°C/W (dependent on air flow, grade of copper and number of VIAs).

Undervoltage Monitor

The IC monitors VSTBY and VCC. If VSTBY is higher than its preset threshold (derived from VREF, with hysteresis), _VSTGD is set HIGH. Operation is identical for VCC and _12 VGD. The CONTROL LOGIC accepts both _VSTGD and _12 VGD to determine the state of the IC.

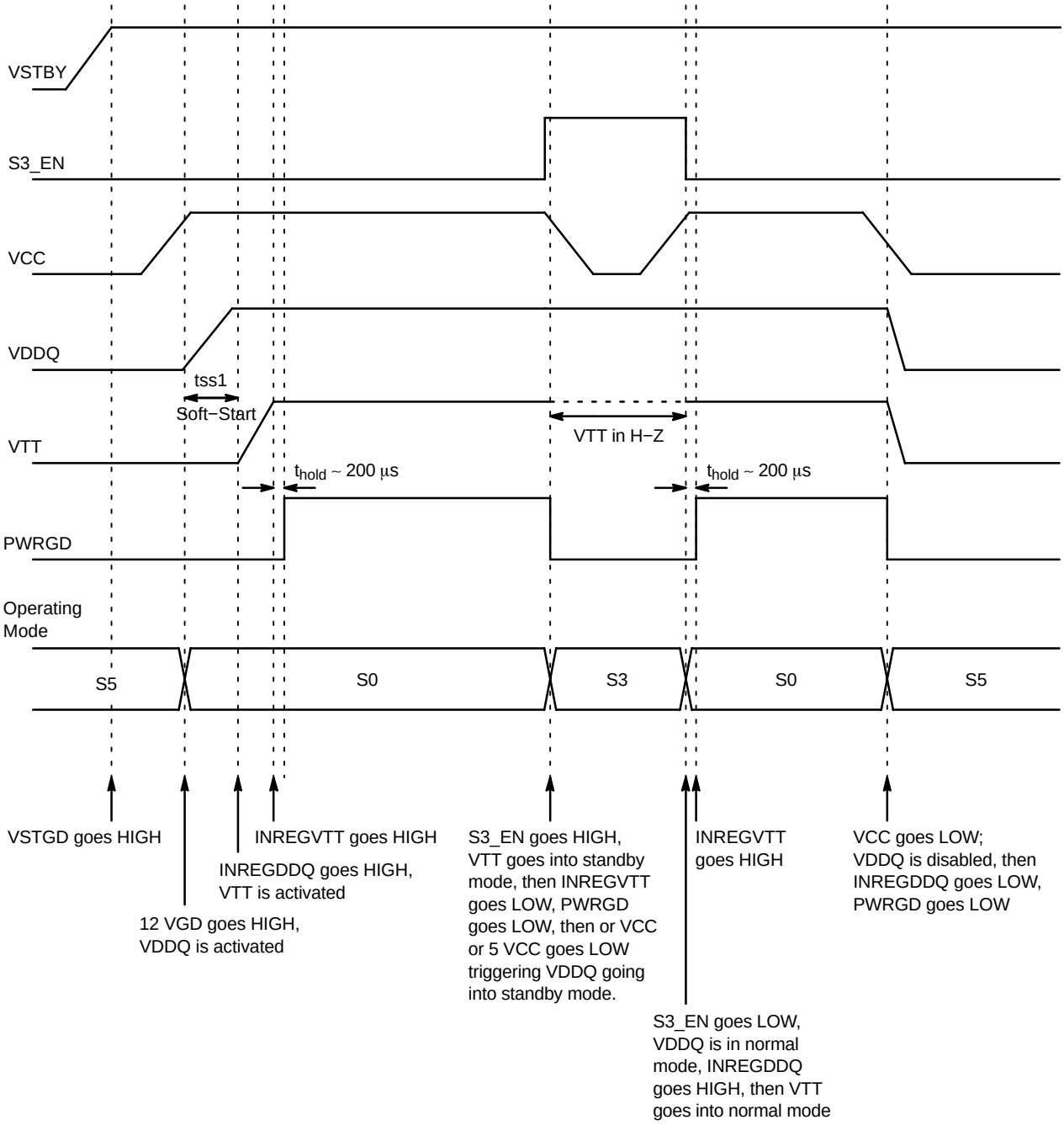
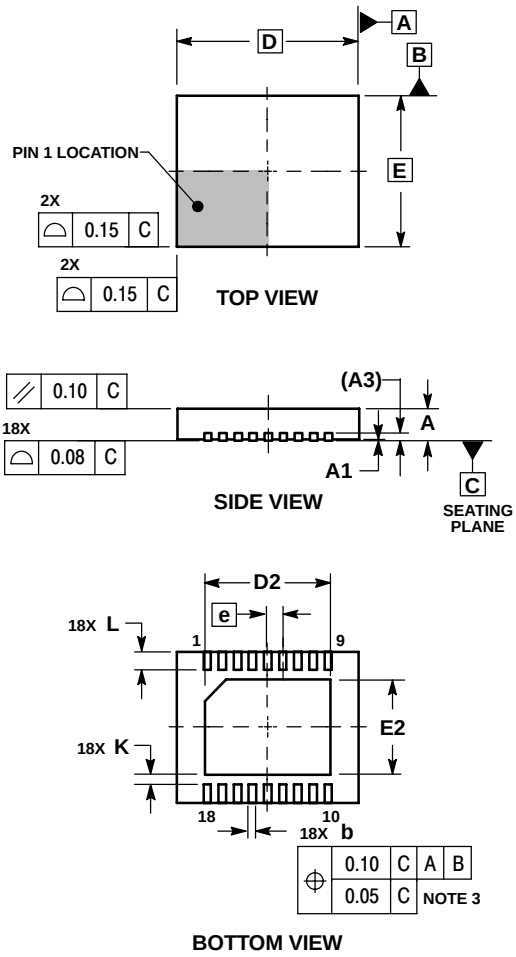


Figure 3. Power−Up and Power−Down Timing Diagram

PACKAGE DIMENSIONS

DFN−18
CASE 505−01
ISSUE B



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	6.00 BSC	
D2	3.98	4.28
E	5.00 BSC	
E2	2.98	3.28
e	0.50 BSC	
K	0.20	−−−
L	0.45	0.65

PUBLICATION ORDERING INFORMATION

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