H-bridge Motor Driver with Integrated Current Sense and Regulation

FEATURES

- AEC-Q100 qualified for automotive applications:
  – Temperature grade 2:-40°C to +105°C,TA
- N-Channel H-bridge Motor Driver:
  Drives One Bidirectional Brushed DC Motor, Two Unidirectional Brushed DC Motors, or Other Resistive and Inductive Loads
- Wide 4.5V to 37V Operating Voltage
- 3.5A Peak Current Drive
- Integrated Current Sensing and Regulation
- PH/EN and PWM H-bridge control modes
  - Independent half-bridge control mode
- Cycle-by-cycle or Fixed Off-Time Current Regulation
- Supports 1.8V, 3.3V, 5V Logic Inputs
- Built-in 5V Reference Output
- Ultra-Low Power Sleep Mode
- VM Under voltage Lockout (UVLO)
- Over current Protection (OCP)
- Automatic retry or outputs latched off (IMODE)
- Thermal Shutdown (TSD)
- Automatic Fault Recovery and Indicator Pin
- Small Packages
  - TMI8116-Q1: HTSSOP16

APPLICATIONS

- Rotational screen
- Side mirror tilt and fold
- E-shifter adjust and lock
- Ac charging gun
- Tail gas circulating valve

GENERAL DESCRIPTION

The TMI8116-Q1 is a motor driver for wide variety of end applications. The device integrates an H-bridge, charge pump regulator, current sensing and regulation, current proportional output, and protection circuitry. The charge pump improves efficiency by allowing for both high and low side N-channels MOSFETs and 100% duty cycle support.

Integrated current sensing allows for the driver to regulate the motor current during start up and high load events. A current limit can be set with an adjustable external voltage reference. Additionally, the device provides an output current proportional to the motor load current. This can be used to detect motor stall or change in load conditions.

A low-power sleep mode is provided to achieve ultra- low quiescent current draw by shutting down most of the internal circuitry. The device is fully protected from faults and short circuits, including undervoltage lockout (UVLO), output over-current protection (OCP), and device thermal shutdown (TSD). Fault conditions are indicated on nFAULT.

TYPICAL APPILCATION

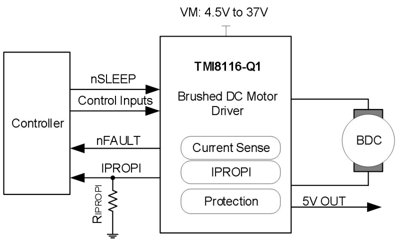


Figure 1. Basic Application Circuit

ABSOLUTE MAXIMUM RATINGS (Note 1)

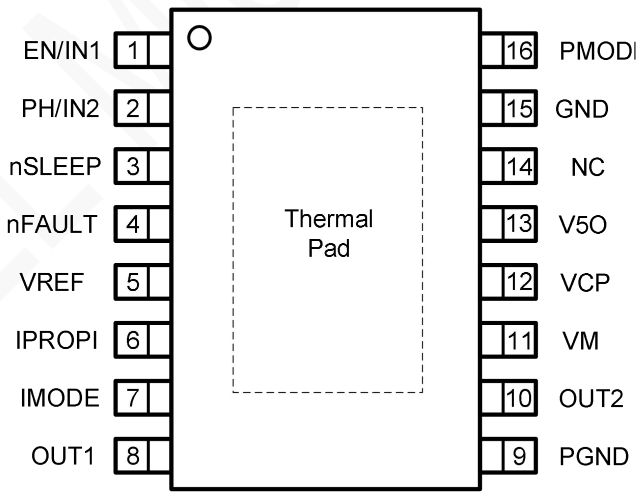
Parameter	Min	Max	Unit
Power supply voltage (VM)	-0.3	40	V
Voltage difference between ground pins (GND, PGND)	-0.3	0.3	V
Logic input voltage (EN/IN1, PH/IN2, IMODE, nSLEEP, PMODE)	-0.3	6	V
Reference input pin voltage (VREF)	-0.3	6	V
Open-drain output pin voltage (nFAULT)	-0.3	6	V
Output pin voltage (OUT1, OUT2)	-0.7	VM+0.7	V
Proportional current output pin voltage (IPROPI)	-0.3	6	V
T_A, Operating ambient temperature	-40	105	°C
T_J, operating junction temperature (Note 2)	-40	150	°C
T_{stg}, Storage temperature	-40	150	°C

ESD RATING

Items	Description	Value	Unit
V_{ESD}	Human body model(HBM), per AEC Q100-002(1)	±2000	V
	Charged device model (CDM), per AEC Q100-011	±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

PACKAGE/ORDER INFORMATION



HTSSOP16 (Top Viewer)

Part Number	Package	Top mark	Quantity/ Reel
TMI8116-Q1	HTSSOP16	TMI8116-Q1 XXXXX	4,000

The TMI8116-Q1 devices is Pb-free and RoHS compliant.

PIN FUNCTIONS

Pin			Function
QFN	HTSSOP	Name	
1	3	nSLEEP	Sleep mode input. Logic high to enable device. Logic low to enter low-power sleep mode. Internal pulldown resistor.
2	4	nFAULT	Fault indicator output. Pulled low during a fault condition. Connect an external pullup resistor for open-drain operation.
3	5	VREF	External reference voltage input to set internal current regulation limit.
4	6	IPROPI	Analog current output proportional to load current.
5	7	IMODE	Current regulation and overcurrent protection mode set pin. Quad- level input.
6	8	OUT1	H-bridge output. Connect to the motor or other load.
7	9	PGND	Device power ground. Connect to system ground.
8	10	OUT2	H-bridge output. Connect to the motor or other load.
9	11	VM	4.5 to 37V power supply input. Connect a 0.1μF bypass capacitor to ground, as well as a sufficient bulk capacitance rated for VM.
10	12	VCP	High side drive supporting voltage. Floating or connect a 0.1μF ceramic capacitor to VM
11	13	V5O	Built-in 5V reference voltage output.
12	14	NC	Not connected.
13	15	GND	Device ground. Connect to system ground.
14	16	PMODE	H-bridge control input mode. Tri-level input.
15	1	EN/IN1	H-bridge control input. Internal pulldown resistor.
16	2	PH/IN2	H-bridge control input. Internal pulldown resistor.
-	-	GND	Thermal pad. Connect to device power ground.

RECOMMENDED OPERATING CONDITIONS

Items	Description	Min	Max	Unit
VM	Power supply voltage range	4.5	37	V
VIN	Logic input voltage	0	5.5	V
f_{PWM}	PWM frequency	0	100	kHz
V_{OD}	Open drain pullup voltage	0	5.5	V
I_{OD}	Open drain output current	0	5	mA
I_{OUT}	Peak output current	0	3.5	A
I_{IPROPI}	Current sense output current	0	3	mA
V_{VREF}	Current limit reference voltage	0	3.6	V

Thermal Information

THERMAL METRIC(1)		TMI8166-Q1 PWP (HTSSOP) 16 PINS	UNIT
$R_{\theta J}$	Junction-to-ambient thermal resistance	45.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.10	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	21.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.3	°C/W

ELECTRICAL CHARACTERISTICS

T_A = 25°C, (unless otherwise noted.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY (VM)						
VM operating voltage	VM		4.5		37	V
VM operating current	I_{VM}	VM = 24V		3	5	mA
VM sleep current	$I_{VMSLEEP}$	VM = 24V, nSLEEP = 0V			5	μA
Turn-on time (Note 3)	t_{WAKE}	nSLEEP active			1	ms
Turn-off time	t_{SLEEP}	Sleep mode			1	ms
Output dead time	t_{DEAD}	Body diode conducting		300		ns
Charge pump regulator voltage	V_{VCP}	VM=24V, VCP with respect to VM		5		V
Charge pump switching frequency	f_{VCP}			1.2		MHz
LOGIC-LEVEL INPUTS (IN1, IN2, nSLEEP)						
Input logic low voltage	V_{IL}		0		0.7	V
Input logic high voltage	V_{IH}		1.5		5.5	V
Input logic hysteresis	V_{HYS}			0.25		V
Input logic low current	I_{IL}	VIN = 0V	–5		6	μA
Input logic high current	I_{IH}	VIN = 5V		50	75	μA
Pulldown resistance	R_{PD}	Pull down to GND		100		kΩ
TRI-LEVEL INPUTS (PMODE)						
Tri-level input low voltage	V_{TIL}		0		0.65	V
Tri-level input Hi-Z voltage	V_{TIZ}		0.9		1.2	V
Tri-level input high voltage	V_{TIH}		1.5		5.5	V
Tri-level input low current	I_{TIL}	VIN = 0V		-32		μA
Tri-level input Hi-Z current	I_{TIZ}	VIN = 1.1V	-5		5	μA
Tri-level input high current	I_{TIH}	VIN = 5V			150	μA
Tri-level pull-down resistance	R_{TPD}	Pull down to GND		40		kΩ
Tri-level pull-up resistance	R_{TPU}	Pull up to internal 5V		156		kΩ
QUAD-LEVEL INPUTS (IMODE)						
Quad-level input level 1	V_{QI2}	Voltage to set quad-level 1	0		0.45	V
Quad-level input level 2	R_{QI2}	Resistance to GND to set quad-level 2	18.6	20	21.4	kΩ
Quad-level input level 3	R_{QI3}	Resistance to GND to set quad-level 3	57.6	62	66.4	kΩ
Quad-level input level 4	V_{QI3}	Voltage to set quad-level 4	2.5		5.5	V
Quad-level pull-down resistance	R_{QPD}	Pull down to GND		136		kΩ
Quad-level pull-up resistance	R_{QPU}	Pull up to internal 5V		68		kΩ

ELECTRICAL CHARACTERISTICS (Continued)

T_A = 25°C, (unless otherwise noted.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
MOTOR DRIVER OUTPUTS (OUT1, OUT2)						
High-side FET on resistance	$R_{(ON)\_High}$	VM = 24 V, I_{OUT} = 1A		250		mΩ
Low-side FET on resistance	$R_{(ON)\_Low}$	VM = 24 V, I_{OUT} = 1A		240		mΩ
Output dead time	t_{DEAD}	Body diode conducting		300		ns
Output rise time	t_{RISE}	VM = 24 V, OUTx rising 10% to 90%		165		ns
Output fall time	t_{FALL}	VM = 24 V, OUTx falling 90% to 10%		150		ns
Input to output propagation delay	t_{PD}	EN/IN1, PH/EN2 OUTx, 200Ω from OUTx to GND		650		ns
Body diode forward voltage	V_d	I_{OUT} = 1A		0.9		V
OPEN-DRAIN OUTPUTS (nFAULT)						
Output logic low voltage	V_{OL}	I_{OD} = 5mA			0.7	V
Output logic high current	I_{OZ}	V_{OD} = 5V	-2		2	μA
CURRENT REGULATION						
Current mirror scaling factor	A_{VIPRO}			1000		μA/A
Current mirror scaling error	A_{ERR}	I_{OUT} < 0.15 A, 5.5 V ≤ V_{VM} ≤ 37 V	-7.5		7.5	mA
		0.15 A ≤ I_{OUT} < 0.5 A, 5.5 V ≤ V_{VM} ≤ 37 V	-5		5	%
		0.5 A ≤ I_{OUT} ≤ 2 A, 5.5 V ≤ V_{VM} ≤ 37 V, –40°C ≤ T_J < 125°C	-4		4	%
		0.5 A ≤ I_{OUT} ≤ 2 A, 5.5 V ≤ V_{VM} ≤ 37 V, 125°C≤ T_J ≤ 150°C	-5		5	%
PWM off-time	t_{OFF}			25		μs
Current sense delay time	t_{DELAY}			2.1		μs
Current regulation deglitch time	t_{DEG}			1.2		μs
PWM blanking time	t_{BLANK}			3.5		μs
Built-in 5V REGULATION						
Built-in 5V regulator output voltage	V_{V5O}	External Load 0 to 30mA		5		V

ELECTRICAL CHARACTERISTICS (Continued)

T_A = 25°C, (unless otherwise noted.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PROTECTION CIRCUITS						
VM undervoltage lockout	V_{UVLO_fall}	VM falls until UVLO triggers			4.2	V
	V_{UVLO_rise}	VM rises until operation recovers	4.6			V
VM undervoltage hysteresis	V_{UV_HYS}	Rising to falling		140		mV
OCP trip level	I_{OCP}		3.5	5.6		A
Overcurrent deglitch time	t_{OCP}			5		µs
Overcurrent retry time	t_{RETRY}			1.7		ms
Thermal shutdown threshold	T_{SD} (Note 4)			175		°C
Thermal shutdown hysteresis	T_{HYS} (Note 4)			40		°C

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula: $T_J = T_A + P_D \times \theta_{JA}$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_{D\ (MAX)} = (T_{J(MAX)}-T_A)/\theta_{JA}$.

Note 3: t_{WAKE} applies when the device initially powers up, and when it exits sleep mode.

Note 4: Thermal shutdown threshold and hysteresis are guaranteed by design.

OPERATION

Overview

The TMI8116-Q1 device is a brushed DC motor driver that operates from 4.5V to 37V supporting a wide range of output load currents for various types of motors and loads. The device integrates an H-bridge output power stage that can be operated in different control modes set be the PMODE pin setting. This allows for driving a single bidirectional brushed DC motor, two unidirectional brushed DC motors, or other output load configurations. The device integrates a charge pump regulator to support more efficient high-side N-channel MOSFETs and 100% duty cycle operation. The device operates off a single power supply input (VM) which can be directly connected to a battery or DC voltage supply. The nSLEEP pin provides an ultra-low power mode to minimize current draw during system inactivity.

The TMI8116-Q1 device also integrates output current sensing using current mirrors on the low-side power MOSFETs. A proportional current is then sent out on the IPROPI pin and can be converted to a proportional voltage using an external resistor (R_{IPRO}). The integrated current sensing allows the TMI8116 to limit the output current with a fixed off-time PWM chopping scheme and provide load information to the external controller to detect change in load or stall conditions. The integrated current sensing out performs traditional external shunt resistor sensing by providing current information even during the off-time slow decay recirculating period and removing the need for an external power shunt resistor. The off-time PWM current regulation level can be configured during motor operation through the VREF pin to limit the load current accordingly to the system demands.

A variety of integrated protection features protect the device in the case of a system fault. These include undervoltage lockout (UVLO), charge pump undervoltage (CPUV), overcurrent protection (OCP), and overtemperature shutdown (TSD). Fault conditions are indicated on the nFAULT pin.

Control Modes

The TMI8116-Q1 provides three modes to support different control schemes with the EN/IN1 and PH/IN2 pins. The control mode is selected through the PMODE pin with either logic low, logic high, or setting the pin Hi-Z as shown in Table 1. The PMODE pin state is latched when the device is enabled through the nSLEEP pin. The PMODE state can be changed by taking the nSLEEP pin logic low, waiting the t_{SLEEP} time, changing the PMODE pin input, and then enabling the device by taking the nSLEEP pin back logic high.

Table 1. PMODE Functions

PMODE STATE	CONTROL MODE
PMODE = Logic Low	PH/EN
PMODE = Logic High	PWM
PMODE = Hi-Z	Independent Half-Bridge

The inputs can accept static or pulse-width modulated (PWM) voltage signals for either 100% or PWM drive modes. The device input pins can be powered before VM is applied with no issues. By default, the EN/IN1 and PH/IN2 pins have an internal pulldown resistor to ensure the outputs are Hi-Z if no inputs are present.

The sections below show the truth table for each control mode. Note that these tables do not take into account the internal current regulation feature. Additionally, the TMI8116-Q1 automatically handles the dead-time generation when switching between the high-side and low-side MOSFET of a half-bridge.

PH/EN Control Mode (PMODE = Logic Low)

When the PMODE pin is logic low on power up, the device is latched into PH/EN mode. PH/EN mode allows for the H-bridge to be controlled with a speed and direction type of interface. The truth table for PH/EN mode is shown in Table 2.

Table 2. PH/EN Control Mode

nSLEEP	EN	PH	OUT1	OUT2	DESCRIPTION
0	X	X	High-Z	High-Z	Sleep
1	0	X	L	L	Brake
1	1	0	L	H	Reverse
1	1	1	H	L	Forward

PWM Control Mode (PMODE = Logic High)

When the PMODE pin is logic high on power up, the device is latched into PWM mode. PWM mode allows for the H-bridge to enter the Hi-Z state without taking the nSLEEP pin logic low. The truth table for PWM mode is shown in Table 3.

Table 3. PWM Control Mode

nSLEEP	IN1	IN2	OUT1	OUT2	DESCRIPTION
0	X	X	High-Z	High-Z	Sleep
1	0	0	High-Z	High-Z	Coast
1	0	1	L	H	Reverse
1	1	0	H	L	Forward
1	1	1	L	L	Brake

Independent Half-Bridge Control Mode (PMODE = Hi-Z)

When the PMODE pin is Hi-Z on power up, the device is latched into independent half-bridge control mode. This mode allows for each half-bridge to be directly controlled in order to support high-side slow decay or driving two independent loads. The truth table for independent half-bridge mode is shown in Table 4.

In independent half-bridge control mode, current sensing and feedback are still available, but the internal current regulation is disabled since each half-bridge is operating independently. Additionally, if both low-side MOSFETs are conducting current at the same time, the IPROPI scaled output will be the sum of the currents.

Table 4. Independent Half-Bridge Control Mode

nSLEEP	INx	OUTx	DESCRIPTION
0	X	High-Z	Sleep
1	0	L	OUTx Low-Side On
1	1	H	OUTx High-Side On

Current Sensing

The TMI8116-Q1 integrates current sensing, regulation, and feedback. These features allow for the device to sense the output current without an external sense resistor or sense circuitry reducing system size, cost, and complexity. This also allows for the device to limit the output current in the case of motor stall or high torque events and give detailed feedback to the controller about the load current through a current proportional output.

Current Regulation

The TMI8116-Q1 device integrates current regulation using either a fixed off-time or cycle-by-cycle PWM current chopping scheme. The current chopping scheme is selectable through the IMODE quad-level input. This allows the devices to limit the output current in case of motor stall, high torque, or other high current load events.

The IMODE level can be set by leaving the pin floating (Hi-Z), connecting the pin to GND, or connecting a resistor between IMODE and GND. The IMODE pin state is latched when the device is enabled through the nSLEEP pin. The IMODE state can be changed by taking the nSLEEP pin logic low, waiting the t_{SLEEP} time, changing the IMODE pin input, and then enabling the device by taking the nSLEEP pin back logic high. The IMODE input is also used to select the device response to an overcurrent event.

The internal current regulation can be disabled by tying IPROPI to GND and setting the VREF pin voltage greater than GND (if current feedback isn't required) or if current feedback is required, setting V_{VREF} and R_{IPROPI} such that V_{IPROPI} never reaches the V_{VREF} threshold. In independent half-bridge control mode (PMODE = Hi-Z), the internal current regulation is automatically disabled since the outputs are operating independently and the current sense and regulation is shared between half-bridges.

Table 5. IMODE Functions

IMODE STATE		IMODE FUNCTION		nFAULT Response
		Current Chopping Mode	Overcurrent Response	
Quad-Level 1	R_{IMODE}=GND	Fixed Off-Time	Automatic Retry	Overcurrent Only
Quad-Level 2	R_{IMODE}=20kΩ to GND	Cycle-By-Cycle	Automatic Retry	Current Chopping and Overcurrent
Quad-Level 3	R_{IMODE}=62kΩ to GND	Cycle-By-Cycle	Latched Off	Current Chopping and Overcurrent
Quad-Level 4	R_{IMODE}=Hi-Z	Fixed Off-Time	Latched Off	Overcurrent Only

In TMI8116-Q1, motor peak current can be limited by the analog reference input VREF and the resistance of external sense resistor on the IPROPI pin according to the below equation:

$$I_{TRIP}\ (A)=\frac{VREF\ (V)}{A_{IPROPI}(\mu A/A)\times R_{IPROPI}(\Omega)}$$

For example, if V_{VREF} = 2.5 V, R_{IPROPI} = 2000 Ω, and A_{IPROPI} = 1000 μA/A, then I_{TRIP} will be approximately 1.25 A.

VM Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the undervoltage-lockout threshold voltage, all FETs in the H-bridge will be disabled. Operation resumes when VM rises above the UVLO threshold.

Overcurrent Protection (OCP)

If the output current exceeds the OCP threshold, I_{OCP}, for longer than t_{OCP}, all FETs in the H-bridge are disabled.
As to TMI8116-Q1, after a duration of t_{RETRY}, the H-bridge is re-enabled according to the state of the INx pins. If the overcurrent fault is still present, the cycle repeats, otherwise normal device operation resumes.

Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge are disabled. After the die temperature has fallen to a safe level, operation automatically resumes.

Device Functional Modes

The TMI8116-Q1 device can be used in multiple ways to drive a brushed DC motor.

Control with Current Regulation

This scheme uses all of the capabilities of the device. The I_{TRIP} current is set above the normal operating current, and high enough to achieve an adequate spin-up time, but low enough to constrain current to a desired level. Motor speed is controlled by the duty cycle of one of the inputs, while the other input is static. Brake or slow decay is typically used during the off-time.

Control Without Current Regulation

If current regulation is not required, the IPROPI pin should be directly connected to the PCB ground plane. The VREF voltage must still be 0.3V to 5 V, and larger voltages provide greater noise margin. This mode provides the highest-possible peak current which is up to 3.5 A for a few hundred milliseconds (depending on PCB characteristics and the ambient temperature). If current exceeds 3.5 A, the device might reach overcurrent protection (OCP) or overtemperature shutdown (TSD). If that happens, the device disables and protects itself for about 2ms (t_{RETRY}) and then resumes normal operation.

Static Inputs with Current Regulation

The IN1 and IN2 pins can be set high and low for 100% duty cycle drive, and I_{TRIP} can be used to control the current of the motor, speed, and torque capability.

VM Control

In some systems, varying VM as a means of changing motor speed is desirable.

APPLICATION INFORMATION

Application information

The TMI8116-Q1 device is typically used to drive one brushed DC motor as below

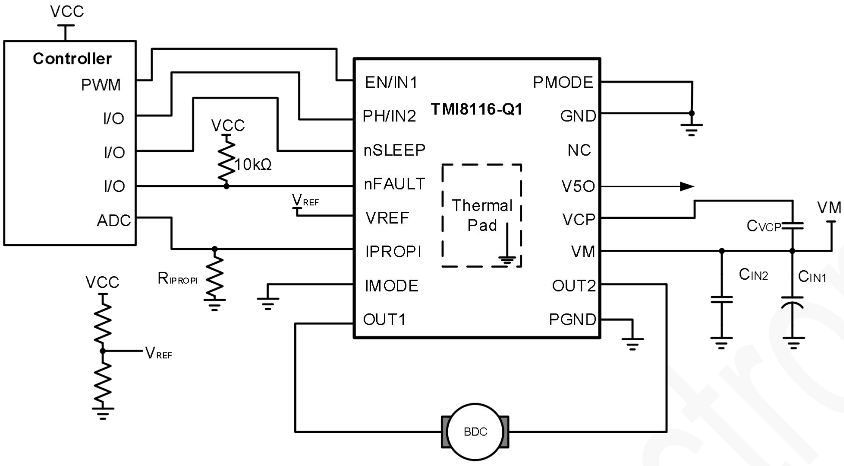


Figure 2.TMI8116-Q1 Typical Application

Block Diagram

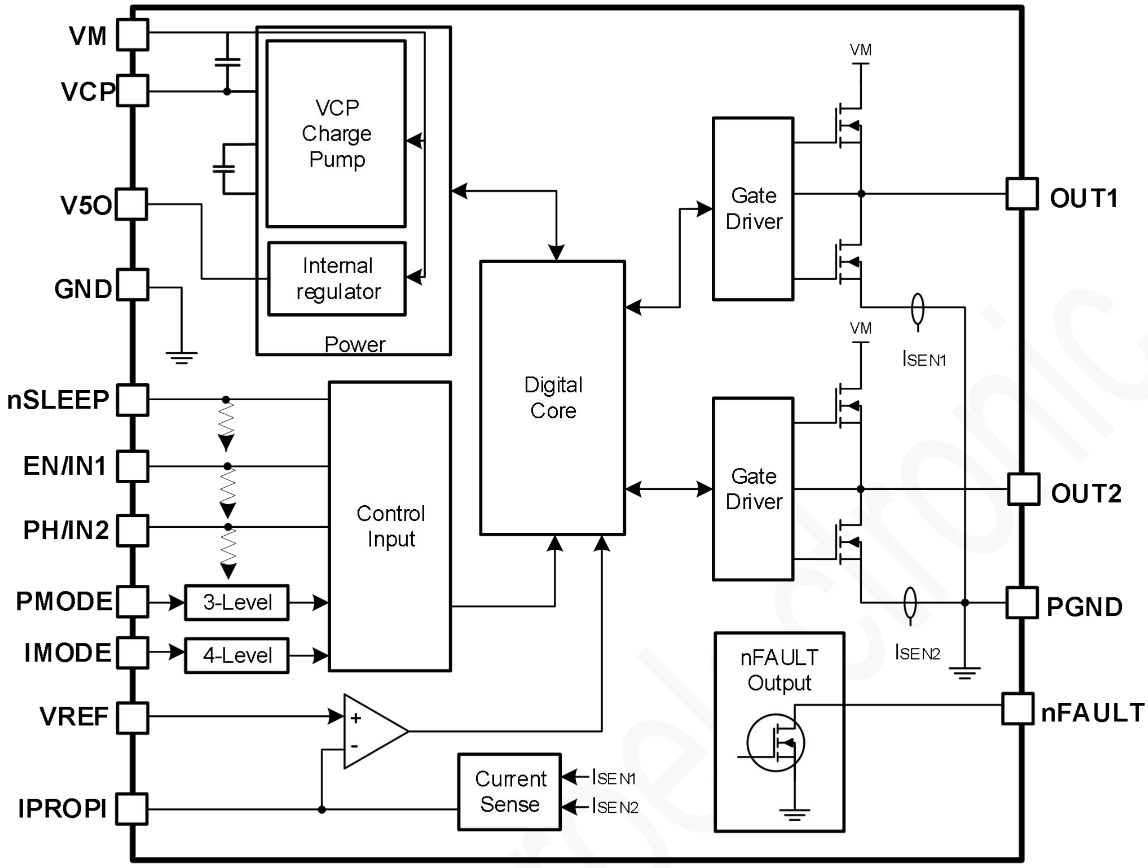
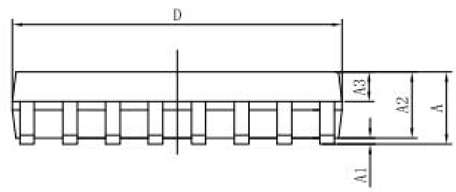
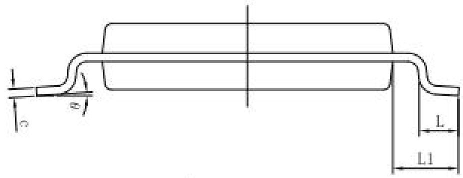


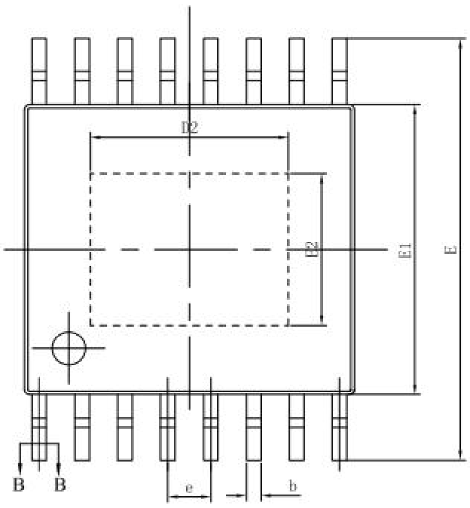
Figure 3. TMI8116-Q1 Block Diagram

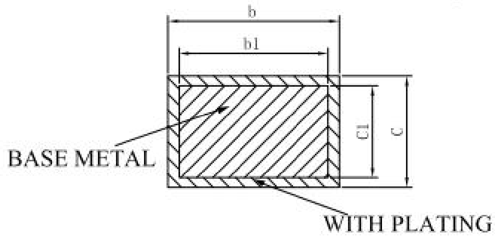
PACKAGE INFORMATION

HTSSOP16

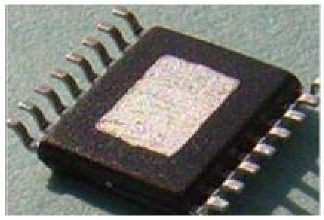








SECTION B-B



Unit: mm

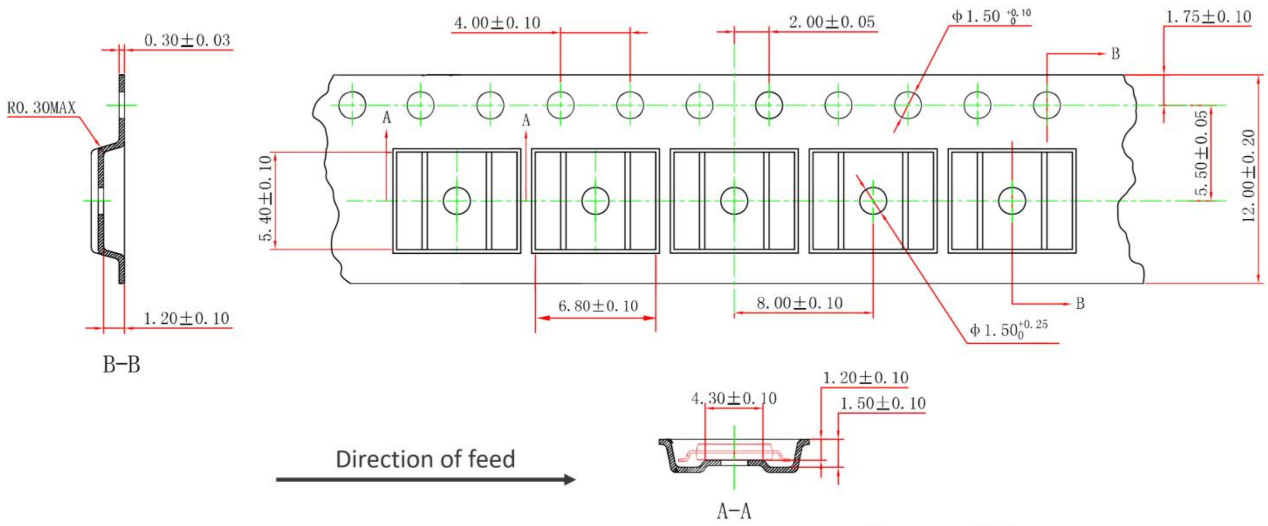
Symbol	Dimensions In Millimeters			Symbol	Dimensions In Millimeters		
	Min	NOM	Max		Min	NOM	Max
A	-	-	1.20	c1	0.12	0.13	0.14
A1	0.00	-	0.15	D	4.90	5.00	5.10
A2	0.90	1.00	1.05	E	6.20	6.40	6.60
A3	0.39	0.44	0.49	E1	4.30	4.40	4.50
b	0.20	-	0.28	e	0.65BSC		
b1	0.19	0.22	0.25	L	0.45	-	0.75
c	0.13	-	0.17	L1	1.00BSC		
θ	0	-	8°	E2	2.80REF		
D2	2.80REF						

Note:

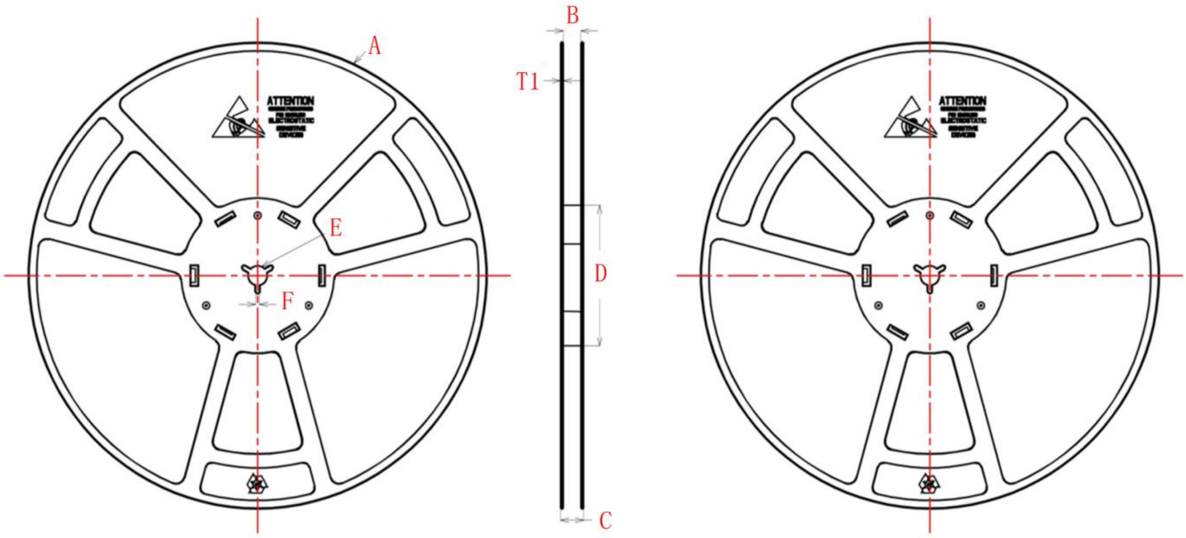
1) All dimensions are in millimeters.
2) Package length does not include mold flash, protrusion or gate burr.
3) Package width does not include inter lead flash or protrusion.
4) Lead popularity (bottom of leads after forming) shall be 0.10 millimeters max.
5) Pin 1 is lower left pin when reading top mark from left to right.

TAPE AND REEL INFORMATION

TAPE DIMENSIONS: HTSSOP16



REEL DIMENSIONS: HTSSOP16



Unit: mm

A	B	C	D	E	F	T1
Ø 330±1.0	12.4 $^{+1.0}_{-0.0}$	17.6 $^{+1.0}_{-0.0}$	Ø 100.0±0.5	Ø 13.0±0.2	1.9±0.4	1.9±0.2

Note:

1) All Dimensions are in Millimeter
2) Quantity of Units per Reel is 4000
3) MSL level is level 3.

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