SCALE-2™ Family
2SP0430T

Datasheet

Gate Driver for 1.2 kV and 1.7 kV PrimePACK™ 3+ Power Modules
Supporting 2-level and 3-level NPC-1 Applications

Product Highlights

Highly Integrated, Compact Footprint

- Ready-to-use gate driver solution for PrimePACK™ 3+ IGBT power modules with 1200 V and 1700 V blocking voltage
- Dual channel gate driver
- Electrical primary-side interface with reinforced isolation
- Available for 2-level and 3-level NPC-1 applications
- ±30 A peak output gate current
- 2 W output power per channel at maximum ambient temperature
- -40 °C to +85 °C operating ambient temperature

Protection and Safety Features

- Reinforced insulation between primary and secondary side
- Undervoltage lock-out (UVLO) protection for primary-side (low voltage side) and secondary-side (high voltage side)
- Short-circuit protection
- Dynamic Advanced Active Clamping (DA²C)
- Applied double sided conformal coating

Full Safety and Regulatory Compliance

- 100% production partial discharge and HIPOT test according to
  - A version: EN 50178:1997
  - B version: IEC 62109:2010
- Clearance and creepage distances requirements between primary and secondary sides according to
  - A version: IEC 62497-1:2013 and EN 50178:1997
  - B version: IEC 62109-1:2010
- Clearance and creepage distances requirements between both secondary sides according to
  - A version: EN 50178:1997
  - B version: IEC 62109-1:2010

Applications

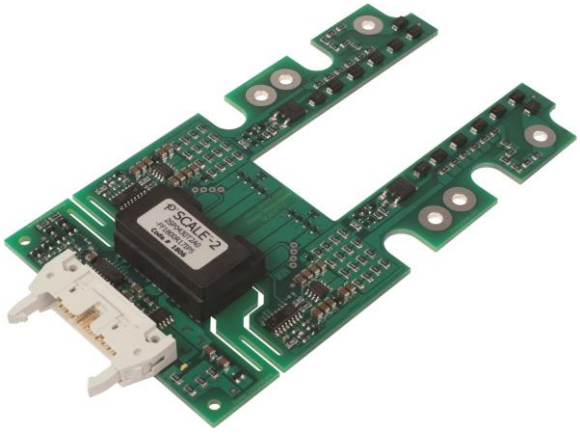
- Wind and solar power
- Traction inverter
- Industrial drives
- Other industrial applications

Description

The plug-and-play 2SP0430T gate driver family is optimized for operation of 1200 V and 1700 V PrimePACK™ 3+ IGBT power modules in 2-level and 3-level NPC-1 applications.

The gate driver features an electrical interface with 15 V logic and built-in DC/DC power supply.

Power Integrations' Dynamic Advanced Active Clamping allows an extended DC-link voltage range in IGBT off-state for up to 60 s in solar and regenerating applications (e.g. traction).



A version

B version

Figure 1. 2SP0430T Versions with Standard (A version, left) and Increased (B version, right) Isolation Test Voltage.

Product Portfolio 2SP0430T

Product	Power Module Technology	Voltage Class	Current Class	Package	Power Module Supplier
2SP0430T2A0C-FF1500R12IE5	Si-IGBT, Si-Diode	1200 V	1500 A	PrimePACK™ 3+	Infineon
2SP0430T2B0C-FF1500R12IE5	Si-IGBT, Si-Diode	1200 V	1500 A	PrimePACK™ 3+	Infineon
2SP0430T2A0C-FF1800R12IE5	Si-IGBT, Si-Diode	1200 V	1800 A	PrimePACK™ 3+	Infineon
2SP0430T2B0C-FF1800R12IE5	Si-IGBT, Si-Diode	1200 V	1800 A	PrimePACK™ 3+	Infineon
2SP0430T2A0C-FF1500R17IP5	Si-IGBT, Si-Diode	1700 V	1500 A	PrimePACK™ 3+	Infineon
2SP0430T2B0C-FF1500R17IP5	Si-IGBT, Si-Diode	1700 V	1500 A	PrimePACK™ 3+	Infineon
2SP0430T2A0C-FF1800R17IP5	Si-IGBT, Si-Diode	1700 V	1800 A	PrimePACK™ 3+	Infineon
2SP0430T2B0C-FF1800R17IP5	Si-IGBT, Si-Diode	1700 V	1800 A	PrimePACK™ 3+	Infineon

Table 1. Portfolio 2SP0430T.

Notes:

Interface Description

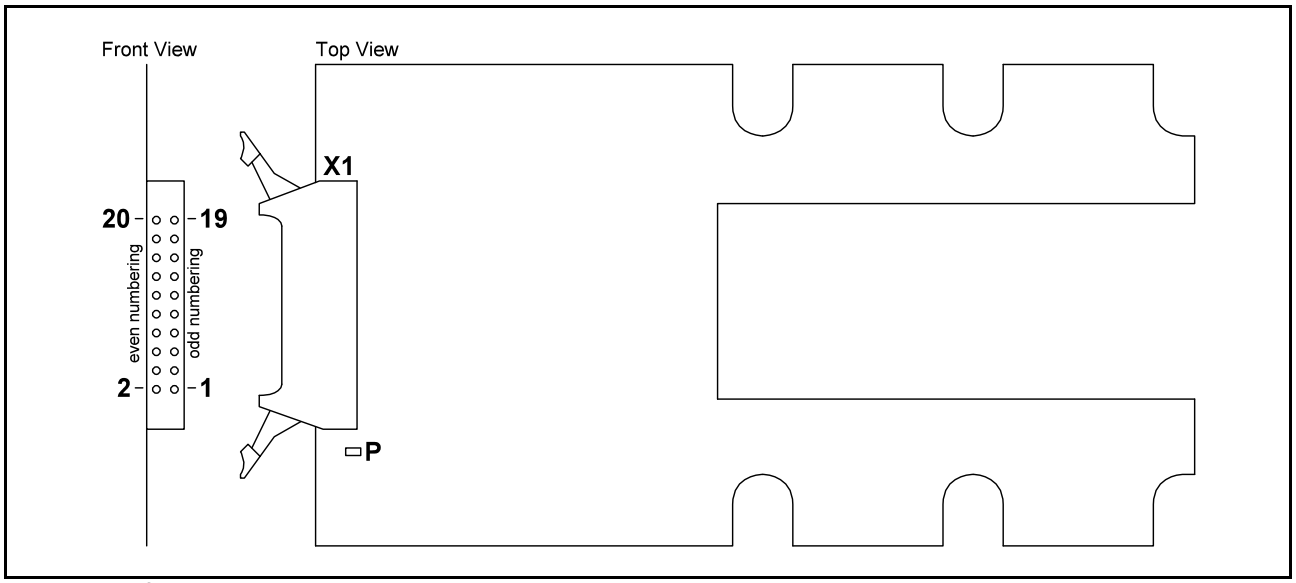


Figure 2. Interface.

Connector X1

To external system controller (DIC-20 connector).

VDC (Pin 1, 3):
These pins are the primary-side 15 V supply voltage connection for the integrated DC/DC converter. It is mandatory to use the same supply for VDC and VCC.

VCC (Pin 5, 7):
These pins are the primary-side 15 V supply voltage connection for the primary-side electronic. It is mandatory to use the same supply for VDC and VCC.

SO2 (Pin 9):
This pin is the status output for channel 2 (high-side switch).

IN2 (Pin 11):
This pin is the command input for channel 2 (high-side switch).

SO1 (Pin 13):
This pin is the status output for channel 1 (low-side switch).

IN1 (Pin 15):
This pin is the command input for channel 1 (low-side switch).

NC (Pins 17, 19):
These pins are electrically not connected.

GND (Pin 2, 4, 6, 8, 10, 12, 14, 16, 18, 20):
These pins are the connection for the primary-side ground potential. All primary-side signals refer to these pins.

Optical Indicator

P
White optical indicator for monitoring the voltage V_{VCC}. During the absence of V_{VCC} the indicator is OFF.

2SP0430T Functional Description

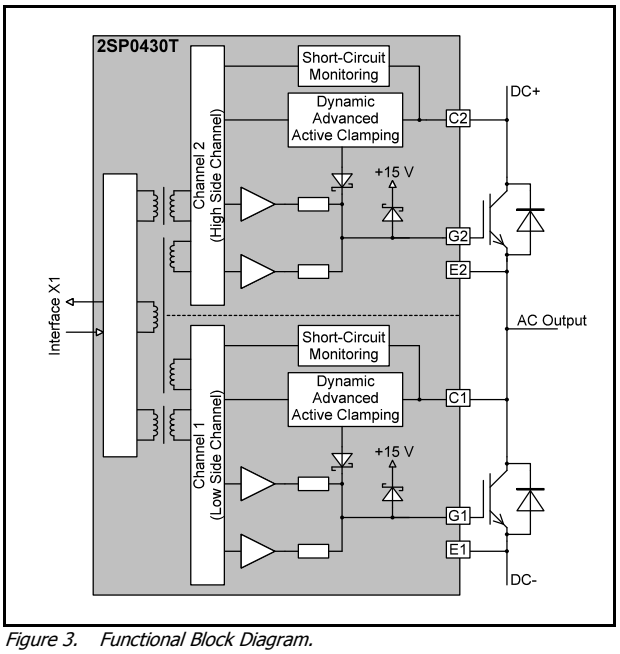


Figure 3. Functional Block Diagram.

The 2SP0430T is a dual channel plug-and-play gate driver for PrimePACK™ 3+ power modules. The gate driver is available in different variants, which all provide reinforced isolation for all primary-side signals:

- 2SP0430T2A0 for PrimePACK™ 3+ power modules. This variant features an isolation rating between primary-side and secondary-side of 5000 V_{RMS}.
- 2SP0430T2B0 for PrimePACK™ 3+ power modules. This variant features an isolation rating between primary-side and secondary-side of 9100 V_{RMS}.

As plug-and-play gate driver the 2SP0430T characteristics match the requirements of the individual power modules.

The operation of the channel 1 (low-side switch) and channel 2 (high-side switch) of the gate driver is independent from each other. Any dead time insertion, to avoid synchronous or overlapping switching of the driven power switches, has to be generated in the external system controller.

⚠ Note: Synchronous or overlapping switching of top and bottom switches within a half-bridge leg may damage or destroy the driven power switche(s) and in conjunction as secondary failure the attached gate driver.

Power Supplies

The 2SP0430T provides two power supply inputs. For both a typical supply voltage level of 15 V is required. The first input VDC supplies the integrated DC/DC converter, which generates the isolated voltage for the secondary-side gate driver channels. The positive rail of the gate driver channels has the voltage level V_{ISOx} and the negative rail the voltage level V_{COMx}. Both are referenced to the emitter potential at terminal E1 or E2 of the driven power semiconductor.

The second input VCC supplies the primary-side electronic of the gate driver. It is mandatory to provide the supply for VDC and VCC from the same source.

Under Voltage Monitoring

The supply voltages are closely monitored. In case of an under voltage condition (UVLO) a failure signal will be provided on the status output of the gate driver. If the UVLO is present on the primary-side supply V_{VCC}, both status output signals will be set to GND and all gate driver channels will be turned-off synchronously. In case of an UVLO on the secondary-side, the status signal of the respective channel will be set to GND and the corresponding power semiconductor will be turned-off.

Inputs (Primary-Side X1)

The input logic of IN1 and IN2 is designed to work with 15 V logic levels to provide sufficient signal/noise ratio. Both inputs have positive logic and are edge triggered.

Gate driver signals are transferred from the IN1 and IN2 pins to the corresponding gate with a propagation delay of $t_{P(LH)}$ for the turn-on and $t_{P(HL)}$ for the turn-off commands.

Outputs (Primary-Side X1)

The gate driver provides a status feedback SOx at pins 9 and 13. The status feedback signal stays at V_{VCC} under no-fault condition. In case of a fault, e.g. detected short-circuit of the driven power module or an under voltage lock-out (UVLO) condition on the secondary-side, the status feedback is set to GND potential for a duration of t_{blk}. In case of a primary-side UVLO condition both status feedback signals remain at GND during the UVLO and are extended by t_{blk}. During this time no gate signals will be transmitted to the respective gate driver channel.

Screw Terminals

The gate driver is mounted on top of the power module and fixed by screws. Details are given in the section Mounting Instruction.

Gate Voltage

2SP0430T possesses a voltage regulator for the positive (turn-on) rail of the gate voltage. Internal current sources are regulating actively the positive gate-emitter voltage independently of actual load conditions within the maximum specified ratings. Therefore, the on-state gate-emitter voltage of the power semiconductor equals in steady state the positive supply voltage V_{ISO}.

The off-state gate-emitter voltage $V_{GE(off)}$ equals in steady state the voltage V_{COM}. This voltage is load dependent. It has its lowest value under no load conditions and is increasing slightly (i.e. getting less negative) with increasing load.

In the event of an under voltage lock-out condition the gate driver changes the control of the positive rail towards control of the negative rail V_{COM}. By this potential parasitic turn-on events of the power semiconductor are avoided.

Short-Circuit Protection

The gate driver uses the semiconductor desaturation effect to detect short-circuits. The desaturation is monitored by using a resistor sensing network. The collector-emitter voltage is checked after the response time t_{res} at turn-on to detect a short circuit. If the voltage is higher than the programmed threshold voltage $V_{CE(stat)}$, the driver detects a

short-circuit condition. The monitored semiconductor is switched off immediately and a fault signal is transmitted to the primary-side status output SOx (pin 9 and/or pin 13) after a delay t_{SOx}.

The fault feedback is automatically reset after the blocking time t_{blk}. The semiconductor is turned-on again as soon as the next positive edge is applied to the respective inputs IN1 or IN2 after the fault status has disappeared.

It should be noted that the response time t_{res} is dependent on the DC-link voltage. It remains constant over a wide range of the higher DC-link voltage range and increases at lower DC-link voltages.

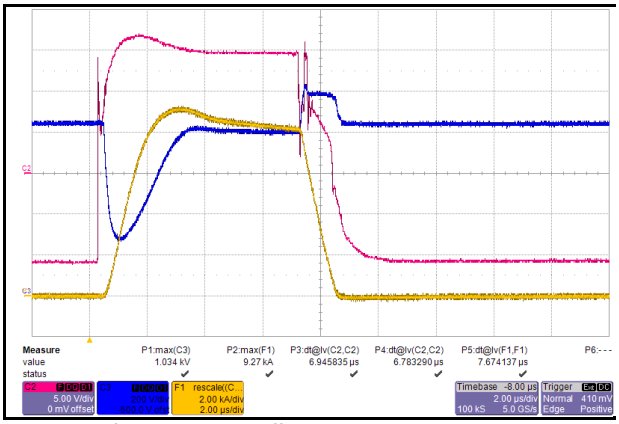


Figure 4. Short-Ciruict Turn-Off.

⚠ Note: The desaturation function is for short-circuit detection only and cannot provide overcurrent protection. However, overcurrent detection has a lower time priority and can be easily provided by the application.

Gate Clamping

In the event of a short-circuit condition the gate voltage is increased due to the high dv/dt between the collector and emitter terminals of the driven power semiconductor. This dv/dt is driving a current through the Miller-capacitance (capacitance between the gate and collector) and charges the gate capacitance, which eventually leads to a gate-emitter voltage larger than the nominal gate-emitter turn-on voltage. In consequence, the short-circuit current is increased due to the transconductance of the power semiconductor.

To ensure that the gate-emitter voltage stays close to the nominal turn-on voltage the gate driver features a gate-clamping circuitry. The gate clamping provides a voltage similar to V_{VISO} to the gate, i.e. 15 V. As the effective short-circuit current is a function of the gate-emitter voltage the short-circuit current is limited. This is shown in Figure 4 where the gate-emitter voltage and in consequence the short-circuit current is kept at a flat plateau. As a result the energy dissipated in the power semiconductor during the short-circuit event is reduced, leading to a junction temperature within the short-circuit safe operating area (SCSOA) limits and enables a safe turn-off of the device.

Dynamic Advanced Active Clamping (DA²C)

Active clamping is a technique designed to partially turn on the IGBT in case the collector-emitter voltage exceeds a predefined threshold. The IGBT is then kept in linear operation. Basic active clamping topologies implement a single feedback path from the IGBT's collector through transient voltage suppressor (TVS) diodes to the IGBT gate. The 2SP0430T gate driver contains Power Integrations' Dynamic Advanced Active Clamping (DA²C) based on this principle:

When active clamping is activated, the turn-off MOSFET of the gate driver is switched off in order to improve the effectiveness of the active clamping and to reduce the losses in the TVS diodes. This feature – called Advanced Active Clamping – is mainly integrated in the secondary-side ASIC of the gate driver.

Additional TVS diodes have been added in series to the TVS diodes required to withstand the maximum DC-link voltage under switching operation. These TVS diodes are short-circuited during the IGBT on state as well as for about 15…20µs after the turn-off command to guarantee efficient active clamping. After this delay, these additional TVS diodes are activated and allow the DC-link voltage to be increased to a higher value during the IGBT off-state. This feature – together with Advanced Active Clamping – is called Dynamic Advanced Active Clamping (DA²C). Note that the time during which the voltage can be applied above the value for switching operation should be limited to short periods (<60s).

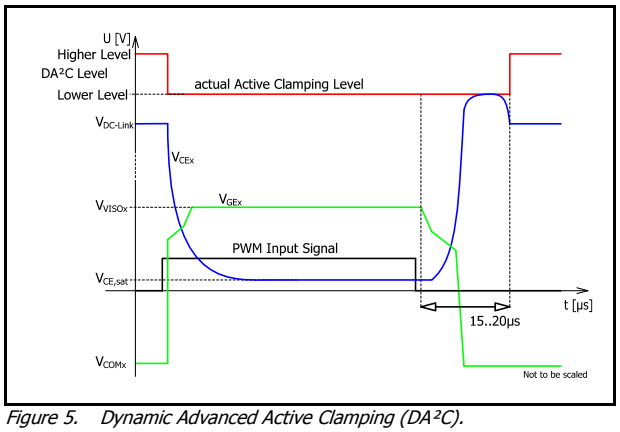


Figure 5. Dynamic Advanced Active Clamping (DA²C).

Optical Indicator

The gate driver as one optical indicator. The white LED (P in Figure 2) monitors the voltage V_{VCC}.

Absolute Maximum Ratings – all 2SP0430T versions if not otherwise specified

Parameters	Symbol	Conditions T_A = -40 °C to 85 °C		Min	Max	Unit
Absolute Maximum Ratings[1]						
Primary-side supply voltage	V_{VDC}	VDC and VCC must be applied in parallel to GND		0	16	V
	V_{VCC}			0	16	
Primary-side supply current	I_{VDC}	Average supply current at full load			480	mA
	I_{VCC}	Average supply current at full load			45	
Logic input voltage (command signal)[2]	V_{INx}	INx to GND, low-state		0	4	V
		INx to GND, high-state		12.6	V_{VCC} + 0.5	V
Logic output voltage (status signal)	V_{SOx}	SOx to GND		0	V_{VCC} + 0.5	V
Gate output power per channel	P_{gx}				2	W
Test voltage primary-side to secondary-side	$V_{iso,ps}$	A versions[3]	50 Hz, 60 s		5000	V_{RMS}
		B versions[3]			9100	V_{RMS}
Test voltage secondary-side to secondary-side	$V_{iso,ss}$	A versions[3]	50 Hz, 60 s		4000	V_{RMS}
		B versions[3]			6000	V_{RMS}
Operating voltage primary-side to secondary-side	V_{op}	A versions[3]	Transient only		1700	V_{pk}
			Permanently applied		1250	V_{DC}
		B versions[3]	Transient only		2050	V_{pk}
			Permanently applied		1500	V_{DC}
DC-link voltage	$V_{DC\text{-}Link}$	1200 V versions	Switching operation		850	V_{pk}
			Off-state, limited to 60 s		1100	V_{DC}
		1700 V versions	Switching operation		1250	V_{pk}
			Off-state, limited to 60 s		1500	V_{DC}
Common-mode transient immunity	|dv/dt|				50	kV/µs
Storage temperature[4]	T_{st}			-40	50	°C
Operating ambient temperature	T_A			-40	85	°C
Surface temperature[5]	T				125	°C
Relative humidity	H_r	No condensation			93	%
Altitude of operation[6]	A_{op}				2000	m

Notes:

1. ⚠ Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device.
2. INx signals must statically be within the given limits. The transition from low-state to high-state and vice-versa must happen within 1µs.
3. Refer to section Part Ordering Information.
4. The storage temperature inside the original package or in case the coating material of coated products may touch external parts must be limited to the given value. Otherwise, it is limited to 85°C.
5. The component surface temperature, which may strongly vary depending on the actual operating conditions, must be limited to the given value for coated gate driver versions to ensure long-term reliability of the coating material.
6. Operation above this level requires a voltage derating to ensure proper isolation coordination.

Recommended Operating Conditions – all 2SP0430T versions

Parameter	Symbol	Conditions T_A = -40 °C to 85 °C	Min	Typ	Max	Unit
Power Supply						
Primary-Side Supply Voltage	V_{VDD}	VDC to GND	14.5	15	15.5	V
	V_{VCC}	VCC to GND	14.5	15	15.5	

Characteristics – all 2SP0430T versions if not otherwised specified

Parameter	Symbol	Conditions T_A = 25 °C		Min	Typ	Max	Unit
Power Supply							
Supply current	I_{VDC}	A versions[7]	V_{VDC} = V_{VCC} = 15 V, without load		32		mA
		B versions[7]			65		
		A versions[7]	V_{VDC} = V_{VCC} = 15 V, f_{SW} = 10 kHz, P_{gx} = 2W, 50 % duty cycle		344		mA
		B versions[7]			384		
	I_{VCC}	A versions[7]	V_{VDC} = V_{VCC} = 15 V, f_{SW} = 0…10 kHz		37		mA
		B versions[7]	V_{VDC} = V_{VCC} = 15 V, f_{SW} = 0…10 kHz		32		mA
Power supply monitoring threshold (primary-side)	$UVLO_{VCC}$	Referenced to GND	Clear fault (resume operation)	11.6	12.6	13.6	V
			Set fault (suspend operation)	11.0	12.0	13.0	V
			Hysteresis	0.35			V
Power supply monitoring threshold (secondary-side)	$UVLO_{VISOx}$	Referenced to respective terminal E1 or E2	Clear fault (resume operation)	11.6	12.6	13.6	V
			Set fault (suspend operation)	11.0	12.0	13.0	V
			Hysteresis	0.35			V
	$UVLO_{COMx}$		Clear fault (resume operation)		-5.15		V
			Set fault (suspend operation)		-4.85		V
			Hysteresis		0.3		V
Output voltage (secondary-side)	V_{VISOx}	A versions[7]	V_{VDC} = V_{VCC} = 15 V Referenced to V_{COMx}, without load		25.9		V
		B versions[7]			24.6		
		A versions[7]	V_{VDC} = V_{VCC} = 15 V Referenced to V_{COMx}, f_{SW} = 10 kHz, P_{gx} = 2W, 50 % duty cycle		24.8		V
		B versions[7]			24.0		
Coupling capacitance	C_{io}	A versions[7]	Primary-side to secondary-side, total per channel		22		pF
		B versions[7]			19		
Logic Inputs and Status Outputs							
Input impedance	R_{INx}			4.4	4.5	4.6	kΩ
Turn-on threshold	$V_{th\text{-}on,INx}$	INx to GND			10.1		V
Turn-off threshold	$V_{th\text{-}off,INx}$	INx to GND			6.4		V
Status output voltage[8]	V_{SOx}	SOx to GND , I_{SOX} < 0.5 mA, no-fault condition		11			V

Notes:

7. Refer to section Part Ordering Information.
8. Internal 4.7 kΩ pull-up resistor is connected to VCC.

Parameter	Symbol	Conditions T_A = 25 °C		Min	Typ	Max	Unit
Timing Characteristics							
Turn-on delay	$t_{P(LH)}$	$V_{th\text{-}on,INx}$ to 50% of $V_{GE(on)}$, no load attached			215		ns
Turn-off delay	$t_{P(LH)}$	$V_{th\text{-}off,INx}$ to 50% of $V_{GE(off)}$, no load attached			145		ns
Transmission delay of fault state	t_{SOX}				450		ns
Blocking time	t_{blk}				98		ms
Gate Output							
Gate turn-on voltage	$V_{GE(on)}$	V_{VDC} = V_{VCC} = 15 V, without load, referenced to terminal E1 or E2			15		V
		V_{VDC} = V_{VCC} = 15 V, f_{SW} = 10 kHz, 50 % duty cycle referenced to terminal E1 or E2			15		
Gate turn-off voltage	$V_{GE(off)}$	A versions[9]	V_{VDC} = V_{VCC} = 15 V Referenced to resp. terminal E1 or E2, without load		-10.9		V
		B versions[9]			-9.6		
		A versions[9]	V_{VDC} = V_{VCC} = 15 V Referenced to resp. terminal E1 or E2, f_{SW} = 10 kHz, P_{gx} = 2W, 50 % duty cycle		-9.8		V
		B versions[9]			-9.0		
Short-Circuit Protection							
Static VCE-monitoring threshold	$V_{CE(stat)}$	1200 V versions			47		V
		1700 V versions			54		
Response time 1200 V versions	t_{res}	10% to 90% of V_{GE}	DC-link voltage = 850 V		6.8		µs
			DC-link voltage = 600 V		7.5		
			DC-link voltage = 500 V		8		
			DC-link voltage = 400 V		9.3		
Response time 1700 V versions			DC-link voltage = 1250 V		7		
			DC-link voltage = 1000 V		7.1		
			DC-link voltage = 800 V		7.4		
			DC-link voltage = 600 V		8.2		
Delay to turn-off power semiconductor after short-circuit detection	$t_{pd,SOx}$				0.2		µs

Notes:

9. Refer to section Part Ordering Information.

Parameter	Symbol	Conditions T_A = 25 °C		Min	Typ	Max	Unit
Electrical Isolation							
Test voltage[10]	$V_{iso,ps}$	A versions[9]	Primary-side to secondary-side	5000			V_{RMS}
		B versions[9]		9100			
	$V_{iso,ss}$	A versions[9]	Secondary-side to secondary-side	4000			V_{RMS}
		B versions[9]		6000			
Partial discharge extinction voltage[11]	$P_{D,ps}$	A versions[9]	Primary-side to secondary-side	1768			V_{pk}
		B versions[9]		3100			
	$P_{D,ss}$	A versions[9]	Secondary-side to secondary-side	1700			V_{pk}
		B versions[9]		2100			
Creepage distance	CPG_{P-S}	Primary-side to secondary-side		30			mm
	CPG_{S-S}	Secondary-side to secondary-side		7			mm
Clearance distance	CLR_{P-S}	Primary-side to secondary-side		12.6			mm
	CLR_{S-S}	Secondary-side to secondary-side		7			mm
Mounting							
Terminal connection torque	M_{M4}	Screw M4		1.8		2.1	Nm
Terminal diameter[12]	d_{M3}	Terminals S1 and S2				8.8	mm
	d_{M4}	Terminals Gx, Ex, and Cx				9.8	mm
Bending[13]	I_{bend}	According to IPC				0.75	%

Notes:

10. The transformer of every production sample has undergone 100% testing at the given value for 1s.
11. Partial discharge measurement is performed on each transformer
12. This refers to the double value of the maximum radius from hole center to the next metallic part (d_{M3}) resp. to the end of the metallic pad (d_{M4}).
13. Refer to section Mounting Instruction for absolute values of allowed bending distances.

Gate parameters – 2SP0430T2A0C-FF1500R12IE5 and 2SP0430T2B0C-FF1500R12IE5

Parameter	Symbol	Conditions T_A = 25 °C	Min	Typ	Max	Unit
Gate Output						
Turn-on gate resistor	$R_{G(on)}$			0.85		Ω
Turn-off gate resistor	$R_{G(off)}$			3.375		Ω
Auxiliary gate capacitor	C_{GE}			n.a.		nF
Switching Frequency	f_{SW}			10		kHz

Gate parameters – 2SP0430T2A0C-FF1800R12IE5 and 2SP0430T2B0C-FF1800R12IE5

Parameter	Symbol	Conditions T_A = 25 °C	Min	Typ	Max	Unit
Gate Output						
Turn-on gate resistor	$R_{G(on)}$			0.85		Ω
Turn-off gate resistor	$R_{G(off)}$			3.375		Ω
Auxiliary gate capacitor	C_{GE}			n.a.		nF
Switching Frequency	f_{SW}			10		kHz

Gate parameters – 2SP0430T2A0C-FF1500R17IP5 and 2SP0430T2B0C-FF1500R17IP5

Parameter	Symbol	Conditions T_A = 25 °C	Min	Typ	Max	Unit
Gate Output						
Turn-on gate resistor	$R_{G(on)}$			0.5875		Ω
Turn-off gate resistor	$R_{G(off)}$			7		Ω
Auxiliary gate capacitor	C_{GE}			n.a.		nF
Switching Frequency	f_{SW}			10		kHz

Gate parameters – 2SP0430T2A0C-FF1800R17IP5 and 2SP0430T2B0C-FF1800R17IP5

Parameter	Symbol	Conditions T_A = 25 °C	Min	Typ	Max	Unit
Gate Output						
Turn-on gate resistor	$R_{G(on)}$			0.5875		Ω
Turn-off gate resistor	$R_{G(off)}$			5.875		Ω
Auxiliary gate capacitor	C_{GE}			n.a.		nF
Switching Frequency	f_{SW}			10		kHz

Mounting Instruction

2SP0430T

The gate driver is mounted on top of the target power module with six screws to the gate, emitter, and collector terminals (Figure 6). The mounting force is given with M_{M4}. The given value refers to the mechanical property of the gate driver only. M_{M4} must not exceed the values given in the respective datasheet of the target power module. Hence, actual mounting torque may be smaller than M_{M4}.

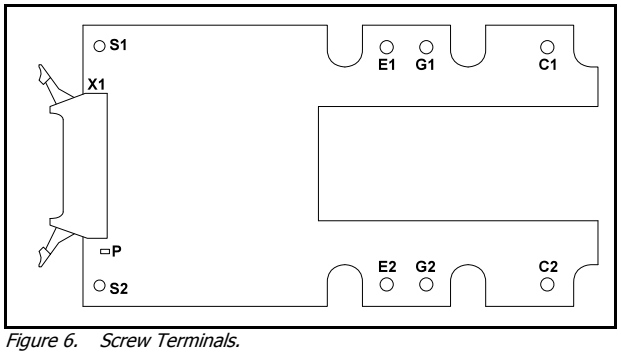


Figure 6. Screw Terminals.

⚠ To maintain the electrical isolation distances, the screw header including any washer must not exceed the available metallic terminal pad of the gate driver. For the terminals G1, E1, C1, G2, E2, and C2 the corresponding distances are given with d_{M4}.

To avoid mechanical stress of the gate driver during and after the mounting process any bending or warping force imposed to the gate driver must not lead to a vaulting or twisting of the housing of more than 0.75 % per axis according to Figure 7:

- Axis 1 and 2: max. 0.9 mm bending
- Axis 3: max. 0.7 mm bending
- Axis 4 and 5: max. 1.2 mm bending

The 2SP0430T possesses two fixation points S1 and S2 (Figure 6) for stand-offs to mitigate any bending force during assembly and operation. The stand-off could be mounted on the heatsink or the frame of the inverter system. The maximum diameter of the screw header and washer for the stand-offs are limited by d_{M3}.

⚠ Note: The stand-offs have to be made of insulating material to avoid any conducting path from the gate driver to the heatsink or inverter frame.

In Figure 8 the minimum required space in front of the power module for mounting the 2SP0430T is given with 88.8 mm. This distance includes also the space for connector X1 with mounted cable. Further dimensions are given in section Product Dimensions.

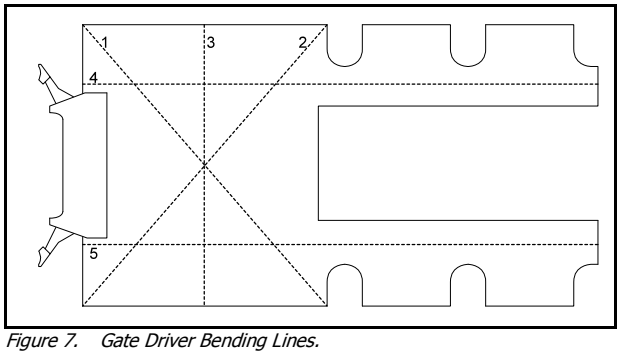


Figure 7. Gate Driver Bending Lines.

To ensure proper cooling by natural or forced convection minimum clearance of 50 mm of the gate driver top side is required as shown in Figure 8. This includes also that the AC and/or DC bus bars are not covering parts or the entire gate driver top side (red circled area in Figure 8).

Cables

⚠ The cable from gate driver connector X1 to the system level controller is not part of the 2SP0430T gate driver and has to be provided by the designer of the system. It is recommended to route the cable with minimum parasitic coupling from the controller to the gate driver. Parasitic coupling in particular to any potential of the secondary-side of the gate driver (i.e. high voltage side) and the AC and/or DC bus bar has to be avoided. Otherwise, increased common-mode currents may circulate, which may cause interferences with command, measurement and/or status feedback signals. Furthermore, usage of pair-wise twisted cables is recommended.

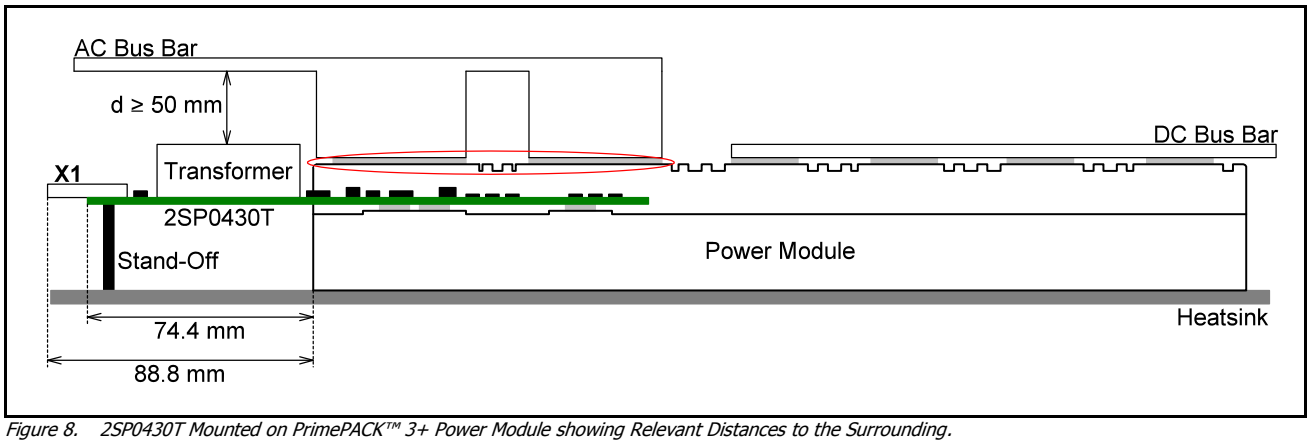


Figure 8. 2SP0430T Mounted on PrimePACK™ 3+ Power Module showing Relevant Distances to the Surrounding.

Application Guidelines

The following guidelines are meant to optimize the overall system performance when using 2SP0430T gate drivers in various applications.

Power Supply

The gate driver has to be supplied by a fixed voltage of typically 15V at VDC and VCC. It is mandatory that one supply is used for both terminals.

DC-Link Design

The mechanical and electrical design of the DC-link of the target application determines during turn-off events of the driven power semiconductor the over voltages ΔV_{CE} according to equation (1). Here, L_σ describes the overall DC-link stray inductance (i.e. sum stray inductance of DC-capacitors, DC-link bus bar and power module) and di_C/dt the collector current change.

$$\Delta V = L_\sigma \cdot \frac{di_C}{dt} \qquad (1)$$

If the over voltage ΔV_{CE} plus the applied DC-link voltage V_{DC} exceed the breakdown voltage of the driven power module (refer to the reverse bias safe operating area RBSOA), the power module may be damaged. In case of excessive turn-off over voltages, one or more of the following application parameters have to be decreased:

- DC-link voltage V_{DC}
- Stray inductance L_σ
- Collector current i_C

Therefore, during the installation and testing of the target application the actual over voltages ΔV_{CE} at different conditions have to be measured.

Note: 2SP0430T gate driver will actively limit any over voltage during turn-off events under normal and over current conditions to safe levels using the implemented Dynamic Advanced Active Clamping scheme. However, it is not recommened that the clamping feature is active during normal switching conditions. It may lead to an over load of the implemented clamping devices. Furthermore, it might lead to an under voltage lock-out (UVLO) condition on the secondary-side power supply of the gate driver.

Paralleling of Power Modules

Paralleling of PrimePACK™ 3+ power modules with 2SP0430T gate driver is in principle possible if the following basic rules are obeyed to ensure minimum load current imbalances and general proper system operation.

The load current sharing between paralleled power modules depends on several factors:

- Deviation of the power modules parameters like IGBT saturation voltage V_{CEsat}, diode forward voltage V_F, rise and fall times t_r and t_f, turn-on and turn-off delay times $t_{d(on)}$ and $t_{d(off)}$. They are influencing the current sharing in the conducting (static) and switching (dynamic) phase.
- Deviation in the cooling of the power modules. The before mentioned parameters are mostly temperature dependent. Inhomogeneous cooling of paralleled power modules influences therefore the static and dynamic current sharing.
- Deviation of the gate loop impedance. It leads to static and dynamic current imbalances.
- Deviation of the apparent DC-link stray inductance and resistance per paralleled power module. It leads to static and dynamic current imbalances.

Power module parameter deviations can be addressed by screening of power modules as offered by some manufacturers. The deviation in cooling can be compensated to a fair degree by the inherent positive temperature coefficient of the power modules. In case one power module takes over more current than the other power modules, it will heat-up more than the others. As a result the saturation voltage is increased, which leads to a reduction of the current in the power module. The system is self-regulated to a certain extent.

Deviations of the gate loop impedances are minimized by design, process and assembly control of 2SP0430T. Part of the gate loop impedance is also the terminal screw connection of the gate driver towards the power module. Here the recommended (i.e. maximum) mounting torque must be obeyed to minimize its influence.

Deviation of the apparent DC-link stray inductance and resistance between paralleled power modules refers to the mechanical arrangement of the power modules and DC-link.

Depending on the actual application conditions is might be required to add inductors in the AC output phases of each paralleled power module to symmetrize load current imbalance.

Note: Do not operate paralleled power modules without connected gate driver. This may lead to half-bridge short-circuits within the power modules and will eventually destroy them.

Multilevel Topologies

2SP0430T gate driver are designed for 2-level and 3-level topologies. For 3-level topologies:

- Cascaded multilevel topologies on system level like for instance Modular Multilevel Converter (MMC) operating with 2-level topologies within one cell are supported without any restriction (implying that required isolation requirements are fulfilled).
- For 3-level systems the turn-off sequence has to be obeyed by the system controller to avoid overvoltage events, which might lead to an RBSOA (reverse biased safe operating area) violation of the power module. However, 2SP0430T gate driver have Power Integrations' Dynamic Advanced Active Clamping (DA²C) implemented, which enables the gate driver to protect the power modules against over voltage conditions arising by wrong turn-off sequences. The suitability of DA²C has to be checked within the target application.

  Note: During short-circuit and/or under voltage events, the gate driver will immediately switch-off the respective power module. No control on the turn-off

sequence is given. Therefore, the suitability of 2SP0430T has to be checked on application level for this kind of topology.

Conformal Coating

The electronic components of the 2SP0430T gate driver are protected with a layer of acrylic conformal coating using ELPEGUARD SL 1307 FLZ/2 from Lackwerke Peters on both sides of the PCB. This coating layer increases the product reliability when exposed to contaminated environments. Nevertheless, standing water (e.g. condensate water) on top of the coating layer is not allowed as this water will diffuse over time through the layer. Eventually it will form a thin film of conducting nature between PCB surface and coating layer, which will cause leakage currents. Such currents may lead to a disturbance of the performance of the 2SP0430T gate driver.

Product Dimensions

2SP0430T2A0C all versions

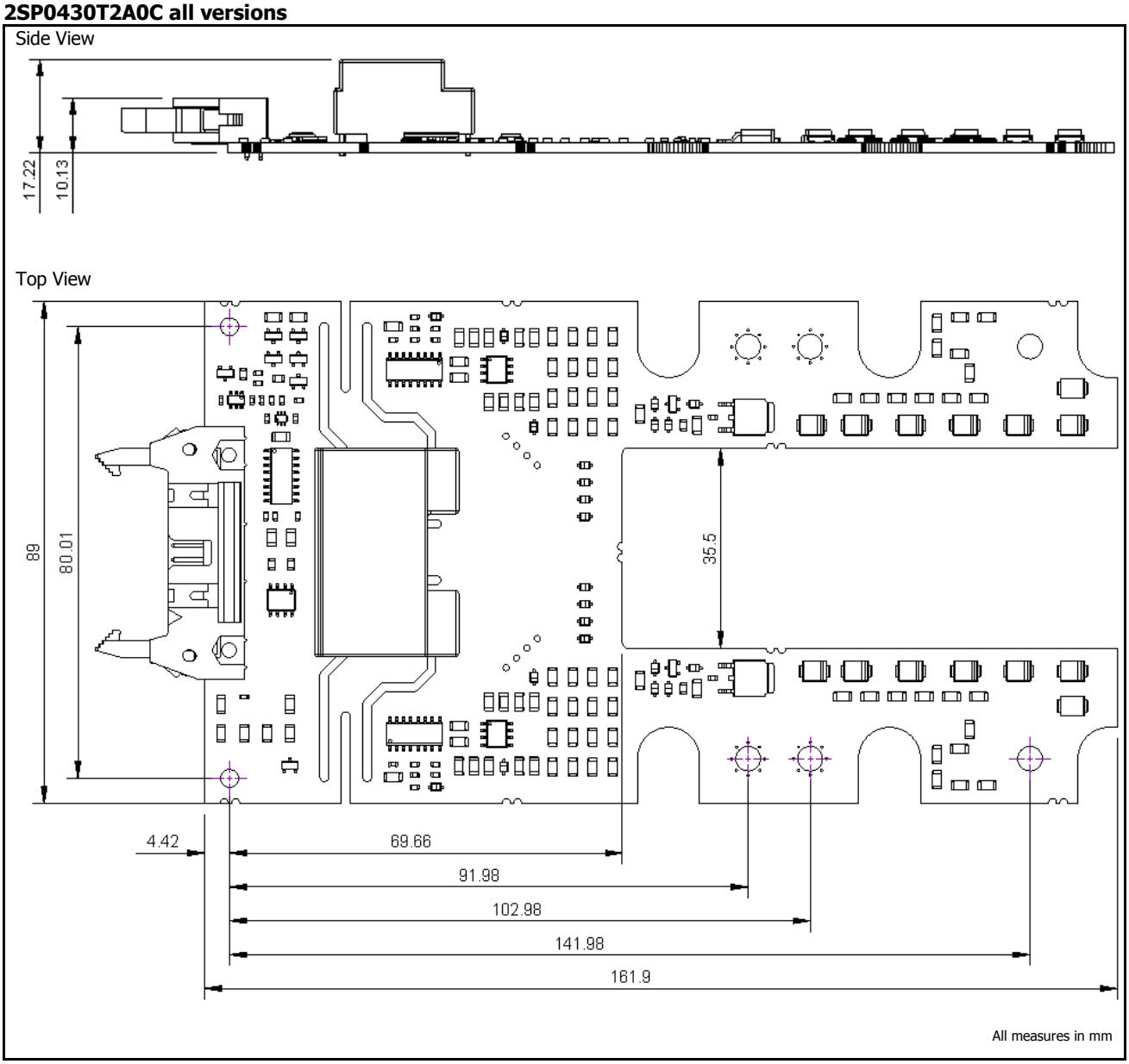


Figure 9. Dimensions.

2SP0430T2B0C all versions

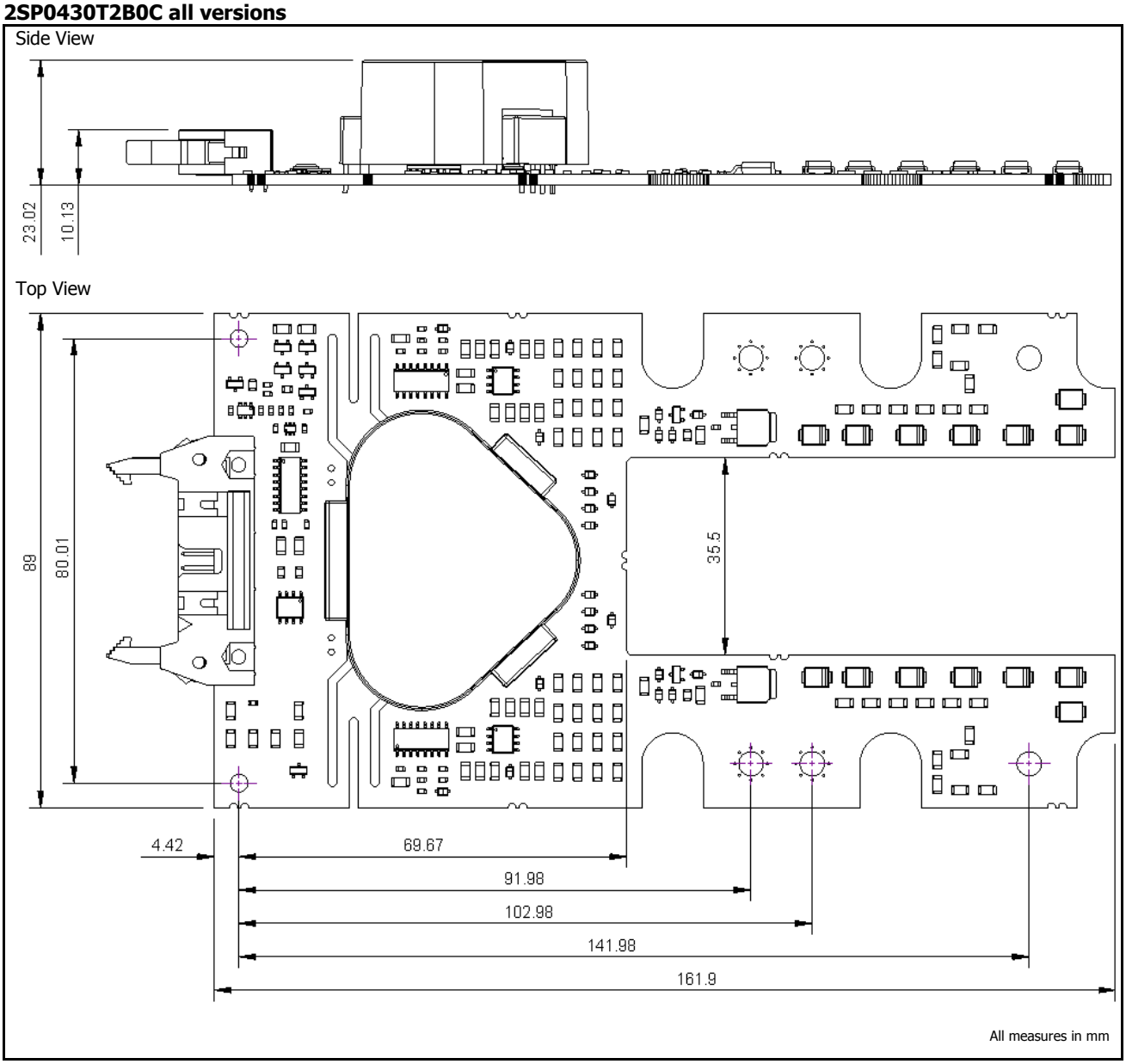


Figure 10. Dimensions.

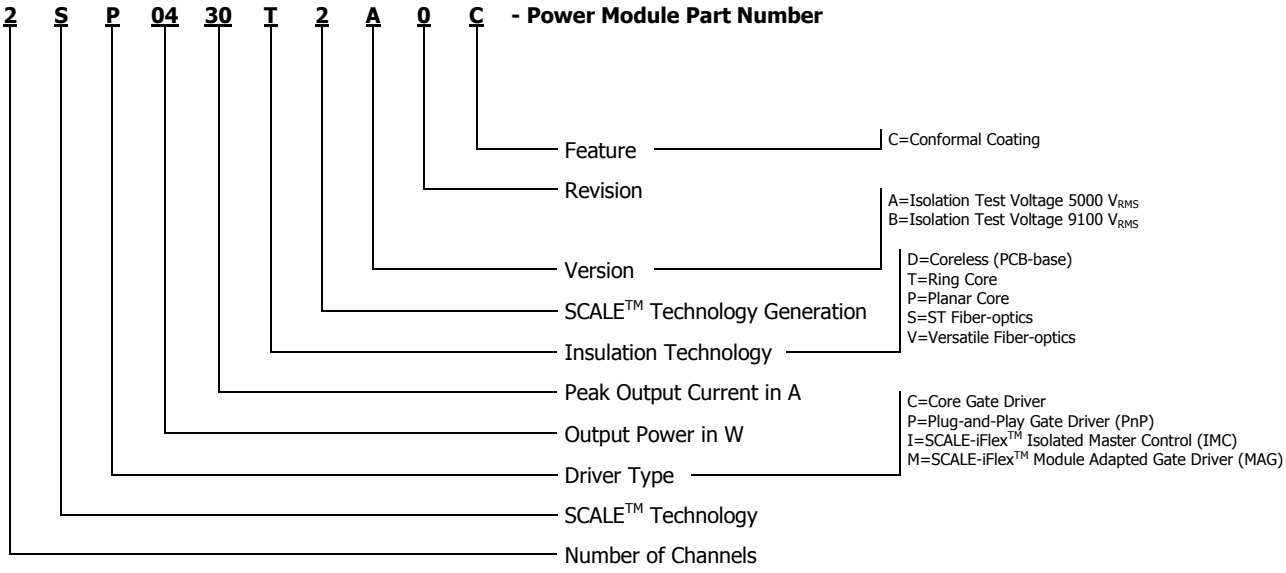
Transportation and Storage Conditions

For transportation and storage conditions refer to Power Integrations' Application Note AN-1501.

RoHS Statement

On the basis of Annexes II and III of European Directive 2011/65/EC of 008 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS), we hereby state that the products described in this datasheet do not contain lead (Pb), mercury (Hg), hexavalent chromium (Cr VI), cadmium (Cd), polibrometo of bipenyl (PBB) or polibrometo diphenyl ether (PBDE) in concentrations exceeding the restrictions set forth in Annex II of 2011/65/EC with due consideration of the applicable exemptions as listed in Annex III of 2011/65/EC.

Part Ordering Information



Revision	Notes	Date
A	Target Datasheet, initial version	10/18

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