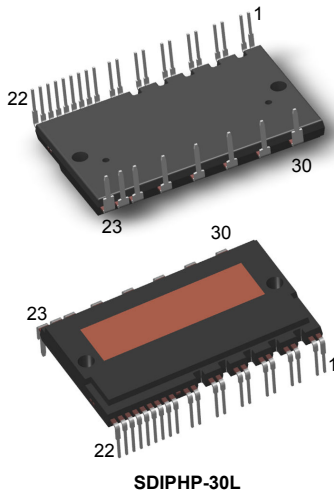


## SLLIMM high power IPM, 3-phase inverter, 10 A, 1200 V short-circuit rugged IGBT



### Product status link

[STGIK10M120T](#)

### Product summary

<b>Order code</b>	STGIK10M120T
<b>Marking</b>	GIK10M120T
<b>Package</b>	SDIPHP-30L
<b>Packing</b>	Tube

### Features

- IPM 1200 V, 10 A 3-phase inverter bridge including control ICs for gates driving
- 3.3 V, 5 V TTL/CMOS inputs with hysteresis
- Undervoltage lockout of gate drivers
- Built-in bootstrap diodes
- Short-circuit protection
- Shutdown input/fault output
- Separate open emitter outputs
- Comparator for fault protection
- Short-circuit rugged
- Very fast, soft recovery diodes
- Fully isolated package
- Isolation rating of 2500 Vrms/min
- 100 kΩ NTC for temperature monitoring
- UL recognition: UL 1557, file E81734

### Application

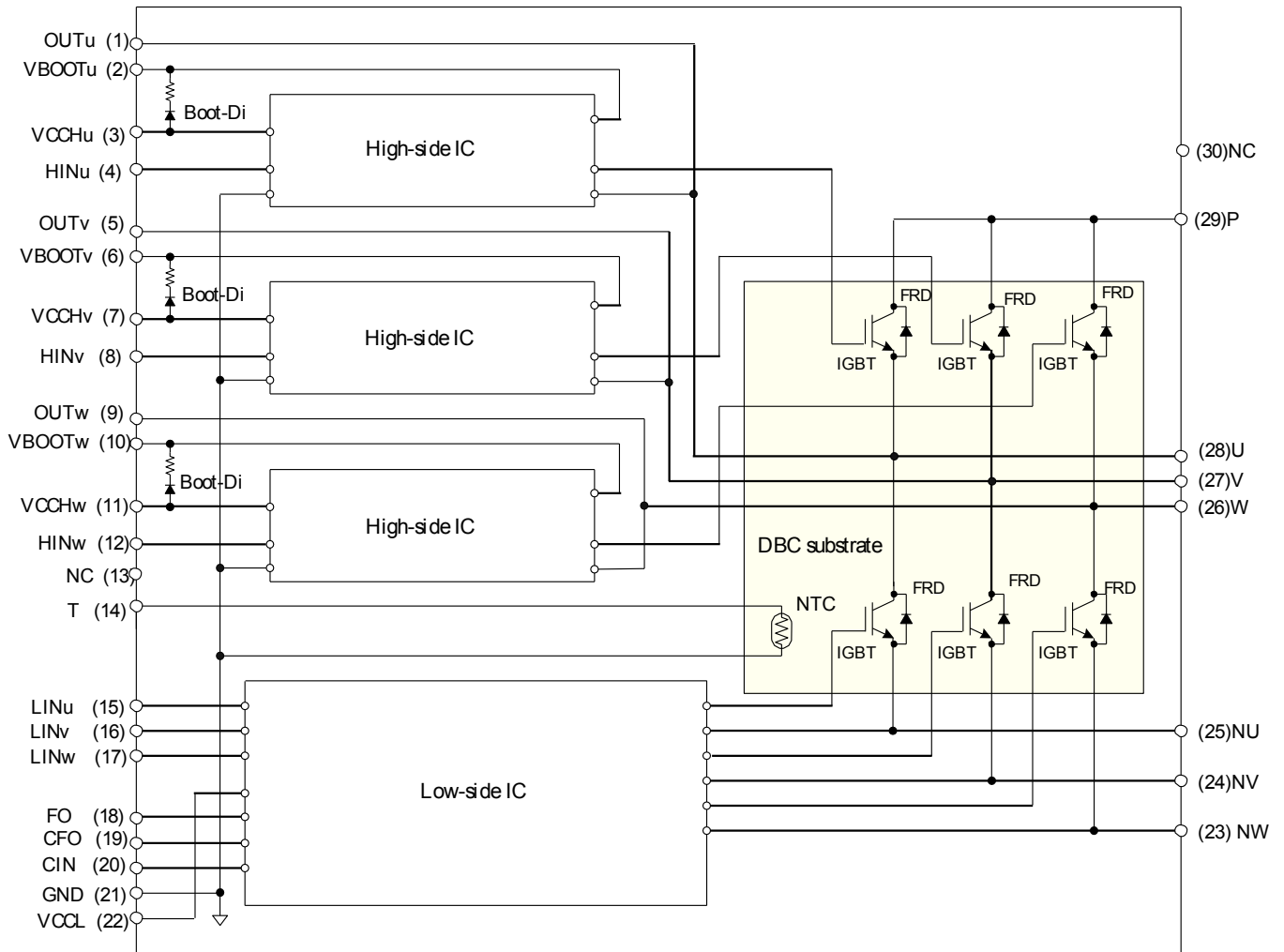
- HVAC
- GPI
- Servo motor
- Pumps and compressors

### Description

This new IPM (intelligent power module) is part of the high power SLLIMM (small low-loss intelligent molded module) family and provides a compact, high-performance AC motor drive in a simple, rugged design. It combines driver control with improved short-circuit rugged 1200 V trench gate field-stop IGBTs, resulting ideal for 3-phase inverters motor drives.

# 1 Internal schematic and pin description

Figure 1. Internal schematic diagram and pin configuration



GADG150720221015GT

**Table 1. Pin description**

Pin	Symbol	Description
1	OUTu	High-side reference output for U phase
2	VBOOTu	Bootstrap voltage for U phase
3	VCCHu	High-side voltage power supply for U phase
4	HINu	High-side logic input for U phase
5	OUTv	High-side reference output for V phase
6	VBOOTv	Bootstrap voltage for V phase
7	VCCHv	High-side voltage power supply for V phase
8	HINv	High-side logic input for V phase
9	OUTw	High-side reference output for W phase
10	VBOOTw	Bootstrap voltage for W phase
11	VCCHw	High-side voltage power supply for W phase
12	HINw	High-side logic input for W phase
13	NC	Not connected (cut pin)
14	T	NTC thermistor output
15	LINu	Low-side logic input for U phase
16	LINv	Low-side logic input for V phase
17	LINw	Low-side logic input for W phase
18	FO	Shutdown/fault output
19	CFO	Capacitor for fault output setting
20	CIN	Comparator input
21	GND	Ground
22	VCCL	Low-side voltage power supply
23	NW	Negative DC input for W phase
24	NV	Negative DC input for V phase
25	NU	Negative DC input for U phase
26	W	W phase output
27	V	V phase output
28	U	U phase output
29	P	Positive DC input
30	NC	Not connected

## 2 Absolute maximum ratings

$T_J = 25\text{ °C}$  unless otherwise noted.

**Table 2. Inverter parts**

Symbol	Parameter	Value	Unit
$V_{PN}$	Supply voltage between P - $N_U$ , - $N_V$ , - $N_W$	900	V
$V_{PN(surge)}$	Supply voltage (surge) between P - $N_U$ , - $N_V$ , - $N_W$	1000	V
$V_{CES}$	Collector-emitter voltage each IGBT	1200	V
$I_C$	Continuous collector current each IGBT	10	A
$I_{CP}$	Peak collector current each IGBT (less than 1 ms)	20	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ °C}$ each IGBT	125	W
$V_{PN(SP)}$	Self-protection supply voltage limit, $V_{CC} = 13.5 - 16.5\text{ V}$ , $T_J = 150\text{ °C}$ , non-repetitive, less than 2 $\mu\text{s}$	800	V

**Table 3. Control parts**

Symbol	Parameter	Min.	Max.	Unit
$V_{CC}$	Supply voltage applied between $V_{CCHx}$ -GND, $V_{CCL}$ -GND	- 0.5	25	V
$V_{BOOT}$	Bootstrap voltage	- 0.5	25	V
$V_{OUT}$	Output voltage applied between $OUTx$ and GND	- 0.5	1200	V
$V_{CIN}$	Comparator input voltage	- 0.5	$V_{CCL}+0.3$	V
$V_{INH}$	Logic input voltage applied between $H_{INx}$ and GND	- 0.5	$V_{CCHx}+0.3$	V
$V_{INL}$	Logic input voltage applied between $L_{INx}$ and GND	- 0.5	$V_{CCL}+0.3$	V
$V_{FO}$	Fault output voltage	- 0.5	$V_{CCL}+0.3$	V
$I_{FO}$	Fault output sink current		1	mA
$\Delta V_{CC}/\Delta t$	Change rate of $V_{CC}$ supply voltage time	-1	1	V/ $\mu\text{s}$

**Table 4. Bootstrap diode**

Symbol	Parameter	Min.	Max.	Unit
$V_{R-BS}$	Bootstrap diode reverse voltage	-	1200	V

**Table 5. Total system**

Symbol	Parameter	Value	Unit
$V_{ISO}$	Isolation withstand voltage applied between each pin and heat sink plate (AC voltage, $t = 60\text{ s}$ )	2500	Vrms
$T_J$	IGBT and FRD operating junction temperature range	-40 to 150	$^{\circ}\text{C}$
	Driver IC and bootstrap diode operating junction temperature range	-40 to 150	
$T_C$	Module case operating temperature range	-40 to 125	$^{\circ}\text{C}$

**Table 6. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance, junction-to-case single IGBT	1	°C/W
	Thermal resistance, junction-to-case single diode	2	

### 3 Electrical characteristics

$T_J = 25\text{ °C}$  unless otherwise specified.

#### 3.1 Inverter parts

**Table 7. Inverter parts**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{CES}$	Collector cut-off current	$V_{CE} = 1200\text{ V}$ , $V_{CC} = V_{boot} = 15\text{ V}$	-	25		$\mu\text{A}$
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_{CC} = V_{boot} = 15\text{ V}$ , $V_{IN}^{(1)} = 5\text{ V}$ , $I_C = 10\text{ A}$	-	1.6	2.2	V
		$V_{CC} = V_{boot} = 15\text{ V}$ , $V_{IN}^{(1)} = 5\text{ V}$ , $I_C = 10\text{ A}$ , $T_J = 150\text{ °C}$	-	1.9		
$V_F$	Diode forward voltage	$V_{IN}^{(1)} = 0\text{ V}$ , $I_C = 10\text{ A}$	-	1.8	2.3	V
		$V_{IN}^{(1)} = 0\text{ V}$ , $I_C = 10\text{ A}$ , $T_J = 150\text{ °C}$	-	2.05		

1. Applied between  $HINx$ ,  $LINx$  and  $GND$  for  $x = U, V, W$ .

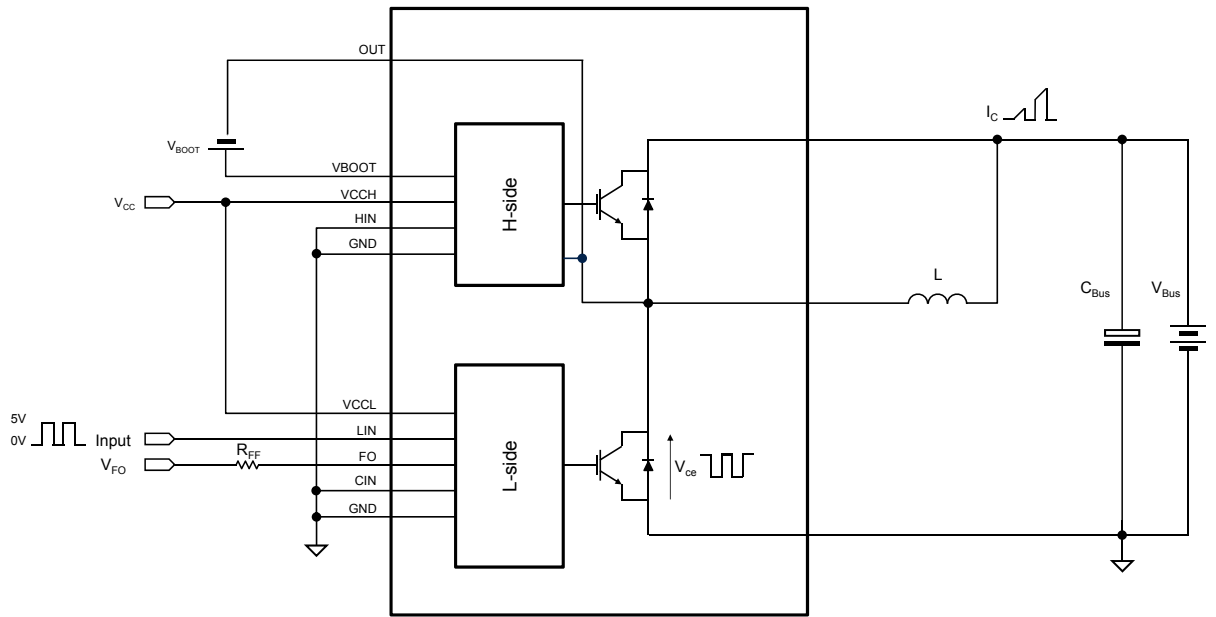
**Table 8. Inductive load switching time and energy**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
<b>High-side</b>						
$t_{on}^{(1)}$	Turn-on time	$V_{DD} = 600\text{ V}$ , $V_{CC} = V_{boot} = 15\text{ V}$ , $V_{IN}^{(2)} = 0\text{ to }5\text{ V}$ , $I_C = 10\text{ A}$	-	722	-	ns
$t_{c(on)}^{(1)}$	Crossover time on		-	202	-	ns
$t_{off}^{(1)}$	Turn-off time		-	1228	-	ns
$t_{c(off)}^{(1)}$	Crossover time off		-	290	-	ns
$t_{rr}^{(1)}$	Reverse recovery time		-	566	-	ns
$E_{on}$	Turn-on switching energy		-	0.89	-	mJ
$E_{off}$	Turn-off switching energy		-	0.82	-	mJ
$E_{rr}$	Reverse recovery energy		-	0.478	-	mJ
<b>Low-side</b>						
$t_{on}^{(1)}$	Turn-on time	$V_{DD} = 600\text{ V}$ , $V_{CC} = V_{boot} = 15\text{ V}$ , $V_{IN}^{(2)} = 0\text{ to }5\text{ V}$ , $I_C = 10\text{ A}$	-	407	-	ns
$t_{c(on)}^{(1)}$	Crossover time on		-	200	-	ns
$t_{off}^{(1)}$	Turn-off time		-	848	-	ns
$t_{c(off)}^{(1)}$	Crossover time off		-	270	-	ns
$t_{rr}^{(1)}$	Reverse recovery time		-	570	-	ns
$E_{on}$	Turn-on switching energy		-	0.90	-	mJ
$E_{off}$	Turn-off switching energy		-	0.82	-	mJ
$E_{rr}$	Reverse recovery energy		-	0.487	-	mJ

1.  $t_{on}$  and  $t_{off}$  include the propagation delay time of the internal drive.  $t_{c(on)}$  and  $t_{c(off)}$  are the switching times of the IGBT itself under the internally given gate driving conditions.

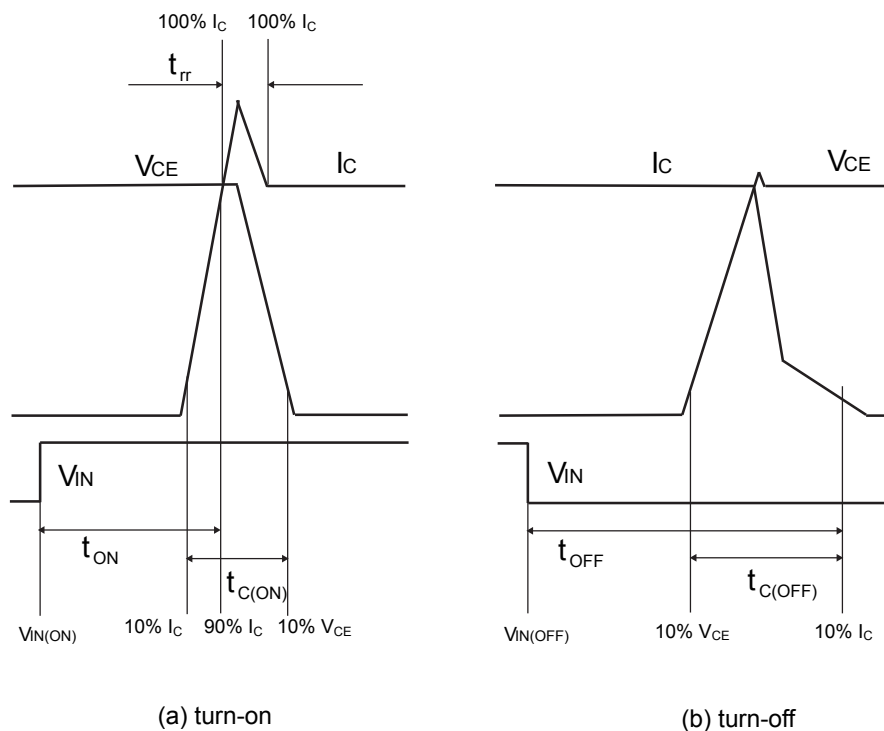
2. Applied between  $HINx$ ,  $LINx$  and  $GND$  for  $x = U, V, W$ .

**Figure 2. Switching time test circuit**



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**Figure 3. Switching time definition**



AM09223V1

### 3.2 Control/protection parts

Unless specifically noted,  $T_C = -40\text{ }^\circ\text{C}$  to  $125\text{ }^\circ\text{C}$ ,  $V_{PN} = 600\text{ V}$ ,  $V_{VCCxH} = V_{VCCL} = 15\text{ V}$ ,  $R_{FF} = 10\text{ k}\Omega$ ,  $C_{FF} = 0\text{ }\mu\text{F}$ , and  $V_{FO} = 5\text{ V}$ . The shipping test is performed at  $T_A = 25\text{ }^\circ\text{C}$  and  $125\text{ }^\circ\text{C}$  for the electrical characteristics shown below (except for the parameters specified by design and not tested in production).

**Table 9. Control/protection parts**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{VCCHx\_H}$	VCCHx pin operating voltage		9.2	10.2	11.3	V
$V_{VCCHx\_L}$	VCCHx pin operating stop voltage		8.7	9.7	10.8	V
$V_{VCCHx\_HYS}$	VCCHx pin hysteresis			0.5		V
$V_{VCCL\_H}$	VCCL pin operating voltage		11.2	12.6	13.3	V
$V_{VCCL\_L}$	VCCL pin operating stop voltage		10.7	11.7	12.8	V
$V_{VCCL\_HYS}$	VCCL pin hysteresis			0.5		V
$V_{VBOOTx-OUTx\_H}$	VBOOTx-OUTx operating voltage		11.0	12.1	12.8	V
$V_{VBOOTx-OUTx\_L}$	VBOOTx-OUTx operating stop voltage		10.5	11.6	12.3	V
$V_{VBOOTx-OUTx\_HYS}$	VBOOTx-OUTx hysteresis			0.5		V
$I_{VCCHx}$	VCCHx pin input current	$V_{HINx} = 0\text{ V}$ , each pin		1.4	2.0	mA
		$V_{HINx} = 5\text{ V}$ , each pin		1.4	2.0	mA
$I_{VCCL}$	VCCL pin input current	$V_{LINx} = 0\text{ V}$		1.9	3.2	mA
		$V_{LINx} = 5\text{ V}$		1.9	3.2	mA
$I_{VBOOTx-OUTx}$	VBOOTx-OUTx input current	$V_{VBOOTx-OUTx} = 15\text{ V}$ , $V_{INxH} = 0\text{ V}$ , in 1-phase operation		0.09	0.30	mA
		$V_{VBOOTx-OUTx} = 15\text{ V}$ , $V_{INxH} = 5\text{ V}$ , in 1-phase operation		0.12	0.30	mA
<b>Input signal</b>						
$V_{HINx\_H}$	HINx pin high-level input threshold voltage			2.0	2.5	V
$V_{HINx\_L}$	HINx pin low-level input threshold voltage		1.0	1.5		V
$V_{HINx\_HYS}$	HINx pin hysteresis			0.5		V
$V_{LINx\_H}$	LINx high-level input threshold voltage			2.0	2.5	V
$V_{LINx\_L}$	LINx pin low-level input threshold voltage		1.0	1.5		V
$V_{LINx\_HYS}$	LINx pin hysteresis			0.5		V
$I_{HINx}$	HINx pin input Current	$V_{HINx} = 5\text{ V}$ , each pin		0.25	0.50	mA
$I_{LINx}$	LINx pin input Current	$V_{LINx} = 5\text{ V}$ , each pin		0.25	0.50	mA
<b>Fault signal output and shutdown signal input</b>						
$V_{FO\_H}$	FO pin shutdown release voltage			2.0	2.5	V
$V_{FO\_L}$	FO pin shutdown threshold voltage		1.0	1.5		V

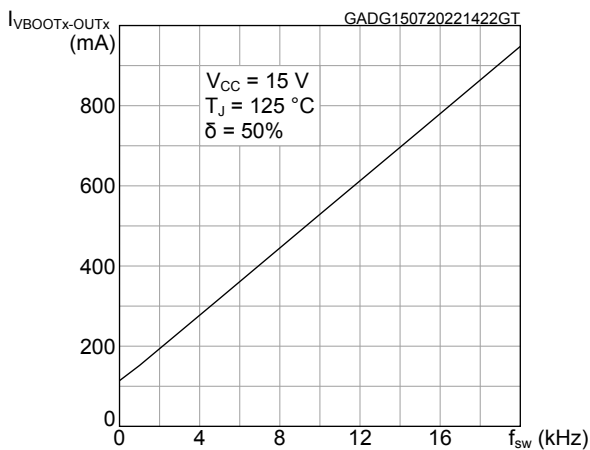


Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{FO\_HYS}$	FO pin shutdown hysteresis			0.5		V
$V_{FO\_H}$	FO pin output voltage in normal operation	$V_{FO} = 5\text{ V}$ , $R_{FF} = 10\text{ k}\Omega$ , $V_{CIN} = 0\text{ V}$	4.8	5.0		V
$V_{FO\_L}$	VFO pin error signal output voltage	$V_{FO} = 5\text{ V}$ , $R_{FF} = 10\text{ k}\Omega$ , $V_{CIN} = 1\text{ V}$	-	0.09	0.50	V
$t_{FO}^{(1)(2)}$	FO pin CIN hold time	$C_{CFO} = 0\text{ }\mu\text{F}$	0.012	0.030	0.060	ms
		$C_{CFO} = 0.001\text{ }\mu\text{F}$	0.20	0.32	0.44	ms
		$C_{CFO} = 0.01\text{ }\mu\text{F}$	2.0	3.2	4.4	ms
		$C_{CFO} = 0.1\text{ }\mu\text{F}$	20	32	44	ms
		$C_{CFO} = 1\text{ }\mu\text{F}$	200	320	440	ms
<b>Protection</b>						
$V_{CIN\_H}$	CIN pin overcurrent detection voltage		0.46	0.50	0.54	V
$V_{CIN\_L}$	CIN pin overcurrent release voltage		0.32	0.38	0.44	V
$V_{CIN\_HYS}$	CIN pin overcurrent hysteresis			0.12		V
$t_{CIN\_DELAY}$	CIN pin detection delay time			0.7	1.5	$\mu\text{s}$
$I_{CIN}$	CIN pin input current	$V_{CIN} = 0.5\text{ V}$		0		$\mu\text{A}$

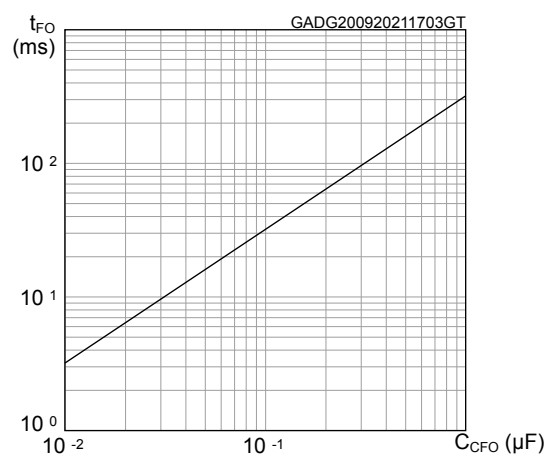
1. Specified by design, not tested in production.

2. For a relation between  $t_{FO}$  and  $C_{CFO}$ , see Figure 5. The shipping test is performed with the condition at  $C_{CFO} = 0.01\text{ }\mu\text{F}$  only.

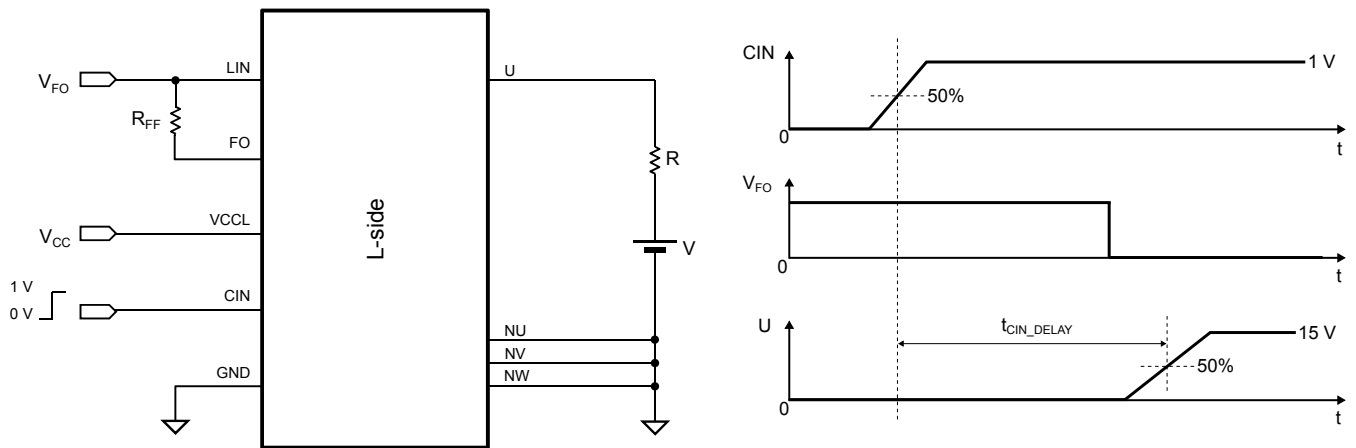
**Figure 4. Total bootstrap current vs  $f_{sw}$**



**Figure 5.  $t_{FO}$  -  $C_{CFO}$  characteristics**



**Figure 6. CIN test circuit and time definition**



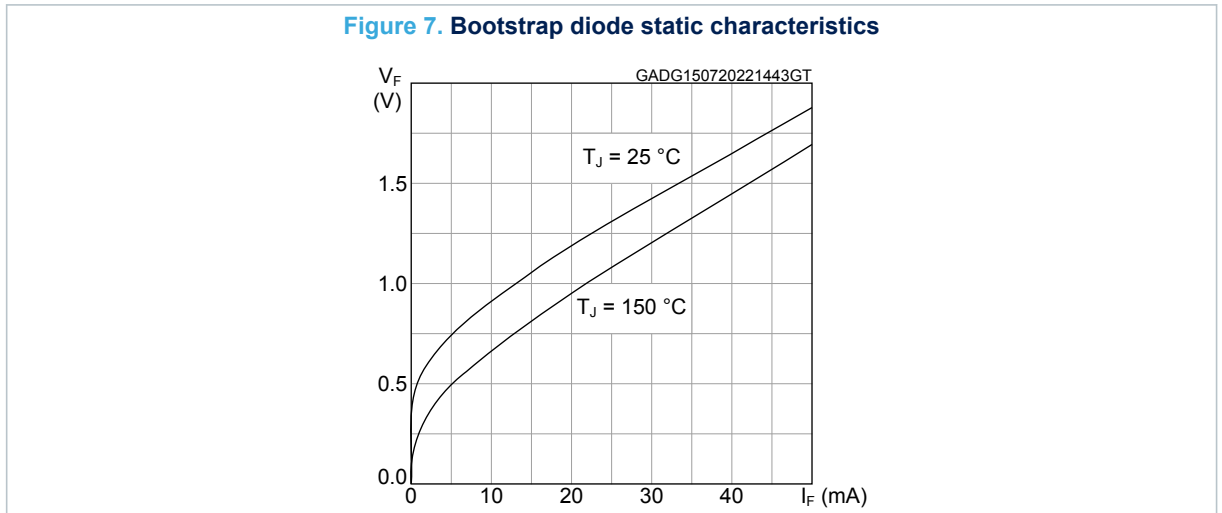
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## 4 Bootstrap diode

Table 10. Bootstrap diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{F\_BS}$	Bootstrap diode forward voltage	$I_{F\_BS} = 10 \text{ mA}$	0.4	0.9	1.4	V
$R_{S\_BS}$	Bootstrap diode series resistor		12	20	28	$\Omega$

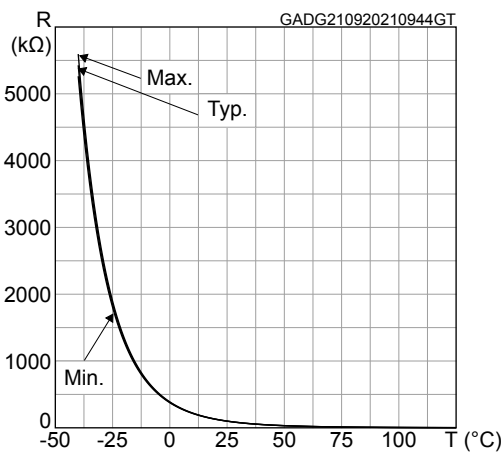
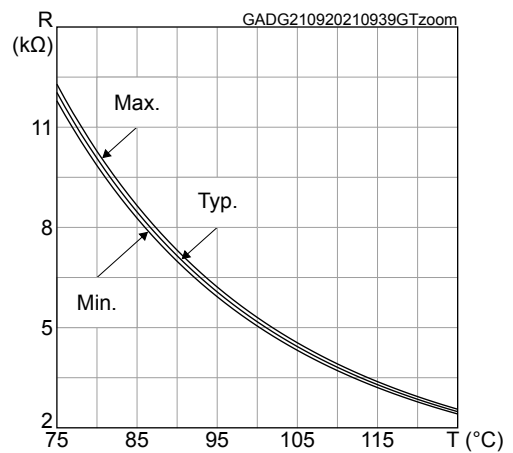
Figure 7. Bootstrap diode static characteristics



## 5 NTC thermistor

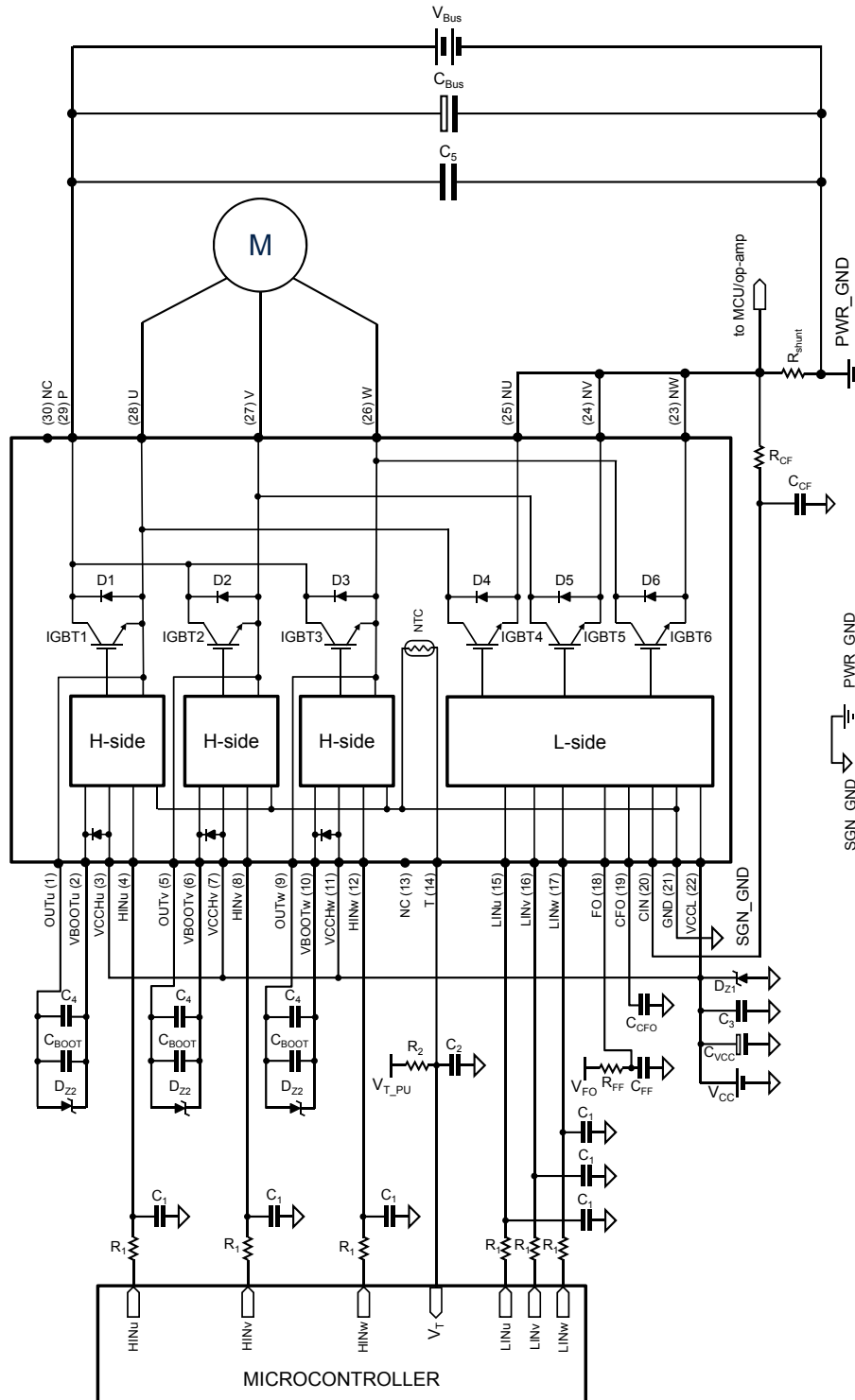
**Table 11. NTC thermistor**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
R <sub>25</sub>	Resistance	T <sub>A</sub> = 25 °C		100		kΩ
B <sub>25/85</sub>	B-constant (25–85 °C)			4395		K
T	Operating temperature range		-40		175	°C

**Figure 8. NTC resistance vs temperature**

**Figure 9. NTC resistance vs temperature zoom**


## 6 Application circuit example

Figure 10. Application circuit example



Application designers are free to use a different scheme according to the device specifications.

## 6.1 Guidelines

1. Input signals HIN, LIN are active-high logic. A 20 k $\Omega$  (typ.) pull-down resistor is built-in for each input pin. To prevent input signal oscillation, the wiring of each input should be as short as possible and the use of RC filters ( $R_1$ ,  $C_1$ ) on each input signal is suggested. The filters should be done with a time constant of about 100 ns and placed as close as possible to the IPM input pins.
2. The use of a bypass capacitor  $C_{VCC}$  (aluminum or tantalum) can help reduce the transient circuit demand on the power supply. Also, to reduce high frequency switching noise distributed on the power lines, it is suggested to place a decoupling capacitor  $C_3$  (100 to 220 nF, with low ESR and low ESL), as close as possible to each  $V_{CC}$  pin and in parallel with the bypass capacitor.
3. The use of RC filter ( $R_{CF}$ ,  $C_{CF}$ ) for preventing protection circuit malfunction is suggested. The time constant ( $R_{CF} \times C_{CF}$ ) should be set to 1  $\mu$ s and the filter must be placed as close as possible to the CIN pin.
4. The FO is an input/output pin. It should be pulled up to a power supply (i.e., MCU bias at 3.3 - 5 V) by a resistor value able to match the  $V_{FO\_L}$  and  $V_{FO\_H}$  threshold voltages mainly. In case of 3.3 or 5 V pull up voltage, the suggested resistor value is from 5.6 k $\Omega$  to 68 k $\Omega$ . The RC filter on FO could have also impact on the re-starting time after a fault event so it must be placed as close as possible to the FO pin.
5. A decoupling capacitor  $C_2$  between 1 nF and 10 nF can be used to increase the noise immunity of the signal on the NTC thermistor. Its effectiveness is improved if the capacitor is placed close to the MCU.
6. The decoupling capacitor  $C_4$  (100 to 220 nF with low ESR and low ESL) in parallel with each  $C_{BOOT}$  is useful to filter high frequency disturbances. Both  $C_{BOOT}$  and  $C_4$  (if present) should be placed as close as possible to each OUTu, OUTv, OUTw and respective  $V_{BOOT}$  pins.
7. To prevent overvoltage on the  $V_{CC}$  pins, a Zener diode ( $D_{Z1}$ ) can be used. Similarly, on the  $V_{BOOT}$  pins, a Zener diode ( $D_{Z2}$ ) can be placed in parallel with each  $C_{BOOT}$ .
8. The use of the decoupling capacitor  $C_5$  (100 to 220 nF, with low ESR and low ESL) in parallel with the electrolytic capacitor  $C_{BUS}$  is useful to prevent surge destruction. Both capacitors  $C_5$  and  $C_{BUS}$  should be placed as close as possible to the IPM ( $C_5$  has priority over  $C_{BUS}$ ).
9. When the application requires a galvanic isolation between low and high voltage, use of high speed (high CMR) opto-coupler is recommended.
10. Low inductance shunt resistors should be used for phase leg current sensing.
11. In order to avoid malfunction, the wiring between N pins, the shunt resistor and PWR\_GND should be as short as possible.
12. The connection of SGN\_GND to PWR\_GND at only one point (close to the shunt resistor terminal) can help to reduce the impact of power ground fluctuation.
13. Parallel connection of switches or legs on the same or multiple IPMs is not suggested.

These guidelines ensure the device specifications for application designs. For further details, please refer to the relevant application note.

**Table 12. Recommended operating conditions**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{PN}$	Supply voltage	Applied between P-Nu, $N_V$ , $N_W$		600	800	V
$V_{CCHx}$	Control supply voltage	Applied between $V_{CCHx}$ -GND	13.5	15	16.5	V
$V_{CCL}$	Control supply voltage	Applied between $V_{CCL}$ -GND	13.5	15	16.5	V
$V_{BS}$	High-side bias voltage	Applied between $V_{BOOTi}$ - $OUT_i$ for $i = U, V, W$	13	15	18.5	V
$t_{dead}$	Blanking time to prevent arm-short	For each input signal	1.5			$\mu$ s
$f_{PWM}$	PWM input signal	-40 $^{\circ}$ C < $T_C$ < 100 $^{\circ}$ C -40 $^{\circ}$ C < $T_J$ < 125 $^{\circ}$ C			20	kHz
$T_C$	Case operation temperature				125	$^{\circ}$ C

## 7 Electrical characteristics (curves)

Figure 11. Output characteristics

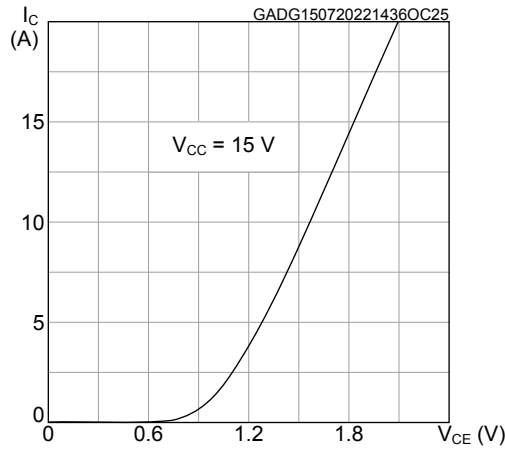


Figure 12.  $V_{CE(sat)}$  vs collector current

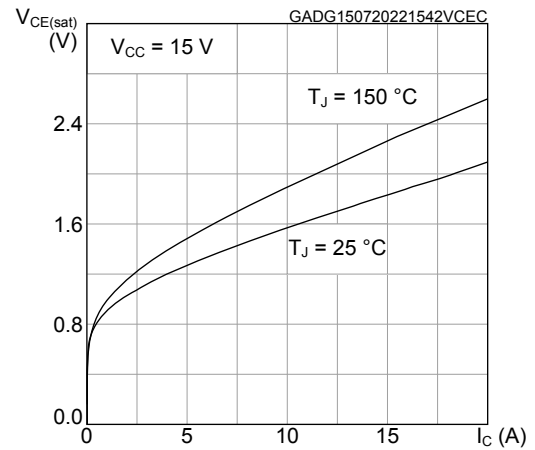


Figure 13.  $I_C$  vs case temperature

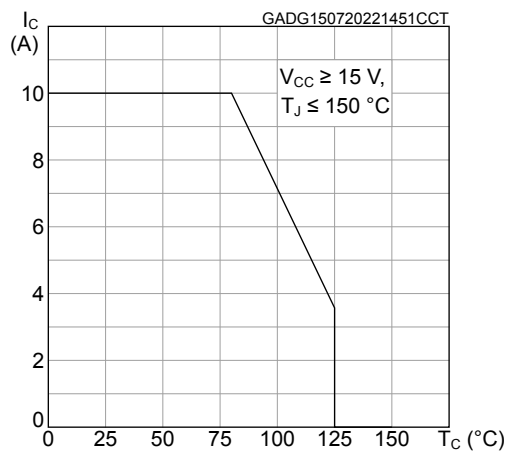


Figure 14. Diode  $V_F$  vs forward current

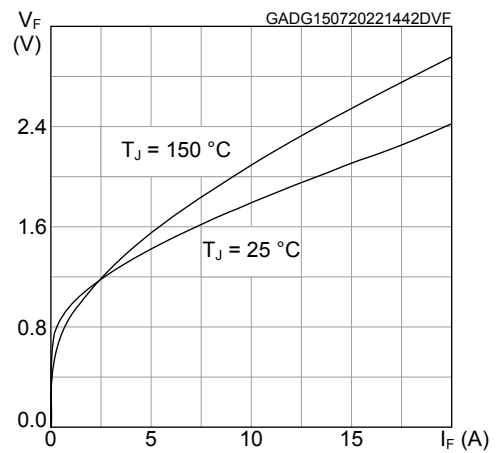


Figure 15.  $E_{on}$  switching energy vs collector current

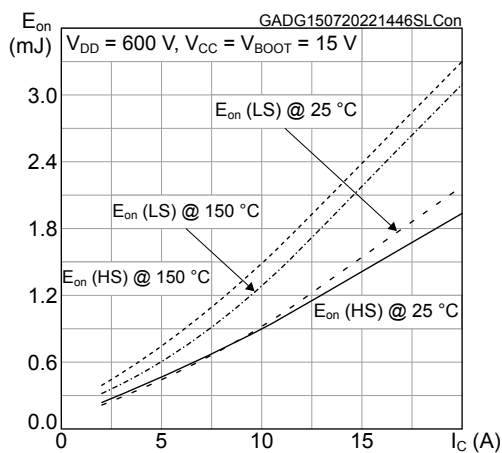


Figure 16.  $E_{off}$  switching energy vs collector current

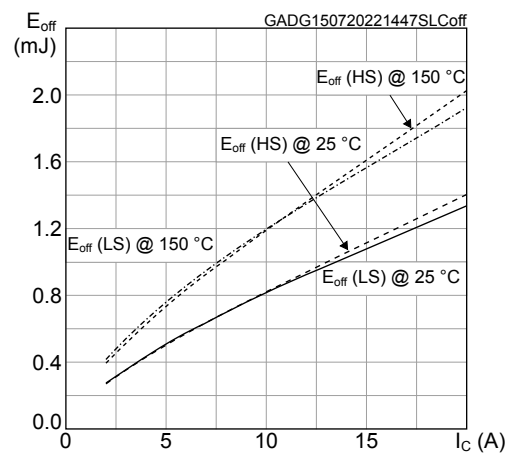


Figure 17. Normalized thermal impedance for IGBT

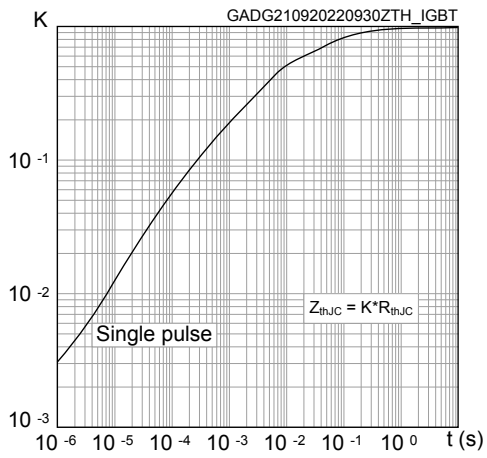
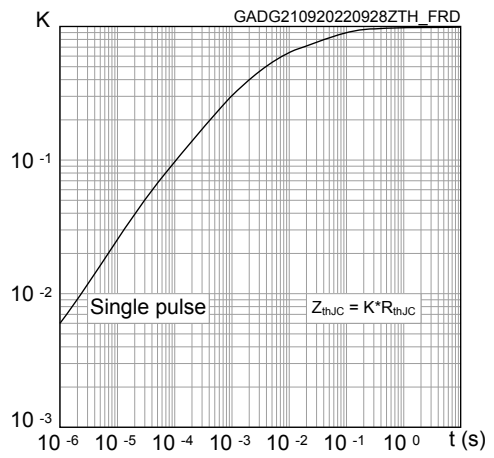


Figure 18. Normalized thermal impedance for FRD







## Revision history

**Table 13. Document revision history**

Date	Revision	Changes
18-Jul-2022	1	First release.
21-Sep-2022	2	Updated <i>Table 2. Inverter parts</i> . Removed " <i>Figure 17. Err reverse recovery energy vs collector current</i> ", added <i>Figure 17. Normalized thermal impedance for IGBT and Figure 18. Normalized thermal impedance for FRD</i> .
12-Dec-2023	3	Updated <i>Table 1. Pin description</i> . Minor text changes.

## Contents

<b>1</b>	<b>Internal schematic and pin description</b> .....	<b>2</b>
<b>2</b>	<b>Absolute maximum ratings</b> .....	<b>4</b>
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