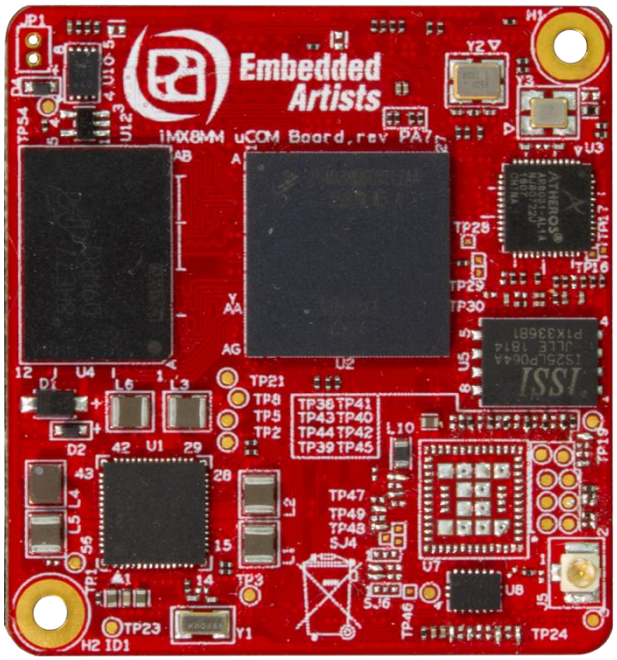
Document status: Preliminary

iMX8M Nano uCOM Board Datasheet



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1 Document Revision History

Revision	*Date*	*Description*
PA1	2020-03-02	First version.
PA2	2020-03-20	Removed references to SAI1/USB2. Updated boot control description.
PA3	2020-04-17	Correction on text in Figure 11.
PA4	2020-07-30	Added section 12.7
PA5	2020-11-04	Added section about USB issue.
PA6	2023-04-17	Added information about iMX8M Nano uCOM Developer's Kit V2 and V3. Corrected pin naming of JB, pin 1-15.
PA7	2023-04-21	Updated information about boot control.
PA8	2023-06-15	Added information about board handling.
PA9	2024-01-19	Added information about JB, pin 16.

2 Introduction

This document is a datasheet that specifies and describes the *iMX8M Nano uCOM Board* mainly from a hardware point of view. Some basic software related issues are also addressed, like booting and functional verification, but there is separate software development documentation that should also be consulted.

2.1 Hardware

The *iMX8M Nano uCOM Board* is a Computer-on-Module (COM) based on NXP's ARM quad-core Cortex-A53 / M7 i.MX 8M Nano System-on-Chip (SoC) application processor. The board provides a quick and easy solution for implementing a high-performance ARM Cortex-A53 / M7 based design. The Cortex-A53 cores run at up to 1.5 GHz (1.4 GHz for industrial temperature version) and the Cortex-M7 core at up to 750 MHz (600 MHz for industrial temperature version).

The heterogeneous core architecture enables the system to run an OS like Linux on the Cortex-A53 cores and a Real-Time OS (RTOS) on the Cortex-M7. This architecture is ideal for real time applications where Linux cannot be used for all time critical tasks. The Cortex-M7 can handle (real time) critical tasks and can also be used to lower power consumption.

The *iMX8M Nano uCOM Board* delivers high computational and graphical performance at low power consumption. The on-board PMIC, supporting DVFS (Dynamic Voltage and Frequency Scaling), together with a DDR4 memory sub-system reduce the power consumption.

The SoC is part of the scalable i.MX8M Nano product family. There is a range of i.MX RT/6/7/8/9 (u)COM Boards from Embedded Artists with single, dual and quad Cortex-A cores, with or without a heterogeneous Cortex-M core. Families of boards (uCOM and COM) share the same basic pinning for maximum flexibility and performance scalability.

The *iMX8M Nano uCOM Board* has an ultra-small form factor and shields the user from a lot of complexity of designing a high performance system. It is a robust and proven design that allows the user to focus the product development, shorten time to market and minimize the development risk.

The *iMX8M Nano uCOM Board* targets a wide range of applications, such as:

- Portable systems
- HMI/GUI solutions
- Portable medical and health care
- Connected vending machines
- Point-of-Sale (POS) applications
- Access control panels
- Audio
- IP phones
- Smart appliances
- Wearables
- Home energy management systems
- Industrial automation
- HVAC Building and Control Systems
- Smart Grid and Smart Metering
- Smart Toll Systems
- Data acquisition
- Communication gateway solutions
- Connected real-time systems
- ...and much more

The picture below illustrates the block diagram of the *iMX8M Nano uCOM Board*.

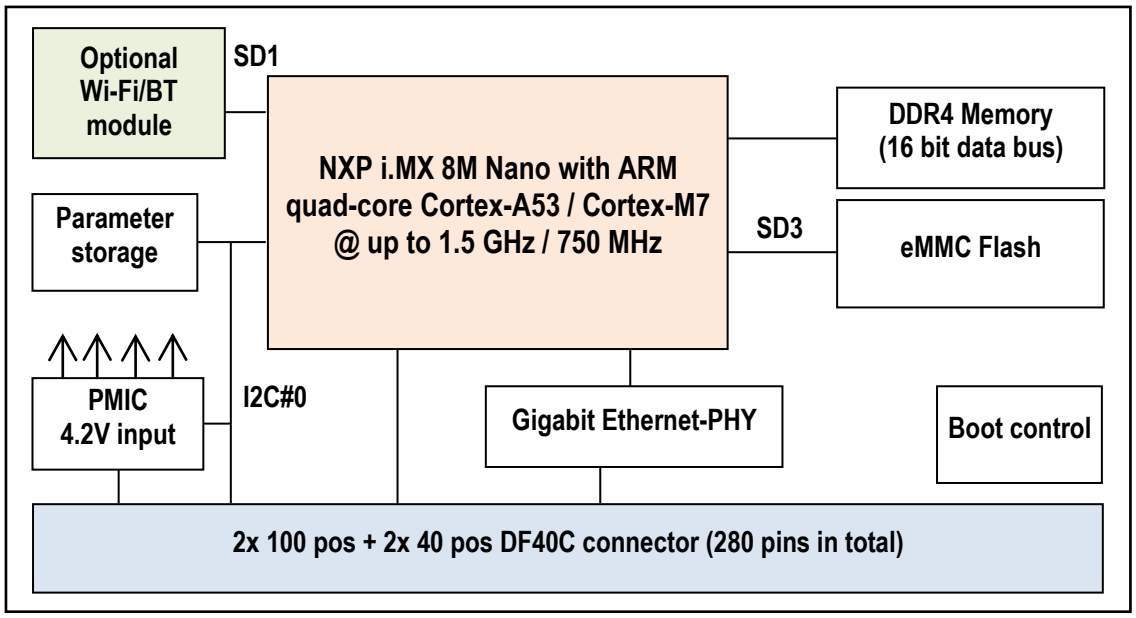

Figure 1 – iMX8M Nano uCOM Board Block Diagram

The *iMX8M Nano uCOM Board* pin assignment focus on direct connection to (carrier board) interface connectors and minimize trace and layer crossing. This is important for high speed, serial interfaces with impedance controlled differential pairs. As a result, carrier boards can be designed with few routing layers. In many cases, a four layer pcb is enough to implement advanced and compact carrier boards. The pin assignment is common for the *iMX RT/7/8/9 uCOM Boards* from Embedded Artists and the general, so called, EAuCOM specification is found in separate document.

2.2 Software

The *iMX8M Nano uCOM Board* has Board Support Packages (BSPs) for Linux and SDK for the Cortex-M7 side. Precompiled images are available. Embedded Artists work with partners that can provide support for other operating systems (OS). For more information contact Embedded Artists support.

This document has a hardware focus and does not cover software development. See other documents related to the *iMX8M Nano uCOM Board* for more information about software development.

2.3 Features and Functionality

The i.MX 8M Nano is a powerful SoC. The full specification can be found in NXP's *i.MX 8M Nano Datasheet* and *i.MX 8M Nano Reference Manual*. The table below lists the main features and functions of the *iMX8M Nano uCOM board* - which represents Embedded Artists integration of the i.MX 8M Nano SoC. Due to pin configuration some functions and interfaces of the i.MX 8M Nano may not be available at the same time. See i.MX 8M Nano SoC datasheet and reference manual for details. Also see pin multiplexing Excel sheet for details.

Group	Feature		iMX8M Nano uCOM Board
CPUs	NXP SoC	commercial temp. range industrial temp. range	MIMX8MN6DVTJZA (0 - 70° C) MIMX8MN6CVTIZA (-40 - 85° C)
	CPU Cores		4x Cortex-A53 1x Cortex-M7 with MPU/FPU
	L1 Instruction cache		32 KByte on each Cortex-A53

	L1 Data cache	32 KByte on each Cortex-A53
	L2 Cache on Cortex-A53 cores	512 KByte unified
	On-chip SRAM (TCM for Cortex-M7)	256 KByte
	NEON SIMD media accelerator on Cortex-A53	✓
	Maximum CPU frequency	1.5/1.4 GHz on Cortex-A53 cores 750/600 MHz on Cortex-M7
Security Functions	ARM TrustZone	✓
	Advanced High Assurance Boot	✓
	Cryptographic Acceleration and Assurance Module	✓
	Secure Non-Volatile Storage	✓
	System JTAG controller	✓
	Resource Domain Controller (RDC)	✓
Memory	DDR4 RAM Size	1 GByte, default. Other on request.
	DDR4 RAM Speed	2400 MT/s
	DDR4 RAM Memory Width	16 bit
	eMMC NAND Flash (8 bit)	8 GByte, default. Other on request.
Graphical Processing	Multimedia Graphics Processing Unit (GPU)	GC7000UL supporting OpenGL ES3.1/3.0/2.0, OpenCL1.2, Vulkan
Graphical Output	MIPI-DSI, 4 lanes	✓ up to 1080p60 resolution
Graphical Input	MIPI-CSI, 4 lanes	✓
Connectivity Interfaces (all functions are not available at the same time)	1x USB2.0 OTG port with Phy	✓
	1000/100/10 Mbps Gigabit Ethernet controller with support for EEE, Audio Video Bridging (AVB) and IEEE1588.	✓ with on-board Gigabit PHY
	QuadSPI with support for XIP	✓
	5x I2S/SAI, SPDIF, 8-ch PDM	✓
	2x SD3.0/MMC 5.0	✓ SD3 interface used on-board to eMMC, SD1 interface used when on-board Wi-Fi/BT mounted
	3x SPI, 4x UART, 4x I²C	✓
	PWMs, WDOG	✓
Other	PMIC supporting DVFS techniques for low power modes	✓
	E2PROM storing board information and Ethernet MAC address	✓
	On-board RTC via PMIC	✓

	On-board watchdog functionality	✓

2.4 Reference Documents

The following documents are important reference documents and should be consulted when integrating the *iMX8M Nano uCOM board*:

- EACOM Board Specification
- EACOM Board Integration Manual

The following NXP documents are also important reference documents and should be consulted for functional details:

- IMX8MNCEC, i.MX 8M Nano Applications Processors - Consumer Products Data Sheet, latest revision
- IMX8MNIEC, i.MX 8M Nano Applications Processors - Industrial Products Data Sheet, latest revision
- IMX8MNRM, i.MX 8M Nano Applications Processors Reference Manual, latest revision
- IMX8MNSRM, Security Reference Manual for i.MX 8M Nano, latest revision
- IMX8MNCE, Chip Errata for the i.MX 8M Nano, latest revision
  Note: It is the user's responsibility to make sure all errata published by the manufacturer are taken note of. The manufacturer's advice should be followed.
- AN12778, i.MX 8M Nano Power Consumption Measurement, latest revision
- AN12xxx <TBD>, i.MX 8M Nano Product Lifetime Usage, latest revision

The following documents are external industry standard reference documents and should also be consulted when applicable:

- eMMC (Embedded Multi-Media Card) the eMMC electrical standard is defined by JEDEC JESD84-B45 and the mechanical standard by JESD84-C44 (www.jedec.org)
- GbE MDI (Gigabit Ethernet Medium Dependent Interface) defined by IEEE 802.3. The 1000Base-T operation over copper twisted pair cabling is defined by IEEE 802.3ab (www.ieee.org)
- The I2C Specification, Version 2.1, January 2000, Philips Semiconductor (now NXP) (www.nxp.com)
- I2S Bus Specification, Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) (www.nxp.com)
- JTAG (Joint Test Action Group) defined by IEEE 1149.1-2001 - IEEE Standard Test Access Port and Boundary Scan Architecture (www.ieee.org)
- SD Specifications Part 1 Physical Layer Simplified Specification, Version 3.01, May 18, 2010, © 2010 SD Group and SD Card Association (Secure Digital) (www.sdcard.org)
- SPI Bus – “Serial Peripheral Interface” – de-facto serial interface standard defined by Motorola. A good description may be found on Wikipedia (http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus)

- DSI (Display Serial Interface) The DSI standard is owned and maintained by the MIPI Alliance (“Mobile Industry Processor Alliance”) (www.mipi.org)
- CSI-2 (Camera Serial Interface version 2) The CSI-2 standard is owned and maintained by the MIPI Alliance (“Mobile Industry Processor Alliance”) (www.mipi.org)
- USB Specifications (www.usb.org)

3 Board Pinning

Embedded Artists has defined the EAuCOM board standard with 42 x 45 mm boards that use Hirose DF40C connectors. Note that this is not the same as the EACOM board standard with module size 82 x 50 mm. Chapter 4 describes an adapter board that converts an EAuCOM board into an EACOM board. This way, the same carrier board can be used for all iMX Developer's Kits. See the *EAuCOM Board specification* document for details and background information. Hereafter this standard will be referred to as **EAuCOM**.

There are four Hirose DF40C expansion connectors; two 100 pos and two 40 pos connectors. The 0.4mm pitch connectors have a board-to-board stacking height of only 1.5mm. There are also versions of the receptacle connectors that give 3.0mm stacking height.

3.1 Pin Numbering

The figure below illustrates the location of the four expansion connectors and their respective pin numbering on the bottom side of the *iMX8M Nano uCOM Board*.

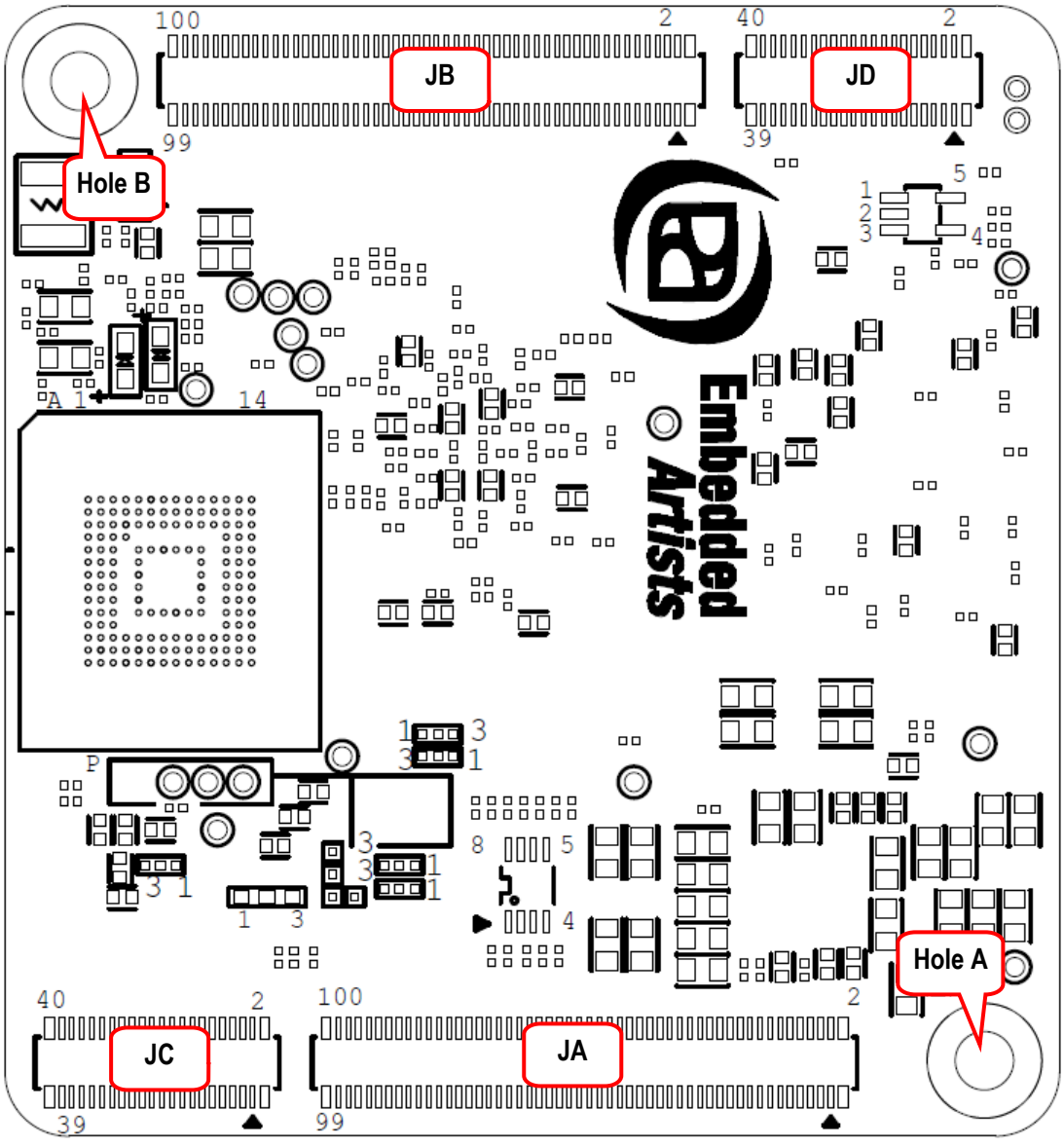

Figure 2 – iMX8M Nano uCOM (EAuCOM standard) Board Pin Numbering, Bottom Side

3.2 Pin Assignment

This section describes the pin assignment of the board, with the following columns:

Connector and Pin number	The pin numbers are listed in consecutive order. Odd pin numbers are on one row and even numbers on the other row.
Non-i.MX 8M Nano signals	Lists signals that are not directly connected to the i.MX 8M Nano SoC. These signals are typically related to powering and connected to the on-board Power Management IC (PMIC).
i.MX 8M Nano Ball Name	The name of the ball of the i.MX 8M Nano SoC that is connected to this pin.
Alternative Pin Function	Information if the signal is a dedicated interface or a general pin that can multiples different signals. See separate Excel sheet for details about available multiplexing alternatives.
Notes	When relevant, the preferred pin function is listed.

Note that some pins are EAuCOM board *type specific*, meaning that these pins might not be compatible with other EAuCOM boards. Using these may result in lost compatibility between EAuCOM boards, but not always. Check details between EAuCOM boards of interest.

The table below lists the pins on expansion connector JA (100-pos connector).

JA Pin Number	EAuCOM Board Signal	i.MX 8M Nano Ball Name	Alternative Pin Function?	Notes
1-8	VIN_VBAT	PMIC: VSYS_4V2		System supply voltage, see chapter 8 for more details.
9-16	GND			
17	VDD1	PMIC: LDO1 (NVCC_SNVS_1V8)		Voltage rail, see chapter 8 for more details.
18	VDD_RTC			Not connected. On-board RTC powered via VIN.
19, 21, 23, 25, 27, 29	VDD_1V8	PMIC: BUCK7 (NVCC_1V8)		1.8V voltage rail, see chapter 8 for more details.
20, 22, 24, 26, 28, 30	VDD_3V3	PMIC: BUCK6 (NVCC_3V3)		3.3V voltage rail, see chapter 8 for more details.
31-32	GND			
33	Board specific	-		Not connected
34, 36, 38, 40, 42	VDD_RF			Not connected per default. Can optionally power on-board RF-module. Requires special order for this mounting option.
35	Board specific	-		Not connected
37	Board specific	-		Not connected
39	Board specific	-		Not connected
41	GND			
43	Board specific	-		Not connected
44	GND			
45	Board specific	-		Not connected
46	GND			
47	Board specific	-		Not connected
48	VBAT_TEMP	-		Not connected
49	Board specific	-		Not connected
50	VBAT_CURRP	-		Not connected

51	GND			
52	VBAT_CURRN	-		Not connected
53	Board specific	-		Not connected
54, 56, 58, 60	PSU_5V	-		Not connected
55	Board specific	-		Not connected
57	Board specific	-		Not connected
59	Board specific	-		Not connected
61	GND			
62, 64, 66, 68	VBUS_USB	-		Not connected
63	Board specific	-		Not connected
65	Board specific	-		Not connected
67	Board specific	-		Not connected
69	Board specific	-		Not connected
70-71	GND			
72	Board specific	-		Not connected
73	Board specific	-		Not connected
74	Board specific	GPIO4		Internal signal connected to SD2_VSEL, controlling voltage level on SD2 interface. Do not connect to this signal.
75	Board specific	-		Not connected
76	Board specific	-		Not connected
77	Board specific	-		Not connected
78	Board specific	SPDIF_TX	Yes	
79	Board specific	-		Not connected
80	Board specific	SPDIF_RX	Yes	
81-82	GND			
83	Board specific	-		Not connected
84	Board specific	SPDIF_EXT_CLK	Yes	
85	Board specific	SAI3_MCLK	Yes	
86	Board specific	SAI5_MCLK	Yes	
87	Board specific	SAI3_TXFS	Yes	
88	Board specific	SAI5_RXFS	Yes	
89	Board specific	SAI3_TXC	Yes	
90	Board specific	SAI5_RXC	Yes	
91-92	GND			
93	Board specific	SAI3_TXD	Yes	
94	Board specific	SAI5_RXD0	Yes	
95	Board specific	SAI3_RXFS	Yes	
96	Board specific	SAI5_RXD1	Yes	
97	Board specific	SAI3_RXC	Yes	
98	Board specific	SAI5_RXD2	Yes	
99	Board specific	SAI3_RXD	Yes	
100	Board specific	SAI5_RXD3	Yes	

The table below lists the pins on expansion connector JB (100-pos connector).

JB Pin Number	EAuCOM Board Signal	i.MX 8M Nano Ball Name	Alternative Pin Function?	Notes
1	UART-C_RXD	UART1_RXD	Yes	Not connected if Wi-Fi/BT module mounted
2	GPIO-A	GPIO0	Yes	
3	UART-C_TXD	UART1_TXD	Yes	Not connected if Wi-Fi/BT module mounted
4	GPIO-B	GPIO1	Yes	
5	UART-A_RXD	UART2_RXD	Yes	
6	GPIO-C	GPIO5	Yes	
7	UART-A_TXD	UART2_TXD	Yes	
8	GPIO-D	GPIO6	Yes	
9	UART-C_CTS	UART3_RXD	Yes	Not connected if Wi-Fi/BT module mounted
10	GPIO-E	GPIO7	Yes	
11	UART-C_RTS	UART3_TXD	Yes	Not connected if Wi-Fi/BT module mounted
12	GPIO-F	GPIO8	Yes	
13	UART-B_RXD	UART4_RXD	Yes	
14	GPIO-G	GPIO9	Yes	
15	UART-B_TXD	UART4_TXD	Yes	
16	GPIO-H	GPIO11		Note. GPIO11 is only available on rev B1 boards, and later (when the new Ethernet-Phy was introduced, RTL8211FDI-CG, GPIO11 became available and was routed to this pin).
17	GND			
18	GPIO-J	-		Not connected
19	SD-A_VDD	NVCC_SD2	No	Supply voltage for SD2 interface. Note: this is an output, not an input. No external load except pull-up resistors on the SD2 signals is allowed.
20	GPIO-K	-	Yes	
21	GND			
22	GPIO-L	SD2_VSEL	No	Internal signal connected to SD2_VSEL, controlling voltage level on SD2 interface. Do not connect to this signal.
23	SD-A_CLK	SD2_CLK	Yes	
24	GPIO-M	PMIC: CLK_32K_OUT	No	Connects to PMIC (BD71847AMWV) CLK_32K_OUT output. Any external load on this signal can affect power consumption on deep-sleep mode.
25	SD-A_CMD	SD2_CMD	Yes	
26	GND			
27	SD-A_DATA0	SD2_DATA0	Yes	
28	SPI-A_SCLK	ECSPI1_SCLK	Yes	
29	SD-A_DATA1	SD2_DATA1	Yes	
30	SPI-A_MISO	ECSPI1_MISO	Yes	
31	SD-A_DATA2	SD2_DATA2	Yes	
32	SPI-A_MOSI	ECSPI1_MOSI	Yes	
33	SD-A_DATA3	SD2_DATA3	Yes	
34	SPI-A_SS0	ECSPI1_SS0	Yes	

35	GND			
36	GND			
37	SD-A_WP	SD2_WP	Yes	Note: the logic level of this signal can be either 3.3V or 1.8V, depending on signal SD2_VSEL. This can change during run time.
38	SPI-B_SCLK	ECSPI2_SCLK	Yes	
39	SD-A_NCD	SD2_NCD	Yes	Note: the logic level of this signal can be either 3.3V or 1.8V, depending on signal SD2_VSEL. This can change during run time.
40	SPI-B_MISO	ECSPI2_MISO	Yes	
41	SD-A_NRST	SD2_NRST	Yes	Note: the logic level of this signal can be either 3.3V or 1.8V, depending on signal SD2_VSEL. This can change during run time.
42	SPI-B_MOSI	ECSPI2_MOSI	Yes	
43	USB-A_OC	GPIO13	Yes	
44	SPI-B_SS0	ECSPI2_SS0	Yes	
45	USB-A_PWR	GPIO12	Yes	
46	GND			
47	USB-A_VBUS	USB1_VBUS	No	
48	I2C-A_SCL	I2C1_SCL	No	Note: Do not change pin function. Must be an I2C channel since the interface is used on-board.
49	USB-A_DN	USB1_DN	No	
50	I2C-A_SDA	I2C1_SDA	No	Note: Do not change pin function. Must be an I2C channel since the interface is used on-board.
51	USB-A_DP	USB1_DP	No	
52	I2C-B_SCL	I2C2_SCL	Yes	The signal has an on-board 2.2Kohm pull-up resistor
53	USB-A_ID	USB1_ID	No	
54	I2C-B_SDA	I2C2_SDA	Yes	The signal has an on-board 2.2Kohm pull-up resistor
55	GND			
56	I2C-C_SCL	I2C3_SCL	Yes	The signal has an on-board 2.2Kohm pull-up resistor
57	USB-B_OC	GPIO14		
58	I2C-C_SDA	I2C3_SDA	Yes	The signal has an on-board 2.2Kohm pull-up resistor
59	USB-B_PWR	GPIO15		
60	I2C-D_SCL	I2C4_SCL	Yes	Note: this signal is also available on connector JD pin 33. The signal has no on-board pull-up resistor.
61	USB-B_VBUS	-		Not connected
62	I2C-D_SDA	I2C4_SDA	Yes	The signal has no on-board pull-up resistor
63	USB-B_DN	-		Not connected
64	GND			
65	USB-B_DP	-		Not connected
66	GND			
67	USB-B_ID	-		Not connected
68	PERI_PWR_EN	PMIC: BUCK6 (NVCC_3V3)	No	**Power enable signal for external peripherals. No external must drive any signal to the i.MX8M Nano SoC before this signal is active.** The signal is active high and is connected to the on-board generate 3.3V supply rail. If all external circuits that can drive a signal to the i.MX8M Nano CPU are powered from the uCOM-generated 3.3V and 1.8V supplies, this gating signal

				can be ignored.
69	GND			
70	POR_B	POR_B		Connected to POR_B on the i.MX 8M Nano SoC. Signal shall normally only be used to connect to debug interface connector. Use signals RESET_IN (JB pin 74) to cause a power cycle reset of the board.
71	ETH_LED_10/100	ETH_LED_10/100		Connected to on-board Gigabit Ethernet PHY
72	ONOFF	ONOFF		Connected to ONOFF on the i.MX 8M Nano SoC
73	ETH_LED_1000	ETH_LED_1000		Connected to on-board Gigabit Ethernet PHY
74	PWRON_B	PMIC: PWRON_B		A falling edge on this input cause a power cycle reset of the board. Connects to PMIC (BD71847AMWV) PWRON_B input.
75	ETH_LED_ACT	ETH_LED_ACT		Connected to on-board Gigabit Ethernet PHY
76	BOOT_MODE0	BOOT_MODE0	No	This signal shall be left unconnected under normal operation. The Boot Mode is controlled by signals ISP_ENABLE (JB pin 100) and BOOT_CTRL (JB pin 98). Note. This signal is 1.8V logic level.
77	GND			
78	BOOT_MODE1	BOOT_MODE1	No	This signal shall be left unconnected under normal operation. The Boot Mode is controlled by signals ISP_ENABLE (JB pin 100) and BOOT_CTRL (JB pin 98). Note. This signal is 1.8V logic level.
79	ETH_TRXP1	ETH_TRXP1		Connected to on-board Gigabit Ethernet PHY
80	TEST_MODE	BOOT_MODE3		Leave this signal unconnected.
81	ETH_TRXN1	ETH_TRXN1		Connected to on-board Gigabit Ethernet PHY
82	JTAG_VCC	PMIC: BUCK7 (NVCC_1V8)		The supply voltage of the JTAG debug interface, 1.8V
83	GND			
84	GND			
85	ETH_TRXP0	ETH_TRXP0		Connected to on-board Gigabit Ethernet PHY
86	JTAG_TCK	JTAG_TCK	No	
87	ETH_TRXN0	ETH_TRXN0		Connected to on-board Gigabit Ethernet PHY
88	JTAG_TMS	JTAG_TMS	No	
89	GND			
90	JTAG_TDI	JTAG_TDI	No	
91	ETH_TRXN3	ETH_TRXN3		Connected to on-board Gigabit Ethernet PHY
92	JTAG_TDO	JTAG_TDO	No	
93	ETH_TRXP3	ETH_TRXP3		Connected to on-board Gigabit Ethernet PHY
94	JTAG_TRST	BOOT_MODE2	No	Leave this signal unconnected.
95	GND			
96	JTAG_MOD	JTAG_MOD	No	
97	ETH_TRXN2	ETH_TRXN2		Connected to on-board Gigabit Ethernet PHY
98	BOOT_CTRL			Pull input low to ground to boot with default settings (controlled by on-board pullup/pulldown resistors. This is the default mode. Connect this pin to the ground via a zero-ohm resistor. Never directly to ground. This would make it easy to leave the pin floating, if ever needed. Leave floating/open to boot from OTP fuses (on the i.MX 8M Nano SoC). Note that the OTP fuses must first be

				programmed, typically via UUU. See chapter 7 for more details about boot control and options.
99	ETH_TRXP2	ETH_TRXP2		Connected to on-board Gigabit Ethernet PHY
100	ISP_ENABLE			Leave floating/open for normal boot. Pull low to ground to place i.MX 8M Nano SoC in USB OTG boot mode (during next power cycle). See chapter 7 for more detail about boot control and options.

The table below lists the pins on expansion connector JC (40-pos connector). **Note that this connector is typically not mounted if the Wi-Fi/BT module is mounted (because the signals available on this connector are all used to connect to the Wi-Fi/BT module).**

JC Pin Number	EAuCOM Board Signal	i.MX 8M Nano Ball Name	Alternative Pin Function?	Notes
1	SD-B_VCC	NVCC_SD1_EXT		The SD1 interface is powered with 1.8V as default. This signal can optionally control voltage level on the SD1 interface. Note: requires a special order for this feature/mounting option.
2	GND			
3	SD-B_CLK	SD1_CLK	Yes	Note. This signal is 1.8V logic level.
4	Board specific	-		Not connected
5	SD-B_CMD	SD1_CMD	Yes	Note. This signal is 1.8V logic level.
6	Board specific	-		Not connected
7	SD-B_DATA0	SD1_DATA0	Yes	Note. This signal is 1.8V logic level.
8	Board specific	-		Not connected
9	SD-B_ DATA1	SD1_DATA1	Yes	Note. This signal is 1.8V logic level.
10	Board specific	-		Not connected
11	SD-B_ DATA2	SD1_DATA2	Yes	Note. This signal is 1.8V logic level.
12	GND			
13	SD-B_ DATA3	SD1_DATA3	Yes	Note. This signal is 1.8V logic level.
14	Board specific	-		Not connected
15	Board specific	SD1_DATA4	Yes	Note. This signal is 1.8V logic level.
16	Board specific	-		Not connected
17	Board specific	SD1_DATA5	Yes	Note. This signal is 1.8V logic level.
18	Board specific	-		Not connected
19	Board specific	SD1_DATA6	Yes	Note. This signal is 1.8V logic level.
20	Board specific	-		Not connected
21	Board specific	SD1_DATA7	Yes	Note. This signal is 1.8V logic level.
22	GND			
23	Board specific	SD1_NRST	Yes	Note. This signal is 1.8V logic level.
24	Board specific	-		Not connected
25	Board specific	SD1_STROBE	Yes	Note. This signal is 1.8V logic level.
26	Board specific	PMIC: BUCK7 (NVCC_1V8)		Power supply for external QSPI memory
27	SAI_TXFS	SAI2_TXFS	Yes	Note. This signal is 1.8V logic level.
28	Board specific	NAND_CE0_B/ QSPIA_NSS0	Yes	Note. This signal is 1.8V logic level.

29	SAI_TXD	SAI2_TXD	Yes	Note. This signal is 1.8V logic level.
30	Board specific	NAND_ALE/ QSPIA_SCLK	Yes	Note. This signal is 1.8V logic level.
31	SAI_TXC	SAI2_TXC	Yes	Note. This signal is 1.8V logic level.
32	GND			
33	SAI_RXD	SAI2_RXD	Yes	Note. This signal is 1.8V logic level.
34	Board specific	NAND_DATA00/ QSPIA_DATA0	Yes	Note. This signal is 1.8V logic level.
35	Board specific	SAI2_RXFS	Yes	Note. This signal is 1.8V logic level.
36	Board specific	NAND_DATA01/ QSPIA_DATA1	Yes	Note. This signal is 1.8V logic level.
37	Board specific	SAI2_RXC	Yes	Note. This signal is 1.8V logic level.
38	Board specific	NAND_DATA02/ QSPIA_DATA2	Yes	Note. This signal is 1.8V logic level.
39	Board specific	SAI2_MCLK	Yes	Note. This signal is 1.8V logic level.
40	Board specific	NAND_DATA03/ QSPIA_DATA3	Yes	Note. This signal is 1.8V logic level.

The table below lists the pins on expansion connector JD (40-pos connector).

JD Pin Number	EAuCOM Board Signal	i.MX 8M Nano Ball Name	Alternative Pin Function?	Notes
1	DSI_DN3	DSI_DN3	No	
2	CSI_CKN	CSI_CKN	No	
3	DSI_DP3	DSI_DP3	No	
4	CSI_CKP	CSI_CKP	No	
5	GND			
6	GND			
7	DSI_DN0	DSI_DN0	No	
8	CSI_DN0	CSI_DN0	No	
9	SDI_DP0	SDI_DP0	No	
10	CSI_DP0	CSI_DP0	No	
11	GND			
12	GND			
13	DSI_DN2	DSI_DN2	No	
14	CSI_DN1	CSI_DN1	No	
15	DSI_DP2	DSI_DP2	No	
16	CSI_DP1	CSI_DP1	No	
17	GND			
18	GND			
19	DSI_DN1	DSI_DN1	No	
20	CSI_DN2	CSI_DN2	No	
21	DSI_DP1	DSI_DP1	No	
22	CSI_DP2	CSI_DP2	No	
23	GND			

24	GND			
25	DSI_CKN	DSI_CKN	No	
26	CSI_DN3	CSI_DN3	No	
27	DSI_CKP	DSI_CKP	No	
28	CSI_DP3	CSI_DP3	No	
29	GND			
30	GND			
31	Board specific	-		Not connected
32	PCIE_RXN	-		Not connected
33	PCIE_CLKREQ_B	-		Not connected
34	PCIE_RXP	-		Not connected
35	GND			
36	GND			
37	PCIE_CLKN	-		Not connected
38	PCIE_TXN	-		Not connected
39	PCIe_CLKP	-		Not connected
40	PCIE_TXP	-		Not connected

4 iMX Developer's Kit V2 – uCOM Adapter Board

This chapter is only relevant if you have an iMX8M Nano uCOM Developer's Kit V2. In that case, a uCOM Adapter Board is needed and this chapter presents this board. **Skip this chapter if you have an iMX8M Nano uCOM Developer's Kit V3.**

Embedded Artists has defined the EACOM board standard that is based on the SMARC form factor; module size 82 x 50 mm. Note that pinning is different from the SMARC standard. See the *EACOM Board specification* document for details and background information. Hereafter this standard will be referred to as **EACOM**.

Embedded Artists has also defined the **EAuCOM** board standard with 42 x 45 mm boards that use Hirose DF40C connectors. The *uCOM Adapter Board* has been designed to convert an EAuCOM board into an EACOM board. This way, the same carrier board can be used for all *iMX Developer's Kits*.

The *iMX8M Nano uCOM Developers Kit V2* consists of:

- One *iMX8M Nano uCOM Board, mounted on*
- One *uCOM Adapter Board*, mounted on
- One *COM Carrier Board V2*

The *uCOM Adapter Board* contains the following functions (see schematic for details):

- MIPI-DSI to HDMI bridge
- MIPI-DSI interface directly to LCD, including backlight LED driver and touch interface
- Boot control
- Battery connector
- JTAG connector
- Optional 3.6V RF supply voltage for uCOM boards with on-board Wi-Fi/BT module
- Possibility to measure input and output currents on supply nets
- Voltage level translation on some signals
- USB multiplexor (for iMX8M Nano, which only have one USB interface)

The carrier board connector has 314 pins with 0.5 mm pitch and the *uCOM Adapter Board* is inserted in a right angle (R/A) style. The connector is originally defined for use with MXM3 graphics cards. There are multiple sources for carrier board (MXM3) connectors due to the popular standard. The signal integrity is excellent and suitable for data rates up to 5 GHz.

4.1 Pin Numbering

The figures below show the pin numbering for *uCOM Adapter Board*, which is compatible with EACOM boards. Top side edge fingers are numbered P1-P156. Bottom side edge fingers are numbered S1-S158. There is an alternative pin numbering that follows the MXM3 standard with even numbers on the bottom and odd numbers on the top. This numbering is from 1-321, with 7 numbers/pins (150-156) removed due to the keying.

The picture below also illustrates where the *iMX8M Nano uCOM board* is mounted on the *uCOM Adapter Board*.

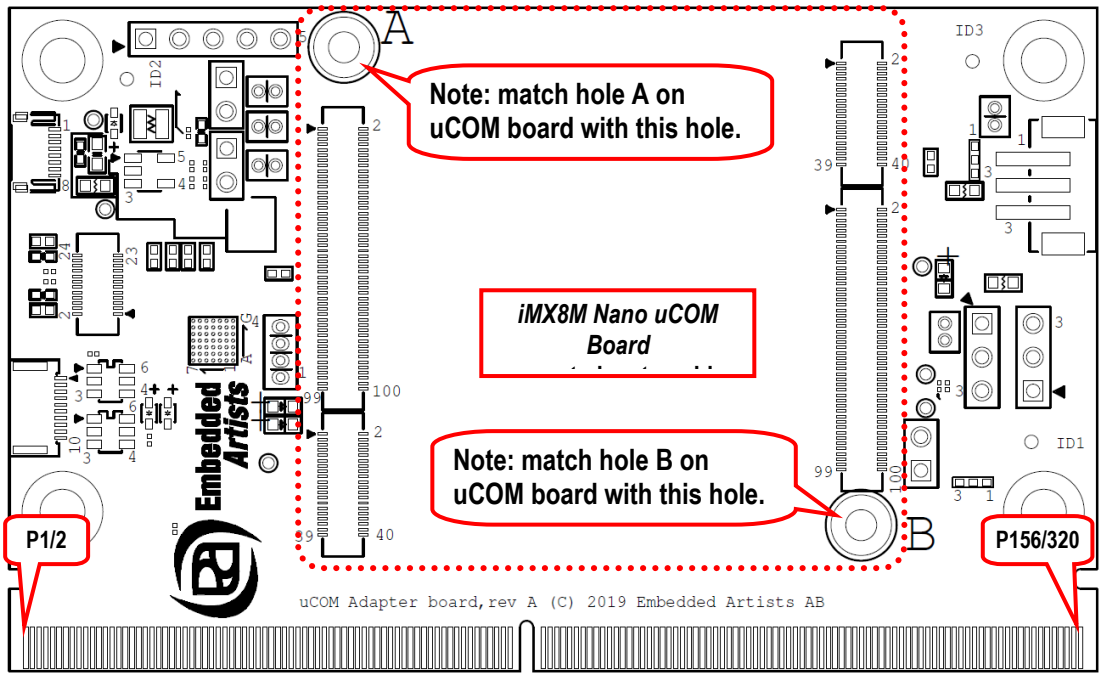

Figure 3 – uCOM Adapter Board Pin Numbering, Top Side

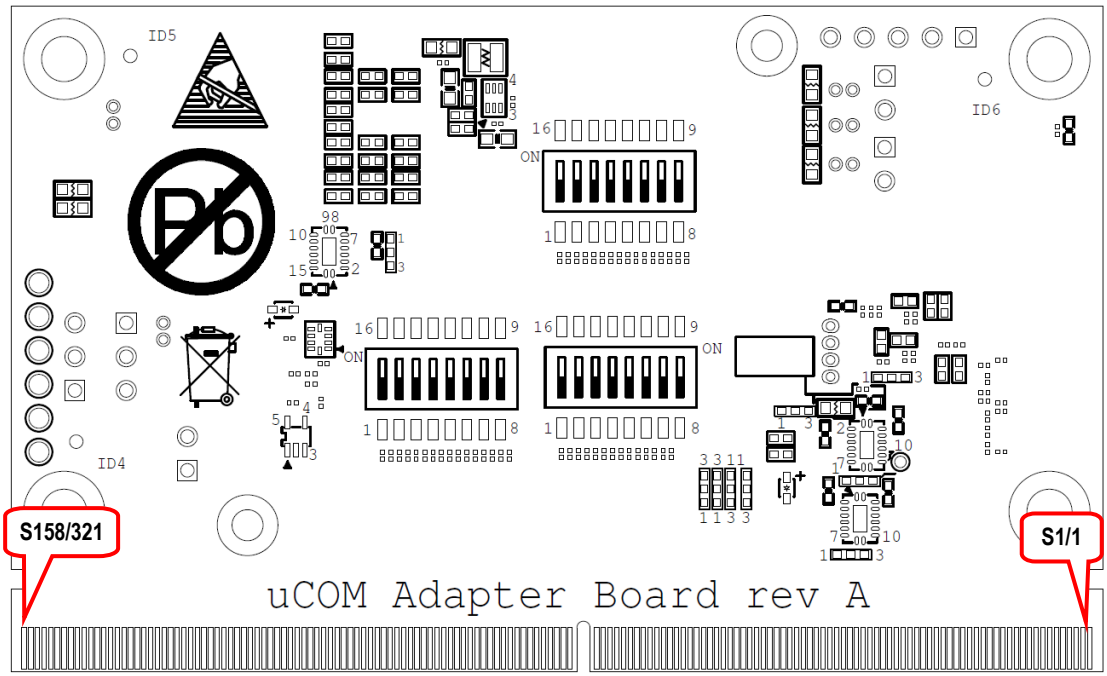

Figure 4 – uCOM Adapter Board Pin Numbering, Bottom Side

4.2 Pin Assignment

This section describes the pin assignment of the board, with the following columns:

Pin number	**Px** are top side edge fingers. **Sx** are bottom side edge fingers. An alternative, consecutive, numbering is also shown with odd numbers on the top and even numbers on the bottom side.

EACOM Board	Describe the typical usage of the pin according to EACOM. This pin usage should be followed to get compatibility between different COM boards. If this is not needed, then any of the alternative functions on the pin can also be used.
i.MX 8M Nano Ball Name	The name of the ball of the i.MX 8M Nano SoC (or other component on the uCOM board) that is connected to this pin.
Notes	When relevant, the preferred pin function is listed.

There are 45 ground pins, which equal to about 15%, and 10 input voltage supply pins.

Note that some pins are EACOM board *type specific*, meaning that these pins might not be compatible with other EACOM boards. Using these may result in lost compatibility between EACOM boards, but not always. Check details between EACOM boards of interest.

Note that not all EACOM-defined pins are connected on anything, typically because an interface is not supported or there are not enough free pins in the i.MX 8M Nano SoC.

Further, some pins are *COM board type specific*, meaning that these pins might not be compatible with other EACOM boards. Using *type specific* pins may result in lost compatibility between EACOM boards, but not always. Check details between EACOM boards of interest.

The table below lists the top side pins, P1-P156, odd numbers.

Top Side Pin Number	EAuCOM Board	EACOM Board	i.MX 8M Nano Ball Name	Alternative pin functions?	Notes
P1/2	JC pin 025 SD-B_STROBE	GPIO-F	SD1_STROBE	Yes	Via 3.3V to 1.8V level translator Hardwired as output from uCOM board (via U7 on uCOM Adapter board) **Note**: Signal has 1.8V logic level.
P2/4	JD pin 033	GPIO-E	I2C4_SCL	Yes	Note: this signal is also available on pin P116/240. The signal has no on-board pull-up resistor.
P3/6	JB pin 039 SD-A_NCD	GPIO-D	SD2_NCD	Yes	**Note**: If NVCC_SD2 is 1.8V, the logic level of this signal will be 1.8V (and not 3.3V). NVCC_SD2 will be 1.8V when accessing an ultra-high speed SD memory card.
P4/8	JB pin 041 SD-A_NRST	GPIO-C	SD2_NRST	Yes	**Note**: If NVCC_SD2 is 1.8V, the logic level of this signal will be 1.8V (and not 3.3V). NVCC_SD2 will be 1.8V when accessing an ultra-high speed SD memory card.
P5/10	JC pin 009 SD-B_DATA1	SD_D1	SD1_DATA1	Yes	**Note**: Signal has 1.8V logic level.
P6/12	JC pin 007 SD-B_DATA0	SD_D0	SD1_DATA0	Yes	**Note**: Signal has 1.8V logic level.
P7/14	JC pin 003 SD-B_CLK	SD_CLK	SD1_CLK	Yes	**Note**: Signal has 1.8V logic level.
P8/16	JC pin 005 SD-B_CMD	SD_CMD	SD1_CMD	Yes	**Note**: Signal has 1.8V logic level.
P9/18	JC pin 013 SD-B_DATA3	SD_D3	SD1_DATA3	Yes	**Note**: Signal has 1.8V logic level.
P10/20	JC pin 011 SD-B_DATA2	SD_D2	SD1_DATA2	Yes	**Note**: Signal has 1.8V logic level.
P11/22	JB pin 019 NVCC_SD	SD_VCC	NVCC_SD2		Supply voltage for SD2 interface (1.8V or 3.3V). This is an output but should never be used to anything else than the SD2 interface.
P12/24	JB pin 029 SD-A_DATA1	MMC_D1	SD2_DATA1	Yes	**Note**: Logic level (3.3V or 1.8V depends on NVCC_SD, which is controlled by the Linux BSP.
P13/26	JB pin 027 SD-A_DATA0	MMC_D0	SD2_DATA0	Yes	**Note**: Logic level (3.3V or 1.8V depends on NVCC_SD, which is controlled by the Linux BSP.

P14/28	Not connected	MMC_D7			Not connected
P15/30	Not connected	MMC_D6			Not connected
P16/32	JB pin 023 SD-A_CLK	MMC_CLK	SD2_CLK	Yes	**Note**: Logic level (3.3V or 1.8V depends on NVCC_SD, which is controlled by the Linux BSP.
P17/34	Not connected	MMC_D5			Not connected
P18/36	JB pin 025 SD-A_CMD	MMC_CMD	SD2_CMD	Yes	**Note**: Logic level (3.3V or 1.8V depends on NVCC_SD, which is controlled by the Linux BSP.
P19/38	Not connected	MMC_D4			Not connected
P20/40	JB pin 033 SD-A_DATA3	MMC_D3	SD2_DATA3	Yes	**Note**: Logic level (3.3V or 1.8V depends on NVCC_SD, which is controlled by the Linux BSP.
P21/42	JB pin 031 SD-A_DATA2	MMC_D2	SD2_DATA2	Yes	**Note**: Logic level (3.3V or 1.8V depends on NVCC_SD, which is controlled by the Linux BSP.
P22/44		GND			
P23/46		HDMI_TXC_N			Connected to DSI-to-HDMI bridge (ADV7533) on uCOM Adapter
P24/48		HDMI_TXC_P			Connected to DSI-to-HDMI bridge (ADV7533) on uCOM Adapter
P25/50		GND			
P26/52		HDMI_TXD0_N			Connected to DSI-to-HDMI bridge (ADV7533) on uCOM Adapter
P27/54		HDMI_TXD0_P			Connected to DSI-to-HDMI bridge (ADV7533) on uCOM Adapter
P28/56		HDMI_HPD			Connected to DSI-to-HDMI bridge (ADV7533) on uCOM Adapter
P29/58		HDMI_TXD1_N			Connected to DSI-to-HDMI bridge (ADV7533) on uCOM Adapter
P30/60		HDMI_TXD1_P			Connected to DSI-to-HDMI bridge (ADV7533) on uCOM Adapter
P31/62		GND			
P32/64		HDMI_TXD2_N			Connected to DSI-to-HDMI bridge (ADV7533) on uCOM Adapter
P33/66		HDMI_TXD2_P			Connected to DSI-to-HDMI bridge (ADV7533) on uCOM Adapter
P34/68		HDMI_CEC			No connection
P35/70		GND			
P36/72	JB pin 079 ETH_TRXP1	ETH1_MD1_P	ETH1_MD1_P		
P37/74	JB pin 081 ETH_TRXN1	ETH1_MD1_N	ETH1_MD1_N		
P38/76		GND			
P39/78	JB pin 085 ETH_TRXP0	ETH1_MD0_P	ETH1_MD0_P		
P40/80	JB pin 087 ETH_TRXN0	ETH1_MD0_N	ETH1_MD0_N		
P41/82	JB pin 073 ETH_LED_1000	ETH1_LINK1000	ETH1_LINK1000		
P42/84	JB pin 075 ETH_LED_ACT	ETH1_ACT	ETH1_ACT		
P43/86	JB pin 071 ETH_LED_10_100	ETH1_LINK	ETH1_LINK		

P44/88	JB pin 091 ETH_TRXN3	ETH1_MD3_N	ETH1_MD3_N		
P45/90	JB pin 093 ETH_TRXP3	ETH1_MD3_P	ETH1_MD3_P		
P46/92		GND			
P47/94	JB pin 097 ETH_TRXN2	ETH1_MD2_N	ETH1_MD2_N		
P48/96	JB pin 099 ETH_TRXP2	ETH1_MD2_P	ETH1_MD2_P		
P49/98		GND			
P50/100	Not connected	ETH2_MD1_P			
P51/102	Not connected	ETH2_MD1_N			
P52/104		GND			
P53/106	Not connected	ETH2_MD0_P			
P54/108	Not connected	ETH2_MD0_N			
P55/110	Not connected	ETH2_LINK1000			
P56/112	Not connected	ETH2_ACT			
P57/114	Not connected	ETH2_LINK			
P58/116	Not connected	ETH2_MD3_N			
P59/118	Not connected	ETH2_MD3_P			
P60/120		GND			
P61/122	Not connected	ETH2_MD2_N			
P62/124	Not connected	ETH2_MD2_P			
P63/126		GND			
P64/128	JB pin 049 USB-A_DN	USB_O1_DN	USB1_DN	No	
P65/130	JB pin 051 USB-A_DP	USB_O1_DP	USB1_DP	No	
P66/132	JB pin 053 USB-A_ID	USB_O1_OTG_ID	USB1_ID	Yes	
P67/134	Not connected	USB_O1_SSTXN			Not connected
P68/136	Not connected	USB_O1_SSTXP			Not connected
P69/138		GND			
P70/140	Not connected	USB_O1_SSRXN			Not connected
P71/142	Not connected	USB_O1_SSRXP			Not connected
P72/144	JB pin 047 USB-A_VBUS	USB_O1_VBUS	USB1_VBUS	No	
P73/146	JB pin 045 USB-A_PWR	USB_O1_PWR_EN	GPIO12	Yes	
P74/148	JB pin 043 USB-A_OC	USB_O1_OC	GPIO13	Yes	
150		Non existing pin			
152		Non existing pin			
154		Non existing pin			
156		Non existing pin			
P75/158	JB pin 059 USB-B_PWR	USB_H1_PWR_EN	GPIO15	Yes	Note: According to the EAuCOM pinning standard, this signal has been allocation to the power-enable output for the USB2 interface. GPIO15 do not have this alternative

					pin function. However, it has USB2_OTG_OC. Allocate the power-enable output as a GPIO output in the Linux *.dts file.
P76/160	JB pin 057 USB-B_OC	USB_H1_OC	GPIO14	Yes	Note: According to the EAuCOM pinning standard, this signal has been allocation to the over-current input for the USB2 interface. GPIO14 do not have this alternative pin function. However, it has USB2_OTG_PWR. Allocate the over-current input as a GPIO input in the Linux *.dts file.
P77/162		GND			
P78/164	Not connected	USB_H1_DN			Not connected
P79/166	Not connected	USB_H1_DP			Not connected
P80/168	Not connected	USB_H1_SSTXN			Not connected
P81/170	Not connected	USB_H1_SSTXP			Not connected
P82/172		GND			
P83/174	Not connected	USB_H1_SSRXN			Not connected
P84/176	Not connected	USB_H1_SSRXP			Not connected
P85/178	Not connected	USB_H1_VBUS			Not connected
P86/180	JA pin 072 Board specific	USB_H2_PWR_EN			Not connected
P87/182	JB pin 072 ONOFF	USB_H2_OC	ONOFF	No	
P88/184		GND			Not connected
P89/186	Not connected	USB_H2_DN			Not connected
P90/188	Not connected	USB_H2_DP			Not connected
P91/190		GND			
P92/192	JC pin 015 SD-B_DATA4	COM board specific	SD1_DATA4	Yes	**Note**: Signal has 1.8V logic level.
P93/194	JC pin 017 SD-B_DATA5	COM board specific	SD1_DATA5	Yes	**Note**: Signal has 1.8V logic level.
P94/196	JC pin 023 SD-B_NRST	COM board specific	SD1_NRST	Yes	**Note**: Signal has 1.8V logic level.
P95/198	Not connected	COM board specific			Not connected
P96/200	Not connected	COM board specific			Not connected
P97/202	Not connected	COM board specific			Not connected
P98/204	Not connected	COM board specific			Not connected
P99/206	Not connected	COM board specific			Not connected
P100/208	Not connected	COM board specific			Not connected
P101/210	Not connected	COM board specific			Not connected
P102/212	Not connected	COM board specific			Not connected
P103/214	Not connected	COM board specific			Not connected
P104/216	Not connected	COM board specific			Not connected
P105/218	Not connected	COM board specific			Not connected
P106/220	Not connected	COM board specific			Not connected
P107/222	Not connected	COM board specific			Not connected
P108/224	Not connected	COM board specific			Not connected
P109/226	Not connected	COM board specific			Not connected
P110/228	JB pin 058	COM board specific	I2C3_SDA	Yes	**Note**: signal has a 2.2Kohm pull-up resistor to 3.3V

	I2C-C_SDA				
P111/230	JB pin 056 I2C-C_SCL	COM board specific	I2C3_SCL	Yes	**Note**: signal has a 2.2Kohm pull-up resistor to 3.3V
P112/232	Not connected	COM board specific			Not connected
P113/234	JB pin 012 GPIO-F	COM board specific	GPIO8	Yes	
P114/236	Not connected	COM board specific			Not connected
P115/238	JB pin 062 I2C-D_SDA	COM board specific	I2C4_SDA	Yes	**Note**: The signal has no on-board pull-up resistor.
P116/240	JB pin 060 I2C-D_SCL	COM board specific	I2C4_SCL	Yes	**Note**: this signal is also available on pin P2/4. The signal has no on-board pull-up resistor.
P117/242	JB pin 002 GPIO-A	COM board specific	GPIO0	Yes	
P118/244		GND			
P119/246	JB pin 044 SPI-B_SSEL	SPI-B_SSEL	ECSPI2_SS0	Yes	
P120/248	JB pin 042 SPI-B_MOSI	SPI-B_MOSI	ECSPI2_MOSI	Yes	
P121/250	JB pin 040 SPI-B_MISO	SPI-B_MISO	ECSPI2_MISO	Yes	
P122/252	JB pin 038 SPI-B_CLK	SPI-B_CLK	ECSPI2_SCLK	Yes	
P123/254	JB pin 034 SPI-A_SSEL	SPI-A_SSEL	ECSPI1_SS0	Yes	
P124/256	JB pin 032 SPI-A_MOSI	SPI-A_MOSI	ECSPI1_MOSI	Yes	
P125/258	JB pin 030 SPI-A_MISO	SPI-A_MISO	ECSPI1_MISO	Yes	
P126/260	JB pin 028 SPI-A_CLK	SPI-A_CLK	ECSPI1_SCLK	Yes	
P127/262		GND			
P128/264	JB pin 013 UART-C_RXD	UART-C_RXD	UART4_RXD	Yes	
P129/266	JB pin 015 UART-C_TXD	UART-C_TXD	UART4_TXD	Yes	
P130/268	JB pin 001 UART-B_RXD	UART-B_RXD	UART1_RXD	Yes	
P131/270	JB pin 009 UART-B_CTS	UART-B_CTS	UART3_RXD	Yes	
P132/272	JB pin 011 UART-B_RTS	UART-B_RTS	UART3_TXD	Yes	
P133/274	JB pin 003 UART-B_TXD	UART-B_TXD	UART1_TXD	Yes	
P134/276	JB pin 005 UART-A_RXD	UART-A_RXD	UART2_RXD	Yes	
P135/278	JB pin 018 GPIO-J	UART-A_CTS			Not connected
P136/280	JB pin 016 GPIO-H	UART-A_RTS			Not connected
P137/282	JB pin 007 UART-A_TXD	UART.A_TXD	UART2_TXD	Yes	
P138/284	JB pin 004	PWM	GPIO1	Yes	

	GPIO-B				
P139/286	JC pin 019 SD-B_DATA6	GPIO-B	SD1_DATA6	Yes	Via 3.3V to 1.8V level translator Hardwired as input to uCOM board (via U7 on uCOM Adapter board) **Note**: Signal has 1.8V logic level.
P140/288	JC pin 021 SD-B_DATA7	GPIO-A	SD1_DATA7	Yes	Via 3.3V to 1.8V level translator Hardwires as input to uCOM board (via D7 on uCOM Adapter board) **Note**: Signal has 1.8V logic level.
P141/290	JB pin 068	PERI_PWR_EN	PMIC: BUCK6 (NVCC_3V3)	No	Enable signal (active high) for carrier board peripheral power supplies. More information about carrier board design can be found in *EACOM Board specification*. **Power enable signal for external peripherals. No external must drive any signal to the i.MX8M Nano SoC before this signal is active.** This signal is connected to the on-board generated 3.3V supply rail.
P142/292	JB pin 074 RESET_IN	RESET_IN	PMIC: PWRON_B		Reset input, active low. A falling edge on this input cause a power cycle reset of the board. There is no need to pull signal high externally. Connects to PMIC (BD71847AMWV) PWRON_B input.
P143/294		RESET_OUT	Copy of POR_B		Reset (open drain) output, active low. Driven low during reset. Has a 10Kohm pull-up resistor to on-board generated 3.3V supply.
P144/296		VIN_SELECT			This output is connected to VIN via a 1Kohm resistor to signal that supply voltage VIN shall be 4.2V. This is for carrier boards that can support EACOM boards that require 3.3V on VIN (in this case, this pin is connected to ground).
P145/298	JA pin 018 VBAT_RTC	VBAT_RTC			Supply voltage from coin cell battery for keeping PMIC and RTC functioning during standby.
P146/300	JB pin 100 ISP_ENABLE	ISP_ENABLE			Should be left open (will write protect the on-board parameter storage E2PROM), or connected to GND (will enable writes to the on-board parameter storage E2PROM and place the i.MX 8M Nano SoC in USB OTG boot mode after a power cycle).
P147/302 P148/304 P149/306 P150/308 P151/310 P152/312 P153/314 P154/316 P155/318 P156/320	JA pin 001 JA pin 002 JA pin 003 JA pin 004 JA pin 005 JA pin 006 JA pin 007 JA pin 008	VIN			Main input voltage supply (4.2V)

The table below lists the bottom side pins, S1-S158, even numbers.

Bottom Side Pin Number	EAuCOM Board	EACOM Board	i.MX 8M Nano Ball Name	Alternative pin functions?	Notes
S1/1	JC pin 035 SAI_RXFS	MQS_RIGHT	SAI2_RXFS	Yes	
S2/3	JC pin 037 SAI_RXC	MQS_LEFT	SAI2_RXC	Yes	
S3/5		GND			
S4/7	JC pin 027 SAI_TXFS	AUDIO_TXFS	SAI2_TXFS	Yes	
S5/9	JC pin 033 SAI_RXD	AUDIO_RXD	SAI2_RXD0	Yes	
S6/11	JC pin 031 SAI_TXC	AUDIO_TXC	SAI2_TXC	Yes	
S7/13	JC pin 029 SAI_TXD	AUDIO_TXD	SAI2_TXD0	Yes	
S8/15	JC pin 039 SAI_MCLK	AUDIO_MCLK	SAI2_MCLK	Yes	
S9/17		GND			
S10/19	JA pin 080 SPDIF_RX	SPDIF_IN	SPDIF_RX	Yes	
S11/21	JA pin 078 SPDIF_TX	SPDIF_OUT	SPDIF_TX	Yes	
S12/23	JB pin 022 GPIO-L	CAN2_TX	GPIO4 (SD2_VSEL)	No	Internal signal connected to SD2_VSEL, controlling voltage level on SD2 interface. Do not connect to this signal.
S13/25	JB pin 020 GPIO-K	CAN2_RX			Not connected
S14/27	JA pin 074 Board specific	CAN1_TX	GPIO4 (SD2_VSEL)	No	Internal signal connected to SD2_VSEL, controlling voltage level on SD2 interface. Do not connect to this signal.
S15/29	JA pin 076 Board specific	CAN1_RX			Not connected
S16/31		GND			
S17/33	Not connected	LVDS1_D3_P			Not connected
S18/35	Not connected	LVDS1_D3_N			Not connected
S19/37	Not connected	GPIO-J			Not connected
S20/39	Not connected	LVDS1_D2_P			Not connected
S21/41	Not connected	LVDS1_D2_N			Not connected
S22/43		GND			
S23/45	Not connected	LVDS1_D1_P			Not connected
S24/47	Not connected	LVDS1_D1_N			Not connected
S25/49		GND			
S26/51	Not connected	LVDS1_D0_P			Not connected
S27/53	Not connected	LVDS1_D0_N			Not connected
S28/55		GND			
S29/57	Not connected	LVDS1_CLK_P			Not connected
S30/59	Not connected	LVDS1_CLK_N			Not connected

S31/61		GND			
S32/63	Not connected	LVDS0_D3_P			Not connected
S33/65	Not connected	LVDS0_D3_N			Not connected
S34/67	Not connected	GPIO-H			Not connected
S35/69	Not connected	LVDS0_D2_P			Not connected
S36/71	Not connected	LVDS0_D2_N			Not connected
S37/73		GND			
S38/75	Not connected	LVDS0_D1_P			Not connected
S39/77	Not connected	LVDS0_D1_N			Not connected
S40/79		GND			
S41/81	Not connected	LVDS0_D0_P			Not connected
S42/83	Not connected	LVDS0_D0_N			Not connected
S43/85		GND			
S44/87	Not connected	LVDS0_CLK_P			Not connected
S45/89	Not connected	LVDS0_CLK_N			Not connected
S46/91	JB pin 050 I2C-A_SDA	I2C-A_SDA	I2C1_SDA	No	Signal must be I2C1_SDA since the signal is connected to on-board PMIC. **Note**: This signal has as 2.2Kohm pullup resistor to an internally generated 3.3V supply.
S47/93	JB pin 048 I2C-A_SCL	I2C-A_SCL	I2C1_SCL	No	Signal must be I2C1_SCL since the signal is connected to on-board PMIC. **Note**: This signal has as 2.2Kohm pullup resistor to an internally generated 3.3V supply.
S48/95	JB pin 054 I2C-B_SDA	I2C-B_SDA	I2C2_SDA	Yes	**Note**: This signal has as 2.2Kohm pullup resistor to an internally generated 3.3V supply.
S49/97	JB pin 052 I2C-B_SCL	I2C-B_SCL	I2C2_SCL	Yes	**Note**: This signal has as 2.2Kohm pullup resistor to an internally generated 3.3V supply.
S50/99		HDMI/I2C-C_SDA			Connected to DSI-to-HDMI bridge (ADV7533) on uCOM Adapter
S51/101		HDMI/I2C-C_SCL			Connected to DSI-to-HDMI bridge (ADV7533) on uCOM Adapter
S52/103	JB pin 006 GPIO-C	TP_RST	GPIO5	Yes	
S53/105	JA pin 100 Board specific	TP_IRQ	SAI5_RXD3	Yes	
S54/107	JA pin 098 Board specific	DISP_PWR_EN	SAI5_RXD2	Yes	
S55/109	JA pin 096 Board specific	BL_PWR_EN	SAI5_RXD1	Yes	
S56/111	JA pin 094 Board specific	BL_PWM	SAI5_RXD0	Yes	
S57/113		GND			
S58/115	JA pin 099 Board specific	LCD_R0	SAI3_RXD	Yes	
S59/117	JA pin 097 Board specific	LCD_R1	SAI3_RXC	Yes	
S60/119	JA pin 095 Board specific	LCD_R2	SAI3_RXFS	Yes	
S61/121	JA pin 093 Board specific	LCD_R3	SAI3_TXD	Yes	

S62/123	JA pin 089 Board specific	LCD_R4	SAI3_TXC	Yes	
S63/125	JA pin 087 Board specific	LCD_R5	SAI3_TXFS	Yes	
S64/127	JA pin 085 Board specific	LCD_R6	SAI3_MCLK	Yes	
S65/129	JA pin 083 Board specific	LCD_R7			Not connected
S66/131	JA pin 079 Board specific	LCD_G0			Not connected
S67/133	JA pin 077 Board specific	LCD_G1			Not connected
S68/135	JA pin 075 Board specific	LCD_G2			Not connected
S69/137	JA pin 073 Board specific	LCD_G3			Not connected
S70/139	JA pin 069 Board specific	LCD_G4			Not connected
S71/141	JA pin 067 Board specific	LCD_G5			Not connected
S72/143	JA pin 065 Board specific	LCD_G6			Not connected
S73/145	JA pin 063 Board specific	LCD_G7			Not connected
S74/147		GND			
S75/149	JA pin 059 Board specific	LCD_B0			Not connected
151		Non existing pin			
153		Non existing pin			
155		Non existing pin			
S76/157	JA pin 057 Board specific	LCD_B1			Not connected
S77/159	JA pin 055 Board specific	LCD_B2			Not connected
S78/161	JA pin 053 Board specific	LCD_B3			Not connected
S79/163	JA pin 049 Board specific	LCD_B4			Not connected
S80/165	JA pin 047 Board specific	LCD_B5			Not connected
S81/167	JA pin 045 Board specific	LCD_B6			Not connected
S82/169	JA pin 043 Board specific	LCD_B7			Not connected
S83/171	JA pin 033 Board specific	LCD_CLK			Not connected
S84/173	JB pin 014 GPIO-G	GPIO-G	GPIO9	Yes	
S85/175	JA pin 035 Board specific	LCD_HSYNC			Not connected
S86/177	JA pin 037 Board specific	LCD_VSYNC			Not connected

S87/179	JA pin 039 Board specific	LCD_ENABLE			Not connected
S88/181		GND			
S89/183	Not connected	AIN_VREF			Not connected
S90/185	Not connected	AIN7			Not connected
S91/187	Not connected	AIN6			Not connected
S92/189	JA pin 090 Board specific	AIN5	SAI5_RXC	Yes	
S93/191	JA pin 088 Board specific	AIN4	SAI5_RXFS	Yes	
S94/193	JA pin 086 Board specific	AIN3	SAI5_MCLK	Yes	
S95/195	JA pin 084 Board specific	AIN2	SPDIF_EXT_CLK	Yes	
S96/197	JD pin 019 DSI_DN1	AIN1	DSI_DN1	No	
S97/199	JD pin 021 DSI_DP1	AIN0	DSI_DP1	No	
S98/201		GND			
S99/203	JD pin 007 DSI_DN0	COM board specific	DSI_DN0	No	
S100/205	JD pin 009 DSI_DP0	COM board specific	DSI_DP0	No	
S101/207		GND			
S102/209	JD pin 025 DSI_CKN	COM board specific	DSI_CKN	No	
S103/211	JD pin 027 DSI_CKP	COM board specific	DSI_CKP	No	
S104/213		GND			
S105/215	Not connected	COM board specific			
S106/217	Not connected	COM board specific			
S107/219	Not connected	COM board specific			
S108/221	Not connected	COM board specific			
S109/223	Not connected	COM board specific			
S110/225	Not connected	COM board specific			
S111/227	JB pin 037 SD-A_WP	COM board specific	SD2_WP	Yes	**Note**: the logic level of this signal can be either 3.3V or 1.8V, depending on signal SD2_VSEL. This can change during run time.
S112/229	JB pin 010 GPIO-E	COM board specific	GPIO7	Yes	
S113/231	JB pin 008 GPIO-D	COM board specific	GPIO6	Yes	
S114/233	Not connected	CSI_HSYNC			Not connected
S115/235	Not connected	CSI_VSYNC			Not connected
S116/237	Not connected	CSI_MCLK			Not connected
S117/239	Not connected	CSI_PCLK			Not connected
S118/241		GND			
S119/243	Not connected	CSI_D0			Not connected
S120/245	Not connected	CSI_D1			Not connected

S121/247	Not connected	CSI_D2			Not connected
S122/249	Not connected	CSI_D3			Not connected
S123/251	Not connected	CSI_D4			Not connected
S124/253	Not connected	CSI_D5			Not connected
S125/255	Not connected	CSI_D6			Not connected
S126/257	Not connected	CSI_D7			Not connected
S127/259		GND			
S128/261	JD pin 026 CSI_DN3	CSI_D3_M	CSI_DN3	No	
S129/263	JD pin 028 CSI_DP3	CSI_D3_P	CSI_DP3	No	
S130/265		GND			
S131/267	JD pin 020 CSI_DN2	CSI_D2_M	CSI_DN2	No	
S132/269	JD pin 022 CSI_DP2	CSI_D2_P	CSI_DP2	No	
S133/271		GND			
S134/273	JD pin 014 CSI_DN1	CSI_D1_M	CSI_DN1	No	
S135/275	JD pin 016 CSI_DP1	CSI_D1_P	CSI_DP1	No	
S136/277		GND			
S137/279	JD pin 008 CSI_DN0	CSI_D0_M	CSI_DN0	No	
S138/281	JD pin 010 CSI_DP0	CSI_D0_P	CSI_DP0	No	
S139/283		GND			
S140/285	JD pin 002 CSI_CKN	CSI_CLK_M	CSI_CKN	No	
S141/287	JD pin 004 CSI_CKP	CSI_CLK_P	CSI_CKP	No	
S142/289		GND			
S143/291	Not connected	SATA_TX_P			Not connected
S144/293	Not connected	SATA_TX_N			Not connected
S145/295		GND			
S146/297	Not connected	SATA_RX_N			Not connected
S147/299	Not connected	SATA_RX_P			Not connected
S148/301		GND			
S149/303		GND			
S150/305	JD pin 039 PCIE_CLKP	PCIE_CLK_P			Not connected
S151/307	JD pin 037 PCIE_CLKN	PCIE_CLK_N			Not connected
S152/309		GND			
S153/311	JD pin 040 PCIE_TXP	PCIE_TX_P			Not connected
S154/313	JD pin 038 PCIE_TXN	PCIE_TX_N			Not connected

S155/315		GND	
S156/317	JD pin 034 PCIE_RXP	PCIE_RX_P	Not connected
S157/319	JD pin 032 PCIE_RXN	PCIE_RX_N	Not connected
S158/321		GND	

5 Pin Mapping

5.1 Functional Multiplexing on I/O Pins

There are a lot of different peripherals inside the i.MX 8M Nano SoC. Many of these peripherals are connected to the IOMUX block, that allows the I/O pins to be configured to carry one of many (up to nine different) alternative functions. This leaves great flexibility to select a function multiplexing scheme for the pins that satisfy the interface need for a particular application.

Some interfaces with specific voltage levels/drivers/transceivers have dedicated pins, like MIPI-DSI, MIPI-CSI and USB. i.MX 8M Nano pins carrying these signals do not have any functional multiplexing possibilities. These interfaces are fixed.

To keep compatibility between EACOM boards the EACOM specified pinning should be followed, but in general there are no restrictions to select alternative pin multiplexing schemes on the *iMX8M Nano uCOM Board*. Note that all EACOM-defined pins are not connected on some EACOM boards, typically because an interface is not supported or there are not enough free pins in the SoC. Further, some EACOM board pins are *type specific*, meaning that these pins might not be compatible with other EACOM boards. Using *type specific* pins may result in lost compatibility between EACOM boards, but not always. Always check details between EACOM boards of interest.

If switching between EACOM boards is not needed, then pin multiplexing can be done without considering the EACOM pin allocation. A custom carrier board design is needed in this case.

Functional multiplexing is normally controlled via the Linux BSP. It can also be done directly via register `IOMUXC_SW_MUX_CTL_PAD_xxx` where `xxx` is the name of the i.MX 8M Nano pin. For more information about the register settings, see the *i.MX 8M Nano Application Processor Reference Manual* from NXP.

Note that input functions that are available on multiple pins will require control of an input multiplexer. This is controlled via register `IOMUXC_xxx_SELECT_INPUT` where `xxx` is the name of the input function. Again, for more information about the register settings see the *i.MX 8M Nano Application Processor Reference Manual* from NXP.

5.1.1 Alternative I/O Function List

There is an accompanying Excel document that lists all alternative functions for each available I/O pin. The reset state is shown as well as the EACOM function allocation. The reset state is typically GPIO, ALT5 function, except for the GPIO1_IO01-15 signals that are ALT0 functions, but that is the GPIO function.

5.2 I/O Pin Control

Each pin also has an additional control register for configuring input hysteresis, pull up/down resistors, push-pull/open-drain driving, drive strength and more. Also in this case, configuration is normally done via the Linux BSP but it is possible to directly access the control registers, which are called `IOMUXC_SW_PAD_CTL_PAD_xxx` where `xxx` is the name of the i.MX 8M Nano pin. For more information about the register settings, see the *i.MX 8M Nano Application Processor Reference Manual* from NXP.

As a general recommendation, select slow slew rate and lowest drive strength (that still result in acceptable signal edges for the system) in order to reduce problems with EMC.

Note that many pins (but not all) are configured as GPIO inputs, some with pull-down resistor, some without, and some with pull-up resistor, after reset. Some pins are configured as Hi-Z outputs. When the bootloader (typically u-boot) executes it is possible to reconfigure the pins.

Also note that due to silicon revision errata in the i.MX8M Nano SoC, the pull-up and pull-down resistors are currently not functional when voltage level is 3.3V, which most of the signals are.

6 Interface Description

The **i.MX 8M Nano datasheet and user manual shall always be consulted** for details about different functions and interfaces. Many interfaces are multiplexed on different pins and not available simultaneously. There is an accompanying Excel document that lists all alternative functions for each available I/O pin. It is recommended to study this document to get an overview of the available pin multiplexing options.

The process of defining the pin/function for a system is:

1. Define which interfaces are needed in the system.
2. Allocate each needed interface to either Cortex-A53 ("Linux side") or M7 side ("real-time side").
3. Consult the Excel sheet and allocate the interfaces to different pins.
    a. If possible, follow the EAuCOM pin and interface allocation. It is not strictly needed, but will simplify if the uCOM board will be replaced in a future update/upgrade.
    b. Note that connector JC (and signals allocated to this connector) will not exist if on-board Wi-Fi/BT module is mounted.
    c. Note that not all signals have 3.3V logic level. Some also have 1.8V logic level.
4. When an suitable pin/function allocation has been done, update the *.dts file under Linux to enable the interfaces that shall be controlled from the A53/Linux side. On the M7 side, peripherals are enabled and initialized via function calls, see the SDK for details.
    a. If pin/function allocation is impossible, the basic architecture under 1) must be reexamined and updated.

This remaining of the chapter is only relevant if you have an iMX8M Nano uCOM Developer's Kit V2. **Skip the rest of this chapter if you have an iMX8M Nano uCOM Developer's Kit V3.**

6.1 Display Interface

The i.MX 8M Nano SoC only has a MIPI-DSI display output. If a display is needed and the display has a MIPI-DSI interface, then the two interfaces can be connected directly. Alternatively, a MIPI-DSI to HDMI or MIPI-DSI to LVDS bridge is used to connect to a display with HDMI or LVDS interface.

The MIPI-DSI interface with two data lanes is allocated to connector JD, see the fourth table in section 3.2 .

The *uCOM Adapter Board* has a MIPI-DSI to HDMI bridge that is connected to the MIPI-DSI interface of the i.MX8M Nano SoC by default. The HDMI connector on the *COM Carrier Board* will carry the HDMI display output.

See section 12.3 for a special note about *COM Carrier Board* versions and how the HDMI DDC I2C channel is connected.

6.2 JTAG

This section lists signals related to the JTAG debug interface.

The i.MX 8M Nano SoC has a module called System JTAG Controller (SJC) that provides a JTAG interface to internal logic, including the ARM Cortex-A53 cores and Cortex-M7 cores. The SJC complies with JTAG TAP standards. The i.MX 8M Nano SoC uses the JTAG port for production, testing, and system debugging.

The i.MX 8M Nano JTAG interface is located on the following pins on connector JB.

JB Pin Number	EAuCOM Board Signal	i.MX 8M Nano Ball Name	Alternative Pin Function?	Notes
JB pin 70	POR_B	POR_B		Connected to RESET0_B on the i.MX 8M Nano SoC. Signal shall normally only be used to connect to debug interface connector. Signal has a 10K ohm pull-up resistor.
JB pin 82	JTAG_VCC	PMIC: BUCK7 (NVCC_1V8)		The supply voltage of the JTAG debug interface. Is connected to the internal 1.8V supply voltage.
JB pin 86	JTAG_TCK	JTAG_TCK	No	Signal has a 10K ohm pull-down resistor.
JB pin 88	JTAG_TMS	JTAG_TMS	No	
JB pin 90	JTAG_TDI	JTAG_TDI	No	
JB pin 92	JTAG_TDO	JTAG_TDO	No	
JB pin 94	JTAG_TRST	BOOT_MODE2	No	Note: this is not a JTAG signal. Leave signal floating.
JB pin 96	JTAG_MOD	JTAG_MOD	No	

The JTAG signals are not available on the MXM3 edge connector. Instead, the signals are available via a 10 pos FPC connector, see picture below for location and orientation.

When using the the *uCOM Adapter Board*, there is a 10 pos FPC connector that is used on all EACOM boards for JTAG access, see picture below for location and orientation.

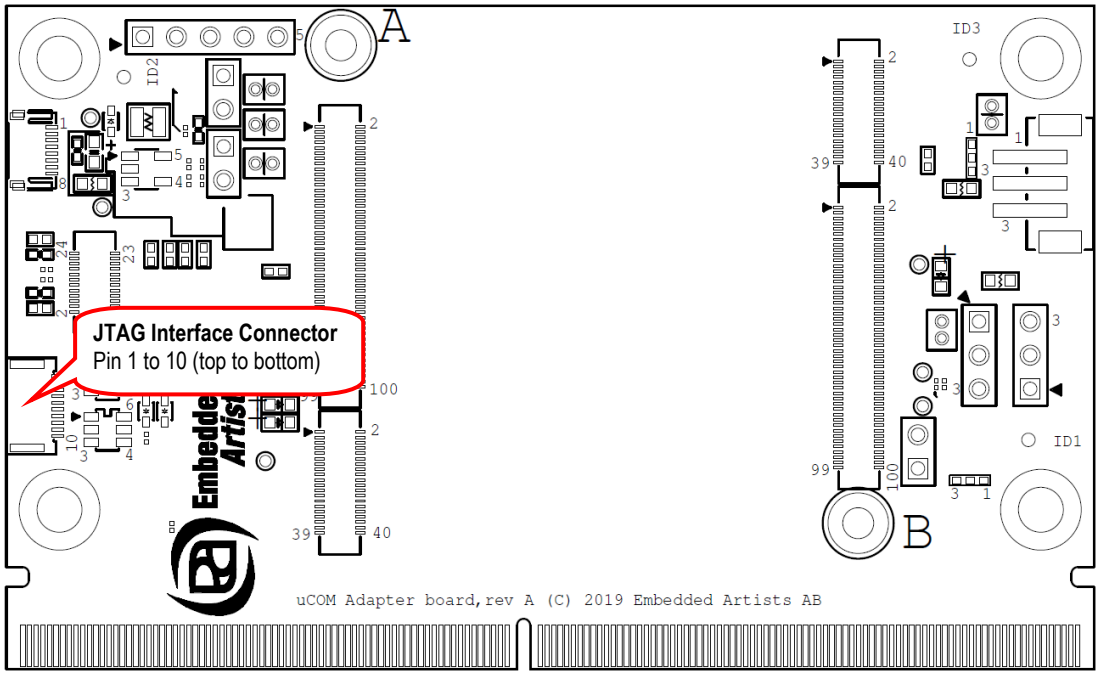

Figure 5 – uCOM Adapter Board, Location of JTAG Interface Connector

The table below lists the 10 signals on the JTAG connector.

JTAG connector Pin Number	Connected to i.MX 8M Nano Ball Name	I/O	Description	Remarks
1	PMIC: BUCK7 (NVCC_1V8)		NVCC_JTAG Logic level supply voltage	Used by external debugger to detect logic level to use for signaling.
2	JTAG_TMS	I	JTAG signal TMS	
3			Ground	
4	JTAG_TCK	I	JTAG signal TCK	Signal has a 10K ohm pull-down resistor.

5			Ground	
6	JTAG_TDO	O	JTAG signal TDO	
7	JTAG_MOD	I	JTAG_MOD	
8	JTAG_TDI	I	JTAG signal TDI	
9	JTAG_TRST	I	JTAG signal TRST	Note: this is not a JTAG signal, but rather BOOT_MODE2. Leave signal floating.
10	POR_B	I	System reset	Signal is active low and controls internal system reset. Signal has a 10K ohm pull-up resistor.

There is on-board ESD protection of the JTAG interface, but it is still important to observe ESD precaution when connecting to this interface. There is no need for external pull-up or pull-down resistors.

The *iMX8M Nano Developer's Kit* contains an adapter board for connection to common debug connectors. The 10 pos connector is Molex 512811094 and has 0.5 mm (20 mil) pitch. FPC length should be kept less than 7 cm.

7 Boot Control

This chapter presents the different boot settings that the *iMX8M Nano uCOM Board* supports.

During development the default boot is fixed to eMMC booting via USDHC3. The slider switches on the bottom side of the *uCOM Adapter board* (if an iMX8M Nano uCOM Developer's Kit **V2**) has no effect on the boot mode. In an end product environment, it is common to control the boot process by programming the OTP fuses, but not strictly needed.

The *iMX8M Nano uCOM Board* supports booting (i.e., from where the i.MX 8M Nano SoC starts downloading code to start executing from) from different sources:

1. On-board eMMC flash, which is the default
2. USB OTG download (also called 'serial download')
3. Other sources, like external SD/MMC memory cards, etc.
   Note that the OTP fuses must be programmed to set the specific source.

Two signals controls the booting source/process, BOOT_CTRL and ISP_ENABLE, see table below:

Boot source	BOOT_CTRL	ISP_ENABLE
Boot from on-board eMMC The board boots according to boot mode 0x02 (eMMC via USDHC3 interface). The boot mode is controlled by on-board logic.	LOW (grounded) Jumper inserted / shorted on carrier board	Floating Jumper open on carrier board
Boot according to OTP fuses (eFuses) • Any boot mode supported by the i.MX 8M Nano SoC and the hardware connected to it can be selected. See *i.MX8M Nano Applications Processor Reference Manual* for details about available sources and OTP fuse settings. • Note that OTP fuse BT_FUSE_SEL must be set to 1 in order to have OTP fuse settings controlling boot source. If not set to 1, the USB OTG boot mode (aka "Serial download") is activated. • Programming OTP fuses is a critical operation. If wrong fuses are programmed boards will likely become unusable and there is no recovery. • Note that *iMX8M Nano uCOM Boards* are delivered without programmed on-chip OTP fuses. Users have full control over these.	Floating Jumper open on carrier board	Floating Jumper open on carrier board
USB OTG This is known as "Serial Download" or "Recovery" mode. This mode is used during development and in production to download the first stage bootloader. It is typically not used by the end-product during normal operation. This mode is activated by pulling signal ISP_ENABLE low regardless of signal BOOT_CTRL.	Do not care	LOW (grounded) Jumper inserted / shorted on carrier board

To summarize:

1. **The *iMX8M Nano uCOM board* is setup to boot from eMMC mode as default. If another source is needed, program the OTP fuses.**
   Leave signal ISP_ENABLE floating and BOOT_CTRL grounded for this mode.
2. If signal ISP_ENABLE is pulled low (grounded), the i.MX 8M Nano SoC boots into USB OTG mode. This mode it typically used during development and also during production (when the program images shall be downloaded the first time). **It is recommended to add a feature on the custom carrier board so that pin ISP_ENABLE can be optionally grounded.**
3. To boot from OTP fuses, leave signal BOOT_CTRL floating and program OTP fuses.

On a custom carrier board, it is recommended to connect signal BOOT_CTRL to the ground via a zero-ohm resistor. Never directly to ground. This would make it easy to leave the pin floating, if ever needed. Also do not forget to control the boot mode with pull-up resistors.

Read section 7.1 - 7.2 (and skip section 7.3) if you have an iMX8M Nano uCOM Developer's Kit V2.

Read section 7.3 (and skip section 7.1 - 7.2) if you have an iMX8M Nano uCOM Developer's Kit V3.

7.1 COM Carrier Board Boot Control Jumpers – Developer's Kit V2

This section describes where to find the two boot control jumpers on the COM Carrier Board. Note that J27 only exist on COM Carrier Board rev E, or later.

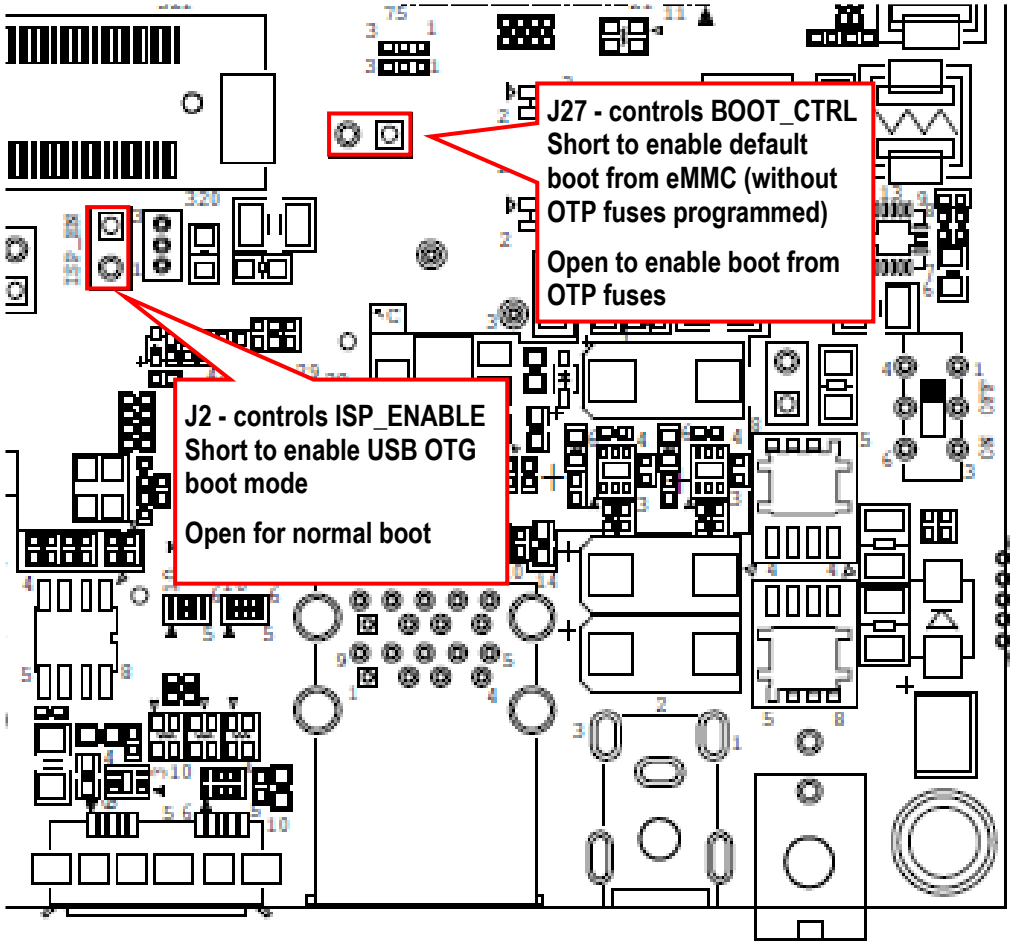

Figure 6 – COM Carrier Board rev E/E1, Boot Control Jumpers

7.2 uCOM Adapter Board Boot Sliders

This section describes how to set the slider switches on the uCOM Adapter Board bottom side for correct boot control.

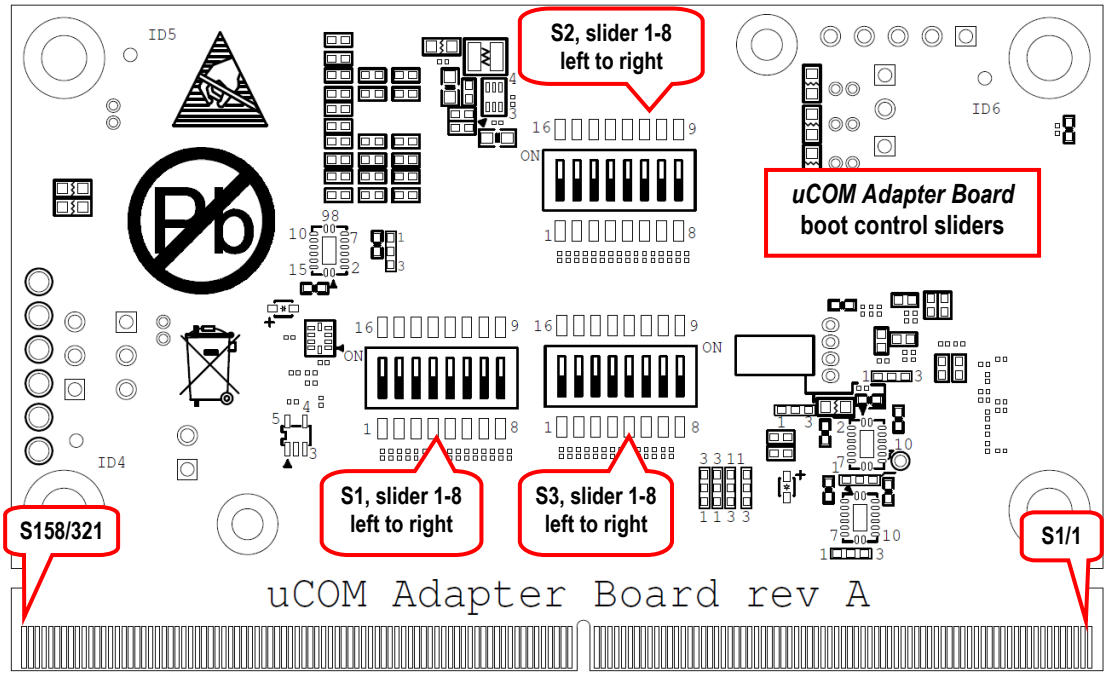

Figure 7 – uCOM Adapter Board Slider Numbering, Bottom Side

Slider Switch	Boot config pin	Default	Description (ON = upper position in Figure 7, OFF = lower position)
S1: 1			Not used
S1:2			Not used
S1:3			Not used
S1:4			Not used
S1:5			Not used
S1:6			Not used
S1:7			Not used
S1:8			Not used
S2:1			Not used
S2:2			Not used
S2:3			Not used
S2:4			Not used
S2:5			Not used
S2:6			Not used
S2:7			Not used

S2:8			Not used
S3:1			Not used
S3:2			Not used
S3:3			Not used
S3:4			Not used
S3:5			Not used
S3:6			Not used
S3:7			Not used
S3:8	USB_SELECT	OFF	OFF: USB-A on uCOM connected to USB-1 (OTG). This is the only setting that is valid when wanting to use USB OTG boot mode. ON: USB-B on uCOM connected to USB-1 (OTG). This connect the single USB interface of the i.MX8M Nano SoC to the USB hub on the *COM Carrier Board*. Note that this setting is **not valid** when wanting to use USB OTG boot mode.

7.3 uCOM Carrier Board Boot Control Jumpers – Developer's Kit V3

This section describes where to find the two boot control jumpers on the uCOM Carrier Board.

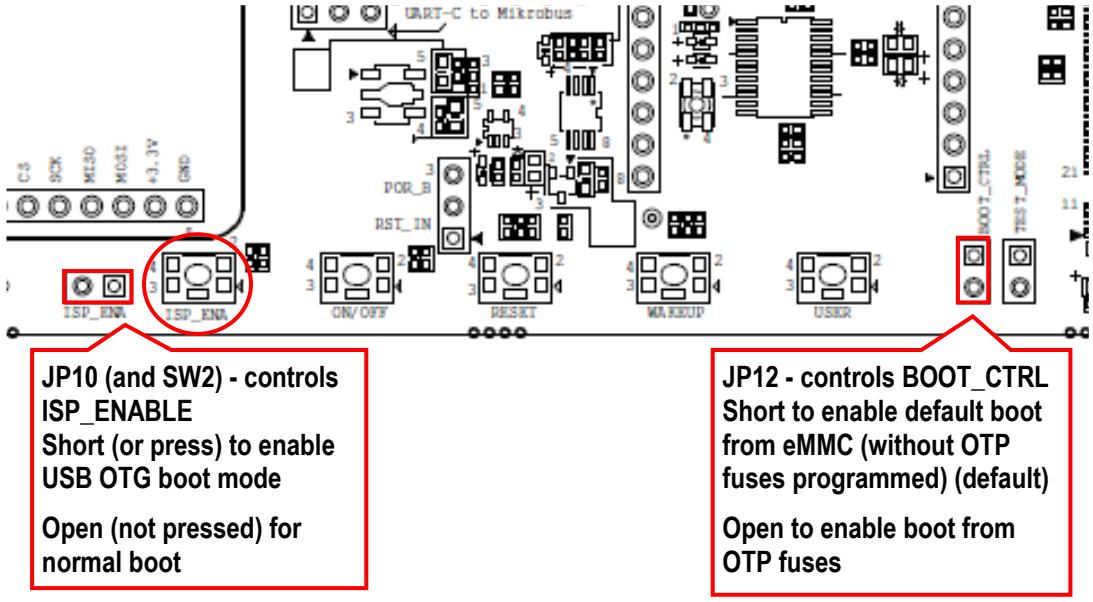

Figure 8 – uCOM Carrier Board, Boot Control Jumpers

8 Powering and PMIC Integration

The i.MX 8M Nano SoC is tightly integrated with the PMIC (BD71847AMWV) in order to achieve high-performance and low-power operation of the *iMX8M Nano uCOM Board*. The BD71847AMWV PMIC is specifically developed for the i.MX 8M Nano SoC. It also includes a real-time clock. See the BD71847AMWV datasheet for details about each function.

The PMIC has multiple linear and DC/DC voltage regulators. Some are available for the carrier board design, reducing integration cost. Designs with moderate power consumptions may not need any external power supply at all. Everything can be handled by the on-board PMIC. Section 8.1 presents the available power rails.

8.1 Available Power Supply Rails

The table below presents the available power rails that can be used on the carrier board that the *iMX8M Nano uCOM Board* is integrated on.

Power Rail Output	Description	Voltage Range	Max Current
NVCC_3V3 **on JA pins 20/22/24/26/28/30**	3.3V for external use.	3.3V	750mA
NVCC_1V8 **on JA pins 19/21/23/25/27/29**	1.8V for external use.	1.8V	500mA

Note that each pin on the Hirose DF40C expansion connectors can carry 300mA maximum. Connect to all pins on the expansion connectors that carry a specific power rail. High current power rails have more than one pin.

Note that external load variations can affect the PMIC operation and potentially disturb the i.MX 8M Nano SoC operation. Make sure that the carrier board electronics does not have abrupt consumption variations and does not generate noise on the power rails. Also **calculate the heat dissipation** of the PMIC in case the carrier board has high current consumption.

8.2 Integration

This integration is very simple. An external 3.5-5.5V supply is basically all that is needed.

- Supply the 3.5-5.0V input voltage to **VSYS_4V2** (connect to all eight pins on connector JA)
- Optionally supply a 3.5-5.0V input voltage to **VBAT_RTC_IN** to power the real-time clock (RTC) and keep it running. If no supply is connected to VBAT_RTC_IN, the RTC is powered from VSYS_4V2 supply input as long as this is valid.
- Leave signals BAT_TEMP, BAT_CURRP and BAT_CURRN unconnected.
- Leave supply inputs PSU_5V on JA pin 54/56/58/60 and VBUS_USB on JA pin 62/64/66/68 unconnected.

9 Murata 1MW Wi-Fi/BT Module Mounting Option

There is a mounting option for the iMX8M Nano uCOM board where a very power-efficient Wi-Fi/BT module, 1MW from Murata is mounted. The picture below illustrates where the 1MW module is mounted in the board. The u.fl. antenna connector is located in the lower left corner.

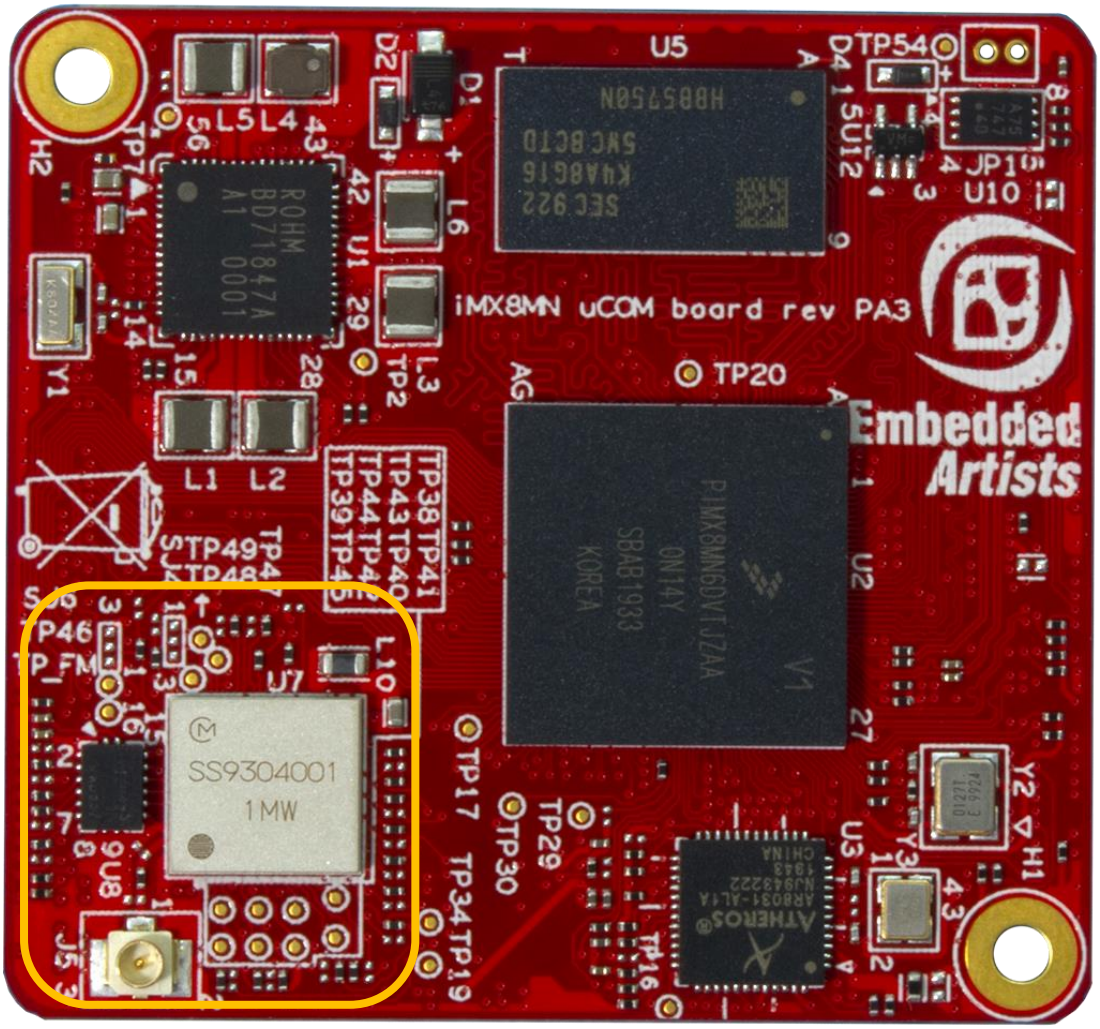

Figure 9 – 1MW Wi-Fi/BT Module Mounted on iMX8M Nano uCOM Board

With this mounting option, JC is not mounted. The signals available on this connector are all used to connect to the Wi-Fi/BT module. A UART channel is also dedicated to the Bluetooth interface, so the following pins are also not available:

- **JB pin 1 (UART-C_RXD/ UART1_RXD)**
- **JB pin 3 (UART-C_TXD/ UART1_TXD)**
- **JB pin 9 (UART-C_CTS/ UART3_RXD)**
- **JB pin 11 (UART-C_RTS/ UART3_TXD)**

The Wi-Fi/BT module is powered by default from the on-board generated 3.3V (from PMIC BUCK6). There is a mounting option that allows for the Wi-Fi/BT module to be powered from an external 3.3-3.6V supply. Contact Embedded Artists for further information.

Note that this version is not a stocked mounting option. A minimum order quantity (MOQ) will apply. Contact Embedded Artists for further information.

10 Technical Specification

10.1 Absolute Maximum Ratings

All voltages are with respect to ground, unless otherwise noted. Stress above these limits may cause malfunction or permanent damage to the board.

Symbol	Description	Min	Max	Unit
VSYS_4V2	Main input supply voltage	-0.3	5.5	V
VBAT_RTC_IN	RTC supply voltage	-0.3	5.5	V
VIO	Vin/Vout (I/O VDD + 0.3): 3.3V IO	0	3.6	V
	Vin/Vout (I/O VDD + 0.3): 1.8V IO	0	1.98	V
USB_xx_VBUS	USB VBUS signals	-0.3	5.25	V
USB_xx_DP/DN	USB data signal pairs	-0.3	3.63	V

10.2 Recommended Operating Conditions

All voltages are with respect to ground, unless otherwise noted.

Symbol	Description	Min	Typical	Max	Unit
VSYS_4V2	Main input supply voltage	3.5		5.0	V
	Ripple with frequency content < 10 MHz			50	mV
	Ripple with frequency content ≥ 10 MHz			10	mV
VBAT_RTC_IN	RTC supply voltage	3.5		5.0	V
	Note: This voltage must remain valid at all times for correct operation of the board (including, but not limited to the RTC).				
USB_xx_VBUS	USB VBUS signals		5	5.25	V

10.3 Power Ramp-Up Time Requirements

Input supply voltages (VIN and VBAT) shall have smooth and continuous ramp from 10% to 90% of final set-point. Input supply voltages shall reach recommended operating range in 1-20 ms.

10.4 Electrical Characteristics

For DC electrical characteristics of specific pins, see i.MX 8M Nano Datasheet. The internal VDD operating point for GPIOs is 3.3V or 1.8V for all signals.

10.4.1 Reset Input

The reset input is triggered by pulling the reset input low (0.2 V max) for 10 us minimum. The internal reset pulse will be 140-560 mS long, before the i.MX 8M Mini boot process starts.

10.5 Power Consumption

There are several factors that determine power consumption of the *iMX8M Nano uCOM Board*, like input voltage, operating temperature, DDR4 activity, operating frequencies for the different cores, DVFS levels and software executed (i.e., Linux distribution).

The values presented are typical values and should be regarded as an estimate. Always measure current consumption in the real system to get a more accurate estimate.

Symbol	Description (VIN = 4.2V, Toperating = 25°C)	Typical	Max Observed	Unit
I_{VIN}_MAX	Maximum CPU load, 1.5 GHz ARM frequency, without Ethernet		TBD	mA
I_{VIN}_IDLE	System idle state, uBoot prompt Linux prompt		TBD TBD	mA
I_{VIN}_DSM	Deep-Sleep mode (DSM), aka "Dormant mode" or "Suspend-to-RAM" in Linux BSP	TBD		mA
I_{VIN}_STB	Linux standby	TBD		mA
I_{VBAT}_BACKUP	Current consumption to keep internal RTC running	TBD		uA

10.6 Mechanical Dimensions

The table below presents the mechanical dimensions of the module.

Dimension	Value (±0.1 mm)	Unit
Module width	42	mm
Module height	45	mm
Module top side height	2.0	mm
Module bottom side height	1.4	mm
PCB thickness	1.4	mm
Mounting hole diameter	2.3	mm
Module weight	2 ±0.5 gram	gram

The picture below illustrates the mechanical details of the *iMX8M Nano uCOM Board*. The outer measurement is 42 x 45 mm. Note that the picture is seen from the bottom side.

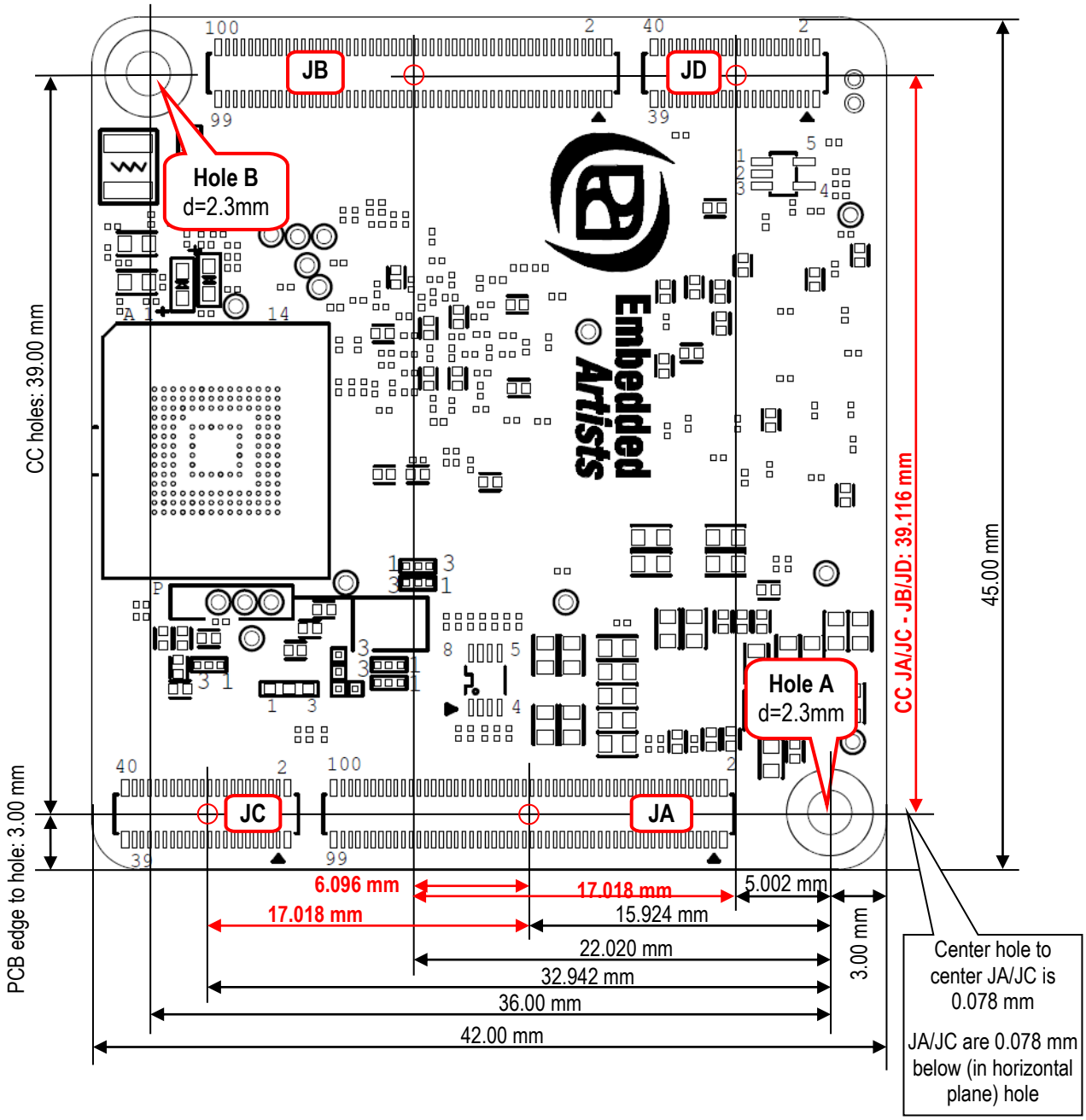

Figure 10 – iMX8M Nano uCOM Board Mechanical Outline, View from Bottom Side

Note that placement of the connectors on the carrier board is very important. They must be parallel and have a placement tolerance of +-0.1mm (non-accumulative). Make sure the relative measures between the connectors (marked with red in the picture above) are correct.

Note that the mounting hole location shall be measured relative to the three connectors, not relative to the pcb edge.

Since the stacking height is only 1.5mm in normal case, make sure no components other than the three connectors are within the dotted red line. When using 3mm stacking height it is possible to have low-profile components under the *iMX8M Nano uCOM Board*. The picture below illustrates the principal dimensions.

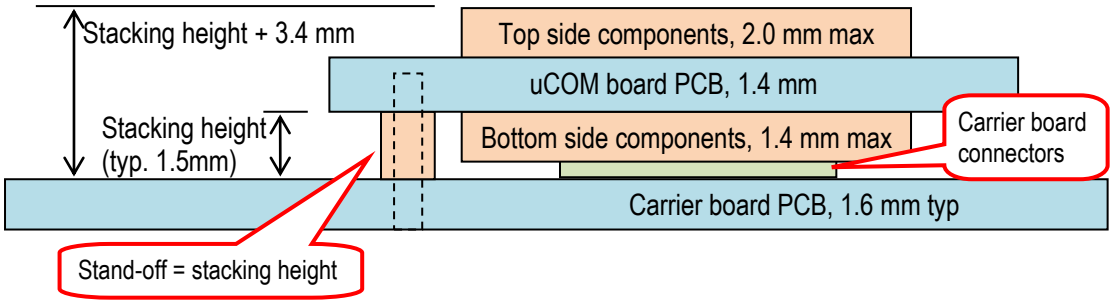

Figure 11 – uCOM Board Mounting on Carrier Board, Stacking Height

10.6.1 DF40C Socket

The headers mounted on the *iMX8M Nano uCOM Board* are DF40C-100DP-0.4V(51) (for JA / JB) and DF40C-40DP-0.4V(51) (for JC / JD).

The receptacles that are needed on the carrier board are, depending on stacking height:

Connector	1.5 mm stacking height (standard)	3.0 mm stacking height
100-pos (JA / JB)	DF40C-100DS-0.4V(51) HRS number: 684-4033-4 51	DF40HC(3.0)-100DS-0.4V(51) HRS number: 684-4151-0 51
40-pos (JC / JD)	DF40C-40DS-0.4V(51) HRS number: 684-4008-7 51	DF40HC(3.0)-40DS-0.4V(51) HRS number: 684-4169-6 51

If any of the connectors are not needed on the carrier board design, these do not have to be mounted. This typically applies to JC and JD.

10.6.2 Module Assembly Hardware

The *iMX8M Nano uCOM Board* has two 2.3mm mounting holes for securing a good mechanical mounting. Use M2 screws and associated standoffs that have the same height as the stacking height (1.5mm or 3 mm, depending on carrier board connectors).

When mounting the iMX8M Nano uCOM board, match hole A on the carrier board with hole A on the uCOM board before the final mounting.

10.7 Environmental Specification

10.7.1 Operating Temperature

Ambient temperature (T_A)

Parameter		Min	Max	Unit
Operating temperature range:	commercial temperature range industrial temperature range	0 -40	70[1] 85[1]	°C °C
Storage temperature range		-40	85	°C
Junction temperature i.MX 8M Nano SoC, operating:	comm. temp. range ind. temp. range.	0 -40	95 105	°C °C

[1] Depends on cooling/heat management solution.

10.7.2 Relative Humidity (RH)

Parameter	Min	Max	Unit
Operating: 0°C ≤ T_A ≤ 70°C, non-condensing (comm. temp. range) Operating: -40°C ≤ T_A ≤ 85°C, non-condensing (ind. temp. range)	10	90	%
Non-operating/Storage: -40°C ≤ T_A ≤ 85°C, non-condensing	5	90	%

10.8 Thermal Design Considerations

Heat dissipation from the i.MX 8M Nano SoC depends on many operating conditions, like operating frequency, operating voltage, activity type, activity cycle duration and duty cycle. Dissipated heat can be up to 3 Watt but is typically much lower.

Whether external cooling is needed, or not, depends on dissipated heat and ambient temperature range. In most cases it is possible to operate the *iMX8M Nano uCOM Board* without external cooling, at least with ambient temperature up to +50° Celsius. Above this, care must be taken not to exceed max junction temperature of the i.MX 8M Nano SoC.

The i.MX 8M Nano SoC implements DVFS (Dynamic Voltage and Frequency Scaling) and Thermal Throttling via the Linux BSP. This enables the system to continuously adjust operating frequency and voltage in response to changes in workload and temperature. In general, this results in higher performance at lower average power consumption.

The i.MX 8M Nano SoC has an integrated temperature sensor for monitoring the junction (i.e., die) temperature, which affects several factors:

- A lower junction temperature, Tj, will result in longer SoC lifetime. See the following document for details: i.MX 8M Nano Product Lifetime Usage.
- A lower die temperature will result in lower power consumption due to lower leakage current.

10.8.1 Thermal Parameters

The i.MX 8M Nano SoC thermal parameters are listed in the table below.

Parameter	Typical	Unit
Thermal Resistance, CPU Junction to ambient ($R_{\theta JA}$), natural convection	22.9	°C/W
Thermal Resistance, CPU Junction to package top ($R_{\theta JC}$)	4	°C/W

10.9 Product Compliance

Visit Embedded Artists' website at http://www.embeddedartists.com/product_compliance for up to date information about product compliances such as CE, RoHS2/3, Conflict Minerals, REACH, etc.

11 Functional Verification and RMA

There is a separate document that presents several functional tests that can be performed on the *iMX8M Nano uCOM Board* to verify correct operation on the different interfaces. Note that these tests must be performed on the carrier board that is supplied with the *iMX8M Nano uCOM Developer's Kit* and with a precompiled kernel from Embedded Artists.

The tests can also be done to troubleshoot a board that does not seem to operate properly. It is strongly advised to read through the list of tests and actions that can be done before contacting Embedded Artists. The different tests can help determine if there is a problem with the board, or not. For return policy, please read Embedded Artists' General Terms and Conditions document (http://www.embeddedartists.com/sites/default/files/docs/General_Terms_and_Conditions.pdf).

12 Things to Note

This chapter presents a number of issues and considerations that users must note.

12.1 Shared Pins and Multiplexing

The i.MX 8M Nano SoC has multiple on-chip interfaces that are multiplexed on the external pins. It is not possible to use all interfaces simultaneously and some interface usage is prohibited by the *iMX8M Nano uCOM* on-board design. Check if the needed interfaces are available to allocation before starting a design. See chapter 5 for details.

12.2 Use COM Carrier Board, rev E/E1 or Later

When using the *iMX8M Nano uCOM board*, only use *COM Carrier Board* rev E/E1, or later. Earlier *COM Carrier Board* versions do not support the 4.2V input supply voltage that is needed for the iMX8M Nano uCOM board.

Note that *iMX Developer's Kits* that use the *COM Carrier Board* rev E/E1, or later, are called "*iMX Developer's Kits V2*".

Also note that there is a newer iMX8M Nano Developer's Kit V3 that is sold from 2021.

12.3 COM Carrier Board Revision and HDMI Interface

This section is only relevant if you have an iMX8M Nano uCOM Developer's Kit V2. **Skip it if you have an iMX8M Nano uCOM Developer's Kit V3.**

Two versions of the COM Carrier board have been released, rev E and rev E1. Of these, only the latest revision (rev E1 and later) will allow the HDMI DDC interface to work correctly, see table below:

Board revisions	COM Carrier Board, rev E HDMI DDC interface connected to I2C-B	COM Carrier Board, rev E1 HDMI DDC interface connected to I2C-C
iMX8M Nano uCOM board, rev A plus **uCOM Adapter Board, rev A/A1** HDMI DDC interface connected to I2C-C by default	On *uCOM Adapter Board*, move zero ohm resistors (0402 size) on SJ4, SJ5, SJ7 and SJ8 to 2-3 position (from 1-2 position). The HDMI DDC interface will be using I2C-B interface after the rework. Note that after the rework, the M.2 I2C connection will no longer work (PCA expander).	Will work out-of-the-box.

12.4 Handle the uCOM Board with Great Care

Handle the *iMX8M Nano uCOM board* with great mechanical care. Only remove/unmount it from the *uCOM Carrier board* if absolutely needed. Only use small movements and small force. Do not insert a screwdriver between the uCOM board and uCOM Carrier board and bend without having first watched the Youtube video we have published about this topic:
https://www.youtube.com/watch?v=-a1UGi_rrLM, title "How to mount and unmount a uCOM board"

12.5 Note uCOM Orientation When Mounting

It is possible to mount the uCOM board with incorrect orientation. Doing that will damage the uCOM board beyond repair and can also damage the carrier board. Make sure (production) mounting instructions are particular about the orientation and how to identify the correct orientation of the uCOM. It is recommended to add notes on the silk screen on the carrier board to make operators aware of the issue. The picture below illustrates the silk screen text found on the *uCOM Carrier Board*.

Always match the "A" and "B" marking on the uCOM with the "A" and "B" on the *Carrier Board*.

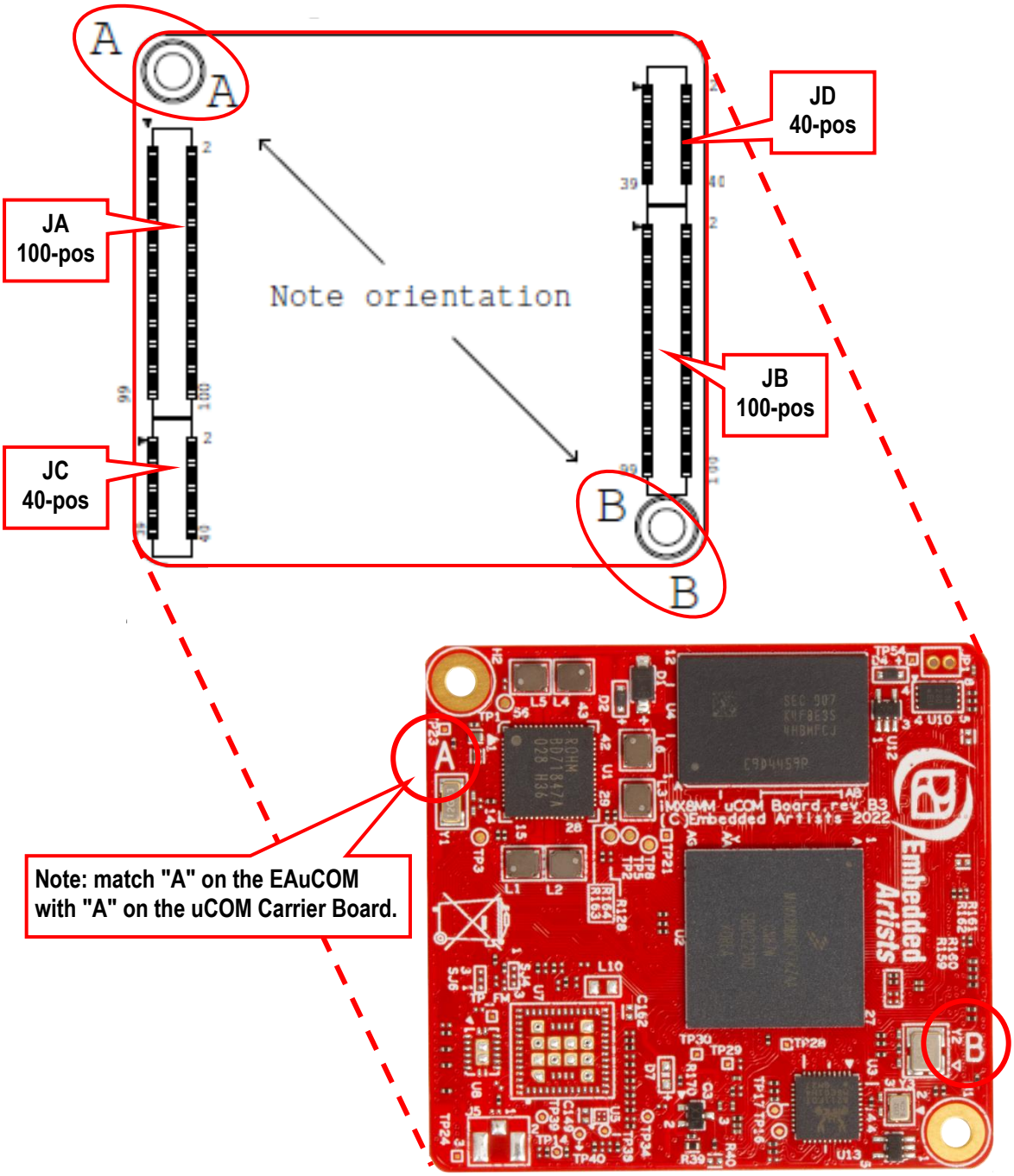

Figure 12 – Orientation of uCOM Board when Mounting on Carrier Board

12.6 uCOM Adapter Board rev A/A1 and Different uCOM Modules

This section is only relevant if you have an iMX8M Nano uCOM Developer's Kit V2. **Skip it if you have an iMX8M Nano uCOM Developer's Kit V3.**

The *uCOM Adapter Board* is designed for different uCOM modules that can have different voltage levels on signals with common pinning. One such example is UART-B, which has 1.8V logic level on the *iMX7ULP uCOM* and 3.3V on the *iMX8M Nano uCOM*.

On rev A of the uCOM Adapter board, SJ10 controls the logic level on UART-B signals and need to be differently set for the two uCOM modules. The picture below illustrates where SJ10 can be found and the two settings available.

Note that SJ10 will be correctly set when buying an *iMX 8M Nano uCOM Developer's Kit* or an *iMX7ULP uCOM Developer's Kit* but when switching uCOM modules on a *uCOM Adapter Board* SJ10 must be checked and adjusted, if needed.

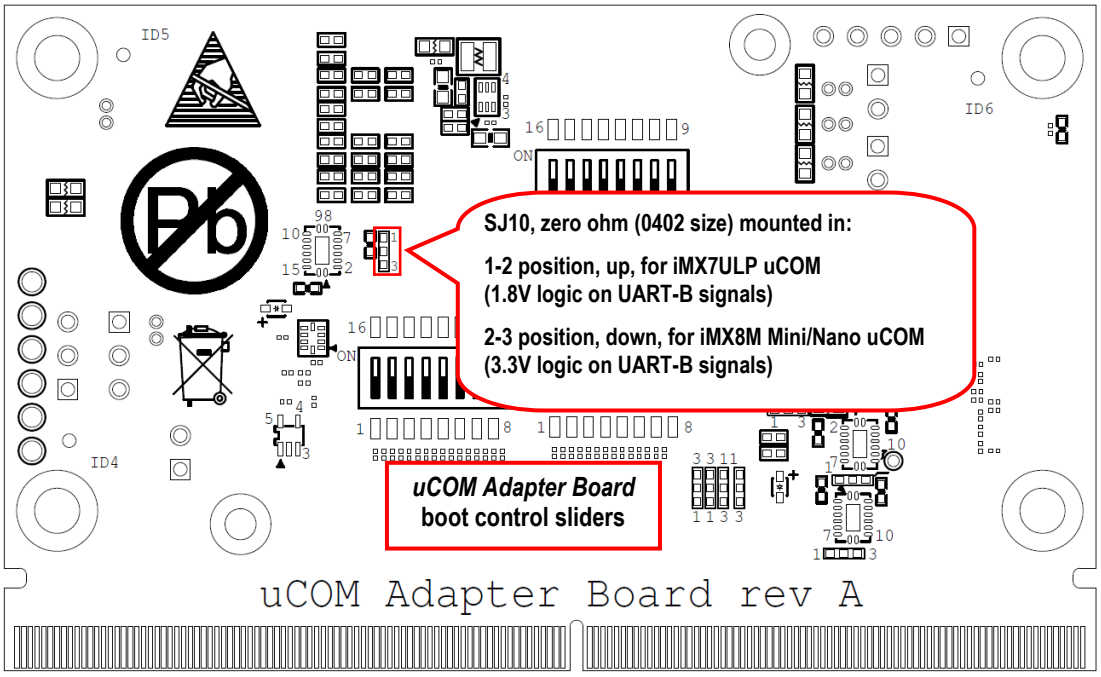

Figure 13 – uCOM Adapter Board rev A, SJ10 Location, Bottom Side

On rev A1 of the uCOM Adapter board, J13 controls the logic level on UART-B signals and need to be differently set for the two uCOM modules. The picture below illustrates where J13 can be found and the two settings available.

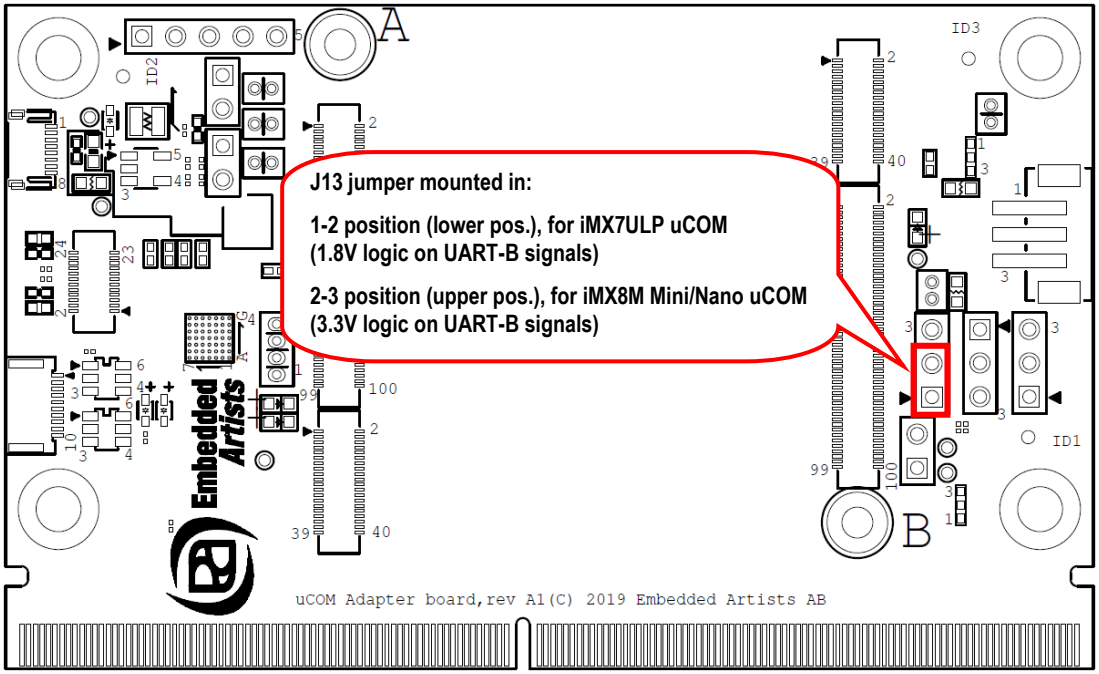

Figure 14 – uCOM Adapter Board rev A1, J13 Location, Top Side

12.7 uCOM Adapter Board rev A/A1 and J12 Usage

This section is only relevant if you have an iMX8M Nano uCOM Developer's Kit V2. **Skip it if you have an iMX8M Nano uCOM Developer's Kit V3.**

The *uCOM Adapter Board* is designed to support different uCOM modules that can have slightly different behavior and functionality. Most uCOM boards control the PERI_PWR_EN signal from hardware. For these boards J12 shall be in the default 1-2 position. When using UUU to download new images, the console (UART) will work as expected.

When using the iMX7ULP uCOM board, the signal PERI_PWR_EN signal is controlled from the Cortex-M4 application. On an unprogrammed board (from production), signal PERI_PWR_EN is always inactive and the console (UART) communication channel will then not be powered. By moving J12 to 2-3 position, signal PERI_PWR_EN is a copy of the reset signal and will allow the console (UART) will work as expected even though the Cortex-M4 application is not programmed.

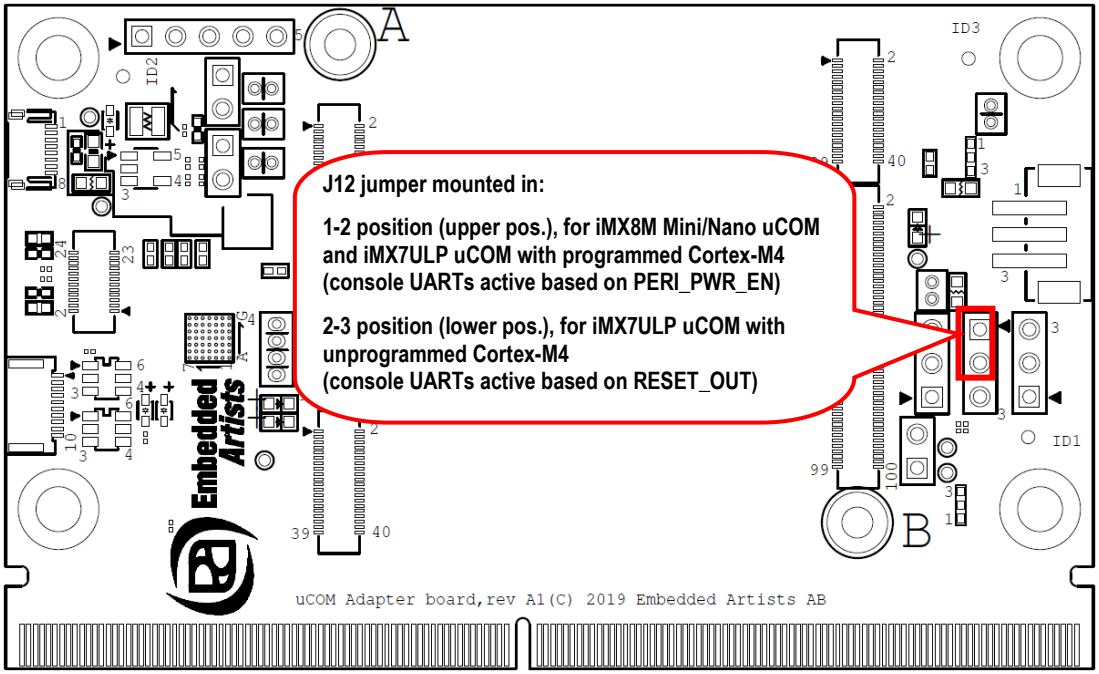

Figure 15 – uCOM Adapter Board rev A/A1, J12 Location, Top Side

12.8 LIBUSB_ERROR_PIPE message during UUU flashing

There is an issue with iMX8M Nano during UUU flashing. It is documented in NXP's errata for the processor: USB Serial Download mode supports maximum 3 devices per USB host. The issue is that the ROM USB HID driver supports up to a maximum of 3 devices per host for simultaneous download, when the SOC is in Serial Download mode. The work around is to allows up to 3 devices to be connected to a single USB host channel (when in Serial Download Mode, also known as USB OTG boot mode).

There seems to be also a random issue when using the "RAM-Linux" downloaded in UUU. Note that this is only observed with the Linux kernel downloaded in RAM from UUU, never in the final Linux kernel. What is observed from time to time (but not always), is that flashing is aborted with an error message on the PC stating LIBUSB_ERROR_PIPE. The error occurs when the file system is being flashed on the target and it can appear at any time during that operation.

Tests have shown that connecting the USB cable for flashing directly to a USB3 port on the PC and without using any USB hubs increases the chances of success.

The solution that Embedded Artists has right now (October 2020) is to switch from the .tar.bz2 packed root file system that we use today to a .wic file. The reason why this file format change makes a difference is that the wic file can be flashed from the u-boot while the .tar.bz2 format requires the target to boot into Linux.

Flashing using the wic fil has never reporter to fail:

The old way to flash the file system:
1) Copying tmp/deploy/images/imx8mnea-ucom/ea-image-base-imx8mnea-ucom.tar.bz2 file from your yocto build to the files/ folder of uuu
2) Run "uuu full_tar.uuu"

The new way:
1) On your machine that you run yocto on, go to the build dir, for example ea-bsp/build-dir/
2) Copy and then unpack the wic-file
   $ cp tmp/deploy/images/imx8mnea-ucom/ea-image-base-imx8mnea-ucom.wic.bz2 .
   $ bunzip2 -d -k ea-image-base-imx8mnea-ucom.wic.bz2

3) Copy ea-image-base-imx8mnea-ucom.wic to the files/ folder of uuu on your PC
4) Run "uuu wic_example.uuu"

Note 1: After flashing the .wic file the file system will not take up all the space on the eMMC as it will when you use .tar.bz2. Embedded Artists is working on a solution but it is not ready for publishing. Contact Embedded Artists for guidance if this is an issue.

Note 2: The wic_example.uuu is only available in uuu zip files from http://imx.embeddedartists.com after 2020-10-26 and only for 5.4.24 and later.

12.9 Only Use EA Board Support Package (BSP)

The *iMX8M Nano uCOM board* uses multiple on-board interfaces for the internal design, for example PMIC, eMMC and watchdog. Only use the BSP that is delivered from Embedded Artists. Do not change interface initialization and/or pin assignment for the on-board interfaces. Changing BSP settings can result in permanent board failure.

Note that Embedded Artists does not replace iMX8M Nano uCOM Boards that have been damaged because of improper interface initialization and/or improper pin assignment.

12.10 OTP Fuse Programming

The i.MX 8M Nano SoC has on-chip OTP fuses that can be programmed, see NXP documents *iMX 8M Nano Datasheet* and *iMX 8M Nano Reference Manual* for details. Once programmed, there is no possibility to reprogram them.

iMX8M Nano uCOM Boards are delivered without any OTP fuse programming. It is completely up to the COM board user to decide if OTP fuses should be programmed and, in that case, which ones.

Note that Embedded Artists does not replace iMX8M Nano uCOM Boards because of wrong OTP programming. It's the user's responsibility to be absolutely certain before OTP programming and not to program the fuses by accident.

12.11 Write Protect on Parameter Storage E2PROM

The parameter storage E2PROM contains important system data like DDR memory initialization settings and Ethernet MAC addresses. The content should not be erased or overwritten. The E2PROM is write protected if signal ISP_ENABLE (JB pin 100 on DF40C connector and P146/300 on MXM3 connector) is left unconnected, i.e. floating. This should always be the case.

Note that all carrier board design should include the possibility to ground this pin.

The signal ISP_ENABLE has dual functions. By pulling the signal low, the i.MX 8M Nano SoC will boot into USB OTG boot mode (also called 'serial download' or 'factory recovery' mode).

12.12 Integration - Contact Embedded Artists

It is strongly recommended to contact Embedded Artists at an early stage in your project. A wide range of support during evaluation and the design-in phase are offered, including but not limited to:

- iMX Developer's Kit to simplify evaluation
- Custom Carrier board design, including 'ready-to-go' standard carrier boards
- Display solutions

- Mechanical solutions
- Schematic review of customer carrier board designs
- Driver and application development

The *iMX8M Nano uCOM Board* targets a wide range of applications, such as:

- HMI/GUI solutions
- Connected vending machines
- Point-of-Sale (POS) applications
- Access control panels
- Audio
- IP phones
- Smart appliances
- Home energy management systems
- Industrial automation
- HVAC Building and Control Systems
- Smart Grid and Smart Metering
- Smart Toll Systems
- Data acquisition
- Communication gateway solutions
- Connected real-time systems
- ...and much more

For more harsh use and environments, and where fail-safe operation, redundancy or other strict reliability or safety requirements exists, always contact Embedded Artists for a discussion about suitability.

There are application areas that the *iMX8M Nano uCOM Board* is not designed for (and such usage is strictly prohibited), for example:

- Military equipment
- Aerospace equipment
- Control equipment for nuclear power industry
- Medical equipment related to life support, etc.
- Gasoline stations and oil refineries

If not before, **it is essential to contact Embedded Artists before production begins**. In order to ensure a reliable supply for you, as a customer, we need to know your production volume estimates and forecasts. Embedded Artists can typically provide smaller volumes of the *iMX8M Nano uCOM Board* directly from stock (for evaluation and prototyping), but **larger volumes need to be planned**.

The more information you can share with Embedded Artists about your plans, estimates and forecasts the higher the likelihood is that we can provide a reliable supply to you of the *iMX8M Nano uCOM Board*.

12.13 ESD Precaution when handling iMX8M Nano uCOM Board

Please note that the *iMX8M Nano uCOM Board* come without any case/box and all components are exposed for finger touches – and therefore extra attention must be paid to ESD (electrostatic discharge) precaution, for example use of static-free workstation and grounding strap. Only qualified personnel shall handle the product.

Make it a habit always to first touch the mounting hole (which is grounded) for a few seconds with both hands before touching any other parts of the boards. That way, you will have the same potential as the board and therefore minimize the risk for ESD.

In general, touch as little as possible on the boards in order to minimize the risk of ESD damage. The only reasons to touch the board are when mounting/unmounting it on a carrier board.

Note that Embedded Artists does not replace boards that have been damaged by ESD.

12.14 EMC / ESD

The *iMX8M Nano uCOM Board* has been developed according to the requirements of electromagnetic compatibility (EMC). Nevertheless, depending on the target system, additional anti-interference measurement may still be necessary to adhere to the limits for the overall system.

The *iMX8M Nano uCOM Board* must be mounted on carrier board (typically an application specific board) and therefore EMC and ESD tests only make sense on the complete solution.

No specific ESD protection has been implemented on the *iMX8M Nano uCOM Board*. ESD protection on board level is the same as what is specified in the i.MX 8M Nano SoC datasheet. **It is strongly advised to implement protection against electrostatic discharges (ESD) on the carrier board** on all signals to and from the system. Such protection shall be arranged directly at the inputs/outputs of the system.

13 Custom Design

This document specifies the standard *iMX8M Nano uCOM Board* design. Embedded Artists offers many custom design services. Contact Embedded Artists for a discussion about different options.

Examples of custom design services are:

- Mounting a Wi-Fi/BT module.
- Different memory sizes on SDRAM and eMMC Flash.
- Different I/O voltage levels on all or parts of the pins.
- Different mounting options, for example remove Ethernet interface.
- Different pinning on DF40C connectors.
- Different board form factor, for example SODIMM-200, high-density connectors on bottom side or MXM3 compatible boards that are higher (>50 mm).
- Different input supply voltage range.
- Single Board Computer solutions, where the core design of the *iMX8M Nano uCOM Board* is integrated together with selected interfaces.
- Changed internal pinning to make certain pins available.

Embedded Artists also offers a range of services to shorten development time and risk, such as:

- Standard Carrier boards ready for integration
- Custom Carrier board design
- Display solutions
- Mechanical solutions

14 Disclaimers

Embedded Artists reserves the right to make changes to information published in this document, including, without limitation, specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Customer is responsible for the design and operation of their applications and products using Embedded Artists' products, and Embedded Artists accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Embedded Artists' product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. Customer is required to have expertise in electrical engineering and computer engineering for the installation and use of Embedded Artists' products.

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Embedded Artists does not accept any liability and no warranty is given for any unexpected software behavior due to deficient components.

Customer is required to take note of manufacturer's specification of used components, for example PMIC and eMMC. Such specifications, if applicable, contain additional information that must be taken note of for the safe and reliable operation. These documents are stored on Embedded Artists' product support page.

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