Features

- Analog Switch Voltage: 3.3V, 5V, 10V, ±5V
- Low ON-State Resistance:
  - typical 50Ω at Vs = ±4.5V or 9V
  - typical 60Ω at Vs = 4.5V
  - typical 300Ω at Vs = 3V
- Bandwidth: 200 MHz
- Fast switching times: t_{ON} = 60ns, t_{OFF} = 50ns
- Break-Before-Make Switching
- Operation Temperature Range: –40°C to 125°C

Applications

- Industry control systems
- Battery-powered systems
- Audio Signal Routing
- Instrumentation

Description

The TPW4051 is a single-pole octal-throw analog switch (SP8T) suitable for use in analog or digital 8:1 multiplexer/demultiplexer applications. The switch features three digital select inputs (S0, S1 and S2), eight independent inputs/outputs (An), a common input/output (A) and a digital enable input (/E). When /E is HIGH, the switches are turned off.

The device is designed on an enhanced process that provides lower power dissipation yet gives high switching speeds. These devices can operate equally well as either multiplexers or de-multiplexers and have an input range that extends to the supplies. All channels exhibit break-before-make switching action, preventing momentary shorting when switching channels.

Switch Selection Guide

Product	Switch Configuration	Supply Voltage(V)	Ron(OHM)	Bandwidth(MHz)	Package
TPW4051	8:1	12	50	200	SOIC-16, TSSOP-16, QFN-16
TPW4052	(4:1)*2	12	50	200	SOIC-16, TSSOP-16
TPW4053	(2:1)*3	12	50	200	SOIC-16, TSSOP-16
TPW3111	1:1	5.5	1	100	SC70-5
TPW3115	1:1	5.5	5	250	SC70-5, SOT23-5
TPW4157	2:1	5.5	1	100	SC70-6
TPW3157A	2:1	5.5	2	100	SC70-6
TPW3221	(2:1)*2	5.5	1	100	MSOP-10
TPW3223	(2:1)*2	5.5	1	100	QFN-10, 1.4*1.8mm

Table of Contents

Revision History

Date	Revision	Notes
2018/8/8	Rev.Pre	Pre-Release Version
2019/3/4	Rev.0	Initial Version
2019/10/2	Rev.0.01	HBM: 2KV -> 1KV
2019/12/25	Rev.0.02	Correct test conditions of RON and switch leakage to follow the product test(Product test is not changed): all of “0V” -> “VEE”; On Resistance Match between Channels at 3 to 3.6V Vcc: -> remove; On Resistance Match between Channels at 9 to 11V Vcc: VIS = 3.5V -> VIS = 1V; On Resistance Match between Channels at 4.5 to 5.5V Vcc, Vee = -4.5V to 5.5V: VIS = 3.5V -> VIS = -3.5V
2020/1/14	Rev.0.03	Correct the “P0” information of TR in Tape and Reel Information
2020/11/26	Rev.A.0	Correct the Quantity of TPW4051-QF4R in order information: 3000 -> 4000
2022/4/21	Rev.A.1	Add the thermal information and update the high POD of QFN-16 package

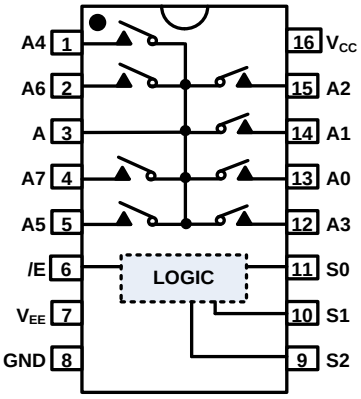
Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity
TPW4051-SR	-40 to 125°C	16-Pin SOIC	W4051	3	Tape and Reel, 2500
TPW4051-TR	-40 to 125°C	16-Pin TSSOP	W4051	3	Tape and Reel, 3000
TPW4051-QF4R	-40 to 125°C	16-Pin QFN3X3	W4051	3	Tape and Reel, 4000

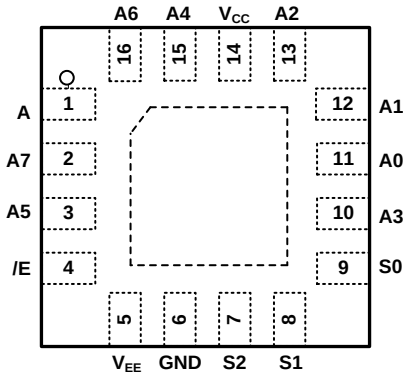
Pin Configuration, Description and Functional Table Note 1

TPW4051

TPW4051
16-Pin SOIC/TSSOP



TPW4051
16-Pin QFN 3*3



Pin Description of SOIC and TSSOP

Pin No.	Pin Name	Input / Output	Description	Pin No.	Pin Name	Input / Output	Description
1	A4	Input / Output	Channel 4 input or output	9	S2	Input	Control Input
2	A6	Input / Output	Channel 6 input or output	10	S1	Input	Control Input
3	A	Input / Output	Common input or output	11	S0	Input	Control Input
4	A7	Input / Output	Channel 7 input or output	12	A3	Input / Output	Channel 3 input or output
5	A5	Input / Output	Channel 5 input or output	13	A0	Input / Output	Channel 0 input or output
6	/E	Input	Enable switchs, active low	14	A1	Input / Output	Channel 1 input or output
7	V_{EE}		Negative Power Input	15	A2	Input / Output	Channel 2 input or output
8	GND		Ground	16	V_{CC}		Positive Power Input

Pin Description of QFN

Pin No.	Pin Name	Input / Output	Description	Pin No.	Pin Name	Input / Output	Description
1	A	Input / Output	Common input or output	9	S0	Input	Control Input
2	A7	Input / Output	Channel 7 input or output	10	A3	Input / Output	Channel 3 input or output
3	A5	Input / Output	Channel 5 input or output	11	A0	Input / Output	Channel 0 input or output
4	/E	Input	Enable switchs, active low	12	A1	Input / Output	Channel 1 input or output
5	V_{EE}		Negative Power Input	13	A2	Input / Output	Channel 2 input or output
6	GND		Ground	14	V_{CC}		Positive Power Input
7	S2	Input	Control Input	15	A4	Input / Output	Channel 4 input or output
8	S1	Input	Control Input	16	A6	Input / Output	Channel 6 input or output

Functional Table

/E, Enable	S2	S1	S0	ON Channel
L	L	L	L	A0
L	L	L	H	A1
L	L	H	L	A2
L	L	H	H	A3
L	H	L	L	A4
L	H	L	H	A5
L	H	H	L	A6
L	H	H	H	A7
H	X	X	X	None

X = Don’t care

Absolute Maximum Ratings Note 1

Parameters	Rating
Supply Voltage, V_{CC} - V_{EE}	-0.5V to 13V
Supply Voltage, V_{CC} - GND	-0.5V to 13V
Supply Voltage, V_{EE} - GND	-6.5V to 0.5V
Analog Switch Voltage	V_{EE} – 0.5V to V_{CC} + 0.5V
Analog Switch Current	±25mA
Analog Switch Diode Current	±20mA
Digital Input Voltage, /E, S2, S1, S0	GND to V_{CC} + 0.5V
Digital Input Diode Current	±20mA
Maximum Junction Temperature	150°C
Storage Temperature Range	–65 to 150°C
Lead Temperature (Soldering, 10 sec)	260°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD Rating

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001	1	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002	1	kV

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
16-Pin SOIC	100	50	°C/W
16-Pin TSSOP	150	60	°C/W
16-Pin QFN	65	41	°C/W

Recommended Operating Conditions Note 1

Over operating temperature range

Parameters	Min	Max	Unit
Supply Voltage, V_{CC} - V_{EE}	3	12	V
Supply Voltage, V_{CC} – GND Note2	3	12	V
Supply Voltage, V_{EE} – GND Note2	-6	0	V
Select Input Voltage	0	V_{CC}	V
Input Transition Rise and Fall Rate		100	ns/V
Switch I/O Port Voltage	V_{EE}	V_{CC}	V
Operating Temperature Range	–40	125	°C

Note 1: Select input must be held HIGH or LOW and it must not float.

Note 2: The voltage of V_{CC}, V_{EE} need be in the range of V_{CC}-V_{EE}

Electrical Characteristics

Single Supply, V_{CC} = 4.5 to 5.5V, V_{EE} = 0V, GND = 0V, unless otherwise noted.

Symbol	Parameter	Conditions	V_{CC} (V)	25°C	-40°C to 85°C	-40°C to 125°C	Limit	Unit
Power Supply								
I_{CC}	Quiescent Supply Current	V_{IN} = V_{EE} or V_{CC}	5.5	4	6	8	Max	μA
Digital Input								
V_{IH}	Input Voltage High				2.0	2.0	Min	V
V_{IL}	Input Voltage Low				0.8	0.8	Max	V
I_{IN}	Control Input Leakage	V_{IN} = 0V or V_{CC}	5.5	±0.4	±1	±1	Max	μA
Analog Switch								
R_{ON}	(1)	I_{OUT} = 1mA, V_{IS} = V_{EE} or V_{CC}	4.5	60			Typ	Ω
R_{ON}		I_{OUT} = 1mA, V_{IS} = V_{EE} or V_{CC}	4.5	100	130	150	Max	Ω
ΔR_{ON}	On Resistance Match between Channels	I_{OUT} = 1mA, V_{IS} = 2.5V	4.5	20	30	35	Max	Ω
$R_{FLAT(ON)}$	On Resistance Flatness	I_{OUT} = 1mA	4.5	60	80	80	Max	Ω
$I_{CH(OFF)}$	Switch OFF Leakage Current on Channel	V_{IS} = V_{EE}, V_{OS} = V_{CC}; or V_{IS} = V_{CC}, V_{OS} = V_{EE}	5.5	±0.4	±1	±1	Max	μA
$I_{COM(OFF)}$	Switch OFF Leakage Current on Common	V_{IS} = V_{EE}, V_{OS} = V_{CC}; or V_{IS} = V_{CC}, V_{OS} = V_{EE},	5.5	±0.4	±4	±4	Max	μA
$I_{(ON)}$	Switch ON Leakage Current	V_{IS} = V_{EE} or V_{CC}	5.5	±0.4	±4	±4	Max	μA
Dynamic Characteristics								
t_{PHL}, t_{PLH}	Switch IN to OUT time (1)	C_L = 50pF	4.5	5			Typ	ns
t_{ON}	Switch turn-on time	C_L = 50pF	4.5	60			Max	ns
t_{OFF}	Switch turn-off time	C_L = 50pF	4.5	50			Max	ns
	OFF-Isolation (1)	f = 1MHz, R_L = 50Ω, C_L = 10pF	5	-70			Typ	dB
	Crosstalk in channel (1)	f = 1MHz, R_L = 50Ω, C_L = 10pF	5	-70			Typ	dB
	Crosstalk in control (1)	Between control and any switch; RL = 600Ω; f = 1 MHz; E or Sn square wave between V_{CC} and GND	5	110			Typ	mV
BW	Bandwidth (1)	R_L = 50Ω	5	200			Typ	MHz
THD	Total Harmonic Distortion (1)	R_L = 10kΩ, f = 1kHz	5	0.05			Typ	%
Capacitance								
C_{IN}	Switch Input Capacitance (1)		5	5			Typ	pF
C_{COM}	Common Output Capacitance (1)		5	25			Typ	pF
C_{PD}	Power Dissipation Capacitance (1)		5	50			Typ	pF

(1) Test data based on bench test and design simulation

Single Supply, V_{CC} = 3 to 3.6V, V_{EE} = 0V, GND = 0V, unless otherwise noted.

Symbol	Parameter	Conditions	V_{CC} (V)	25°C	-40°C to 85°C	-40°C to 125°C	Limit	Unit
Power Supply								
I_{CC}	Quiescent Supply Current	V_{IN} = V_{EE} or V_{CC}	3.6	4	6	8	Max	μA
Digital Input								
V_{IH}	Input Voltage High				2.0	2.0	Min	V
V_{IL}	Input Voltage Low				0.8	0.8	Max	V
I_{IN}	Control Input Leakage	V_{IN} = 0V or V_{CC}	3.6		±1	±1	Max	μA
Analog Switch								
R_{ON}	(1)	I_{OUT} = 1mA, V_{IS} = V_{EE} or V_{CC}	3	300			Typ	Ω
$R_{FLAT(ON)}$	On Resistance Flatness (1)	I_{OUT} = 1mA	3	100			Typ	Ω
$I_{CH(OFF)}$	Switch OFF Leakage Current on Channel	V_{IS} = V_{EE}, V_{OS} = V_{CC}; or V_{IS} = V_{CC}, V_{OS} = V_{EE}	3.6	±0.4	±1	±1	Max	μA
$I_{COM(OFF)}$	Switch OFF Leakage Current on Common	V_{IS} = V_{EE}, V_{OS} = V_{CC}; or V_{IS} = V_{CC}, V_{OS} = V_{EE},	3.6	±0.4	±4	±4	Max	μA
$I_{(ON)}$	Switch ON Leakage Current	V_{IS} = V_{EE} or V_{CC}	3.6	±0.4	±4	±4	Max	μA
Dynamic Characteristics								
t_{PHL}, t_{PLH}	Switch IN to OUT time (1)	C_L = 50pF	3	5			Typ	ns
t_{ON}	Switch turn-on time (1)	C_L = 50pF	3	70			Typ	ns
t_{OFF}	Switch turn-off time (1)	C_L = 50pF	3	60			Typ	ns
	OFF-Isolation (1)	f = 1MHz, R_L = 50Ω, C_L = 10pF	3.3	-70			Typ	dB
	Crosstalk (1)	f = 1MHz, R_L = 50Ω, C_L = 10pF	3.3	-70			Typ	dB
	Crosstalk in control (1)	Between control and any switch; RL = 600Ω; f = 1 MHz; E or Sn square wave between V_{CC} and GND	3.3	110			Typ	mV
BW	Bandwidth (1)	R_L = 50Ω	3.3	100			Typ	MHz
THD	Total Harmonic Distortion (1)	R_L = 10kΩ, f = 1kHz	3.3	0.2			Typ	%
Capacitance								
C_{IN}	Switch Input Capacitance (1)		3.3	5			Typ	pF
C_{COM}	Common Output Capacitance (1)		3.3	25			Typ	pF
C_{PD}	Power Dissipation Capacitance (1)		3.3	50			Typ	pF

(1) Test data based on bench test and design simulation

Single Supply, V_{CC} = 9V to 11V, V_{EE} = 0V, GND = 0V, unless otherwise noted.

Symbol	Parameter	Conditions	V_{CC} (V)	25°C	-40°C to 85°C	-40°C to 125°C	Limit	Unit
Power Supply								
I_{CC}	Quiescent Supply Current	V_{IN} = V_{EE} or V_{CC}	9	8	12	16	Max	μA
Digital Input								
V_{IH}	Input Voltage High				2.4	2.4	Min	V
V_{IL}	Input Voltage Low				0.8	0.8	Max	V
I_{IN}	Control Input Leakage	V_{IN} = 0V or V_{CC}	11	±0.4	±1	±1	Max	μA
Analog Switch								
R_{ON}	(1)	I_{OUT} = 1mA, V_{IS} = V_{EE} or V_{CC}	9	50			Typ	Ω
R_{ON}		I_{OUT} = 1mA, V_{IS} = V_{EE} or V_{CC}	9	80	95	105	Max	Ω
ΔR_{ON}	On Resistance Match between Channels	I_{OUT} = 1mA, V_{IS} = 1V	9	15	25	30	Max	Ω
$R_{FLAT(ON)}$	On Resistance Flatness	I_{OUT} = 1mA	9	30	40	40	Max	Ω
$I_{CH(OFF)}$	Switch OFF Leakage Current on Channel	V_{IS} = V_{EE}, V_{OS} = V_{CC}; or V_{IS} = V_{CC}, V_{OS} = V_{EE}	11	±0.4	±1	±1	Max	μA
$I_{COM(OFF)}$	Switch OFF Leakage Current on Common	V_{IS} = V_{EE}, V_{OS} = V_{CC}; or V_{IS} = V_{CC}, V_{OS} = V_{EE},	11	±0.4	±4	±4	Max	μA
$I_{(ON)}$	Switch ON Leakage Current	V_{IS} = V_{EE} or V_{CC}	11	±0.4	±4	±4	Max	μA
Dynamic Characteristics								
t_{PHL}, t_{PLH}	Switch IN to OUT time (1)	C_L = 50pF	9	5			Typ	ns
t_{ON}	Switch turn-on time	C_L = 50pF	9	60			Max	ns
t_{OFF}	Switch turn-off time	C_L = 50pF	9	50			Max	ns
	OFF-Isolation (1)	f = 1MHz, R_L = 50Ω, C_L = 10pF	10	-70			Typ	dB
	Crosstalk (1)	f = 1MHz, R_L = 50Ω, C_L = 10pF	10	-70			Typ	dB
	Crosstalk in control (1)	Between control and any switch; RL = 600Ω; f = 1 MHz; E or Sn square wave between V_{CC} and GND	10	220			Typ	mV
BW	Bandwidth (1)	R_L = 50Ω	10	200			Typ	MHz
THD	Total Harmonic Distortion (1)	R_L = 10kΩ, f = 1kHz	10	0.03			Typ	%
Capacitance								
C_{IN}	Switch Input Capacitance (1)		10	5			Typ	pF
C_{COM}	Common Output Capacitance (1)		10	25			Typ	pF
C_{PD}	Power Dissipation Capacitance (1)		10	50			Typ	pF

(1) Test data based on bench test and design simulation

Dual Supply, V_{CC} = 4.5 to 5.5V, V_{EE} = -4.5 to 5.5V, GND = 0V, unless otherwise noted.

Symbol	Parameter	Conditions	V_{CC} /V_{EE}(V)	25°C	-40°C to 85°C	-40°C to 125°C	Limit	Unit
Power Supply								
I_{CC}	Quiescent Supply Current	V_{IN} = V_{EE} or V_{CC}	5.5/-5.5	8	12	16	Max	μA
Digital Input								
V_{IH}	Input Voltage High				70%* V_{CC}	70%* V_{CC}	Min	V
V_{IL}	Input Voltage Low				30%* V_{CC}	30%* V_{CC}	Max	V
I_{IN}	Control Input Leakage	V_{IN} = 0V or V_{CC}	5.5/-5.5	±0.4	±1	±1	Max	μA
Analog Switch								
R_{ON}	(1)	I_{OUT} = 1mA, V_{IS} = V_{EE} or V_{CC}	4.5/-4.5	50			Typ	Ω
R_{ON}		I_{OUT} = 1mA, V_{IS} = V_{EE} or V_{CC}	4.5/-4.5	80	95	105	Max	Ω
ΔR_{ON}	On Resistance Match between Channels	I_{OUT} = 1mA, V_{IS} = -3.5V	4.5/-4.5	15	25	30	Max	Ω
$R_{FLAT(ON)}$	On Resistance Flatness	I_{OUT} = 1mA	4.5/-4.5	30	40	40	Max	Ω
$I_{CH(OFF)}$	Switch OFF Leakage Current on Channel	V_{IS} = V_{EE}, V_{OS} = V_{CC}; or V_{IS} = V_{CC}, V_{OS} = V_{EE}	5.5/-5.5	±0.4	±1	±1	Max	μA
$I_{COM(OFF)}$	Switch OFF Leakage Current on Common	V_{IS} = V_{EE}, V_{OS} = V_{CC}; or V_{IS} = V_{CC}, V_{OS} = V_{EE},	5.5/-5.5	±0.4	±4	±4	Max	μA
$I_{(ON)}$	Switch ON Leakage Current	V_{IS} = V_{EE} or V_{CC}	5.5/-5.5	±0.4	±4	±4	Max	μA
Dynamic Characteristics								
t_{PHL}, t_{PLH}	Switch IN to OUT time (1)	C_L = 50pF	4.5/-4.5	5			Typ	ns
t_{ON}	Switch turn-on time	C_L = 50pF	4.5/-4.5	60			Max	ns
t_{OFF}	Switch turn-off time	C_L = 50pF	4.5/-4.5	50			Max	ns
	OFF-Isolation (1)	f = 1MHz, R_L = 50Ω, C_L = 10pF	5/-5	-70			Typ	dB
	Crosstalk (1)	f = 1MHz, R_L = 50Ω, C_L = 10pF	5/-5	-70			Typ	dB
	Crosstalk in control (1)	Between control and any switch; RL = 600Ω; f = 1 MHz; E or Sn square wave between V_{CC} and GND	5/-5	220			Typ	mV
BW	Bandwidth (1)	R_L = 50Ω	5/-5	200			Typ	MHz
THD	Total Harmonic Distortion (1)	R_L = 10kΩ, f = 1kHz	5/-5	0.03			Typ	%
Capacitance								
C_{IN}	Switch Input Capacitance (1)		5/-5	5			Typ	pF
C_{COM}	Common Output Capacitance (1)		5/-5	25			Typ	pF
C_{PD}	Power Dissipation Capacitance (1)		5/-5	50			Typ	pF

(1) Test data based on bench test and design simulation

Typical Performance Characteristics

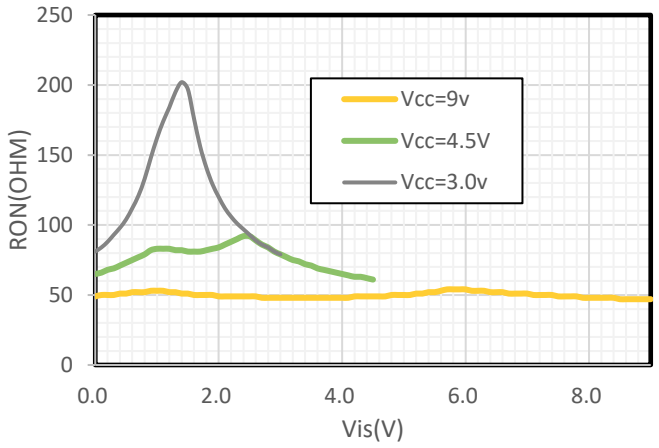


Figure 1. R_{ON} vs. V_{IS}

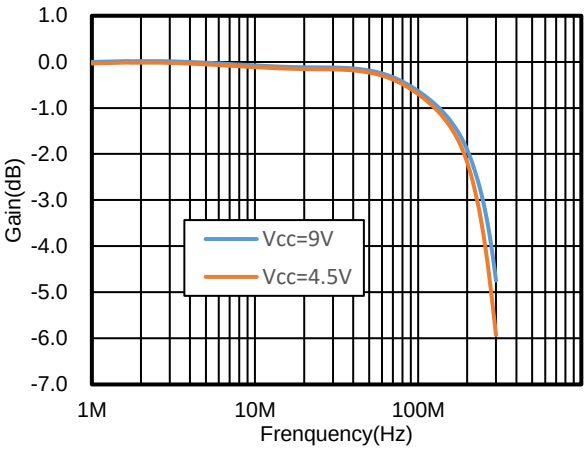
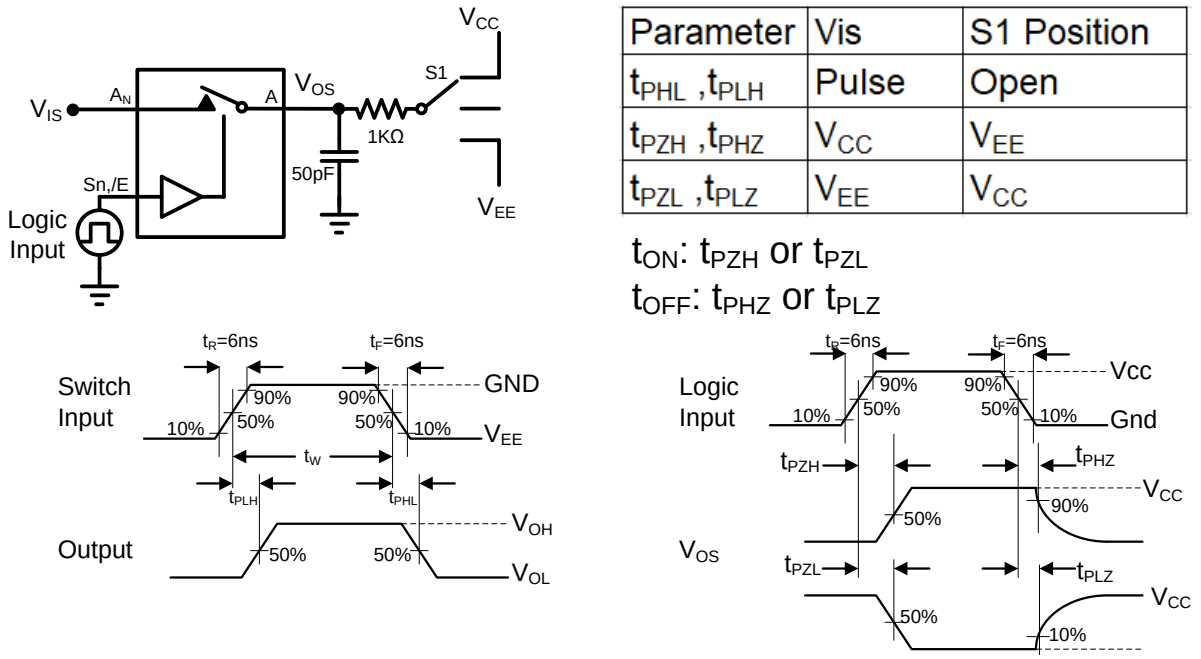


Figure 2. Bandwidth

Test Circuit and Waveforms



Parameter	Vis	S1 Position
t_{PHL} ,t_{PLH}	Pulse	Open
t_{PZH} ,t_{PHZ}	V_{CC}	V_{EE}
t_{PZL} ,t_{PLZ}	V_{EE}	V_{CC}

t_{ON}: t_{PZH} or t_{PZL}

t_{OFF}: t_{PHZ} or t_{PLZ}

Figure 3 AC Test Circuit and Test Waveforms

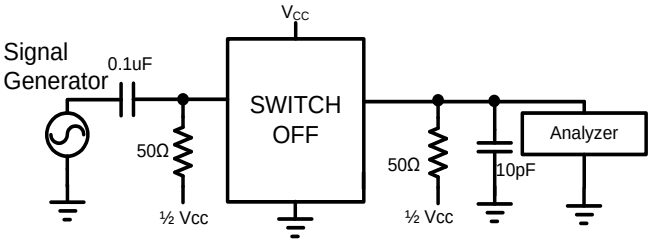


Figure 4 Off Isolation

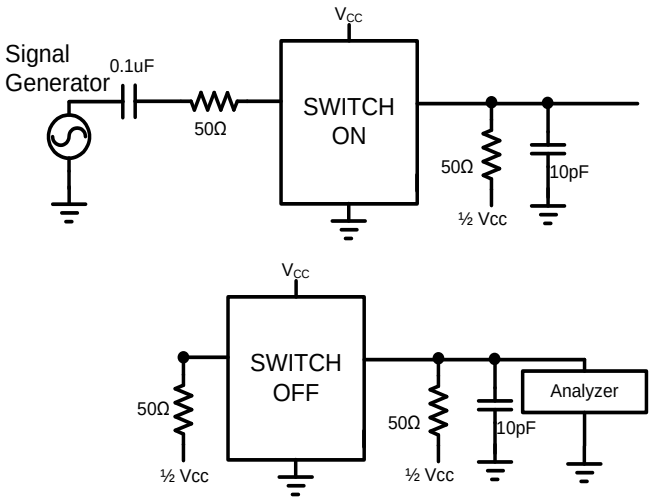
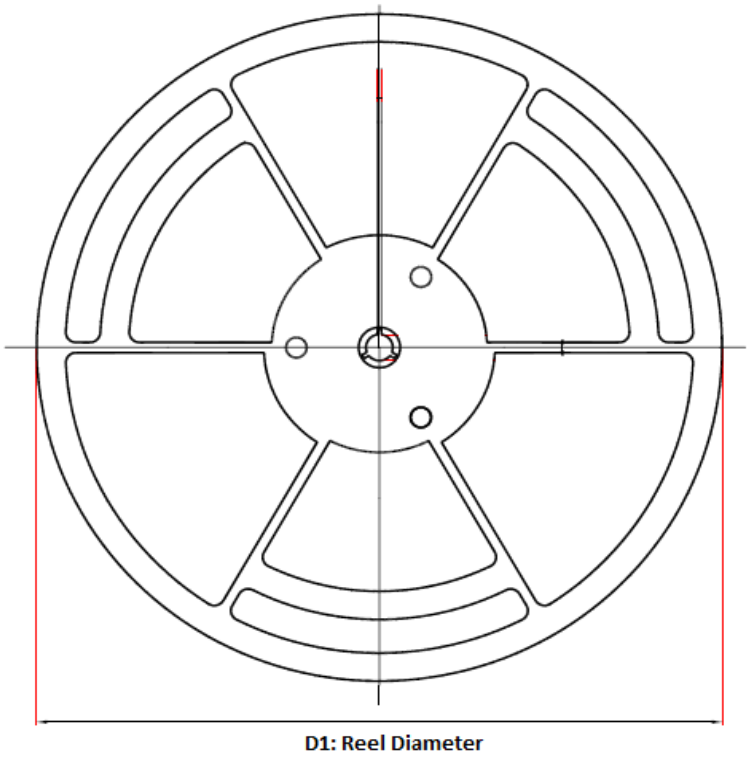


Figure 5 Crosstalk

Application Information

A 0.1-μF bypass capacitor on V_{CC} and GND is recommended to prevent power disturbance, another 0.1-μF bypass capacitor on V_{EE} and GND is also recommended if the V_{EE} is not connected to GND.

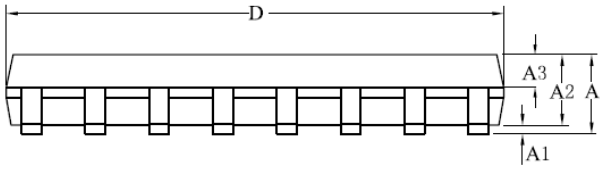
Tape and Reel Information

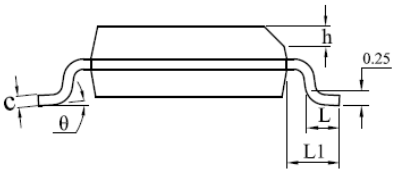


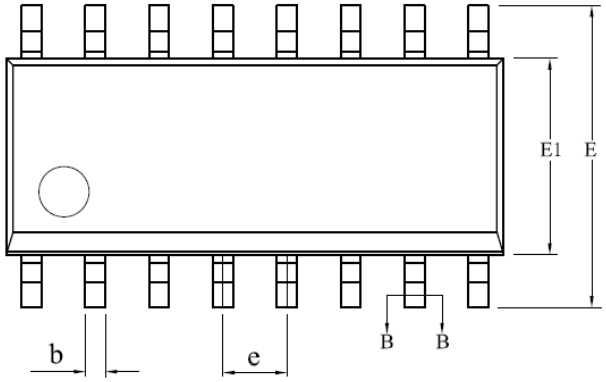
Order Number	Package	D1	W1	A0	B0	K0	P0	W0	Pin1 Quadrant
TPW4051-SR	SOIC-16	330	21.6	6.7±0.1	10.4±0.1	2.1±0.1	8.0±0.1	16.0±0.3	Q1
TPW4051-TR	TSSOP-16	330	17.6	6.8±0.1	5.4±0.1	1.3±0.1	8.0±0.1	12.0±0.1	Q1
TPW4051-QF4R	QFN-16	330	17.6	3.3±0.1	3.3±0.1	1.0±0.1	8.0±0.1	12.0±0.1	Q1

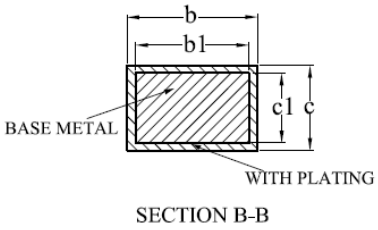
Package Outline Dimensions

SOIC-16







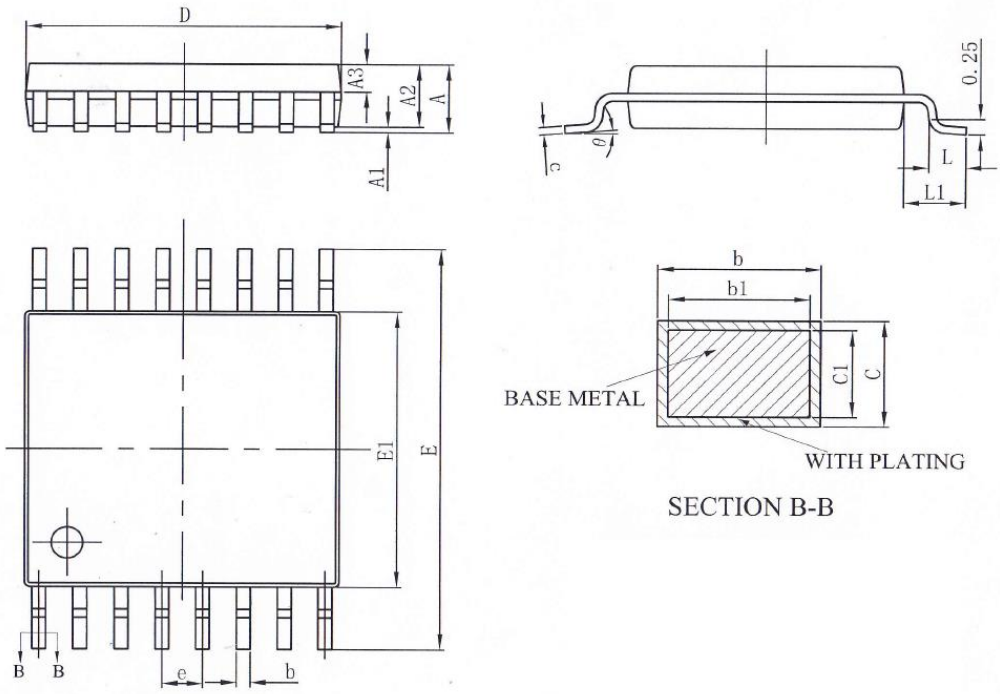


SECTION B-B

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	–	–	1.75
A1	0.10	–	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	–	0.47
b1	0.38	0.41	0.44
c	0.20	–	0.24
c1	0.19	0.20	0.21
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

Package Outline Dimensions

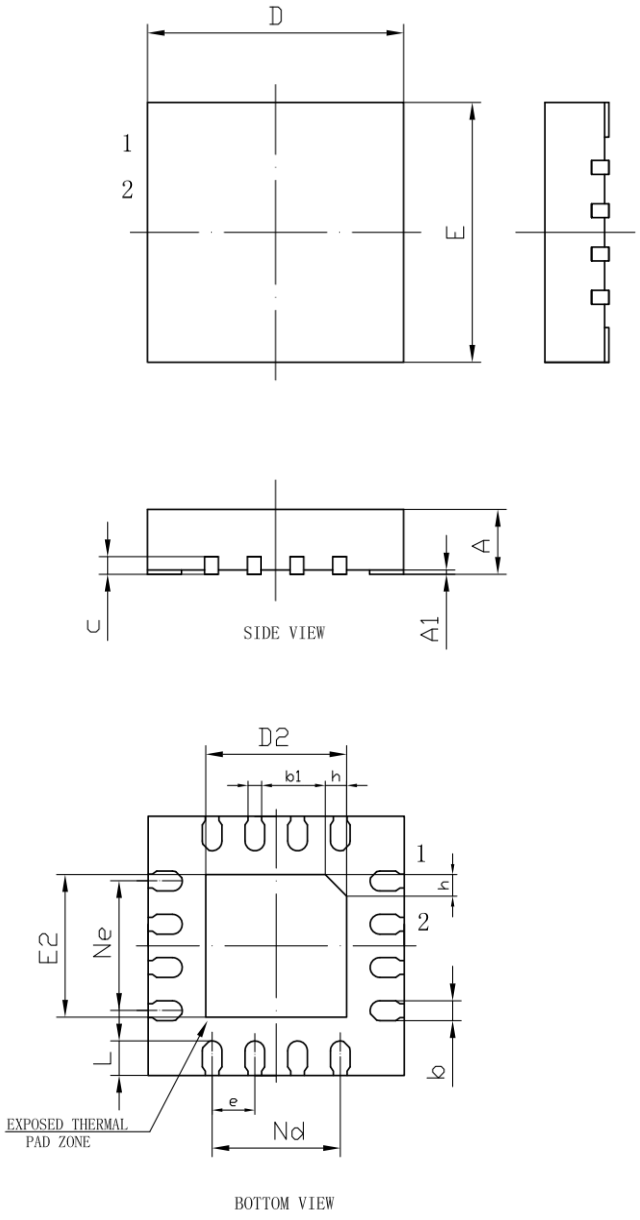
TSSOP-16



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.28
b1	0.19	0.22	0.25
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	4.90	5.00	5.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	—	8°

Package Outline Dimensions

QFN-16



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.18	0.25	0.30
b1	0.16REF		
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	1.55	1.65	1.75
e	0.50BSC		
Ne	1.50BSC		
Nd	1.50BSC		
E	2.90	3.00	3.10
E2	1.55	1.65	1.75
L	0.35	0.40	0.45
h	0.20	0.25	0.30
L/F载体尺寸 (mil)	75x75		

IMPORTANT NOTICE AND DISCLAIMER

Performance Information. Performance tests or performance range contained in this document/material are either results of design simulation or actual tests conducted under designated testing environment. Any variation in testing environment or simulation environment, including but not limited to testing method, testing process or testing temperature, may affect actual performance of the product.

Disclaimer. 3PEAK provides technical and reliability data (including data sheets), design resources (including reference designs), application or other design recommendations, networking tools, security information and other resources "As Is". 3PEAK makes no warranty as to the absence of defects, and makes no warranties of any kind, express or implied, including without limitation, implied warranties as to merchantability, fitness for a particular purpose or non-infringement of any third-party's intellectual property rights. Unless otherwise specified in writing, products supplied by 3PEAK are not designed to be used in any life-threatening scenarios, including critical medical applications, automotive safety-critical systems, aviation, aerospace, or any situations where failure could result in bodily harm, loss of life, or significant property damage. 3PEAK disclaims all liability for any such unauthorized use.