

## IRF510SPBF-VB Datasheet

### N-Channel 100-V (D-S) MOSFET

#### PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
100	0.100 at $V_{GS} = 10$ V	20

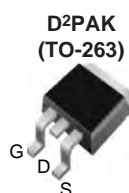
#### FEATURES

- Trench Power MOSFET
- 175 °C Junction Temperature
- Low Thermal Resistance Package
- 100 %  $R_g$  Tested


**RoHS**  
 COMPLIANT

#### APPLICATIONS

- Isolated DC/DC Converters



N-Channel MOSFET

#### ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 175$ °C)	$I_D$	20	A
		16	
Pulsed Drain Current	$I_{DM}$	70	
Avalanche Current	$I_{AS}$	20	mJ
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	200	
Maximum Power Dissipation <sup>b</sup>	$P_D$	105	W
		3.75	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 175	°C

#### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Junction-to-Ambient	$R_{thJA}$	40	°C/W
Junction-to-Case (Drain)	$R_{thJC}$	0.4	

Notes:

a. Package limited.

 b. Duty cycle  $\leq 1$  %.

c. See SOA curve for voltage derating.

d. When Mounted on 1" square PCB (FR-4 material).

SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{DS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	100			V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1		3	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^{\circ}\text{C}$			50	
		$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, T_J = 175\text{ }^{\circ}\text{C}$			250	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	120			A
Drain-Source On-State Resistance <sup>a</sup>	$r_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		0.100		$\Omega$
		$V_{GS} = 10\text{ V}, I_D = 20\text{ A}, T_J = 125\text{ }^{\circ}\text{C}$		0.110		
		$V_{GS} = 10\text{ V}, I_D = 20\text{ A}, T_J = 175\text{ }^{\circ}\text{C}$		0.120		
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 20\text{ A}$	25			S
Dynamic <sup>b</sup>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$		950		pF
Output Capacitance	$C_{oss}$			280		
Reverse Transfer Capacitance	$C_{rss}$			110		
Total Gate Charge <sup>c</sup>	$Q_g$	$V_{DS} = 100\text{ V}, V_{GS} = 10\text{ V}, I_D = 65\text{ A}$			28	nC
Gate-Source Charge <sup>c</sup>	$Q_{gs}$				4.8	
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$				15	
Gate Resistance	$R_g$		0.5	1.7	3.3	$\Omega$
Turn-On Delay Time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = 100\text{ V}, R_L = 1.5\text{ }\Omega$ $I_D \cong 65\text{ A}, V_{GEN} = 10\text{ V}, R_g = 2.5\text{ }\Omega$		8		ns
Rise Time <sup>c</sup>	$t_r$			120		
Turn-Off Delay Time <sup>c</sup>	$t_{d(off)}$			25		
Fall Time <sup>c</sup>	$t_f$			50		
Source-Drain Diode Ratings and Characteristics $T_C = 25\text{ }^{\circ}\text{C}^b$						
Continuous Current	$I_S$				65	A
Pulsed Current	$I_{SM}$				140	
Forward Voltage <sup>a</sup>	$V_{SD}$	$I_F = 65\text{ A}, V_{GS} = 0\text{ V}$		1.0	1.5	V
Reverse Recovery Time	$t_{rr}$	$I_F = 50\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		130	200	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			8	12	A
Reverse Recovery Charge	$Q_{rr}$			0.52	1.2	$\mu\text{C}$

Notes:

a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

b. Guaranteed by design, not subject to production testing.

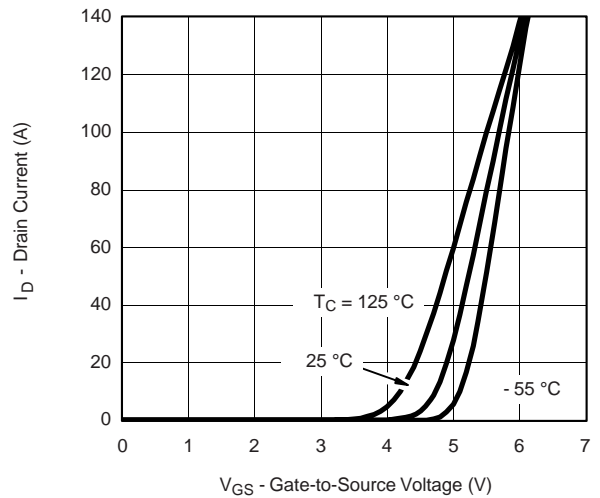
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



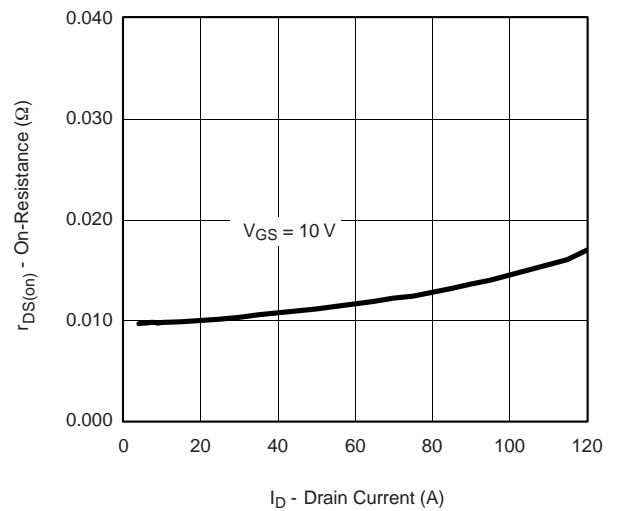
**Output Characteristics**



**Transfer Characteristics**



**Transconductance**



**On-Resistance vs. Drain Current**



**Capacitance**



**Gate Charge**

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



**On-Resistance vs. Junction Temperature**



**Source-Drain Diode Forward Voltage**



**Avalanche Current vs. Time**



**Drain Source Breakdown vs. Junction Temperature**

THERMAL RATINGS



Technical drawing of a lead tip assembly, showing front, side, and detail views with dimensions and tolerances.

**Front View:** Shows the lead tip assembly with dimensions  $E$ ,  $D$ ,  $H$ ,  $L1$ ,  $L2$ ,  $L3$ ,  $L4$ ,  $b1$ ,  $b2$ ,  $b3$ ,  $c1$ ,  $c2$ ,  $c$ , and  $A$ . It includes feature control frames for surface texture ( $Ra$ ), circular runout ( $\phi$ ), and position ( $\perp$ ). Datum A is indicated.

**Side View:** Shows the lead tip assembly with dimensions  $E$ ,  $D$ ,  $H$ ,  $L1$ ,  $L2$ ,  $L3$ ,  $L4$ ,  $b1$ ,  $b2$ ,  $b3$ ,  $c1$ ,  $c2$ ,  $c$ , and  $A$ . It includes feature control frames for surface texture ( $Ra$ ), circular runout ( $\phi$ ), and position ( $\perp$ ). Datum A is indicated.

**Detail A:** Shows a magnified view of the lead tip assembly with dimensions  $E$ ,  $D$ ,  $H$ ,  $L1$ ,  $L2$ ,  $L3$ ,  $L4$ ,  $b1$ ,  $b2$ ,  $b3$ ,  $c1$ ,  $c2$ ,  $c$ , and  $A$ . It includes feature control frames for surface texture ( $Ra$ ), circular runout ( $\phi$ ), and position ( $\perp$ ). Datum A is indicated.

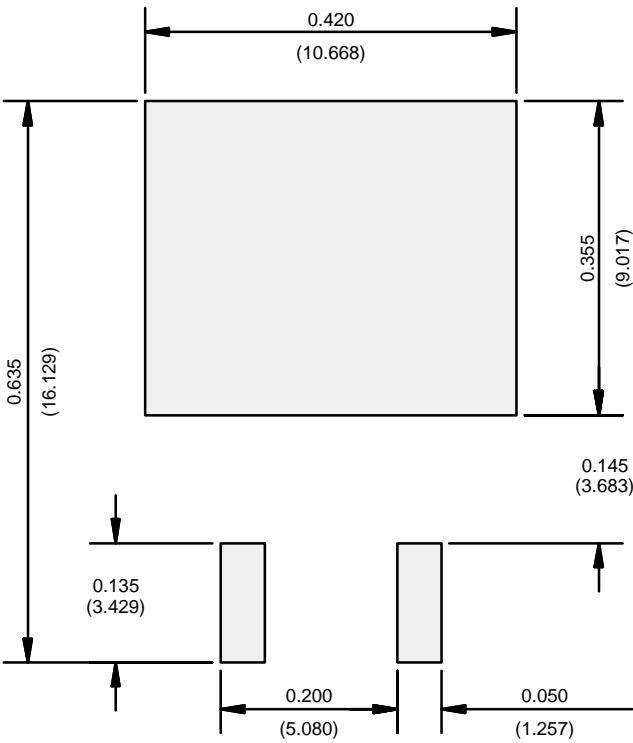
**Section B - B and C - C:** Shows cross-sections of the lead tip assembly with dimensions  $E$ ,  $D$ ,  $H$ ,  $L1$ ,  $L2$ ,  $L3$ ,  $L4$ ,  $b1$ ,  $b2$ ,  $b3$ ,  $c1$ ,  $c2$ ,  $c$ , and  $A$ . It includes feature control frames for surface texture ( $Ra$ ), circular runout ( $\phi$ ), and position ( $\perp$ ). Datum A is indicated.

**View A - A:** Shows a cross-section of the lead tip assembly with dimensions  $E$ ,  $D$ ,  $H$ ,  $L1$ ,  $L2$ ,  $L3$ ,  $L4$ ,  $b1$ ,  $b2$ ,  $b3$ ,  $c1$ ,  $c2$ ,  $c$ , and  $A$ . It includes feature control frames for surface texture ( $Ra$ ), circular runout ( $\phi$ ), and position ( $\perp$ ). Datum A is indicated.

	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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