

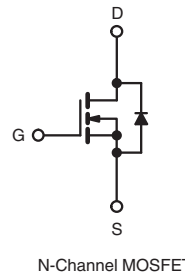
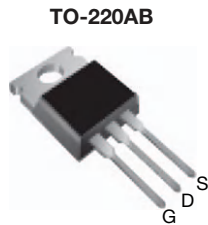
K3519-01-VB Datasheet

N-Channel 500V (D-S)Power MOSFET

| PRODUCT SUMMARY | | |
|----------------------------|------------------------|-------|
| V _{DS} (V) | 500 | |
| R _{DS(on)} (Ω) | V _{GS} = 10 V | 0.660 |
| Q _g (Max.) (nC) | 81 | |
| Q _{gs} (nC) | 20 | |
| Q _{gd} (nC) | 36 | |
| Configuration | Single | |

FEATURES

- Lower Gate Charge Q_g Results in Simpler Drive Requirements
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage
- Compliant to RoHS Directive 2002/95/EC




| ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted) | | | | |
|---|-----------------------------------|-------------------------|-------|----------|
| PARAMETER | SYMBOL | LIMIT | UNIT | |
| Drain-Source Voltage | V _{DS} | 500 | V | |
| Gate-Source Voltage | V _{GS} | ± 20 | | |
| Continuous Drain Current | V _{GS} at 10 V | T _C = 25 °C | 13 | A |
| | | T _C = 100 °C | 8.1 | |
| Pulsed Drain Current ^a | I _{DM} | 50 | | |
| Linear Derating Factor | | 2.0 | W/°C | |
| Single Pulse Avalanche Energy ^b | E _{AS} | 560 | mJ | |
| Avalanche Current ^a | I _{AR} | 13 | A | |
| Repetitive Avalanche Energy ^a | E _{AR} | 25 | mJ | |
| Maximum Power Dissipation | T _C = 25 °C | P _D | 250 | W |
| Peak Diode Recovery dV/dt ^c | dV/dt | 9.2 | V/ns | |
| Operating Junction and Storage Temperature Range | T _J , T _{stg} | - 55 to + 150 | °C | |
| Soldering Recommendations (Peak Temperature) | for 10 s | 300 ^d | | |
| Mounting Torque | 6-32 or M3 screw | 10 | | lbf · in |
| | | 1.1 | N · m | |

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting T_J = 25 °C, L = 5.7 mH, R_g = 25 Ω, I_{AS} = 14 A, dV/dt = 7.6 V/ns (see fig. 12a).
- I_{SD} ≤ 14 A, dI/dt ≤ 250 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C.
- 1.6 mm from case.

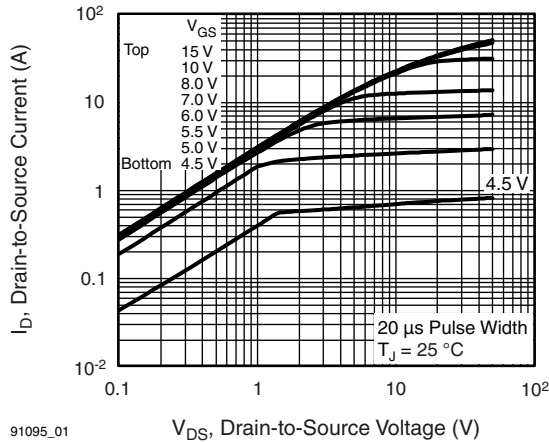
| THERMAL RESISTANCE RATINGS | | | | |
|------------------------------------|------------|------|------|------|
| PARAMETER | SYMBOL | TYP. | MAX. | UNIT |
| Maximum Junction-to-Ambient | R_{thJA} | - | 62 | °C/W |
| Case-to-Sink, Flat, Greasd Surface | R_{thCS} | 0.50 | - | |
| Maximum Junction-to-Case (Drain) | R_{thJC} | - | 0.50 | |

| SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted) | | | | | | | |
|---|-----------------------|---|---|------|-------|-----------|---------------|
| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
| Static | | | | | | | |
| Drain-Source Breakdown Voltage | V_{DS} | $V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$ | | 500 | - | - | V |
| V_{DS} Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$ | | - | 0.55 | - | V/°C |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ | | 2.0 | - | 4.0 | V |
| Gate-Source Leakage | I_{GSS} | $V_{GS} = \pm 20\text{ V}$ | | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$ | | - | - | 25 | μA |
| | | $V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$ | | - | - | 250 | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}$ | $I_D = 8.4\text{ A}^b$ | - | 0.660 | - | Ω |
| Forward Transconductance | g_{fs} | $V_{DS} = 50\text{ V}, I_D = 8.4\text{ A}$ | | 8.1 | - | - | S |
| Dynamic | | | | | | | |
| Input Capacitance | C_{iss} | $V_{GS} = 0\text{ V},$ $V_{DS} = 25\text{ V},$ $f = 1.0\text{ MHz},$ see fig. 5 | | - | 1910 | - | pF |
| Output Capacitance | C_{oss} | | | - | 290 | - | |
| Reverse Transfer Capacitance | C_{rss} | | | - | 11 | - | |
| Output Capacitance | C_{oss} | $V_{GS} = 0\text{ V}$ | $V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$ | - | 2730 | - | pF |
| | | | $V_{DS} = 400\text{ V}, f = 1.0\text{ MHz}$ | - | 82 | - | |
| Effective Output Capacitance | $C_{oss\text{ eff.}}$ | $V_{DS} = 0\text{ V to } 400\text{ V}^c$ | | - | 160 | - | |
| Total Gate Charge | Q_g | $V_{GS} = 10\text{ V}$ | $I_D = 14\text{ A}, V_{DS} = 400\text{ V},$ see fig. 6 and 13 ^b | - | - | 81 | nC |
| Gate-Source Charge | Q_{gs} | | | - | - | 20 | |
| Gate-Drain Charge | Q_{gd} | | | - | - | 36 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{GS} = 10\text{ V}$ | $V_{DD} = 250\text{ V}, I_D = 14\text{ A},$ $R_g = 7.5\text{ }\Omega,$ see fig. 10 ^b | - | 15 | - | ns |
| Rise Time | t_r | | | - | 39 | - | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | - | 39 | - | |
| Fall Time | t_f | | | - | 31 | - | |
| Drain-Source Body Diode Characteristics | | | | | | | |
| Continuous Source-Drain Diode Current | I_S | MOSFET symbol showing the integral reverse p - n junction diode  | | - | - | 13 | A |
| Pulsed Diode Forward Current ^a | I_{SM} | | | - | - | 56 | |
| Body Diode Voltage | V_{SD} | $T_J = 25\text{ }^\circ\text{C}, I_S = 14\text{ A}, V_{GS} = 0\text{ V}^b$ | | - | - | 1.5 | V |
| Body Diode Reverse Recovery Time | t_{rr} | $T_J = 25\text{ }^\circ\text{C}, I_F = 14\text{ A},$ $T_J = 125\text{ }^\circ\text{C}, dI/dt = 100\text{ A}/\mu\text{s}^b$ | | - | 370 | 550 | ns |
| Body Diode Reverse Recovery Charge | Q_{rr} | | | - | 4.4 | 6.5 | μC |
| Body Diode Reverse Recovery Current | I_{RRM} | | | - | 21 | 31 | A |
| Forward Turn-On Time | t_{on} | Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D) | | | | | |

Notes

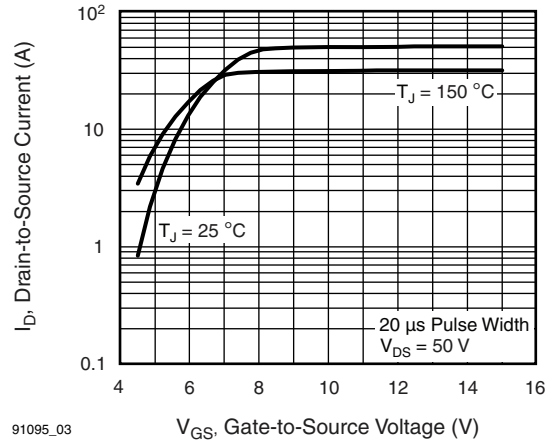
- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
- $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



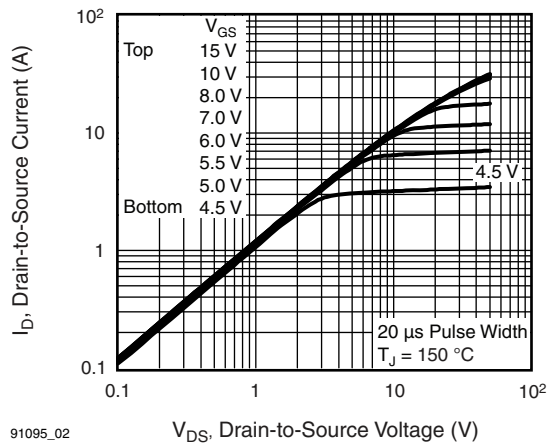
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Fig. 1 - Typical Output Characteristics



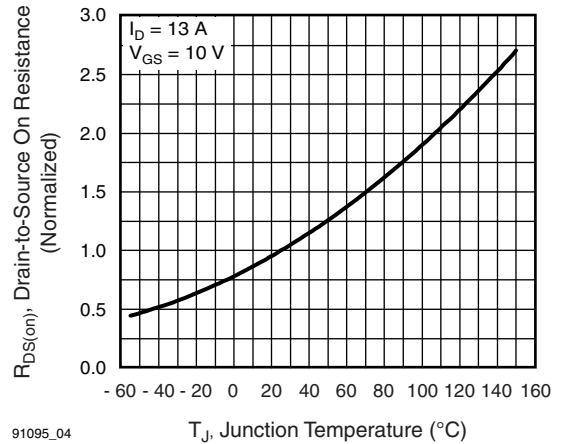
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Fig. 3 - Typical Transfer Characteristics



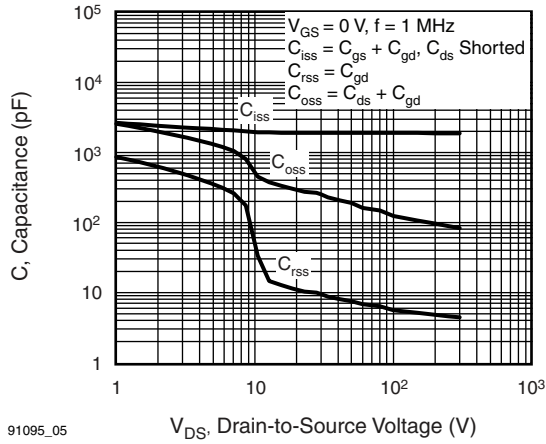
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Fig. 2 - Typical Output Characteristics



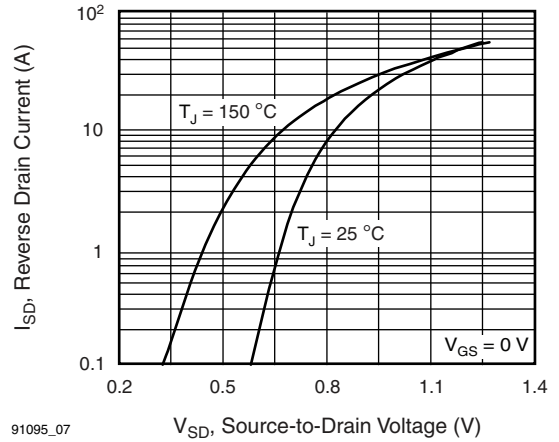
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Fig. 4 - Normalized On-Resistance vs. Temperature



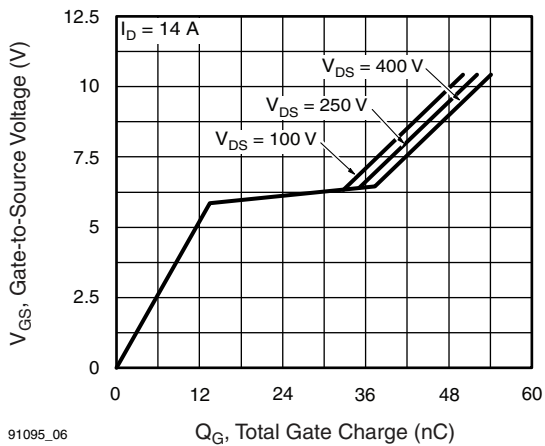
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Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage



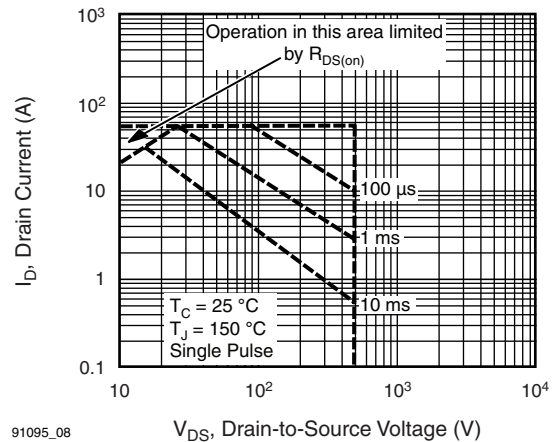
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Fig. 7 - Typical Source-Drain Diode Forward Voltage



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Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



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Fig. 8 - Maximum Safe Operating Area

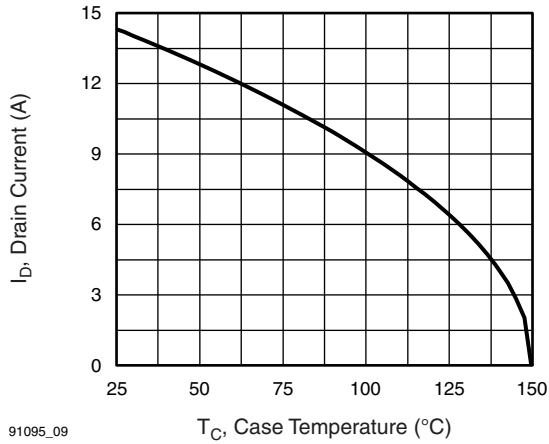


Fig. 9 - Maximum Drain Current vs. Case Temperature

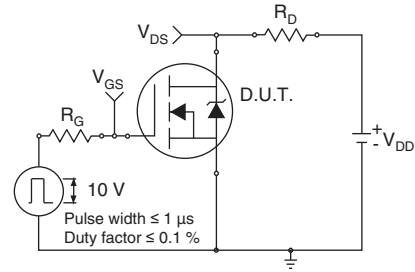


Fig. 10a - Switching Time Test Circuit

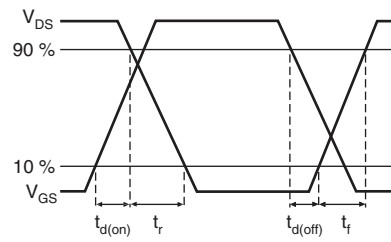


Fig. 10b - Switching Time Waveforms

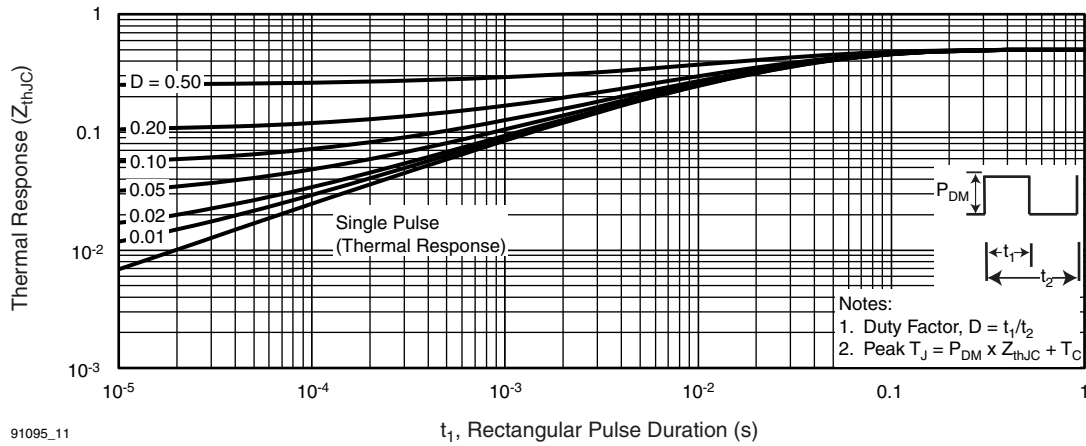


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

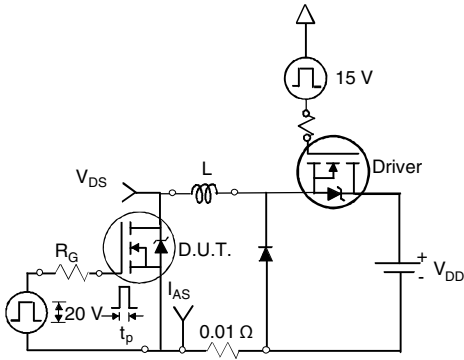


Fig. 12a - Unclamped Inductive Test Circuit

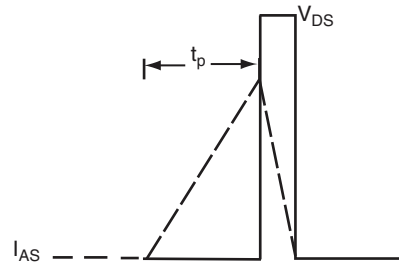


Fig. 12b - Unclamped Inductive Waveforms

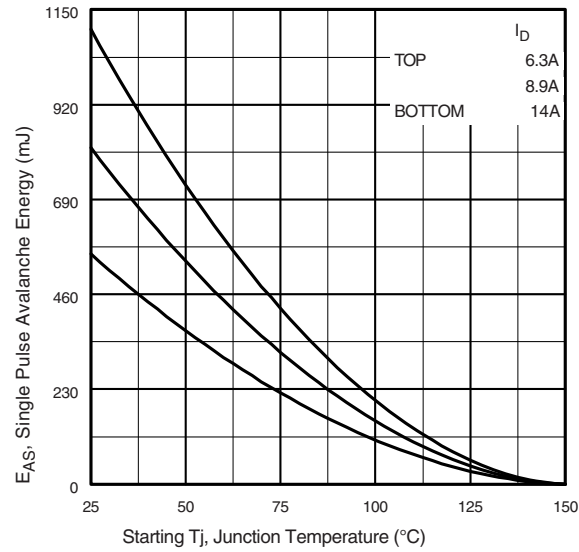


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

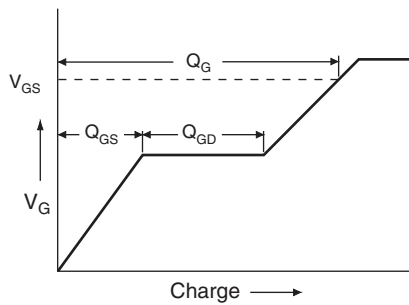


Fig. 13a - Basic Gate Charge Waveform

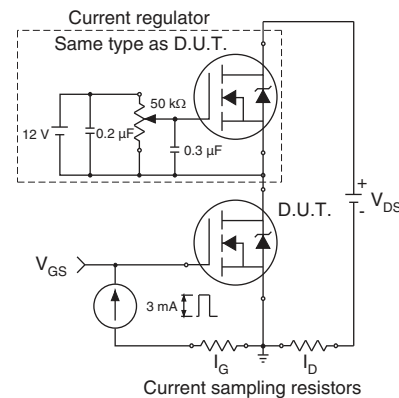
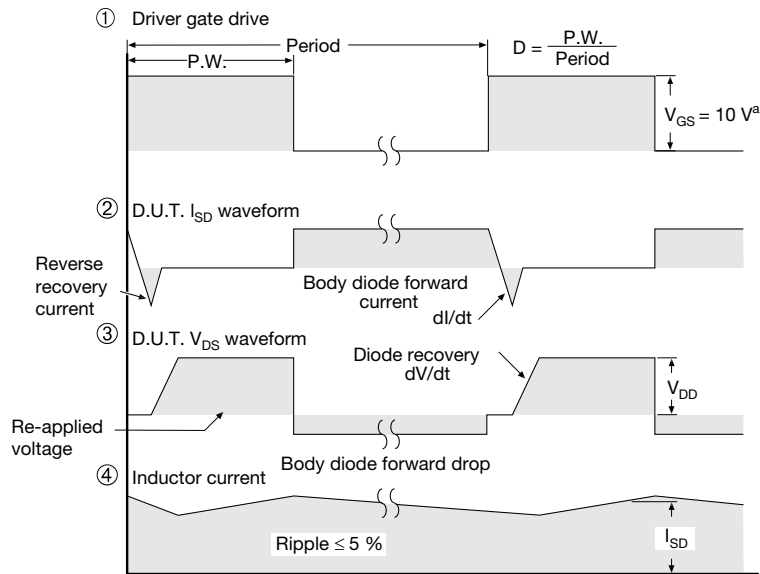
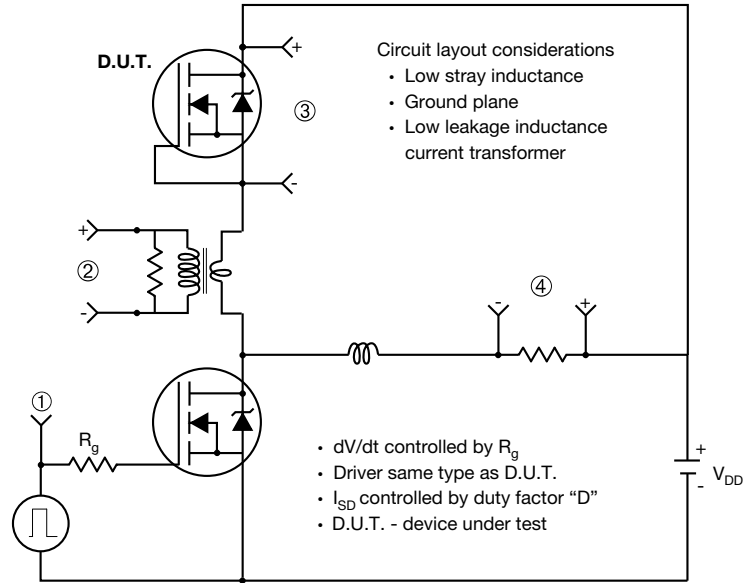


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

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