

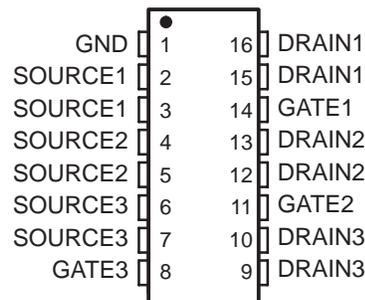
# TPIC5302

## 3-CHANNEL INDEPENDENT POWER DMOS ARRAY

SLIS029B – APRIL 1994 – REVISED SEPTEMBER 1995

- Low  $r_{DS(on)}$  . . . 0.3  $\Omega$  Typ
- High-Voltage Outputs . . . 60 V
- Pulsed Current . . . 7 A Per Channel
- Fast Commutation Speed

D PACKAGE  
(TOP VIEW)

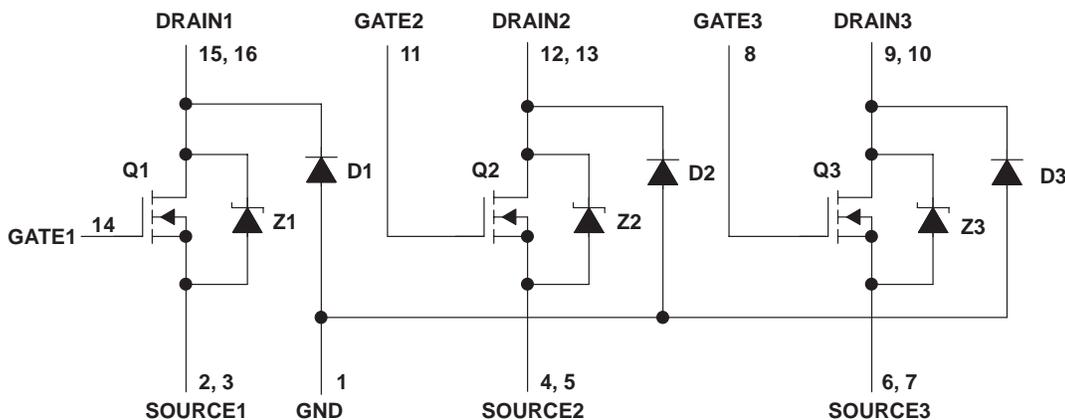


### description

The TPIC5302 is a monolithic power DMOS array that consists of three electrically isolated independent N-channel enhancement-mode DMOS transistors. The TPIC5302 is offered in a standard 16-pin small-outline surface-mount (D) package.

The TPIC5302 is characterized for operation over the case temperature range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

### schematic



### absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, $V_{DS}$ . . . . .	60 V
Source-to-GND voltage . . . . .	100 V
Drain-to-GND voltage . . . . .	100 V
Gate-to-source voltage, $V_{GS}$ . . . . .	$\pm 20$ V
Continuous drain current, each output, all outputs on, $T_C = 25^{\circ}\text{C}$ . . . . .	1.4 A
Continuous source-to-drain diode current . . . . .	1.4 A
Pulsed drain current, each output, $T_C = 25^{\circ}\text{C}$ (see Note 1 and Figure 6) . . . . .	7 A
Single-pulse avalanche energy, $E_{AS}$ , $T_C = 25^{\circ}\text{C}$ (see Figure 4) . . . . .	10.5 mJ
Continuous total power dissipation at (or below) $T_C = 25^{\circ}\text{C}$ . . . . .	1087 mW
Operating virtual junction temperature range, $T_J$ . . . . .	$-40^{\circ}\text{C}$ to $150^{\circ}\text{C}$
Operating case temperature range, $T_C$ . . . . .	$-40^{\circ}\text{C}$ to $125^{\circ}\text{C}$
Storage temperature range, $T_{stg}$ . . . . .	$-65^{\circ}\text{C}$ to $150^{\circ}\text{C}$
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . .	$260^{\circ}\text{C}$

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms and duty cycle = 2%

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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# TPIC5302

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### electrical characteristics, $T_C = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	$I_D = 250\ \mu\text{A}$ ,	$V_{GS} = 0$	60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	$I_D = 1\ \text{mA}$ ,	$V_{DS} = V_{GS}$	1.5	1.85	2.2	V
$V_{(BR)}$	Reverse drain-to-GND breakdown voltage (across D1, D2, and D3)	Drain-to-GND current = $250\ \mu\text{A}$		100			V
$V_{DS(on)}$	Drain-to-source on-state voltage	$I_D = 1.4\ \text{A}$ , See Notes 2 and 3	$V_{GS} = 10\ \text{V}$ ,		0.42	0.49	V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	$I_S = 1.4\ \text{A}$ , $V_{GS} = 0$ (Z1, Z2, Z3), See Notes 2 and 3			0.9	1.1	V
$V_F$	Forward on-state voltage, GND-to-drain	$I_D = 1.4\ \text{A}$			4.8		V
$I_{DSS}$	Zero-gate-voltage drain current	$V_{DS} = 48\ \text{V}$ , $V_{GS} = 0$	$T_C = 25^\circ\text{C}$		0.05	1	$\mu\text{A}$
			$T_C = 125^\circ\text{C}$		0.5	10	
$I_{GSSF}$	Forward gate current, drain short circuited to source	$V_{GS} = 16\ \text{V}$ ,	$V_{DS} = 0$		10	100	nA
$I_{GSSR}$	Reverse gate current, drain short circuited to source	$V_{SG} = 16\ \text{V}$ ,	$V_{DS} = 0$		10	100	nA
$I_{lkg}$	Leakage current, drain-to-GND	$V_R = 48\ \text{V}$	$T_C = 25^\circ\text{C}$		0.05	1	$\mu\text{A}$
			$T_C = 125^\circ\text{C}$		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	$V_{GS} = 10\ \text{V}$ , $I_D = 1.4\ \text{A}$ , See Notes 2 and 3 and Figures 6 and 7	$T_C = 25^\circ\text{C}$		0.3	0.35	$\Omega$
			$T_C = 125^\circ\text{C}$		0.41	0.5	
$g_{fs}$	Forward transconductance	$V_{DS} = 10\ \text{V}$ , See Notes 2 and 3	$I_D = 0.7\ \text{A}$ ,	1.15	1.41		S
$C_{iss}$	Short-circuit input capacitance, common source				135	170	pF
$C_{oss}$	Short-circuit output capacitance, common source	$V_{DS} = 25\ \text{V}$ ,	$V_{GS} = 0$ ,		80	100	
$C_{rss}$	Short-circuit reverse-transfer capacitance, common source	$f = 1\ \text{MHz}$			30	40	

- NOTES: 2. Technique should limit  $T_J - T_C$  to  $10^\circ\text{C}$  maximum and pulse duration  $\leq 5\ \text{ms}$ .  
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

### source-to-drain diode characteristics, $T_C = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{rr(SD)}$	Reverse-recovery time	$I_S = 0.5\ \text{A}$ ,	$V_{GS} = 0$ , $V_{DS} = 48\ \text{V}$ ,		35		ns
$Q_{RR}$	Total diode charge	$di/dt = 100\ \text{A}/\mu\text{s}$ ,	See Figure 1		0.04		$\mu\text{C}$

### GND-to-drain diode characteristics, $T_C = 25^\circ\text{C}$ (see schematic, D1, D2, and D3)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{rr}$	Reverse-recovery time	$I_F = 0.5\ \text{A}$ ,	$V_{DS} = 48\ \text{V}$ ,		130		ns
$Q_{RR}$	Total diode charge	$di/dt = 100\ \text{A}/\mu\text{s}$ ,	See Figure 1		0.4		$\mu\text{C}$

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### resistive-load switching characteristics, $T_C = 25^\circ\text{C}$

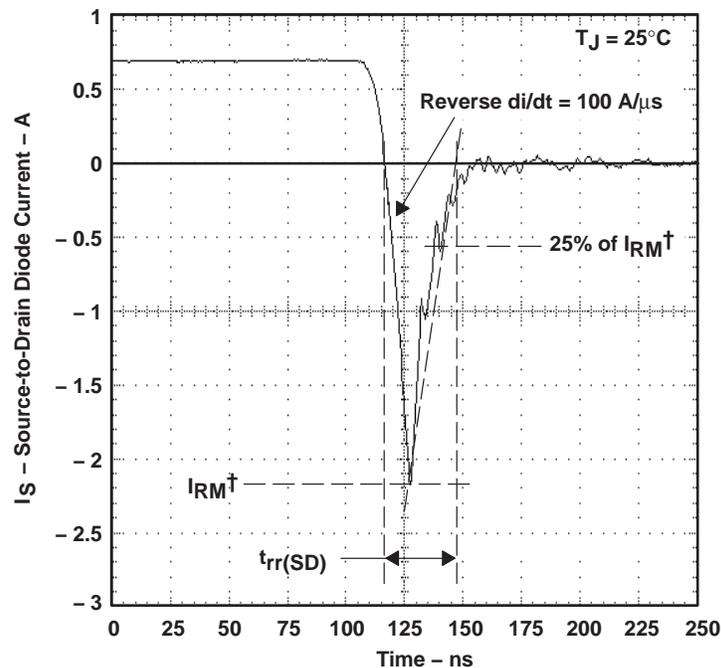
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$ Turn-on delay time	$V_{DD} = 25\text{ V}$ , $R_L = 50\ \Omega$ , $t_{r1} = 10\text{ ns}$ , $t_{f1} = 10\text{ ns}$ , See Figure 2		23	46	ns
$t_{d(off)}$ Turn-off delay time			25	50	
$t_{r2}$ Rise time			5	10	
$t_{f2}$ Fall time			17	34	
$Q_g$ Total gate charge	$V_{DS} = 48\text{ V}$ , $I_D = 0.5\text{ A}$ , $V_{GS} = 10\text{ V}$ , See Figure 3		8	9.8	nC
$Q_{gs(th)}$ Threshold gate-to-source charge			0.5	0.63	
$Q_{gd}$ Gate-to-drain charge			1.5	1.85	
$L_D$ Internal drain inductance			5		nH
$L_S$ Internal source inductance			5		
$R_g$ Internal gate resistance			0.25		$\Omega$

### thermal resistance

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$ Junction-to-ambient thermal resistance	All outputs with equal power, See Note 4		115		$^\circ\text{C/W}$
$R_{\theta JP}$ Junction-to-pin thermal resistance			32		

NOTE 4: Package mounted on an FR4 printed-circuit board with no heat sink

### PARAMETER MEASUREMENT INFORMATION



$^\dagger I_{RM}$  = maximum recovery current

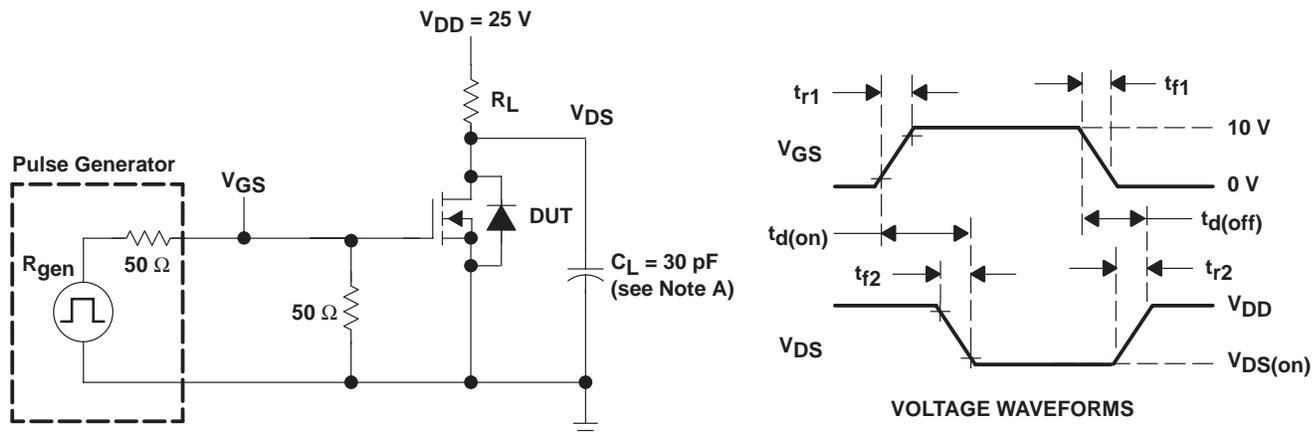
Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode



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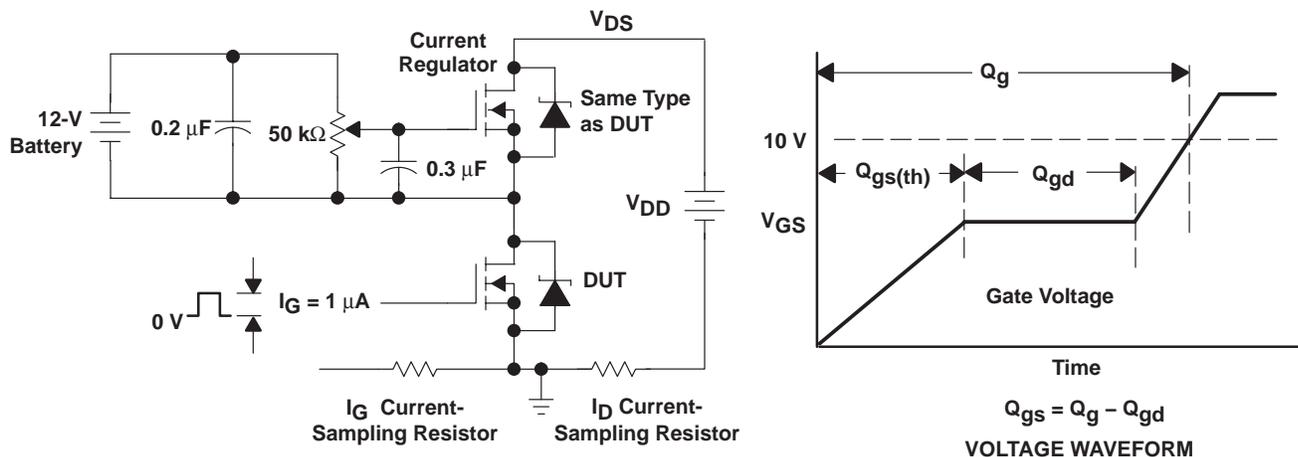
## PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

NOTE A: CL includes probe and jig capacitance.

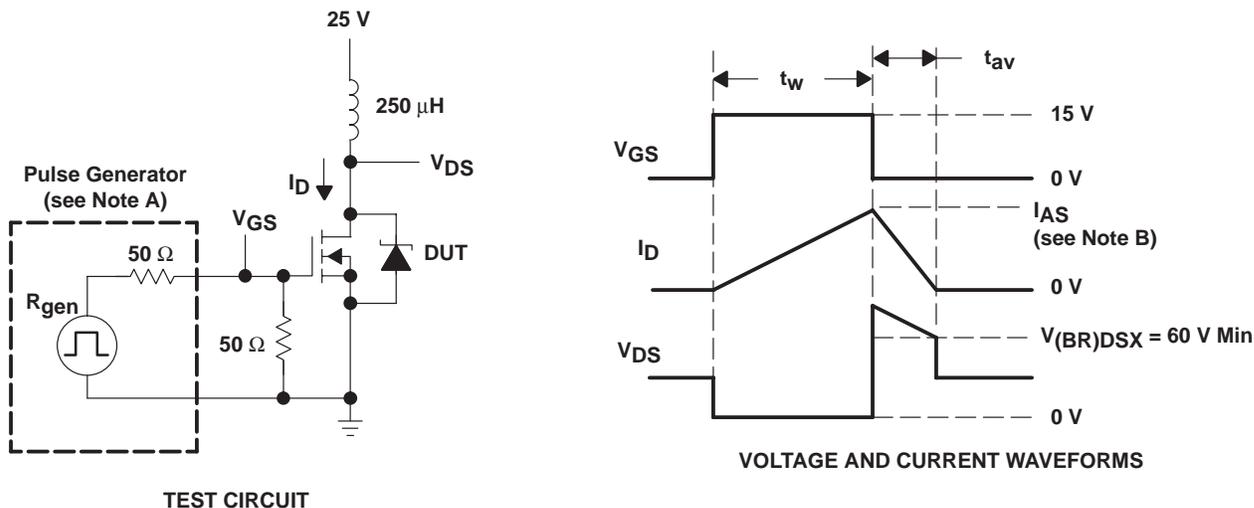
Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms



TEST CIRCUIT

Figure 3. Gate-Charge Test Circuit and Voltage Waveform

**PARAMETER MEASUREMENT INFORMATION**

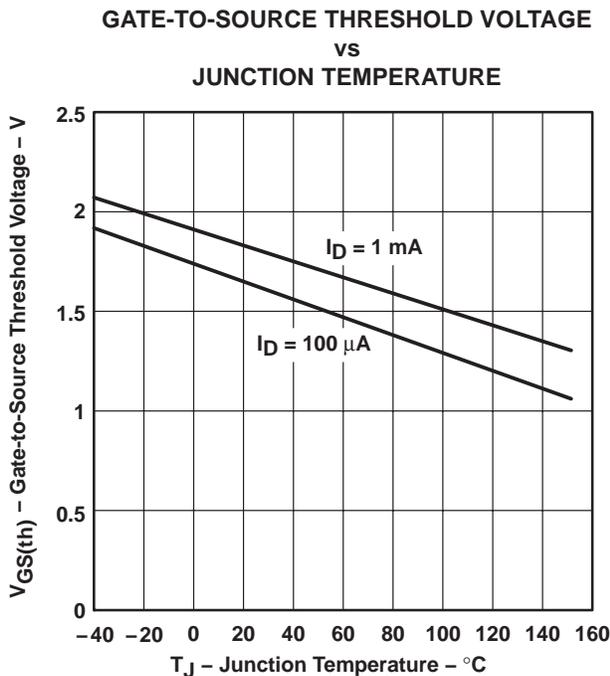


- NOTES: A. The pulse generator has the following characteristics:  $t_r \leq 10$  ns,  $t_f \leq 10$  ns,  $Z_O = 50 \Omega$ .  
 B. Input pulse duration ( $t_w$ ) is increased until peak current  $I_{AS} = 7$  A, where  $t_{av}$  = avalanche time.

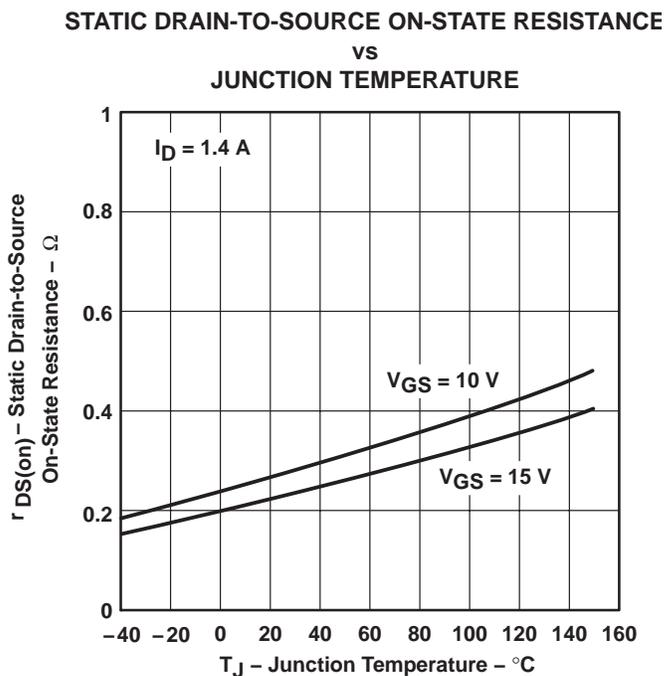
$$\text{Energy test level is defined as } E_{AS} = \frac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 10.5 \text{ mJ}$$

**Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms**

**TYPICAL CHARACTERISTICS**



**Figure 5**



**Figure 6**

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## TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE  
vs  
DRAIN CURRENT

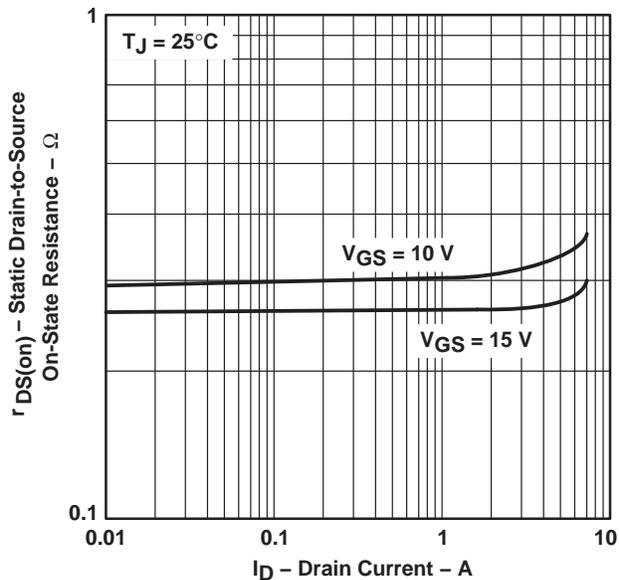


Figure 7

DRAIN CURRENT  
vs  
DRAIN-TO-SOURCE VOLTAGE

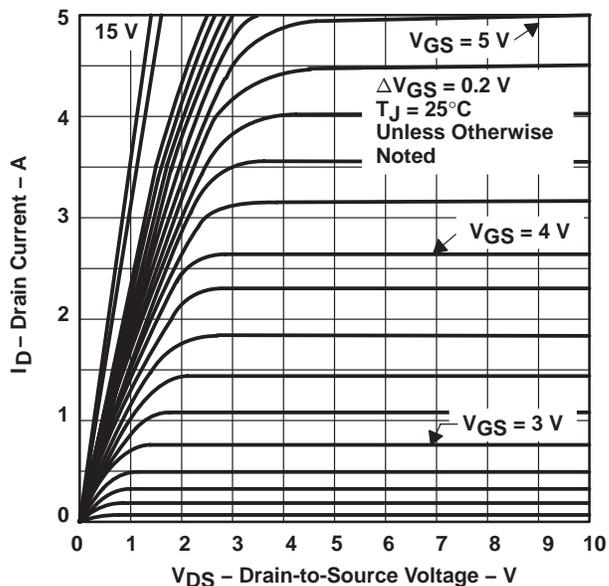


Figure 8

DISTRIBUTION OF  
FORWARD TRANSCONDUCTANCE

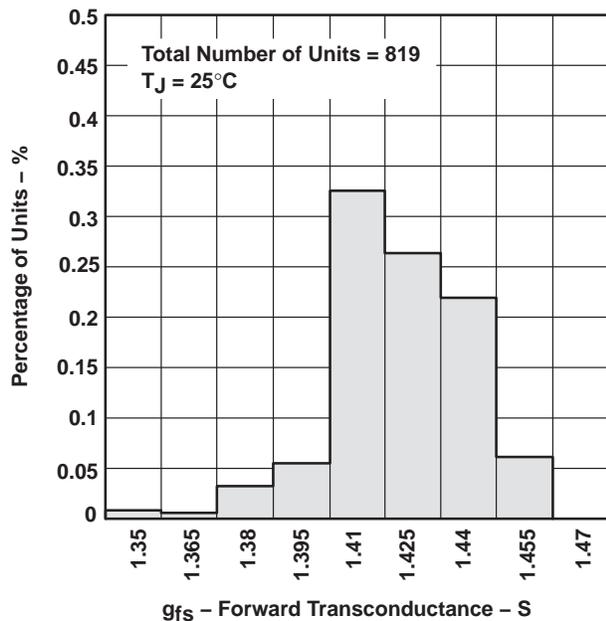


Figure 9

DRAIN CURRENT  
vs  
GATE-TO-SOURCE VOLTAGE

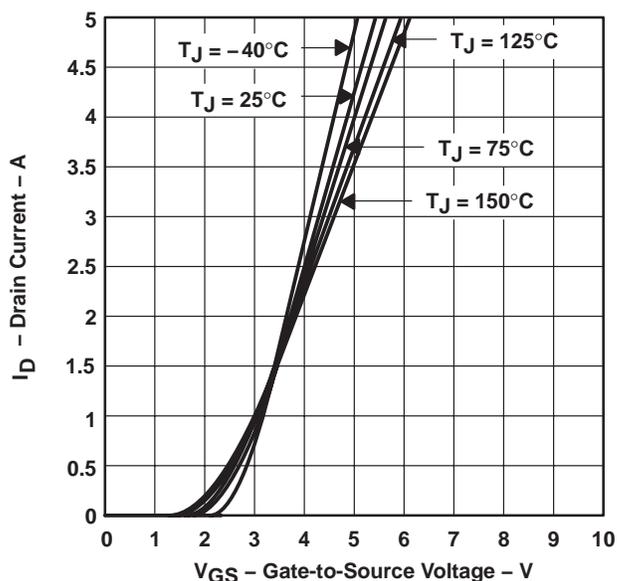


Figure 10

TYPICAL CHARACTERISTICS

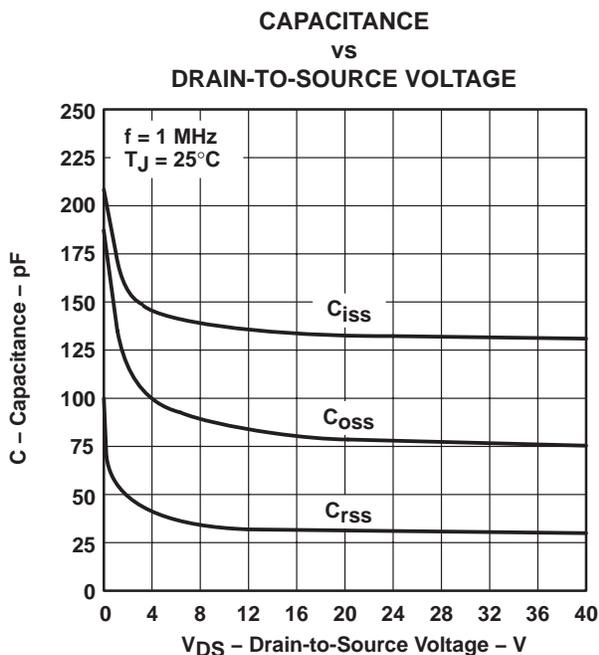


Figure 11

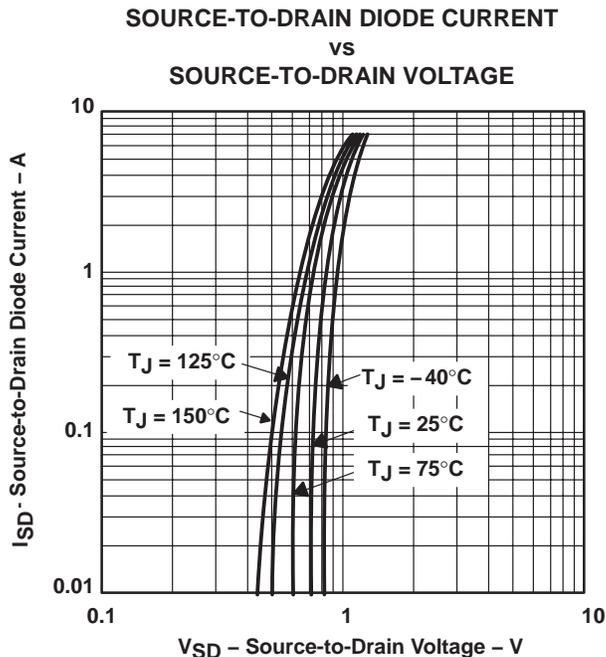


Figure 12

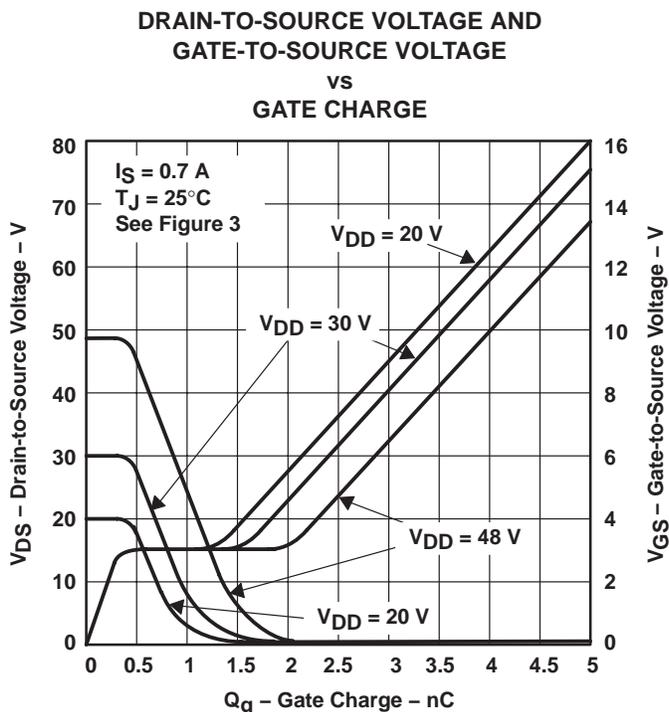


Figure 13

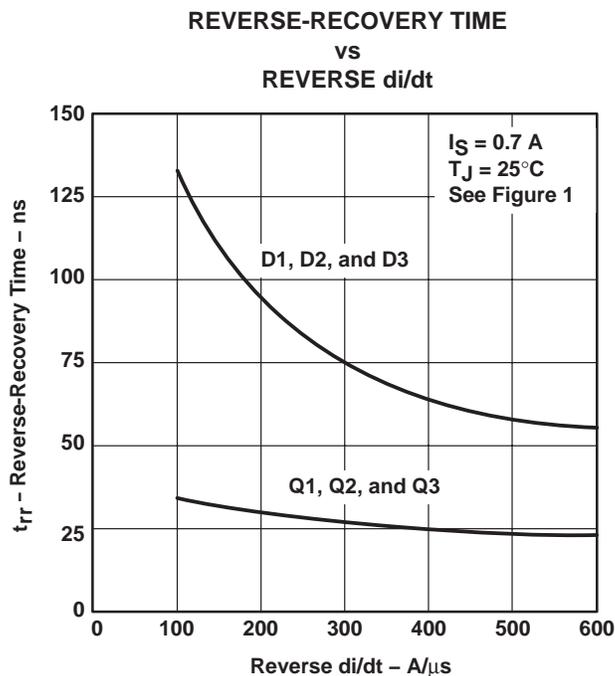
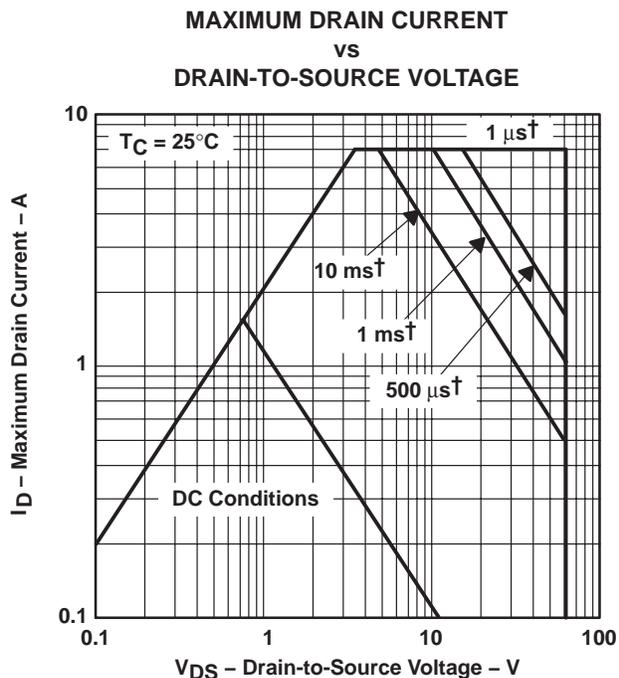


Figure 14

# TPIC5302 3-CHANNEL INDEPENDENT POWER DMOS ARRAY

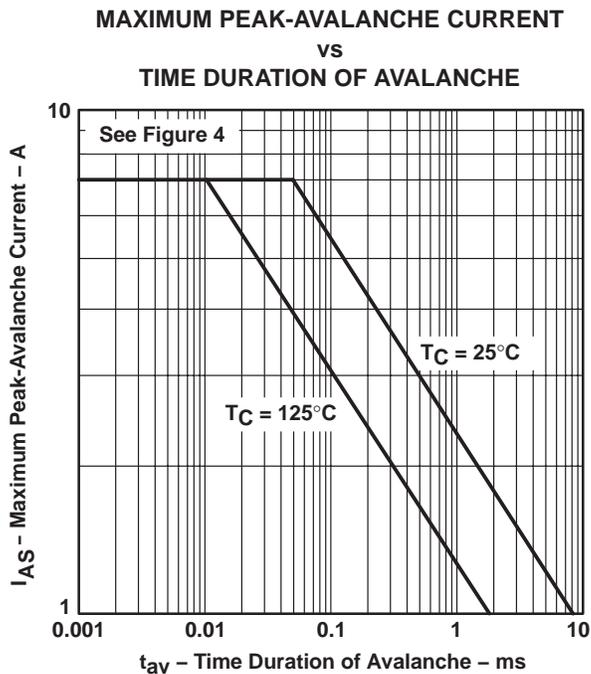
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## THERMAL INFORMATION



† Less than 0.1 duty cycle

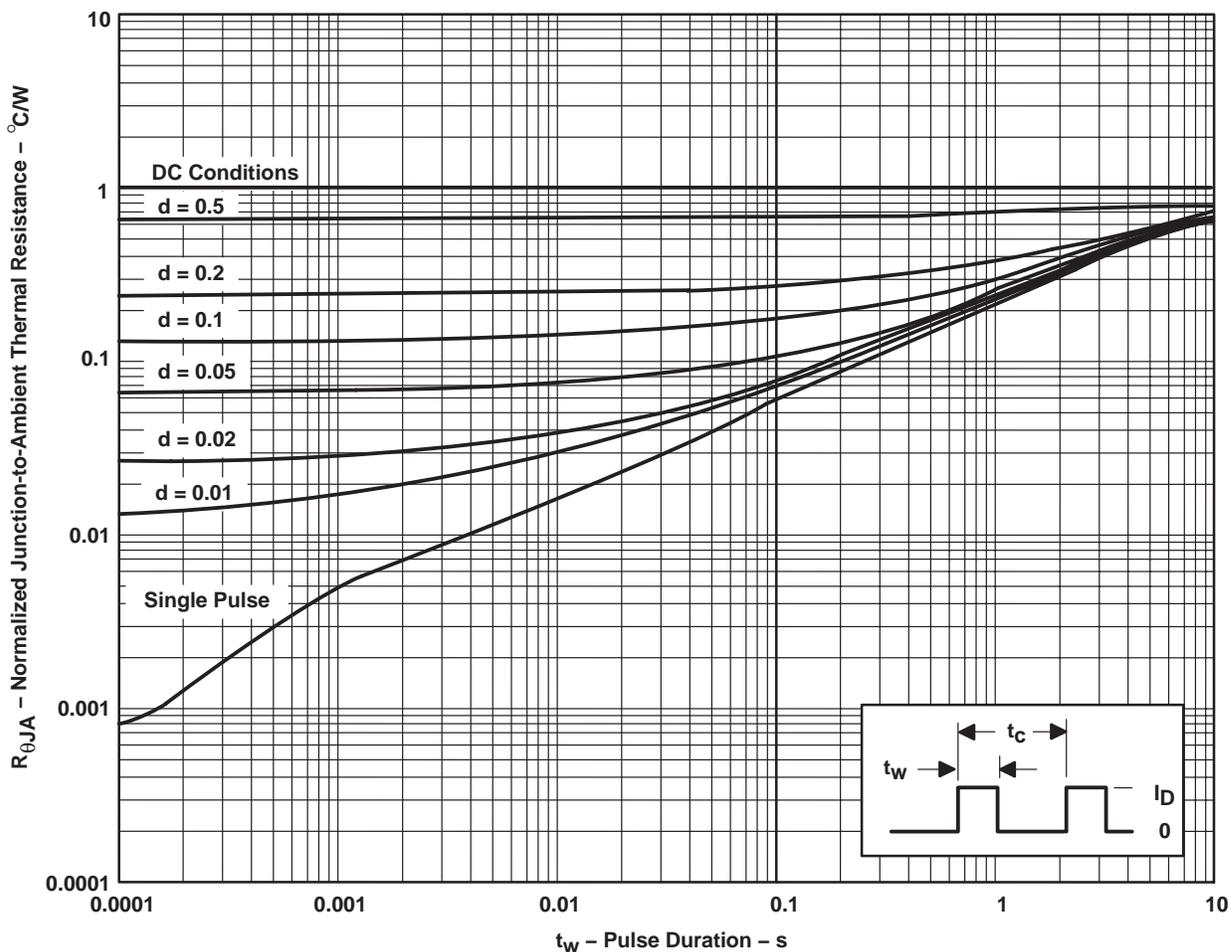
**Figure 15**



**Figure 16**

**THERMAL INFORMATION**

**D PACKAGE†**  
**NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE**  
**VS**  
**PULSE DURATION**



† Device mounted on FR4 printed-circuit board with no heat sink

NOTE A:  $Z_{\theta A}(t) = r(t) R_{\theta JA}$   
 $t_w$  = pulse duration  
 $t_c$  = cycle time  
 $d$  = duty cycle =  $t_w/t_c$

**Figure 17**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TPIC5302D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

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<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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