

CSD19505KCS 80 V N-Channel NexFET™ Power MOSFET

1 Features

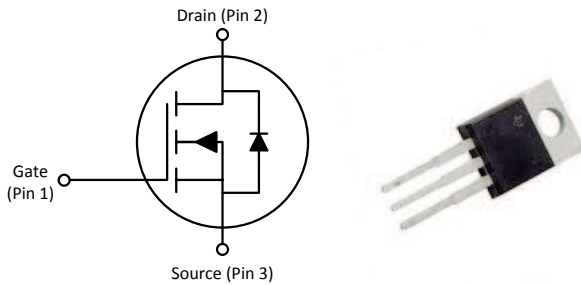
- Ultra-Low Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Pb-Free Terminal Plating
- RoHS Compliant
- Halogen Free
- TO-220 Plastic Package

2 Applications

- Secondary Side Synchronous Rectifier
- Motor Control

3 Description

This 80 V, 2.6 mΩ, TO-220 NexFET™ power MOSFET is designed to minimize losses in power conversion applications.



Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	80		V
Q_g	Gate Charge Total (10 V)	76		nC
Q_{gd}	Gate Charge Gate to Drain	11		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = 6\text{ V}$	2.9	mΩ
		$V_{GS} = 10\text{ V}$	2.6	mΩ
$V_{GS(th)}$	Threshold Voltage	2.6		V

Ordering Information⁽¹⁾

Device	Package	Media	Qty	Ship
CSD19505KCS	TO-220 Plastic Package	Tube	50	Tube

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	80	V
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D	Continuous Drain Current (Package limited)	150	A
	Continuous Drain Current (Silicon limited), $T_C = 25^\circ\text{C}$	208	
	Continuous Drain Current (Silicon limited), $T_C = 100^\circ\text{C}$	147	
I_{DM}	Pulsed Drain Current ⁽¹⁾	400	A
P_D	Power Dissipation	300	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	-55 to 175	$^\circ\text{C}$
E_{AS}	Avalanche Energy, single pulse $I_D = 101\text{ A}, L = 0.1\text{ mH}, R_G = 25\ \Omega$	510	mJ

(1) Max $R_{\theta JC} = 0.5^\circ\text{C/W}$, pulse duration $\leq 100\ \mu\text{s}$, duty cycle $\leq 1\%$

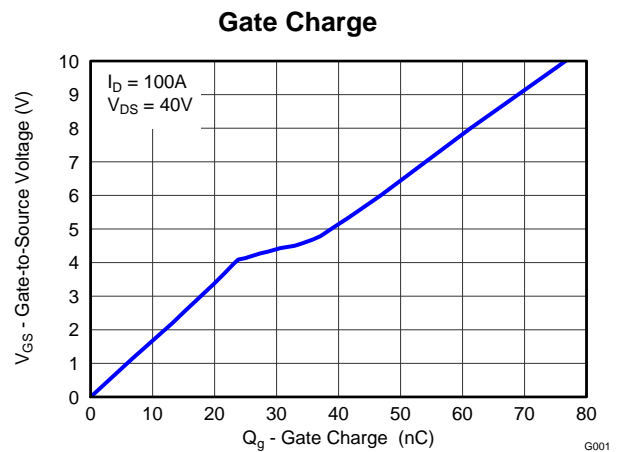
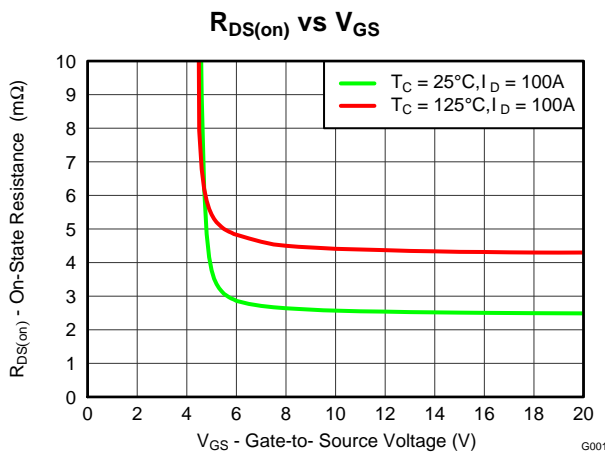


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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2014) to Revision B	Page
• Updated Pulsed Drain Current Conditions	1
• Updated the SOA in Figure 10	6

Changes from Original (January 2014) to Revision A	Page
• Increased Pulsed Drain Current Limit	1
• Updated Figure 9	5

5 Specifications

5.1 Electrical Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
V_{DSS}	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	80			V
I_{DSS}	Drain-to-Source Leakage Current	$V_{GS} = 0\text{ V}, V_{DS} = 64\text{ V}$			1	μA
I_{GSS}	Gate-to-Source Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.2	2.6	3.2	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = 6\text{ V}, I_D = 100\text{ A}$		2.9	3.8	m Ω
		$V_{GS} = 10\text{ V}, I_D = 100\text{ A}$		2.6	3.1	m Ω
g_{fs}	Transconductance	$V_{DS} = 8\text{ V}, I_D = 100\text{ A}$		262		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}, f = 1\text{ MHz}$		6090	7820	pF
C_{oss}	Output Capacitance			1600	2080	pF
C_{rss}	Reverse Transfer Capacitance			26	34	pF
R_G	Series Gate Resistance			1.4	2.8	Ω
Q_g	Gate Charge Total (10 V)	$V_{DS} = 40\text{ V}, I_D = 100\text{ A}$		76		nC
Q_{gd}	Gate Charge Gate to Drain			11		nC
Q_{gs}	Gate Charge Gate to Source			25		nC
$Q_{g(th)}$	Gate Charge at V_{th}			15		nC
Q_{oss}	Output Charge	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$		214		nC
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = 50\text{ V}, V_{GS} = 10\text{ V}, I_{DS} = 100\text{ A}, R_G = 0\ \Omega$		31		ns
t_r	Rise Time			16		ns
$t_{d(off)}$	Turn Off Delay Time			62		ns
t_f	Fall Time			6		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	$I_{SD} = 100\text{ A}, V_{GS} = 0\text{ V}$		0.9	1.1	V
Q_{rr}	Reverse Recovery Charge	$V_{DS} = 40\text{ V}, I_F = 100\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		400		nC
t_{rr}	Reverse Recovery Time			88		ns

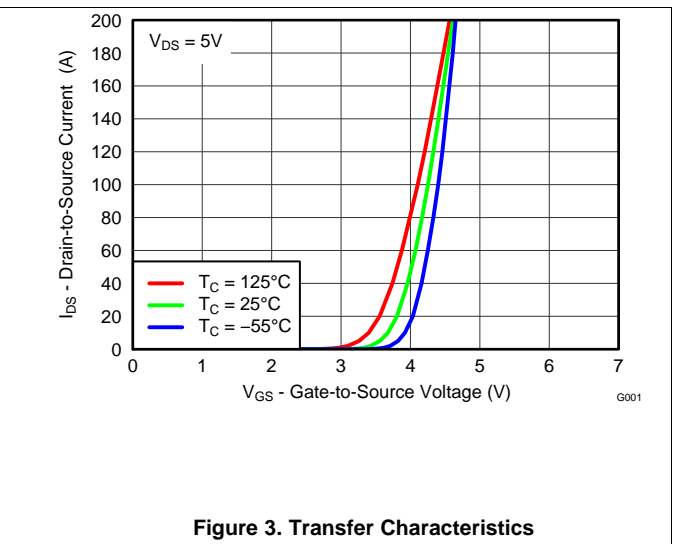
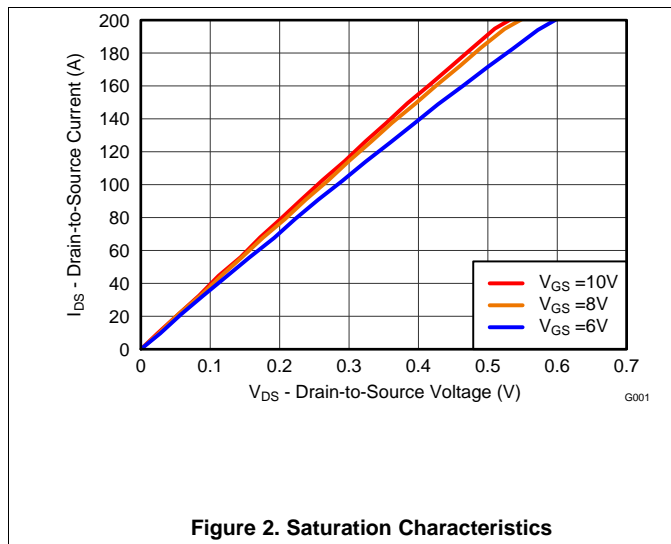
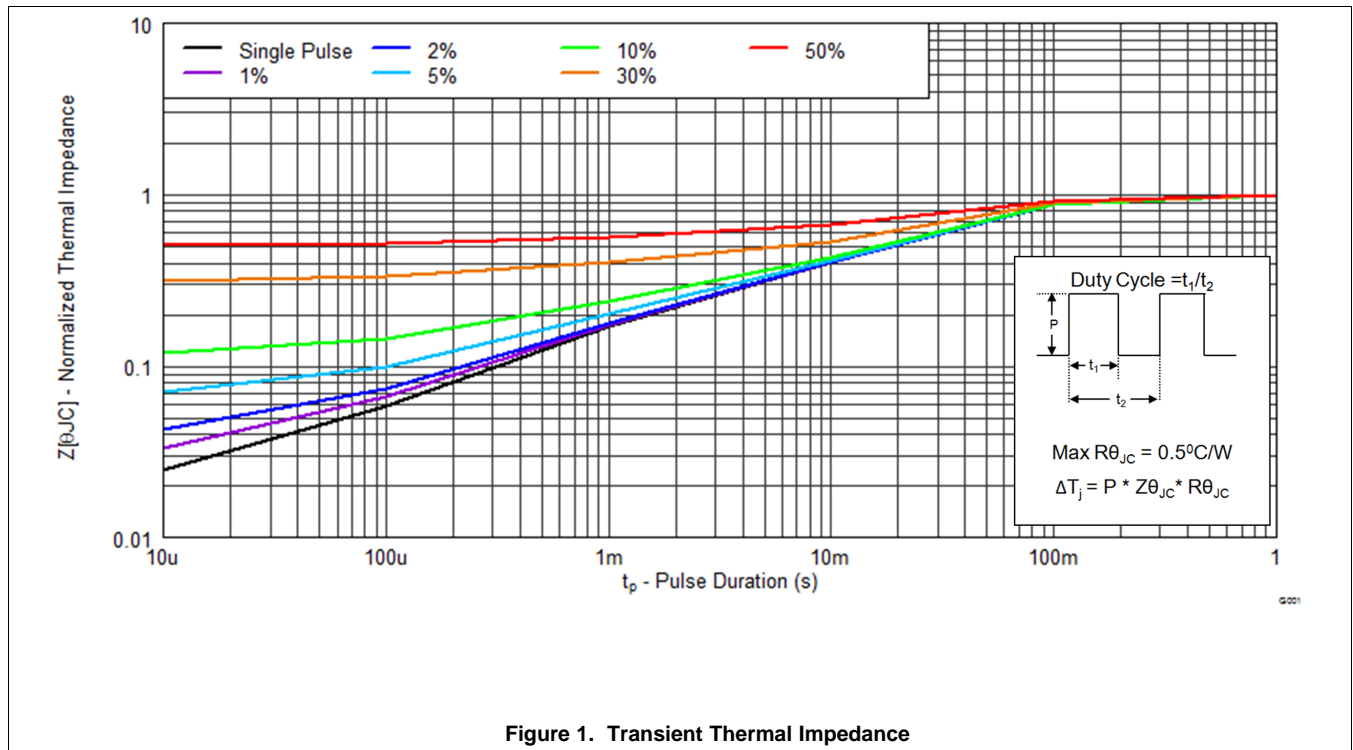
5.2 Thermal Information

($T_A = 25^\circ\text{C}$ unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance			0.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance			62	

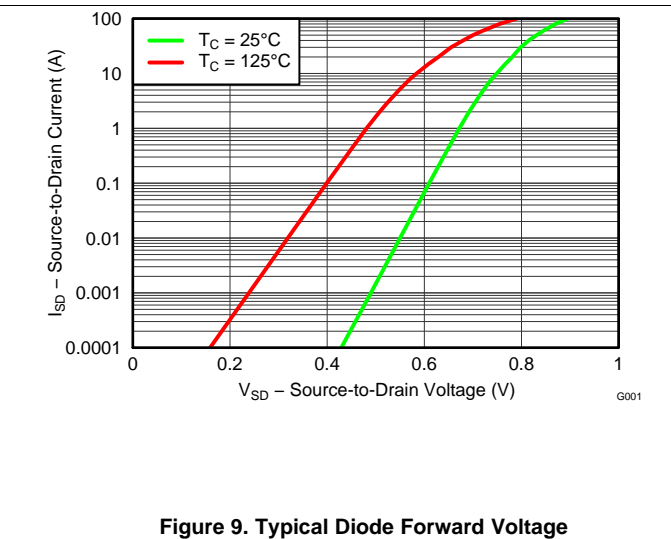
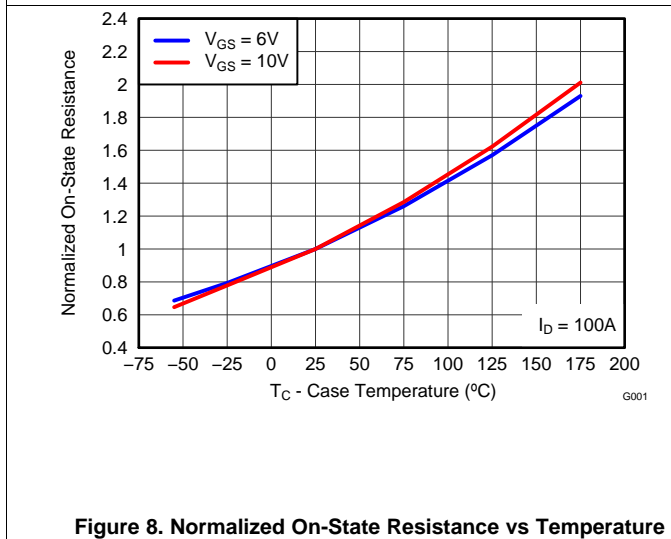
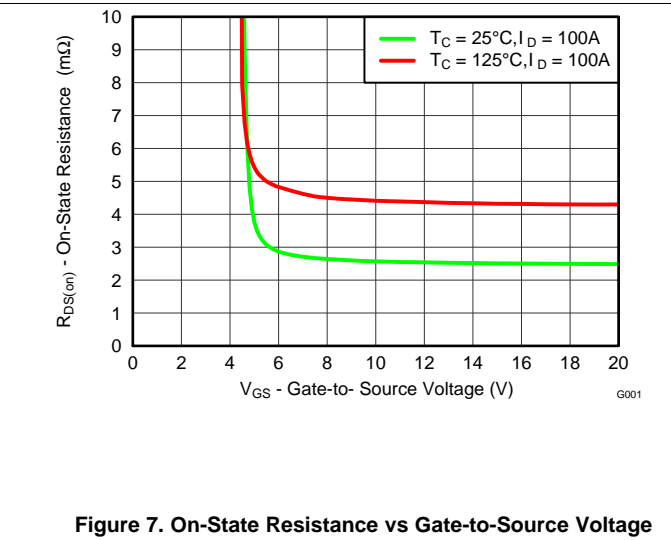
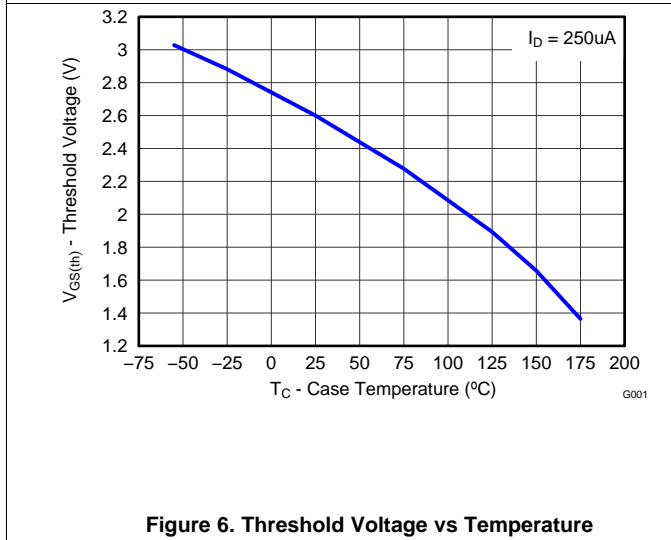
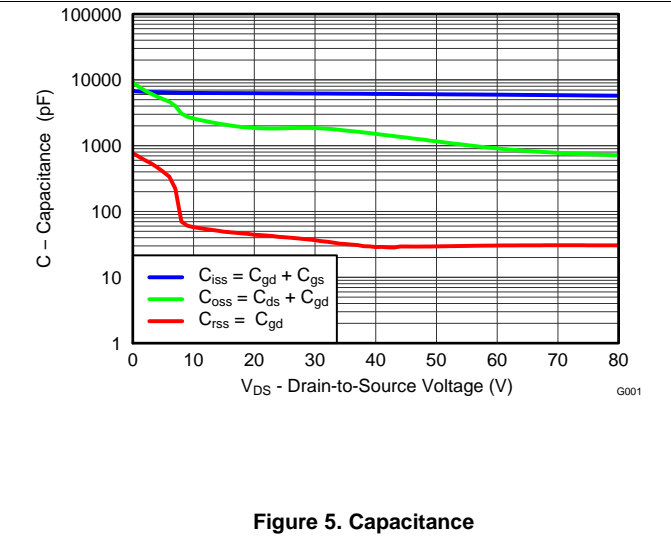
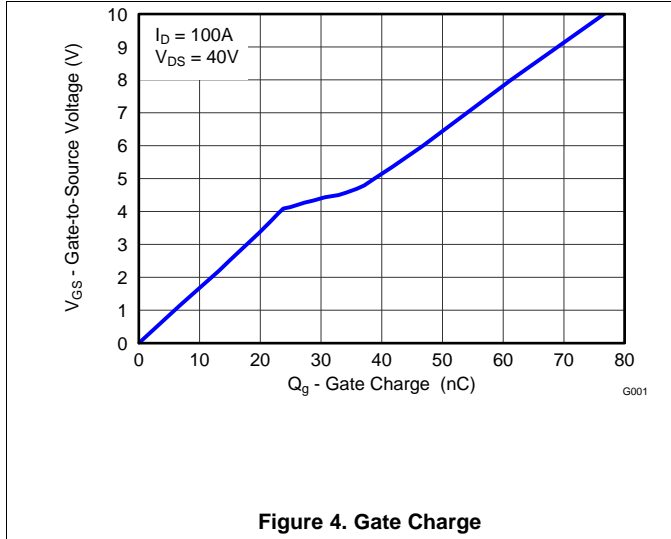
5.3 Typical MOSFET Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)



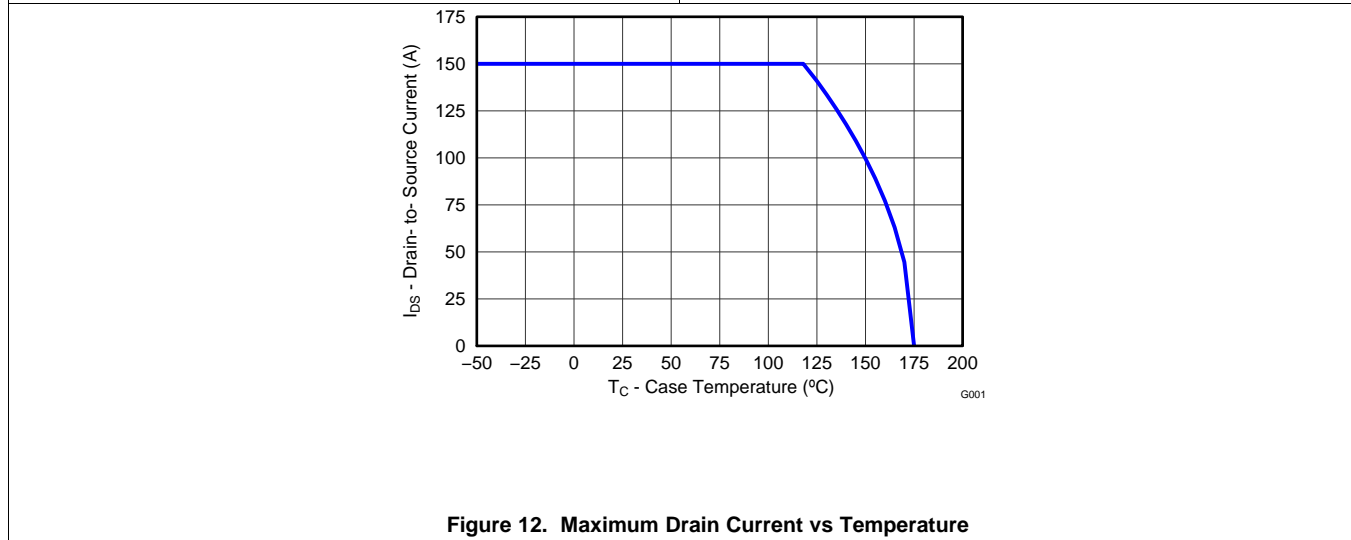
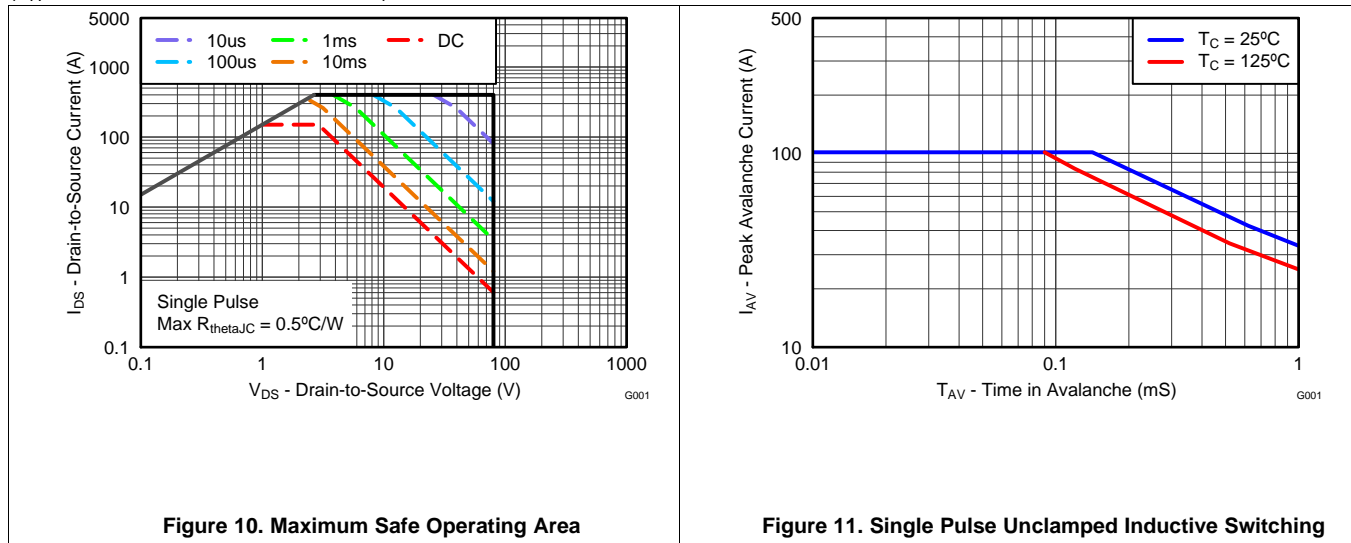
Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)



Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)



6 Device and Documentation Support

6.1 Trademarks

NexFET is a trademark of Texas Instruments.

6.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

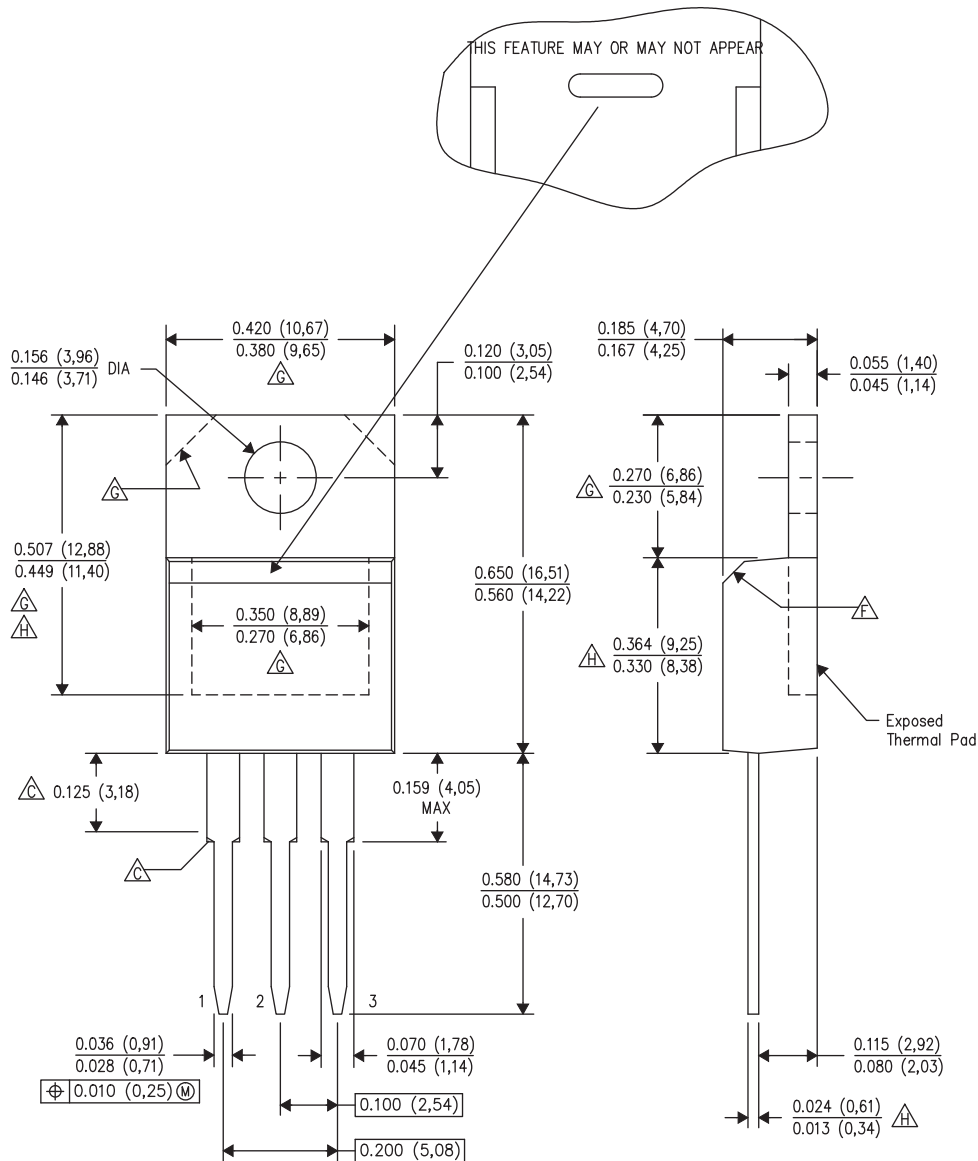
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 KCS Package Dimensions



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Lead dimensions are not controlled within this area. Chamfer may or may not appear
 - D. All lead dimensions apply before solder dip.
 - E. The center lead is in electrical contact with the mounting tab.
 - F. The chamfer is optional.
 - G. Thermal pad contour optional within these dimensions.
 - H. Falls within JEDEC TO-220 variation AB, except minimum lead thickness, minimum exposed pad length, and maximum body length.

Pin Configuration

Position	Designation
Pin 1	Gate
Pin 2 / Tab	Drain
Pin 3	Source

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD19505KCS	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-55 to 175	CSD19505KCS	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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