

- Output Swing includes Both Supply Rails
- Low Noise . . . 12 nV/√Hz Typ at f = 1 kHz
- Low Input Bias Current . . . 1 pA Typ
- Fully Specified for Both Single-Supply and Split-Supply Operation
- Low Power . . . 500 μA Max
- Common-Mode Input Voltage Range Includes Negative Rail
- Low Input Offset Voltage
950 μV Max at T_A = 25°C (TLC2262A)
- Macromodel Included
- Performance Upgrade for the TS27M2/M4 and TLC27M2/M4
- Available in Q-Temp Automotive HighRel Automotive Applications Configuration Control/Print Support Qualification to Automotive Standards

description

The TLC2262 and TLC2264 are dual and quadruple operational amplifiers from Texas Instruments. Both devices exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLC226x family offers a compromise between the micropower TLC225x and the ac performance of the TLC227x. It has low supply current for battery-powered applications, while still having adequate ac performance for applications that demand it. The noise performance has been dramatically improved over previous generations of CMOS amplifiers. Figure 1 depicts the low level of noise voltage for this CMOS amplifier, which has only 200 μA (typ) of supply current per amplifier.

The TLC226x, exhibiting high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micro-power dissipation levels, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLC226xA family is available and has a maximum input offset voltage of 950 μV. This family is fully characterized at 5 V and ±5 V.

The TLC2262/4 also makes great upgrades to the TLC27M2/L4 or TS27M2/L4 in standard designs. They offer increased output dynamic range, lower noise voltage and lower input offset voltage. This enhanced feature set allows them to be used in a wider range of applications. For applications that require higher output drive and wider input voltage range, see the TLV2432 and TLV2442. If your design requires single amplifiers, please see the TLV2211/21/31 family. These devices are single rail-to-rail operational amplifiers in the SOT-23 package. Their small size and low power consumption, make them ideal for high density, battery-powered equipment.

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

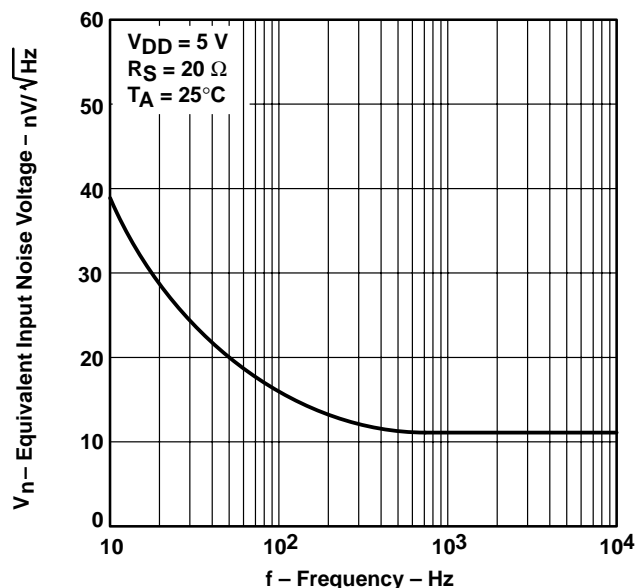


Figure 1



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Advanced LinCMOS is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2001, Texas Instruments Incorporated
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

TLC226x, TLC226xA Advanced LinCMOS™ RAIL-TO-RAIL OPERATIONAL AMPLIFIERS

SLOS177D – FEBRUARY 1997 – REVISED MARCH 2001

TLC2262 AVAILABLE OPTIONS

T _A	V _{IO} max AT 25°C	PACKAGED DEVICES					
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW)	CERAMIC FLATPACK (U)
0°C to 70°C	2.5 mV	TLC2262CD	—	—	TLC2262CP	TLC2262CPW	—
–40°C to 125°C	950 μV 2.5 mV	TLC2262AID TLC2262ID	— —	— —	TLC2262AIP TLC2262IP	TLC2262AIPW —	— —
–40°C to 125°C	950 μV 2.5 mV	TLC2262AQD TLC2262QD	— —	— —	— —	— —	— —
–55°C to 125°C	950 μV 2.5 mV	— —	TLC2262AMFK TLC2262MFK	TLC2262AMJG TLC2262MJG	— —	— —	TLC2262AMU TLC2262MU

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLC2262CDR). The PW package is available only left-end taped and reeled. Chips are tested at 25°C.

TLC2264 AVAILABLE OPTIONS

T _A	V _{IO} max AT 25°C	PACKAGED DEVICES					
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	TSSOP (PW)	CERAMIC FLATPACK (W)
0°C to 70°C	2.5 mV	TLC2264CD	—	—	TLC2264CN	TLC2264CPW	—
–40°C to 125°C	950 μV 2.5 mV	TLC2264AID TLC2264ID	— —	— —	TLC2264AIN TLC2264IN	TLC2264AIPW —	— —
–40°C to 125°C	950 μV 2.5 mV	TLC2264AQD TLC2264QD	— —	— —	— —	— —	— —
–55°C to 125°C	950 μV 2.5 mV	— —	TLC2264AMFK TLC2264MFK	TLC2264AMJ TLC2264MJ	— —	— —	TLC2264AMW TLC2264MW

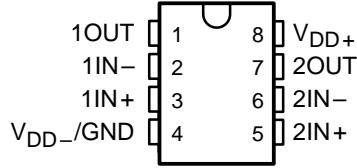
The D packages are available taped and reeled. Add R suffix to device type (e.g., TLC2264CDR). The PW package is available only left-end taped and reeled. Chips are tested at 25°C.



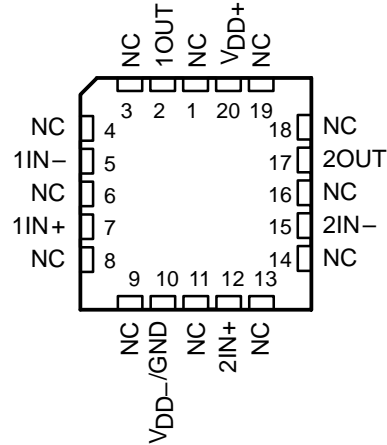
TLC226x, TLC226xA Advanced LinCMOS™ RAIL-TO-RAIL OPERATIONAL AMPLIFIERS

SLOS177D – FEBRUARY 1997 – REVISED MARCH 2001

**TLC2262C, TLC2262AC
TLC2262I, TLC2262AI
TLC2262Q, TLC2262AQ
D, P, OR PW PACKAGE
(TOP VIEW)**

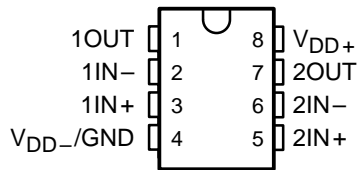


**TLC2262M, TLC2262AM ... FK PACKAGE
(TOP VIEW)**

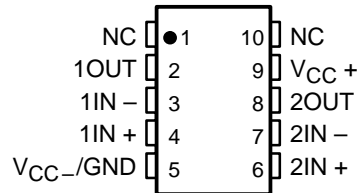


NC – No internal connection

**TLC2262M, TLC2262AM ... JG PACKAGE
(TOP VIEW)**

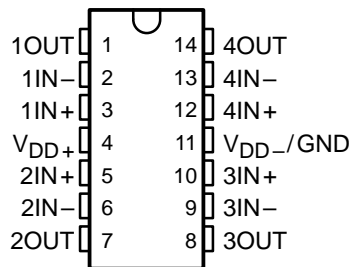


**TLC2262M, TLC2262AM ... U PACKAGE
(TOP VIEW)**

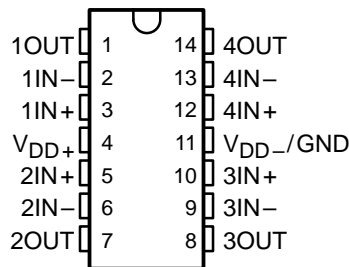


NC – No internal connection

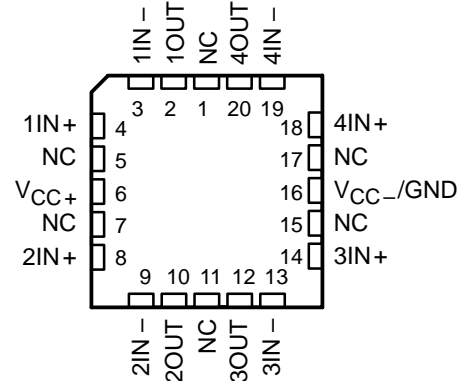
**TLC2264C, TLC2264AC
TLC2264I, TLC2264AI
TLC2264Q, TLC2264AQ
D, N, OR PW PACKAGE
(TOP VIEW)**



**TLC2264M, TLC2264AM ... J OR W PACKAGE
(TOP VIEW)**



**TLC2264M, TLC2264AM ... FK PACKAGE
(TOP VIEW)**

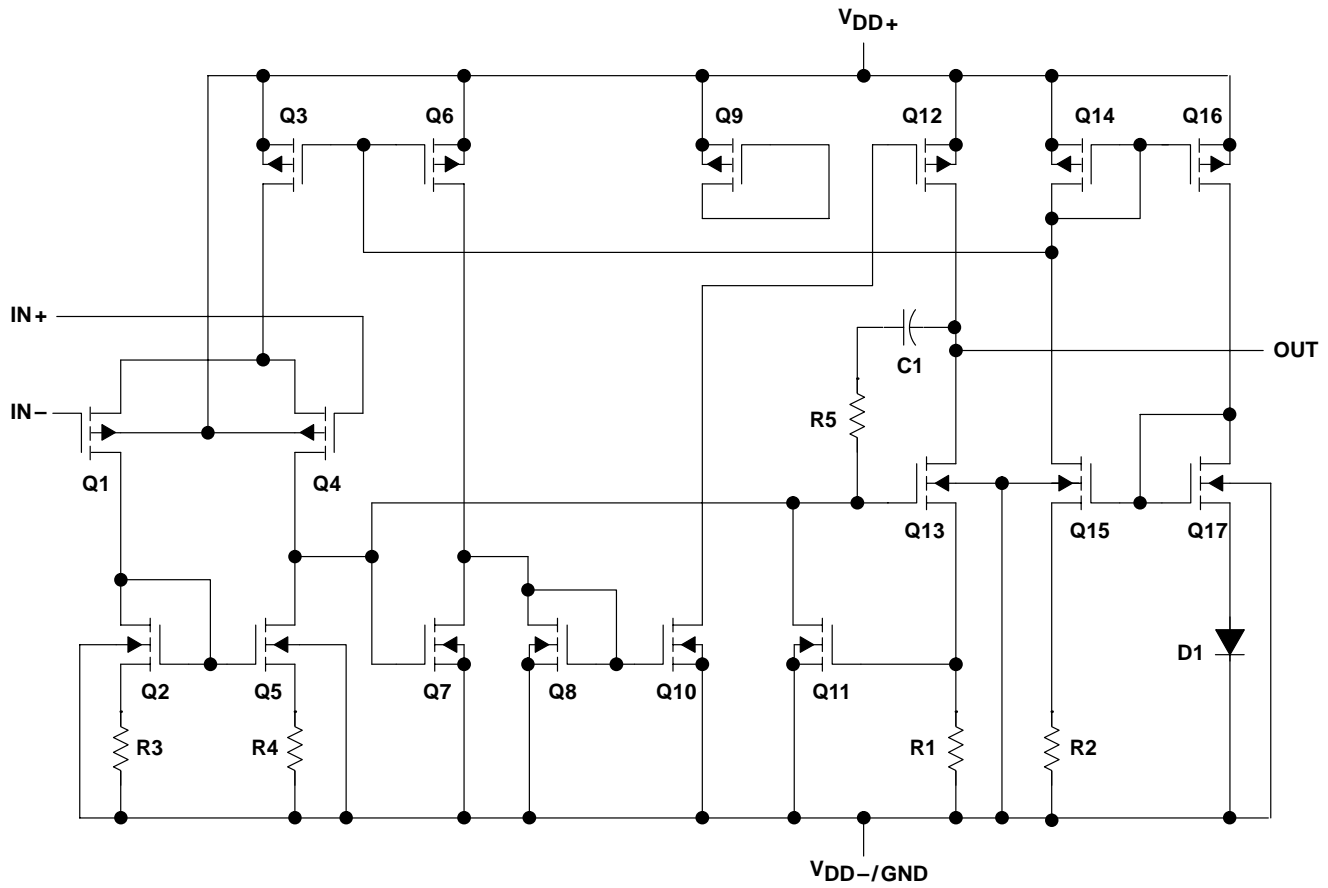


NC – No internal connection

TLC226x, TLC226xA
Advanced LinCMOS™ RAIL-TO-RAIL
OPERATIONAL AMPLIFIERS

SLOS177D – FEBRUARY 1997 – REVISED MARCH 2001

equivalent schematic (each amplifier)



ACTUAL DEVICE COMPONENT COUNT†		
COMPONENT	TLC2262	TLC2264
Transistors	38	76
Resistors	28	56
Diodes	9	18
Capacitors	3	6

† Includes both amplifiers and all ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD+} (see Note 1)	8 V
Supply voltage, V_{DD-} (see Note 1)	–8 V
Differential input voltage, V_{ID} (see Note 2)	±16 V
Input voltage, V_I (any input, see Note 1)	$V_{DD-} - 0.3 \text{ V}$ to V_{DD+}
Input current, I_I (each input)	±5 mA
Output current, I_O	±50 mA
Total current into V_{DD+}	±50 mA
Total current out of V_{DD-}	±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : C suffix	0°C to 70°C
I suffix	–40°C to 125°C
Q suffix	–40°C to 125°C
M suffix	–55°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, P, and PW packages	260°C
J, JG, U, and W packages	300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-} .
2. Differential voltages are at $IN+$ with respect to $IN-$. Excessive current flows if input is brought below $V_{DD-} - 0.3 \text{ V}$.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D–8	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
D–14	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW
PW–8	525 mW	4.2 mW/°C	336 mW	273 mW	105 mW
PW–14	700 mW	5.6 mW/°C	448 mW	364 mW	140 mW
U	700 mW	5.5 mW/°C	452 mW	370 mW	150 mW
W	700 mW	5.5 mW/°C	452 mW	370 mW	150 mW

recommended operating conditions

	C SUFFIX		I SUFFIX		Q SUFFIX		M SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{DD\pm}$	±2.2	±8	±2.2	±8	±2.2	±8	±2.2	±8	V
Input voltage range, V_I	V_{DD-}	$V_{DD+} - 1.5$	V_{DD-}	$V_{DD+} - 1.5$	V_{DD-}	$V_{DD+} - 1.5$	V_{DD-}	$V_{DD+} - 1.5$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+} - 1.5$	V_{DD-}	$V_{DD+} - 1.5$	V_{DD-}	$V_{DD+} - 1.5$	V_{DD-}	$V_{DD+} - 1.5$	V
Operating free-air temperature, T_A	0	70	–40	125	–40	125	–55	125	°C

TLC226x, TLC226xA Advanced LinCMOS™ RAIL-TO-RAIL OPERATIONAL AMPLIFIERS

SLOS177D – FEBRUARY 1997 – REVISED MARCH 2001

TLC2262C electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLC2262C			UNIT
			MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0,$ $V_O = 0,$ $V_{DD} = \pm 2.5\text{ V},$ $R_S = 50\ \Omega$	25°C	300	2500	μV	
		Full range	3000			
α_{VIO} Temperature coefficient of input offset voltage		25°C to 70°C	2		$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)		25°C	0.003		$\mu\text{V}/\text{mo}$	
I_{IO} Input offset current		25°C	0.5		pA	
		Full range	100			
I_{IB} Input bias current	25°C	1		pA		
	Full range	100				
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega,$ $ V_{IO} \leq 5\text{ mV}$	25°C	0 to 4	-0.3 to 4.2	V	
		Full range	0 to 3.5			
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$ $I_{OH} = -100\ \mu\text{A}$ $I_{OH} = -400\ \mu\text{A}$	25°C	4.99		V	
		25°C	4.85	4.94		
		Full range	4.82			
		25°C	4.70	4.85		
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V},$ $I_{OL} = 50\ \mu\text{A}$ $I_{OL} = 500\ \mu\text{A}$ $I_{OL} = 1\text{ mA}$ $I_{OL} = 4\text{ mA}$	25°C	0.01		V	
		25°C	0.09	0.15		
		Full range	0.15			
		25°C	0.2	0.3		
		Full range	0.3			
		25°C	0.7	1		
		Full range	1.2			
		A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V},$ $V_O = 1\text{ V to }4\text{ V}$	25°C		$R_L = 50\ \text{k}\Omega^\ddagger$
Full range						
25°C	$R_L = 1\ \text{M}\Omega^\ddagger$					
$r_{i(d)}$ Differential input resistance		25°C	10^{12}		Ω	
$r_{i(c)}$ Common-mode input resistance		25°C	10^{12}		Ω	
$c_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz},$ P package	25°C	8		pF	
z_o Closed-loop output impedance	$f = 100\text{ kHz},$ $A_V = 10$	25°C	240		Ω	
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.7\text{ V},$ $V_O = 2.5\text{ V},$ $R_S = 50\ \Omega$	25°C	70	83	dB	
		Full range	70			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }16\text{ V},$ $V_{IC} = V_{DD}/2,$ No load	25°C	80	95	dB	
		Full range	80			
I_{DD} Supply current	$V_O = 2.5\text{ V},$ No load	25°C	400	500	μA	
		Full range	500			

† Full range is 0°C to 70°C.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



TLC2262C operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER		TEST CONDITIONS		T_A †	TLC2262C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = 1.5\text{ V to }3.5\text{ V},$ $C_L = 100\text{ pF}‡$	$R_L = 50\text{ k}\Omega‡$	25°C	0.35	0.55	V/ μs	
				Full range	0.3			
V_n	Equivalent input noise voltage	$f = 10\text{ Hz}$		25°C	40		nV/ $\sqrt{\text{Hz}}$	
		$f = 1\text{ kHz}$		25°C	12			
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$		25°C	0.7		μV	
		$f = 0.1\text{ Hz to }10\text{ Hz}$		25°C	1.3			
I_n	Equivalent input noise current			25°C	0.6		fA/ $\sqrt{\text{Hz}}$	
THD + N	Total harmonic distortion plus noise	$V_O = 0.5\text{ V to }2.5\text{ V},$ $f = 20\text{ kHz},$ $R_L = 50\text{ k}\Omega‡$		25°C	$A_V = 1$	0.017%		
					$A_V = 10$	0.03%		
	Gain-bandwidth product	$f = 10\text{ kHz},$ $C_L = 100\text{ pF}‡$	$R_L = 50\text{ k}\Omega‡$	25°C	0.71		MHz	
BOM	Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V},$ $R_L = 50\text{ k}\Omega‡$	$A_V = 1,$ $C_L = 100\text{ pF}‡$	25°C	185		kHz	
t_s	Settling time	$A_V = -1,$ Step = 0.5 V to 2.5 V, $R_L = 50\text{ k}\Omega‡,$ $C_L = 100\text{ pF}‡$	To 0.1%	25°C	6.4		μs	
			To 0.01%		14.1			
ϕ_m	Phase margin at unity gain	$R_L = 50\text{ k}\Omega‡,$	$C_L = 100\text{ pF}‡$	25°C	56°			
	Gain margin			25°C	11		dB	

† Full range is 0°C to 70°C.

‡ Referenced to 2.5 V

TLC226x, TLC226xA
Advanced LinCMOS™ RAIL-TO-RAIL
OPERATIONAL AMPLIFIERS

SLOS177D – FEBRUARY 1997 – REVISED MARCH 2001

TLC2262C electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$ (unless otherwise specified)

PARAMETER	TEST CONDITIONS	T _A †	TLC2262C			UNIT
			MIN	TYP	MAX	
V _{IO} Input offset voltage	V _{IC} = 0, V _O = 0, R _S = 50 Ω	25°C		300	2500	μV
		Full range			3000	
αV _{IO} Temperature coefficient of input offset voltage		25°C to 70°C		2		μV/°C
Input offset voltage long-term drift (see Note 4)		25°C		0.003		μV/mo
I _{IO} Input offset current		25°C		0.5		pA
		Full range			100	
I _{IB} Input bias current		25°C		1		pA
		Full range			100	
V _{ICR} Common-mode input voltage range		V _{IO} ≤ 5 mV, R _S = 50 Ω	25°C	-5 to 4	-5.3 to 4.2	V
			Full range	-5 to 3.5		
V _{OM+} Maximum positive peak output voltage	I _O = -20 μA	25°C		4.99	V	
	I _O = -100 μA	25°C	4.85	4.94		
		Full range	4.82			
	I _O = -400 μA	25°C	4.7	4.85		
Full range		4.6				
V _{OM-} Maximum negative peak output voltage	V _{IC} = 0, I _O = 50 μA	25°C		-4.99	V	
		25°C	-4.85	-4.91		
	V _{IC} = 0, I _O = 500 μA	Full range	-4.85			
		25°C	-4.7	-4.8		
	V _{IC} = 0, I _O = 1 mA	Full range	-4.7			
		25°C	-4	-4.3		
V _{IC} = 0, I _O = 4 mA	Full range	-3.8				
	V _O = ±4 V	25°C	80	200	V/mV	
R _L = 50 kΩ		Full range	55			
		R _L = 1 MΩ	25°C			1000
r _{i(d)} Differential input resistance		25°C		10 ¹²	Ω	
r _{i(c)} Common-mode input resistance		25°C		10 ¹²	Ω	
c _{i(c)} Common-mode input capacitance	f = 10 kHz, P package	25°C		8	pF	
z _o Closed-loop output impedance	f = 100 kHz, A _V = 10	25°C		220	Ω	
CMRR Common-mode rejection ratio	V _{IC} = -5 V to 2.7 V, V _O = 0 V, R _S = 50 Ω	25°C	75	88	dB	
		Full range	75			
k _{SVR} Supply-voltage rejection ratio (ΔV _{DD±} / ΔV _{IO})	V _{DD±} = 2.2 V to ±8 V, V _{IC} = 0, No load	25°C	80	95	dB	
		Full range	80			
I _{DD} Supply current	V _O = 0 V, No load	25°C	425	500	μA	
		Full range		500		

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.



TLC226x, TLC226xA
Advanced LinCMOS™ RAIL-TO-RAIL
OPERATIONAL AMPLIFIERS

SLOS177D – FEBRUARY 1997 – REVISED MARCH 2001

TLC2262C operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$

PARAMETER		TEST CONDITIONS		T_A †	TLC2262C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm 1.9\text{ V}$, $C_L = 100\text{ pF}$	$R_L = 50\text{ k}\Omega$	25°C	0.35	0.55	$\text{V}/\mu\text{s}$	
				Full range	0.3			
V_n	Equivalent input noise voltage			25°C	43		$\text{nV}/\sqrt{\text{Hz}}$	
				25°C	12			
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage			25°C	0.8		μV	
				25°C	1.3			
I_n	Equivalent input noise current			25°C	0.6		$\text{fA}/\sqrt{\text{Hz}}$	
THD + N	Total harmonic distortion pulse duration	$V_O = \pm 2.3\text{ V}$, $f = 20\text{ kHz}$, $R_L = 50\text{ k}\Omega$		25°C	$A_V = 1$	0.014%		
					$A_V = 10$	0.024%		
Gain-bandwidth product		$f = 10\text{ kHz}$, $C_L = 100\text{ pF}$	$R_L = 50\text{ k}\Omega$	25°C	0.73		MHz	
BOM	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6\text{ V}$, $R_L = 50\text{ k}\Omega$,	$A_V = 1$, $C_L = 100\text{ pF}$	25°C	85		kHz	
t_s	Settling time	$A_V = -1$, Step = -2.3 V to 2.3 V , $R_L = 50\text{ k}\Omega$, $C_L = 100\text{ pF}$		25°C	To 0.1%	7.1		
					To 0.01%	16.5		
ϕ_m	Phase margin at unity gain	$R_L = 50\text{ k}\Omega$,	$C_L = 100\text{ pF}$	25°C	57°			
	Gain margin			25°C	11			

† Full range is 0°C to 70°C.

TLC226x, TLC226xA Advanced LinCMOS™ RAIL-TO-RAIL OPERATIONAL AMPLIFIERS

SLOS177D – FEBRUARY 1997 – REVISED MARCH 2001

TLC2264C electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLC2264C			UNIT
			MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0,$ $V_O = 0,$ $V_{DD\pm} = \pm 2.5\text{ V},$ $R_S = 50\ \Omega$	25°C	300	2500	μV	
		Full range	3000			
α_{VIO} Temperature coefficient of input offset voltage		25°C to 70°C	2		$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)		25°C	0.003		$\mu\text{V}/\text{mo}$	
I_{IO} Input offset current		25°C	0.5		pA	
		Full range	100			
I_{IB} Input bias current	25°C	1		pA		
	Full range	100				
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega,$ $ V_{IO} \leq 5\text{ mV}$	25°C	0 to 4	-0.3 to 4.2	V	
		Full range	0 to 3.5			
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C	4.99		V	
	$I_{OH} = -100\ \mu\text{A}$	25°C	4.85	4.94		
	$I_{OH} = -400\ \mu\text{A}$	Full range	4.82			
		25°C	4.70	4.85		
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V},$ $I_{OL} = 50\ \mu\text{A}$	25°C	0.01		V	
		Full range	0.09	0.15		
	$V_{IC} = 2.5\text{ V},$ $I_{OL} = 500\ \mu\text{A}$	25°C	0.09			
		Full range	0.15			
	$V_{IC} = 2.5\text{ V},$ $I_{OL} = 1\text{ mA}$	25°C	0.2	0.3		
		Full range	0.3			
$V_{IC} = 2.5\text{ V},$ $I_{OL} = 4\text{ mA}$	25°C	0.7	1			
	Full range	1.2				
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V},$ $V_O = 1\text{ V to } 4\text{ V}$	$R_L = 50\text{ k}\Omega^\ddagger$	25°C	80	170	V/mV
		$R_L = 1\text{ M}\Omega^\ddagger$	Full range	55		
			25°C	550		
$r_{i(d)}$ Differential input resistance		25°C	10^{12}		Ω	
$r_{i(c)}$ Common-mode input resistance		25°C	10^{12}		Ω	
$c_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz},$ N package	25°C	8		pF	
z_o Closed-loop output impedance	$f = 100\text{ kHz},$ $A_V = 10$	25°C	240		Ω	
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to } 2.7\text{ V},$ $V_O = 2.5\text{ V},$ $R_S = 50\ \Omega$	25°C	70	83	dB	
		Full range	70			
kSVR Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to } 16\text{ V},$ $V_{IC} = V_{DD}/2,$ No load	25°C	80	95	dB	
		Full range	80			
I_{DD} Supply current (four amplifiers)	$V_O = 2.5\text{ V},$ No load	25°C	0.8	1	mA	
		Full range	1			

† Full range is 0°C to 70°C.

‡ Referenced to 2.5 V

NOTE 4. Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



TLC226x, TLC226xA
Advanced LinCMOS™ RAIL-TO-RAIL
OPERATIONAL AMPLIFIERS

SLOS177D – FEBRUARY 1997 – REVISED MARCH 2001

TLC2264C operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER		TEST CONDITIONS		T_A †	TLC2264C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = 1.4\text{ V to }2.6\text{ V}, R_L = 50\text{ k}\Omega^\ddagger, C_L = 100\text{ pF}^\ddagger$		25°C	0.35	0.55	V/ μs	
				Full range	0.3			
V_n	Equivalent input noise voltage			25°C	40		nV/ $\sqrt{\text{Hz}}$	
				25°C	12			
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage			25°C	0.7		μV	
				25°C	1.3			
I_n	Equivalent input noise current			25°C	0.6		fA/ $\sqrt{\text{Hz}}$	
THD + N	Total harmonic distortion plus noise	$V_O = 0.5\text{ V to }2.5\text{ V}, f = 20\text{ kHz}, R_L = 50\text{ k}\Omega^\ddagger$		25°C	$A_V = 1$	0.017%		
					$A_V = 10$	0.03%		
Gain-bandwidth product		$f = 10\text{ kHz}, C_L = 100\text{ pF}^\ddagger$		25°C	0.71		MHz	
BOM	Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V}, R_L = 50\text{ k}\Omega^\ddagger,$		25°C	185		kHz	
t_s	Settling time	$A_V = -1, \text{ Step} = 0.5\text{ V to }2.5\text{ V}, R_L = 50\text{ k}\Omega^\ddagger, C_L = 100\text{ pF}^\ddagger$		25°C	To 0.1%	6.4	μs	
					To 0.01%	14.1		
ϕ_m	Phase margin at unity gain	$R_L = 50\text{ k}\Omega^\ddagger, C_L = 100\text{ pF}^\ddagger$		25°C	56°			
	Gain margin			25°C	11		dB	

† Full range is 0°C to 70°C.

‡ Referenced to 2.5 V

TLC226x, TLC226xA
Advanced LinCMOS™ RAIL-TO-RAIL
OPERATIONAL AMPLIFIERS

SLOS177D – FEBRUARY 1997 – REVISED MARCH 2001

TLC2264C electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$ (unless otherwise specified)

PARAMETER	TEST CONDITIONS	T _A †	TLC2264C			UNIT
			MIN	TYP	MAX	
V _{IO} Input offset voltage	V _{IC} = 0, V _O = 0, R _S = 50 Ω	25°C	300	2500	μV	
		Full range	3000			
α _{VIO} Temperature coefficient of input offset voltage		25°C to 70°C	2		μV/°C	
Input offset voltage long-term drift (see Note 4)		25°C	0.003		μV/mo	
I _{IO} Input offset current		25°C	0.5		pA	
		Full range	100			
I _{IB} Input bias current		25°C	1		pA	
		Full range	100			
V _{ICR} Common-mode input voltage range	V _{IO} ≤ 5 mV, R _S = 50 Ω	25°C	-5 to 4	-5.3 to 4.2	V	
		Full range	-5 to 3.5			
V _{OM+} Maximum positive peak output voltage	I _O = -20 μA	25°C	4.99		V	
	I _O = -100 μA	25°C	4.85	4.94		
		Full range	4.82			
	I _O = -400 μA	25°C	4.7	4.85		
Full range		4.6				
V _{OM-} Maximum negative peak output voltage	V _{IC} = 0, I _O = 50 μA	25°C	-4.99		V	
		25°C	-4.85	-4.91		
	V _{IC} = 0, I _O = 500 μA	Full range	-4.85			
		25°C	-4.7	-4.8		
	V _{IC} = 0, I _O = 1 mA	Full range	-4.7			
		25°C	-4	-4.3		
V _{IC} = 0, I _O = 4 mA	Full range	-3.8				
	A _{VD} Large-signal differential voltage amplification	V _O = ±4 V	R _L = 50 kΩ	25°C	80	200
Full range				55		
R _L = 1 MΩ			25°C	1000		
r _{i(d)} Differential input resistance		25°C	10 ¹²		Ω	
r _{i(c)} Common-mode input resistance		25°C	10 ¹²		Ω	
c _{i(c)} Common-mode input capacitance	f = 10 kHz, N package	25°C	8		pF	
z _o Closed-loop output impedance	f = 100 kHz, A _V = 10	25°C	220		Ω	
CMRR Common-mode rejection ratio	V _{IC} = -5 V to 2.7 V, V _O = 0, R _S = 50 Ω	25°C	75	88	dB	
		Full range	75			
k _{SVR} Supply-voltage rejection ratio (ΔV _{DD±} /ΔV _{IO})	V _{DD±} = ±2.2 V to ±8 V, V _{IC} = 0, No load	25°C	80	95	dB	
		Full range	80			
I _{DD} Supply current (four amplifiers)	V _O = 0, No load	25°C	0.85	1	mA	
		Full range	1			

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TLC2264C operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$

PARAMETER		TEST CONDITIONS		T_A †	TLC2264C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm 1.9\text{ V}$, $C_L = 100\text{ pF}$	$R_L = 50\text{ k}\Omega$	25°C	0.35	0.55	$\text{V}/\mu\text{s}$	
				Full range	0.3			
V_n	Equivalent input noise voltage			25°C	43		$\text{nV}/\sqrt{\text{Hz}}$	
				25°C	12			
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage			25°C	0.8		μV	
				25°C	1.3			
I_n	Equivalent input noise current			25°C	0.6		$\text{fA}/\sqrt{\text{Hz}}$	
THD + N	Total harmonic distortion plus noise	$V_O = \pm 2.3\text{ V}$, $f = 20\text{ kHz}$, $R_L = 50\text{ k}\Omega$		25°C	$A_V = 1$	0.014%		
					$A_V = 10$	0.024%		
Gain-bandwidth product		$f = 10\text{ kHz}$, $C_L = 100\text{ pF}$	$R_L = 50\text{ k}\Omega$	25°C	0.73		MHz	
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6\text{ V}$, $R_L = 50\text{ k}\Omega$	$A_V = 1$, $C_L = 100\text{ pF}$	25°C	70		kHz	
t_s	Settling time	$A_V = -1$, Step = -2.3 V to 2.3 V , $R_L = 50\text{ k}\Omega$, $C_L = 100\text{ pF}$		25°C	To 0.1%	7.1		
					To 0.01%	16.5		
ϕ_m	Phase margin at unity gain	$R_L = 50\text{ k}\Omega$	$C_L = 100\text{ pF}$	25°C	57°			
	Gain margin			25°C	11			

† Full range is 0°C to 70°C.

TLC226x, TLC226xA Advanced LinCMOS™ RAIL-TO-RAIL OPERATIONAL AMPLIFIERS

SLOS177D – FEBRUARY 1997 – REVISED MARCH 2001

TLC2262I electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLC2262I			TLC2262AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{DD\pm} = \pm 2.5\text{ V}$, $V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	25°C	300	2500		300	950		μV
		Full range			3000		1500		
α_{VIO} Temperature coefficient of input offset voltage		25°C to 85°C		2			2		$\mu\text{V}/^\circ\text{C}$
		25°C		0.003			0.003		$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C		0.5			0.5		pA
		85°C			150		150		
		Full range			800		800		pA
I_{IB} Input bias current		25°C		1			1		pA
	85°C			150		150		pA	
	Full range			800		800		pA	
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$, $ V_{IO} \leq 5\text{ mV}$	25°C	0 to 4	-0.3 to 4.2		0 to 4	-0.3 to 4.2		V
		Full range	0 to 3.5			0 to 3.5			
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$ $I_{OH} = -100\ \mu\text{A}$ $I_{OH} = -400\ \mu\text{A}$	25°C		4.99			4.99		V
		25°C	4.85	4.94		4.85	4.94		
		Full range	4.82			4.82			
		25°C	4.7	4.85		4.7	4.85		
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$ $I_{OL} = 500\ \mu\text{A}$ $I_{OL} = 4\text{ mA}$	25°C		0.01			0.01		V
		25°C	0.09	0.15		0.09	0.15		
		Full range		0.15			0.15		
		25°C	0.8	1		0.7	1		
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$, $V_O = 1\text{ V to } 4\text{ V}$	$R_L = 50\ \text{k}\Omega$ ‡	25°C	80	100		80	170	V/mV
			Full range	50			50		
		$R_L = 1\ \text{M}\Omega$ ‡	25°C		550			550	
$r_{i(d)}$ Differential input resistance		25°C		10^{12}			10^{12}	Ω	
$r_{i(c)}$ Common-mode input resistance		25°C		10^{12}			10^{12}	Ω	
$C_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz}$, P package	25°C		8			8	pF	
z_o Closed-loop output impedance	$f = 100\text{ kHz}$, $A_V = 10$	25°C		240			240	Ω	
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to } 2.7\text{ V}$, $V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$	25°C	70	83		70	83	dB	
		Full range	70			70			

† Full range is -40°C to 125°C .

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



TLC2262I operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	T_A †	TLC2262I			TLC2262AI			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX		
k_{SVR}	Supply-voltage re-jection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }16\text{ V}$, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	95	dB	
			Full range	80			80			
I_{DD}	Supply current	$V_O = 2.5\text{ V}$, No load	25°C		400	500		400	500	μA
			Full range			500			500	
SR	Slew rate at unity gain	$V_O = 1.5\text{ V to }3.5\text{ V}$, $R_L = 50\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C	0.35	0.55		0.35	0.55	$\text{V}/\mu\text{s}$	
			Full range	0.25			0.25			
V_n	Equivalent input noise voltage	$f = 10\text{ Hz}$ $f = 1\text{ kHz}$	25°C		40			40	$\text{nV}/\sqrt{\text{Hz}}$	
			25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$ $f = 0.1\text{ Hz to }10\text{ Hz}$	25°C		0.7			0.7	μV	
			25°C		1.3			1.3		
I_n	Equivalent input noise current		25°C		0.6			0.6	$\text{fA}/\sqrt{\text{Hz}}$	
THD + N	Total harmonic distortion plus noise	$V_O = 0.5\text{ V to }2.5\text{ V}$, $f = 20\text{ kHz}$, $R_L = 50\text{ k}\Omega$ ‡	$A_V = 1$	25°C	0.017%		0.017%			
			$A_V = 10$		0.03%		0.03%			
	Gain-bandwidth product	$f = 50\text{ kHz}$, $C_L = 100\text{ pF}$ ‡	$R_L = 50\text{ k}\Omega$ ‡,	25°C	0.82		0.82		MHz	
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V}$, $R_L = 50\text{ k}\Omega$ ‡,	$A_V = 1$, $C_L = 100\text{ pF}$ ‡	25°C	185		185		kHz	
t_s	Settling time	$A_V = -1$, Step = $0.5\text{ V to }2.5\text{ V}$, $R_L = 50\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡	To 0.1%	25°C	6.4		6.4		μs	
			To 0.01%		14.1		14.1			
ϕ_m	Phase margin at unity gain	$R_L = 50\text{ k}\Omega$ ‡,	$C_L = 100\text{ pF}$ ‡	25°C	56°		56°			
	Gain margin			25°C	11		11			dB

† Full range is $-40^\circ\text{C to }125^\circ\text{C}$.

‡ Referenced to 2.5 V

TLC226x, TLC226xA
Advanced LinCMOS™ RAIL-TO-RAIL
OPERATIONAL AMPLIFIERS

SLOS177D – FEBRUARY 1997 – REVISED MARCH 2001

TLC2262I electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLC2262I			TLC2262AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0, V_O = 0$ $R_S = 50\ \Omega$	25°C	300	2500		300	950	μV	
		Full range			3000		1500		
αV_{IO} Temperature coefficient of input offset voltage		25°C to 85°C	2			2			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C	0.003			0.003			$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C	0.5			0.5			pA
		85°C				150			pA
		Full range				800			pA
I_{IB} Input bias current		25°C	1			1			pA
	85°C				150			pA	
	Full range				800			pA	
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega, V_{IO} \leq 5\text{ mV}$	25°C	-5 to 4	-5.3 to 4.2		-5 to 4	-5.3 to 4.2	V	
		Full range	-5 to 3.5			-5 to 3.5			
V_{OM+} Maximum positive peak output voltage	$I_O = -20\ \mu\text{A}$	25°C	4.99		4.99		V		
		Full range	4.82		4.82				
	$I_O = -100\ \mu\text{A}$	25°C	4.7		4.85				
		Full range	4.5		4.5				
V_{OM-} Maximum negative peak output voltage	$V_{IC} = 0, I_O = 50\ \mu\text{A}$	25°C	-4.99		-4.99		V		
		Full range	-4.85		-4.85				
	$V_{IC} = 0, I_O = 500\ \mu\text{A}$	25°C	-4.85		-4.91				
		Full range	-4.85		-4.85				
$V_{IC} = 0, I_O = 4\ \text{mA}$	25°C	-4		-4.3		V			
	Full range	-3.8		-3.8					
	Full range	-3.8		-3.8					
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 4\ \text{V}$	$R_L = 50\ \text{k}\Omega$	25°C	80	200	80	200	V/mV	
			Full range	50		50			
		$R_L = 1\ \text{M}\Omega$	25°C	1000		1000			
$r_{i(d)}$ Differential input resistance		25°C	1012			1012		Ω	
$r_{i(c)}$ Common-mode input resistance		25°C	1012			1012		Ω	
$C_{i(c)}$ Common-mode input capacitance	$f = 10\ \text{kHz}, \text{ P package}$	25°C	8			8		pF	
z_o Closed-loop output impedance	$f = 100\ \text{kHz}, A_V = 10$	25°C	220			220		Ω	
CMRR Common-mode rejection ratio	$V_{IC} = -5\ \text{V to } 2.7\ \text{V}, V_O = 0, R_S = 50\ \Omega$	25°C	75	88	75	88	dB		
		Full range	75		75				
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD} = 4.4\ \text{V to } 16\ \text{V}, V_{IC} = V_{DD}/2, \text{ No load}$	25°C	80	95	80	95	dB		
		Full range	80		80				

† Full range is -40°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



TLC2262I operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$

PARAMETER	TEST CONDITIONS	T_A †	TLC2262I			TLC2262AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{DD} Supply Current	$V_O = 2.5\text{ V}$, No load	25°C	425	500		425	500		
		Full range		500			500		
SR Slew rate at unity gain	$V_O = \pm 1.9\text{ V}$, $R_L = 50\text{ k}\Omega$, $C_L = 100\text{ pF}$	25°C	0.35	0.55		0.35	0.55	V/ μs	
		Full range	0.25			0.25			
V_n Equivalent input noise voltage	$f = 10\text{ Hz}$	25°C		43			43	nV/ $\sqrt{\text{Hz}}$	
	$f = 1\text{ kHz}$	25°C		12			12		
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$	25°C		0.8			0.8	μV	
	$f = 0.1\text{ Hz to }10\text{ Hz}$	25°C		1.3			1.3		
I_n Equivalent input noise current		25°C		0.6			0.6	fA/ $\sqrt{\text{Hz}}$	
THD + N Total harmonic distortion plus noise	$V_O = \pm 2.3\text{ V}$, $R_L = 50\text{ k}\Omega$, $f = 20\text{ kHz}$	$A_V = 1$	25°C		0.014%	0.014%			
		$A_V = 10$	25°C		0.024%	0.024%			
Gain-bandwidth product	$f = 10\text{ kHz}$, $R_L = 50\text{ k}\Omega$, $C_L = 100\text{ pF}$	25°C		0.73			0.73	MHz	
B_{OM} Maximum output-swing bandwidth	$V_{O(PP)} = 4.6\text{ V}$, $R_L = 50\text{ k}\Omega$, $A_V = 1$, $C_L = 100\text{ pF}$	25°C		85			85	kHz	
t_s Settling time	$A_V = -1$, Step = $-2.3\text{ V to }2.3\text{ V}$, $R_L = 50\text{ k}\Omega$, $C_L = 100\text{ pF}$	To 0.1%	25°C		7.1	7.1		μs	
		To 0.01%	25°C		16.5	16.5			
ϕ_m Phase margin at unity gain	$R_L = 50\text{ k}\Omega$, $C_L = 100\text{ pF}$	25°C		57°			57°		
		25°C		11			11		
Gain margin		25°C		11			11	dB	

† Full range is -40°C to 125°C .

TLC226x, TLC226xA Advanced LinCMOS™ RAIL-TO-RAIL OPERATIONAL AMPLIFIERS

SLOS177D – FEBRUARY 1997 – REVISED MARCH 2001

TLC2264I electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLC2264I			TLC2264AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{DD} = \pm 2.5\text{ V}$, $V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	25°C	300	2500		300	950	μV	
		Full range			3000		1500		
αV_{IO} Temperature coefficient of input offset voltage		25°C to 125°C	2			2		$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)		25°C	0.003			0.003		$\mu\text{V}/\text{mo}$	
I_{IO} Input offset current		25°C	0.5			0.5		pA	
		85°C		150		150			
		Full range		800		800			
I_{IB} Input bias current		25°C	1			1		pA	
		85°C		150		150			
		Full range		800		800			
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$, $ V_{IO} \leq 5\text{ mV}$	25°C	0 to 4	-0.3 to 4.2		0 to 4	-0.3 to 4.2	V	
		Full range	0 to 3.5		0 to 3.5				
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C	4.99		4.99		V		
	$I_{OH} = -100\ \mu\text{A}$	25°C	4.85	4.94	4.85	4.94			
		Full range	4.82		4.82				
	$I_{OH} = -400\ \mu\text{A}$	25°C	4.7	4.85	4.7	4.85			
Full range		4.5		4.5					
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$	25°C	0.01		0.01		V		
		Full range	0.09	0.15	0.09	0.15			
	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$	25°C	0.09	0.15	0.09	0.15			
		Full range	0.15		0.15				
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 4\text{ mA}$	25°C	0.8	1	0.7	1	V		
		Full range	1.2		1.2				
	$V_{IC} = 2.5\text{ V}$, $V_O = 1\text{ V to }4\text{ V}$	$R_L = 50\ \text{k}\Omega$ ‡	25°C	80	100	80		170	V/mV
		Full range	50		50				
$R_L = 1\ \text{M}\Omega$ ‡	25°C	550		550					
$r_{i(d)}$ Differential input resistance		25°C	10^{12}		10^{12}		Ω		
$r_{i(c)}$ Common-mode input resistance		25°C	10^{12}		10^{12}		Ω		
$C_{i(c)}$ Common-mode input capacitance	$f = 10\ \text{kHz}$, N package	25°C	8		8		pF		
z_o Closed-loop output impedance	$f = 100\ \text{kHz}$, $A_V = 10$	25°C	240		240		Ω		
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.7\text{ V}$, $V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$	25°C	70	83	70	83	dB		
		Full range	70		70				
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }16\text{ V}$, $V_{IC} = V_{DD}/2$, No load	25°C	80	95	80	95	dB		
		Full range	80		80				

† Full range is -40°C to 125°C .

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



TLC2264I operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	T_A †	TLC2264I			TLC2264AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{DD} Supply current (four amplifiers)	$V_O = 2.5\text{ V}$, No load	25°C	0.8	1		0.8	1	$V/\mu\text{s}$	
		Full range			1		1		
SR Slew rate at unity gain	$V_O = 1.4\text{ V to } 2.6\text{ V}$, $R_L = 50\text{ k}\Omega^\ddagger$, $C_L = 100\text{ pF}^\ddagger$	25°C	0.35	0.55		0.35	0.55	$V/\mu\text{s}$	
		Full range	0.25			0.25			
V_n Equivalent input noise voltage	$f = 10\text{ Hz}$	25°C		40			40	$nV/\sqrt{\text{Hz}}$	
	$f = 1\text{ kHz}$	25°C		12			12		
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to } 1\text{ Hz}$	25°C		0.7			0.7	μV	
	$f = 0.1\text{ Hz to } 10\text{ Hz}$	25°C		1.3			1.3		
I_n Equivalent input noise current		25°C		0.6			0.6	$fA/\sqrt{\text{Hz}}$	
THD + N Total harmonic distortion plus noise	$V_O = 0.5\text{ V to } 2.5\text{ V}$, $f = 20\text{ kHz}$, $R_L = 50\text{ k}\Omega^\ddagger$	$A_V = 1$	25°C			0.017%	0.017%		
		$A_V = 10$	25°C			0.03%	0.03%		
Gain-bandwidth product	$f = 50\text{ kHz}$, $C_L = 100\text{ pF}^\ddagger$	$R_L = 50\text{ k}\Omega^\ddagger$, 25°C		0.71			0.71	MHz	
B_{OM} Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V}$, $R_L = 50\text{ k}\Omega^\ddagger$	$A_V = 1$, $C_L = 100\text{ pF}^\ddagger$, 25°C		185			185	kHz	
t_s Settling time	$A_V = -1$, Step = $0.5\text{ V to } 2.5\text{ V}$, $R_L = 50\text{ k}\Omega^\ddagger$, $C_L = 100\text{ pF}^\ddagger$	To 0.1%	25°C			6.4	6.4	μs	
		To 0.01%	25°C			14.1	14.1		
ϕ_m Phase margin at unity gain	$R_L = 50\text{ k}\Omega^\ddagger$, $C_L = 100\text{ pF}^\ddagger$	25°C		56°			56°		
		25°C		11			11		
Gain margin		25°C		11			11	dB	

† Full range is $-40^\circ\text{C to } 125^\circ\text{C}$.

‡ Referenced to 2.5 V

TLC226x, TLC226xA Advanced LinCMOS™ RAIL-TO-RAIL OPERATIONAL AMPLIFIERS

SLOS177D – FEBRUARY 1997 – REVISED MARCH 2001

TLC2264I electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLC2264I			TLC2264AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage		25°C	300	2500		300	950	μV	
		Full range			3000		1500		
αV_{IO} Temperature coefficient of input offset voltage		25°C to 125°C	2			2		$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)	$V_{IC} = 0, V_O = 0, R_S = 50\ \Omega$	25°C	0.003			0.003		$\mu\text{V}/\text{mo}$	
I_{IO} Input offset current		25°C	0.5			0.5		pA	
	85°C		150		150				
	Full range		800		800				
I_{IB} Input bias current		25°C	1			1		pA	
		85°C		150		150		pA	
		Full range		800		800		pA	
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega, V_{IO} \leq 5\ \text{mV}$	25°C	-5 to 4	-5.3 to 4.2		-5 to 4	-5.3 to 4.2	V	
		Full range	-5 to 3.5			-5 to 3.5			
V_{OM+} Maximum positive peak output voltage	$I_O = -20\ \mu\text{A}$	25°C	4.99			4.99		V	
	$I_O = -100\ \mu\text{A}$	25°C	4.85	4.94		4.85	4.94		
		Full range	4.82			4.82			
	$I_O = -400\ \mu\text{A}$	25°C	4.7	4.85		4.7	4.85		
Full range		4.5			4.5				
V_{OM-} Maximum negative peak output voltage	$V_{IC} = 0, I_O = 50\ \mu\text{A}$	25°C		-4.99			-4.99	V	
		25°C	-4.85	-4.91		-4.85	-4.91		
	$V_{IC} = 0, I_O = 500\ \mu\text{A}$	Full range	-4.85			-4.85			
		$V_{IC} = 0, I_O = 4\ \text{mA}$	25°C	-4	-4.3		-4		-4.3
Full range	-3.8				-3.8				
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 4\ \text{V}$	$R_L = 50\ \text{k}\Omega$	25°C	80	200		80	200	V/mV
			Full range	50			50		
		$R_L = 1\ \text{M}\Omega$	25°C		1000			1000	
$r_{i(d)}$ Differential input resistance		25°C		10^{12}			10^{12}	Ω	
$r_{i(c)}$ Common-mode input resistance		25°C		10^{12}			10^{12}	Ω	
$C_{i(c)}$ Common-mode input capacitance	$f = 10\ \text{kHz}, \text{N package}$	25°C		8			8	pF	
z_o Closed-loop output impedance	$f = 100\ \text{kHz}, A_V = 10$	25°C		220			220	Ω	
CMRR Common-mode rejection ratio	$V_{IC} = -5\ \text{V to } 2.7\ \text{V}, V_O = 0, R_S = 50\ \Omega$	25°C	75	88		75	88	dB	
		Full range	75			75			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm 2.2\ \text{V to } \pm 8\ \text{V}, V_{IC} = V_{DD}/2, \text{No load}$	25°C	80	95		80	95	dB	
		Full range	80			80			

† Full range is -40°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



TLC2264I operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$

PARAMETER	TEST CONDITIONS	T_A †	TLC2264I			TLC2264AI			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{DD} Supply current (four amplifiers)	$V_O = 0$, No load	25°C	0.85	1		0.85	1		
		Full range			1		1		
SR Slew rate at unity gain	$V_O = \pm 1.9\text{ V}$, $C_L = 100\text{ pF}$, $R_L = 50\text{ k}\Omega$	25°C	0.35	0.55		0.35	0.55	V/ μs	
		Full range	0.25			0.25			
V_n Equivalent input noise voltage	$f = 10\text{ Hz}$	25°C		43			43	nV/ $\sqrt{\text{Hz}}$	
	$f = 1\text{ kHz}$	25°C		12			12		
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$	25°C		0.8			0.8	μV	
	$f = 0.1\text{ Hz to }10\text{ Hz}$	25°C		1.3			1.3		
I_n Equivalent input noise current		25°C		0.6			0.6	fA/ $\sqrt{\text{Hz}}$	
THD + N Total harmonic distortion plus noise	$V_O = \pm 2.3\text{ V}$, $R_L = 50\text{ k}\Omega$, $f = 20\text{ kHz}$	$A_V = 1$	25°C			0.014%		0.014%	
		$A_V = 10$	25°C			0.024%		0.024%	
Gain-bandwidth product	$f = 10\text{ kHz}$, $C_L = 100\text{ pF}$, $R_L = 50\text{ k}\Omega$	25°C		0.73			0.73	MHz	
B_{OM} Maximum output-swing bandwidth	$V_{O(PP)} = 4.6\text{ V}$, $R_L = 50\text{ k}\Omega$, $A_V = 1$, $C_L = 100\text{ pF}$	25°C		70			70	kHz	
t_s Settling time	$A_V = -1$, Step = $-2.3\text{ V to }2.3\text{ V}$, $R_L = 50\text{ k}\Omega$, $C_L = 100\text{ pF}$	To 0.1%	25°C			7.1		7.1	
		To 0.01%	25°C			16.5		16.5	
ϕ_m Phase margin at unity gain	$R_L = 50\text{ k}\Omega$, $C_L = 100\text{ pF}$	25°C		57°			57°		
		Gain margin	25°C		11			11	dB

† Full range is -40°C to 125°C .

TLC226x, TLC226xA Advanced LinCMOS™ RAIL-TO-RAIL OPERATIONAL AMPLIFIERS

SLOS177D – FEBRUARY 1997 – REVISED MARCH 2001

TLC2262Q/M electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLC2262Q, TLC2262M			TLC2262AQ, TLC2262AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{DD\pm} = \pm 2.5\text{ V}$, $V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	25°C	300	2500		300	950	μV	
		Full range			3000		1500		
α_{VIO} Temperature coefficient of input offset voltage		Full range		5			5	$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)		25°C		0.003			0.003	$\mu\text{V}/\text{mo}$	
I_{IO} Input offset current		25°C		0.5			0.5	pA	
		125°C			800		800		
I_{IB} Input bias current	25°C		1			1	pA		
	125°C			800		800			
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$, $ V_{IO} \leq 5\text{ mV}$	25°C	0 to 4	-0.3 to 4.2		0 to 4	-0.3 to 4.2	V	
		Full range	0 to 3.5			0 to 3.5			
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C		4.99			4.99	V	
		25°C	4.85	4.94		4.85	4.94		
		Full range	4.82			4.82			
		25°C	4.7	4.85		4.7	4.85		
V_{OL} Low-level output voltage	$I_{OL} = -400\ \mu\text{A}$	25°C		0.01			0.01	V	
		25°C	0.09	0.15		0.09	0.15		
		Full range		0.15			0.15		
		25°C	0.8	1		0.7	1		
V_{OL} Low-level output voltage	$I_{OL} = 500\ \mu\text{A}$	25°C		0.01			0.01	V	
		25°C	0.09	0.15		0.09	0.15		
		Full range		0.15			0.15		
		25°C	0.8	1		0.7	1		
V_{OL} Low-level output voltage	$I_{OL} = 4\text{ mA}$	25°C		0.01			0.01	V	
		25°C	0.09	0.15		0.09	0.15		
		Full range		0.15			0.15		
		25°C	0.8	1		0.7	1		
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$, $V_O = 1\text{ V to }4\text{ V}$	$R_L = 50\text{ k}\Omega$ ‡	25°C	80	100		80	170	V/mV
			Full range	50			50		
		$R_L = 1\text{ M}\Omega$ ‡	25°C		550			550	
$r_{i(d)}$ Differential input resistance		25°C		10^{12}			10^{12}	Ω	
$r_{i(c)}$ Common-mode input resistance		25°C		10^{12}			10^{12}	Ω	
$C_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz}$, P package	25°C		8			8	pF	
Z_o Closed-loop output impedance	$f = 100\text{ kHz}$, $A_V = 10$	25°C		240			240	Ω	
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.7\text{ V}$, $V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$	25°C	70	83		70	83	dB	
		Full range	70			70			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }16\text{ V}$, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	95	dB	
		Full range	80			80			
I_{DD} Supply current	$V_O = 2.5\text{ V}$, No load	25°C		400	500		400	500	μA
		Full range			500			500	

† Full range is -40°C to 125°C for Q suffix, -55°C to 125°C for M suffix.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



TLC2262Q/M operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	T_A †	TLC2262Q, TLC2262M			TLC2262AQ, TLC2262AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain $V_O = 0.5\text{ V to }3.5\text{ V}, R_L = 50\text{ k}\Omega\ddagger, C_L = 100\text{ pF}\ddagger$	25°C	0.35	0.55		0.35	0.55		V/ μs
		Full range	0.25			0.25			
V_n	Equivalent input noise voltage $f = 10\text{ Hz}$ $f = 1\text{ kHz}$	25°C	40			40			nV/ $\sqrt{\text{Hz}}$
		25°C	12			12			
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage $f = 0.1\text{ Hz to }1\text{ Hz}$ $f = 0.1\text{ Hz to }10\text{ Hz}$	25°C	0.7			0.7			μV
		25°C	1.3			1.3			
I_n	Equivalent input noise current	25°C	0.6			0.6			fA/ $\sqrt{\text{Hz}}$
THD + N	Total harmonic distortion plus noise $V_O = 0.5\text{ V to }2.5\text{ V}, f = 20\text{ kHz}, R_L = 50\text{ k}\Omega\ddagger$	25°C	$A_V = 1$			0.017%			
			$A_V = 10$			0.03%			
	Gain-bandwidth product $f = 50\text{ kHz}, C_L = 100\text{ pF}\ddagger$	25°C	0.82			0.82			MHz
B_{OM}	Maximum output-swing bandwidth $V_{O(PP)} = 2\text{ V}, R_L = 50\text{ k}\Omega\ddagger, C_L = 100\text{ pF}\ddagger$	25°C	185			185			kHz
t_s	Settling time $A_V = -1, \text{ Step} = 0.5\text{ V to }2.5\text{ V}, R_L = 50\text{ k}\Omega\ddagger, C_L = 100\text{ pF}\ddagger$	25°C	To 0.1%			6.4			μs
			To 0.01%			14.1			
ϕ_m	Phase margin at unity gain $R_L = 50\text{ k}\Omega\ddagger, C_L = 100\text{ pF}\ddagger$	25°C	56°			56°			
		25°C	11			11			

† Full range is -40°C to 125°C for Q suffix, -55°C to 125°C for M suffix.

‡ Referenced to 2.5 V

TLC226x, TLC226xA Advanced LinCMOS™ RAIL-TO-RAIL OPERATIONAL AMPLIFIERS

SLOS177D – FEBRUARY 1997 – REVISED MARCH 2001

TLC2262Q/M electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLC2262Q, TLC2262M			TLC2262AQ, TLC2262AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0, \quad V_O = 0,$ $R_S = 50\ \Omega$	25°C	300	2500		300	950	μV	
		Full range		3000		1500			
α_{VIO} Temperature coefficient of input offset voltage		Full range	5			5		$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)		25°C	0.003			0.003		$\mu\text{V}/\text{mo}$	
I_{IO} Input offset current		25°C	0.5			0.5		pA	
		125°C		800		800			
I_{IB} Input bias current	25°C	1			1		pA		
	125°C		800		800				
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega, \quad V_{IO} \leq 5\ \text{mV}$	25°C	-5 to 4	-5.3 to 4		-5 to 4	-5.3 to 4.2	V	
		Full range	-5 to 3.5			-5 to 3.5			
V_{OM+} Maximum positive peak output voltage	$I_O = -20\ \mu\text{A}$	25°C	4.99			4.99		V	
		25°C	4.85	4.94		4.85	4.94		
		Full range	4.82			4.82			
		25°C	4.7	4.85		4.7	4.85		
V_{OM-} Maximum negative peak output voltage	$I_O = -400\ \mu\text{A}$	25°C	-4.99			-4.99		V	
		25°C	-4.85	-4.91		-4.85	-4.91		
		Full range	-4.85			-4.85			
		25°C	-4	-4.3		-4	-4.3		
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 4\ \text{V}$	$R_L = 50\ \text{k}\Omega$	25°C	80	200		80	200	V/mV
			Full range	50			50		
		$R_L = 1\ \text{M}\Omega$	25°C	1000			1000		
			Full range						
$r_{i(d)}$ Differential input resistance		25°C	10 ¹²			10 ¹²	Ω		
$r_{i(c)}$ Common-mode input resistance		25°C	10 ¹²			10 ¹²	Ω		
$C_{i(c)}$ Common-mode input capacitance	$f = 10\ \text{kHz}, \quad \text{P package}$	25°C	8			8	pF		
z_o Closed-loop output impedance	$f = 100\ \text{kHz}, \quad A_V = 10$	25°C	220			220	Ω		
CMRR Common-mode rejection ratio	$V_{IC} = -5\ \text{V to } 2.7\ \text{V},$ $V_O = 0, \quad R_S = 50\ \Omega$	25°C	75	88		75	88	dB	
		Full range	75			75			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD} = 4.4\ \text{V to } 16\ \text{V},$ $V_{IC} = V_{DD}/2, \quad \text{No load}$	25°C	80	95		80	95	dB	
		Full range	80			80			
I_{DD} Supply current	$V_O = 0, \quad \text{No load}$	25°C	425	500		425	500	μA	
		Full range		500			500		

† Full range is -40°C to 125°C for Q suffix, -55°C to 125°C for M suffix.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



TLC2262Q/M operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$

PARAMETER	TEST CONDITIONS	T_A †	TLC2262Q, TLC2262M			TLC2262AQ, TLC2262AM			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX		
SR	Slew rate at unity gain $V_O = \pm 2\text{ V}$, $C_L = 100\text{ pF}$	$R_L = 50\text{ k}\Omega$	25°C	0.35	0.55		0.35	0.55	V/ μs	
			Full range	0.25			0.25			
V_n	Equivalent input noise voltage		25°C	43			43			nV/ $\sqrt{\text{Hz}}$
			25°C	12			12			
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		25°C	0.8			0.8			μV
			25°C	1.3			1.3			
I_n	Equivalent input noise current		25°C	0.6			0.6			fA/ $\sqrt{\text{Hz}}$
THD + N	Total harmonic distortion plus noise $V_O = \pm 2.3\text{ V}$, $R_L = 50\text{ k}\Omega$, $f = 20\text{ kHz}$	$A_V = 1$	25°C	0.014%			0.014%			
			$A_V = 10$	0.024%			0.024%			
	Gain-bandwidth product $f = 10\text{ kHz}$, $C_L = 100\text{ pF}$	$R_L = 50\text{ k}\Omega$	25°C	0.73			0.73			MHz
B_{OM}	Maximum output-swing bandwidth $V_{O(PP)} = 4.6\text{ V}$, $R_L = 50\text{ k}\Omega$	$A_V = 1$, $C_L = 100\text{ pF}$	25°C	85			85			kHz
t_s	Settling time $A_V = -1$, Step = -2.3 V to 2.3 V , $R_L = 50\text{ k}\Omega$, $C_L = 100\text{ pF}$	To 0.1%	25°C	7.1			7.1			μs
		To 0.01%		16.5			16.5			
ϕ_m	Phase margin at unity gain $R_L = 50\text{ k}\Omega$	$C_L = 100\text{ pF}$	25°C	57°			57°			
	Gain margin		25°C	11			11			

† Full range is -40°C to 125°C for Q suffix, -55°C to 125°C for M suffix.

TLC226x, TLC226xA Advanced LinCMOS™ RAIL-TO-RAIL OPERATIONAL AMPLIFIERS

SLOS177D – FEBRUARY 1997 – REVISED MARCH 2001

TLC2264Q/M electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLC2264Q, TLC2264M			TLC2264AQ, TLC2264AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage		25°C	300	2500		300	950	μV	
		Full range			3000		1500		
α_{VIO} Temperature coefficient of input offset voltage		Full range	2			2			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)	$V_{DD\pm} = \pm 2.5\text{ V}$, $V_O = 0$, $V_{IC} = 0$, $R_S = 50\ \Omega$	25°C	0.003			0.003			$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C	0.5			0.5			pA
		125°C	800			800			
I_{IB} Input bias current		25°C	1			1			pA
	125°C	800			800				
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$, $ V_{IO} \leq 5\text{ mV}$	25°C	0 to 4	-0.3 to 4.2		0 to 4	-0.3 to 4.2	V	
		Full range	0 to 3.5		0 to 3.5				
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$ $I_{OH} = -100\ \mu\text{A}$ $I_{OH} = -400\ \mu\text{A}$	25°C	4.99			4.99			V
		25°C	4.85	4.94		4.85	4.94		
		Full range	4.82			4.82			
		25°C	4.7	4.85		4.7	4.85		
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$ $I_{OL} = 500\ \mu\text{A}$ $I_{OL} = 4\text{ mA}$	25°C	0.01			0.01			V
		25°C	0.09	0.15		0.09	0.15		
		Full range	0.15			0.15			
		25°C	0.8	1		0.7	1		
AVD Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$, $V_O = 1\text{ V to } 4\text{ V}$	$R_L = 50\ \text{k}\Omega^\ddagger$	25°C	80	100		80	170	V/mV
			Full range	50			50		
		$R_L = 1\ \text{M}\Omega^\ddagger$	25°C	550			550		
$r_{i(d)}$ Differential input resistance		25°C	10^{12}			10^{12}			Ω
$r_{i(c)}$ Common-mode input resistance		25°C	10^{12}			10^{12}			Ω
$C_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz}$, N package	25°C	8			8			pF
z_o Closed-loop output impedance	$f = 100\text{ kHz}$, $A_V = 10$	25°C	240			240			Ω
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to } 2.7\text{ V}$, $V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$	25°C	70	83		70	83	dB	
		Full range	70			70			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to } 16\text{ V}$,	25°C	80	95		80	95	dB	
I_{DD} Supply current (four amplifiers)	$V_O = 2.5\text{ V}$, No load	25°C	0.8	1		0.8	1	mA	
		Full range	1			1			

† Full range is -40°C to 125°C for Q suffix, -55°C to 125°C for M suffix.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



TLC2264Q/M operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	T_A †	TLC2264Q, TLC2264M			TLC2264AQ, TLC2264AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain $V_O = 0.5\text{ V to }3.5\text{ V}, R_L = 50\text{ k}\Omega^\ddagger, C_L = 100\text{ pF}^\ddagger$	25°C	0.35	0.55		0.35	0.55		V/ μs
		Full range	0.25			0.25			
V_n	Equivalent input noise voltage	f = 10 Hz	40			40			nV/ $\sqrt{\text{Hz}}$
		f = 1 kHz	12			12			
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz	0.7			0.7			μV
		f = 0.1 Hz to 10 Hz	1.3			1.3			
I_n	Equivalent input noise current	25°C	0.6			0.6			fA/ $\sqrt{\text{Hz}}$
THD + N	Total harmonic distortion plus noise $V_O = 0.5\text{ V to }2.5\text{ V}, f = 20\text{ kHz}, R_L = 50\text{ k}\Omega^\ddagger$	$A_V = 1$	0.017%			0.017%			
		$A_V = 10$	0.03%			0.03%			
	Gain-bandwidth product f = 50 kHz, $C_L = 100\text{ pF}^\ddagger$	$R_L = 50\text{ k}\Omega^\ddagger, 25^\circ\text{C}$	0.71			0.71			MHz
B_{OM}	Maximum output-swing bandwidth $V_{O(PP)} = 2\text{ V}, R_L = 50\text{ k}\Omega^\ddagger, A_V = 1, C_L = 100\text{ pF}^\ddagger$	25°C	185			185			kHz
t_s	Settling time $A_V = -1, \text{ Step} = 0.5\text{ V to }2.5\text{ V}, R_L = 50\text{ k}\Omega^\ddagger, C_L = 100\text{ pF}^\ddagger$	To 0.1%	6.4			6.4			μs
		To 0.01%	14.1			14.1			
ϕ_m	Phase margin at unity gain $R_L = 50\text{ k}\Omega^\ddagger, C_L = 100\text{ pF}^\ddagger$	25°C	56°			56°			
		25°C	11			11			

† Full range is -40°C to 125°C for Q suffix, -55°C to 125°C for M suffix.

‡ Referenced to 2.5 V

TLC226x, TLC226xA Advanced LinCMOS™ RAIL-TO-RAIL OPERATIONAL AMPLIFIERS

SLOS177D – FEBRUARY 1997 – REVISED MARCH 2001

TLC2264Q/M electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLC2264Q, TLC2264M			TLC2264AQ, TLC2264AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0,$ $R_S = 50\ \Omega$ $V_O = 0,$	25°C	300	2500		300	950	μV	
		Full range			3000		1500		
α_{VIO} Temperature coefficient of input offset voltage		Full range		2			2	$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 4)		25°C		0.003			0.003	$\mu\text{V}/\text{mo}$	
I_{IO} Input offset current		25°C		0.5			0.5	pA	
		125°C			800		800		
I_{IB} Input bias current	25°C		1			1	pA		
	125°C			800		800			
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega,$ $ V_{IO} \leq 5\ \text{mV}$	25°C	-5 to 4	-5.3 to 4.2		-5 to 4	-5.3 to 4.2	V	
		Full range	-5 to 3.5			-5 to 3.5			
V_{OM+} Maximum positive peak output voltage	$I_O = -20\ \mu\text{A}$	25°C		4.99			4.99	V	
	$I_O = -100\ \mu\text{A}$	25°C	4.85	4.94		4.85	4.94		
		Full range	4.82			4.82			
	$I_O = -400\ \mu\text{A}$	25°C	4.7	4.85		4.7	4.85		
Full range		4.5			4.5				
V_{OM-} Maximum negative peak output voltage	$V_{IC} = 0,$ $I_O = 50\ \mu\text{A}$	25°C		-4.99			-4.99	V	
	$V_{IC} = 0,$ $I_O = 500\ \mu\text{A}$	25°C	-4.85	-4.91		-4.85	-4.91		
		Full range	-4.85			-4.85			
	$V_{IC} = 0,$ $I_O = 4\ \text{mA}$	25°C	-4	-4.3		-4	-4.3		
Full range		-3.8			-3.8				
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 4\ \text{V}$	$R_L = 50\ \text{k}\Omega$	25°C	80	200		80	200	V/mV
			Full range	50			50		
		$R_L = 1\ \text{M}\Omega$	25°C		1000			1000	
$r_{i(d)}$ Differential input resistance		25°C		10^{12}			10^{12}	Ω	
$r_{i(c)}$ Common-mode input resistance		25°C		10^{12}			10^{12}	Ω	
$C_{i(c)}$ Common-mode input capacitance	$f = 10\ \text{kHz},$ N package	25°C		8			8	pF	
z_o Closed-loop output impedance	$f = 100\ \text{kHz},$ $A_V = 10$	25°C		220			220	Ω	
CMRR Common-mode rejection ratio	$V_{IC} = -5\ \text{V to } 2.7\ \text{V},$ $V_O = 0,$ $R_S = 50\ \Omega$	25°C	75	88		75	88	dB	
		Full range	75			75			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm 2.2\ \text{V to } \pm 8\ \text{V},$ $V_{IC} = V_{DD}/2,$ No load	25°C	80	95		80	95	dB	
		Full range	80			80			
I_{DD} Supply current (four amplifiers)	$V_O = 0,$ No load	25°C		0.85	1		0.85	1	mA
		Full range			1			1	

† Full range is -40°C to 125°C for Q suffix, -55°C to 125°C for M suffix.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



TLC2264Q/M operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$

PARAMETER	TEST CONDITIONS		T_A †	TLC2264Q, TLC2264M			TLC2264AQ, TLC2264AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm 2\text{ V}$, $C_L = 100\text{ pF}$	$R_L = 50\text{ k}\Omega$,	25°C	0.35	0.55		0.35	0.55	V/ μ s
				Full range	0.25			0.25		
V_n	Equivalent input noise voltage			25°C	43		43		nV/ $\sqrt{\text{Hz}}$	
				25°C	12		12			
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage			25°C	0.8		0.8		μ V	
				25°C	1.3		1.3			
I_n	Equivalent input noise current			25°C	0.6		0.6		fA/ $\sqrt{\text{Hz}}$	
THD + N	Total harmonic distortion plus noise	$V_O = \pm 2.3\text{ V}$, $R_L = 50\text{ k}\Omega$, $f = 20\text{ kHz}$		25°C	$A_V = 1$		0.014%			
					$A_V = 10$		0.024%			
	Gain-bandwidth product	$f = 10\text{ kHz}$, $C_L = 100\text{ pF}$	$R_L = 50\text{ k}\Omega$,	25°C	0.73		0.73		MHz	
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6\text{ V}$, $R_L = 50\text{ k}\Omega$,	$A_V = 1$, $C_L = 100\text{ pF}$	25°C	70		70		kHz	
t_s	Settling time	$A_V = -1$, Step = -2.3 V to 2.3 V , $R_L = 50\text{ k}\Omega$, $C_L = 100\text{ pF}$		25°C	To 0.1%		7.1		μ s	
					To 0.01%		16.5			
ϕ_m	Phase margin at unity gain	$R_L = 50\text{ k}\Omega$,	$C_L = 100\text{ pF}$	25°C	57°		57°			
	Gain margin			25°C	11		11			dB

† Full range is -40°C to 125°C for Q suffix, -55°C to 125°C for M suffix.

TLC226x, TLC226xA
Advanced LinCMOS™ RAIL-TO-RAIL
OPERATIONAL AMPLIFIERS

SLOS177D – FEBRUARY 1997 – REVISED MARCH 2001

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution vs Common-mode input voltage	2 – 5 6, 7
α_{VIO}	Input offset voltage temperature coefficient	Distribution	8 – 11
I_{IB}/I_{IO}	Input bias and input offset currents	vs Free-air temperature	12
V_I	Input voltage range	vs Supply voltage vs Free-air temperature	13 14
V_{OH}	High-level output voltage	vs High-level output current	15
V_{OL}	Low-level output voltage	vs Low-level output current	16, 17
V_{OM+}	Maximum positive output voltage	vs Output current	18
V_{OM-}	Maximum negative output voltage	vs Output current	19
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	20
I_{OS}	Short-circuit output current	vs Supply voltage vs Free-air temperature	21 22
V_O	Output voltage	vs Differential input voltage	23, 24
	Differential gain	vs Load resistance	25
A_{VD}	Large-signal differential voltage amplification	vs Frequency vs Free-air temperature	26, 27 28, 29
z_o	Output impedance	vs Frequency	30, 31
CMRR	Common-mode rejection ratio	vs Frequency vs Free-air temperature	32 33
k_{SVR}	Supply-voltage rejection ratio	vs Frequency vs Free-air temperature	34, 35 36
I_{DD}	Supply current	vs Supply voltage vs Free-air temperature	37, 38 39, 40
SR	Slew rate	vs Load capacitance vs Free-air temperature	41 42
V_O	Inverting large-signal pulse response		43, 44
	Voltage-follower large-signal pulse response		45, 46
	Inverting small-signal pulse response		47, 48
	Voltage-follower small-signal pulse response		49, 50
V_n	Equivalent input noise voltage	vs Frequency	51, 52
	Noise voltage (referred to input)	Over a 10-second period	53
	Integrated noise voltage	vs Frequency	54
THD + N	Total harmonic distortion plus noise	vs Frequency	55
	Gain-bandwidth product	vs Supply voltage vs Free-air temperature	56 57
ϕ_m	Phase margin	vs Frequency vs Load capacitance	26, 27 58
	Gain margin	vs Load capacitance	59
B_1	Unity-gain bandwidth	vs Load capacitance	60
	Overestimation of phase margin	vs Load capacitance	61



TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC2262
 INPUT OFFSET VOLTAGE

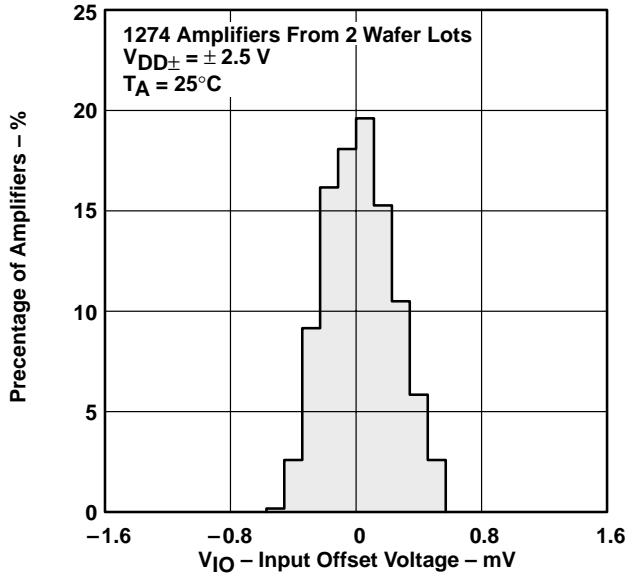


Figure 2

DISTRIBUTION OF TLC2262
 INPUT OFFSET VOLTAGE

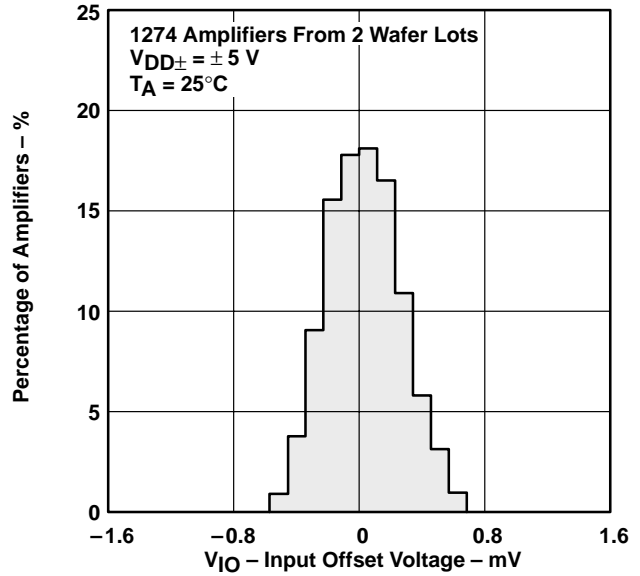


Figure 3

DISTRIBUTION OF TLC2264
 INPUT OFFSET VOLTAGE

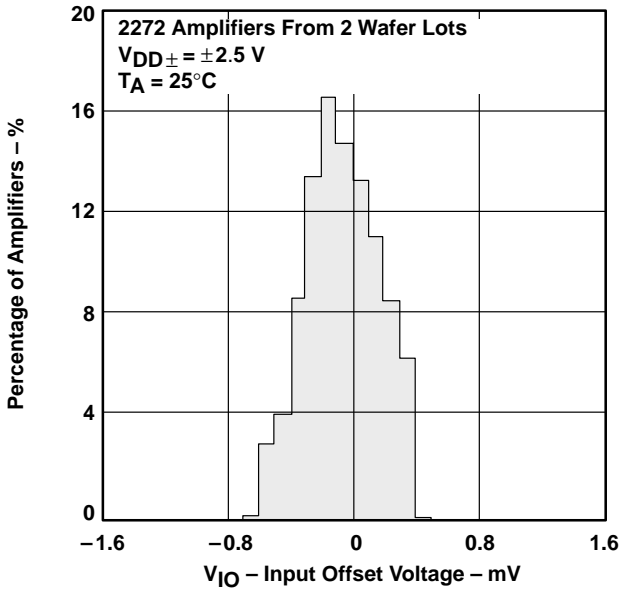


Figure 4

DISTRIBUTION OF TLC2264
 INPUT OFFSET VOLTAGE

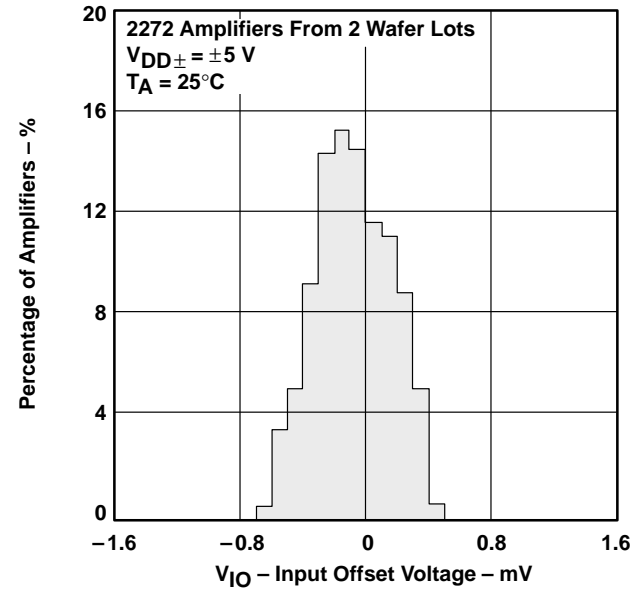


Figure 5

TYPICAL CHARACTERISTICS

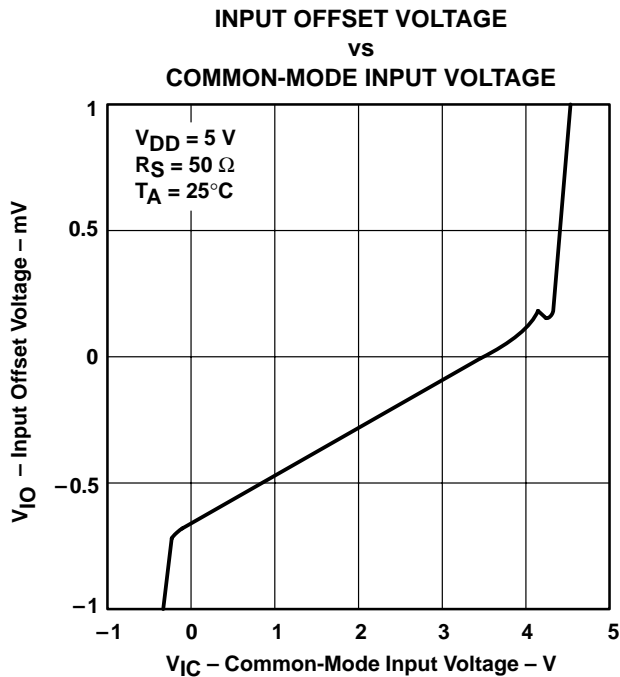


Figure 6

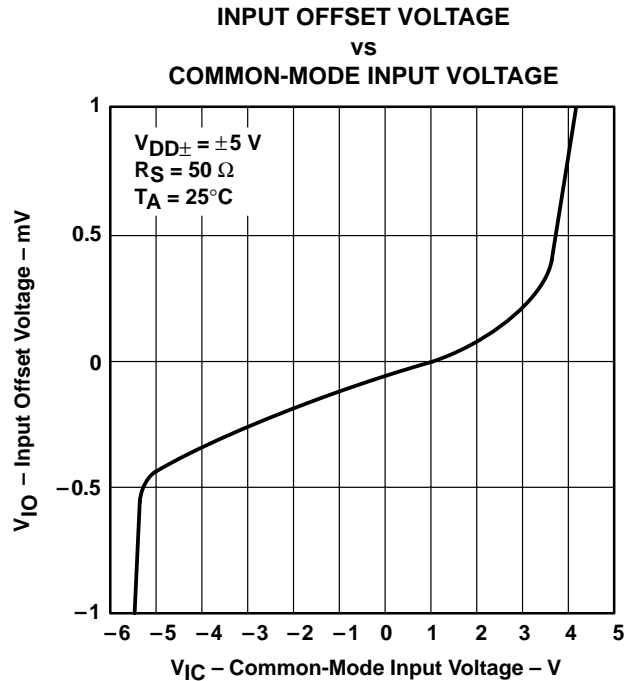


Figure 7

† For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.

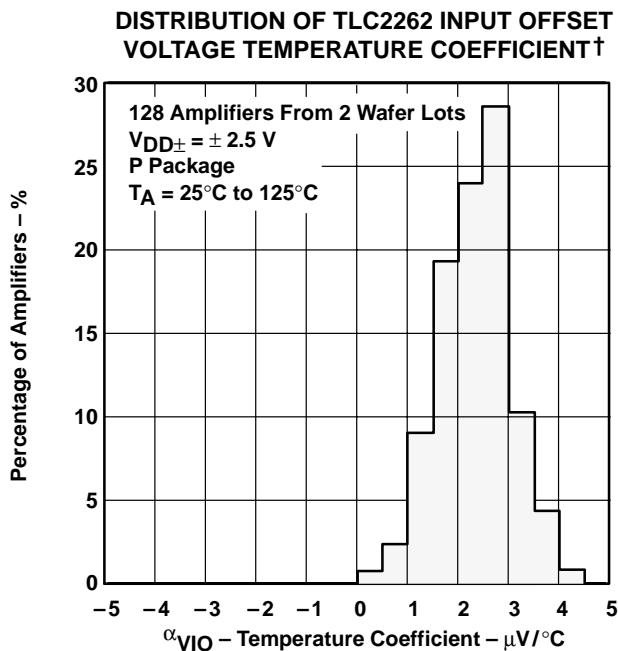


Figure 8

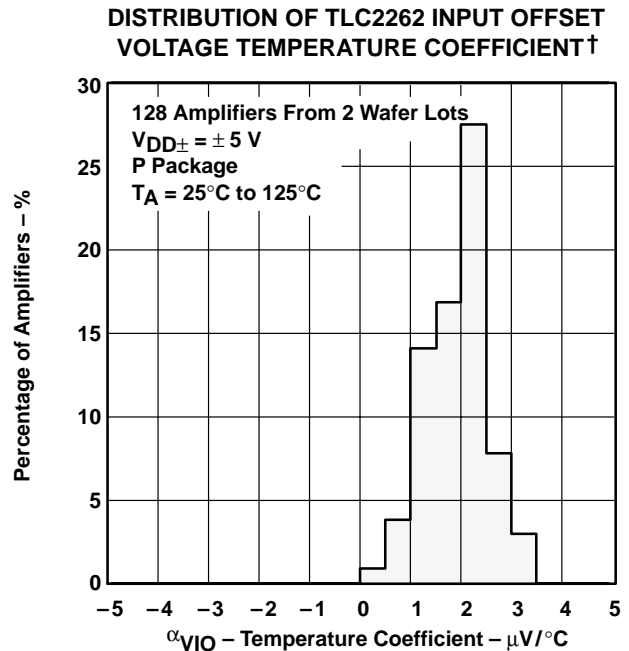


Figure 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

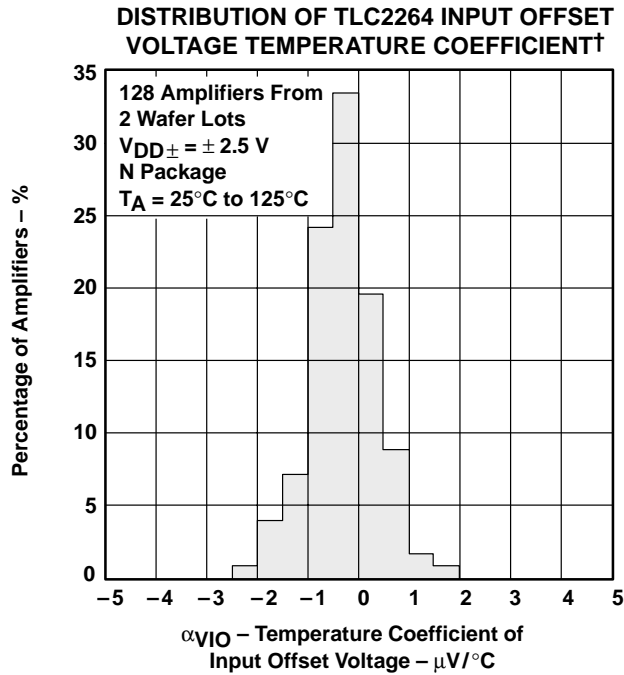


Figure 10

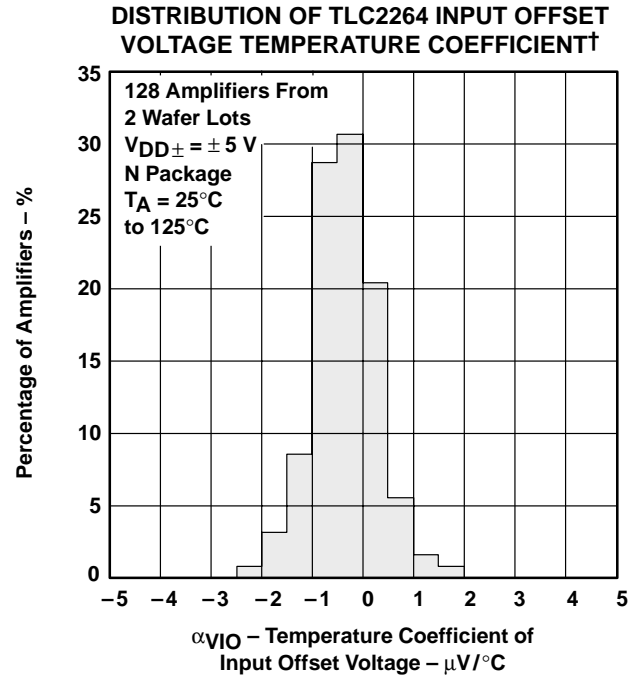


Figure 11

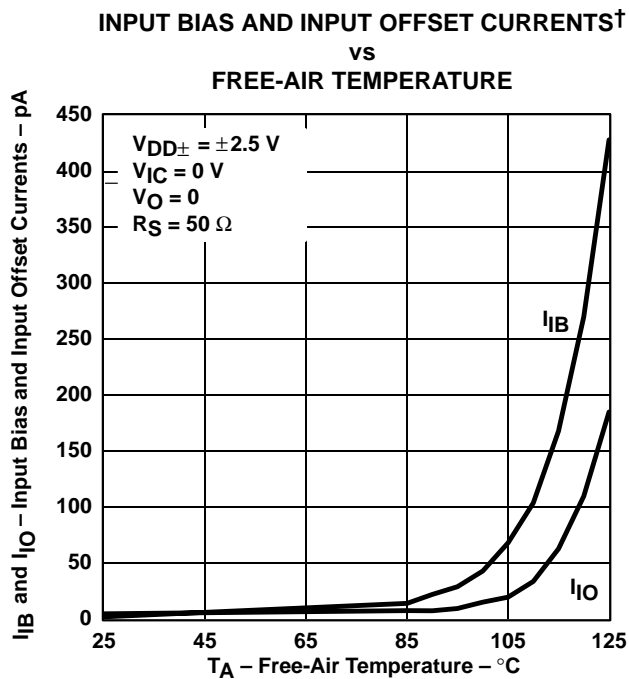


Figure 12

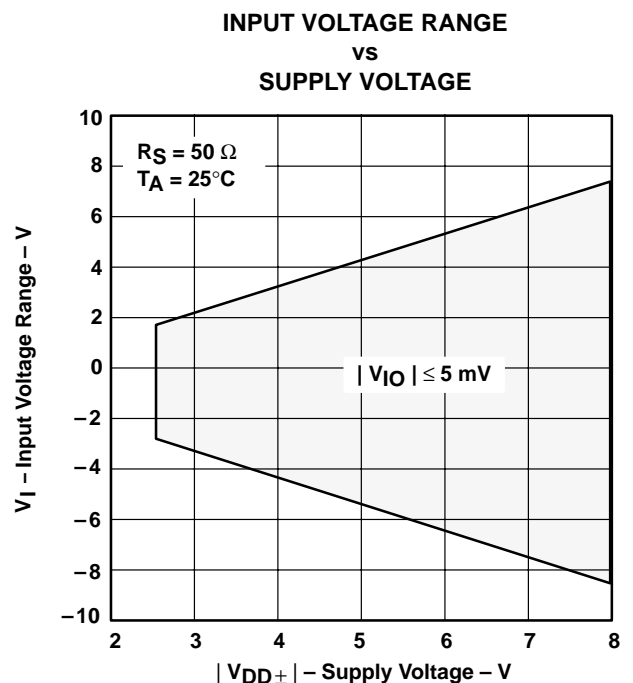


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

INPUT VOLTAGE RANGE†‡
 vs
 FREE-AIR TEMPERATURE

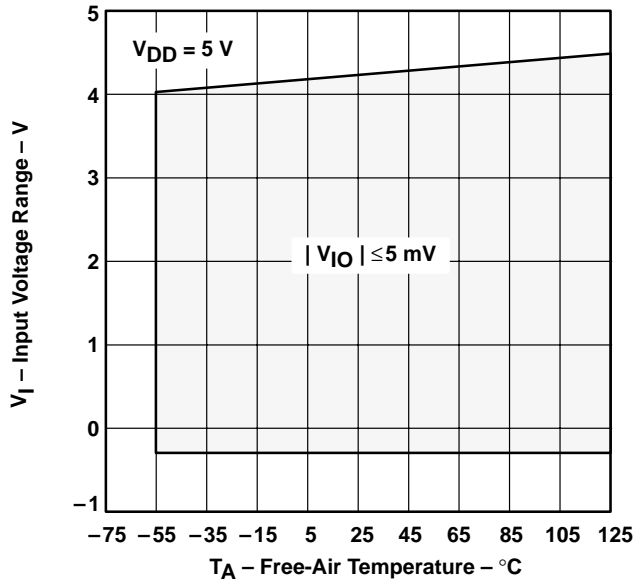


Figure 14

HIGH-LEVEL OUTPUT VOLTAGE†‡
 vs
 HIGH-LEVEL OUTPUT CURRENT

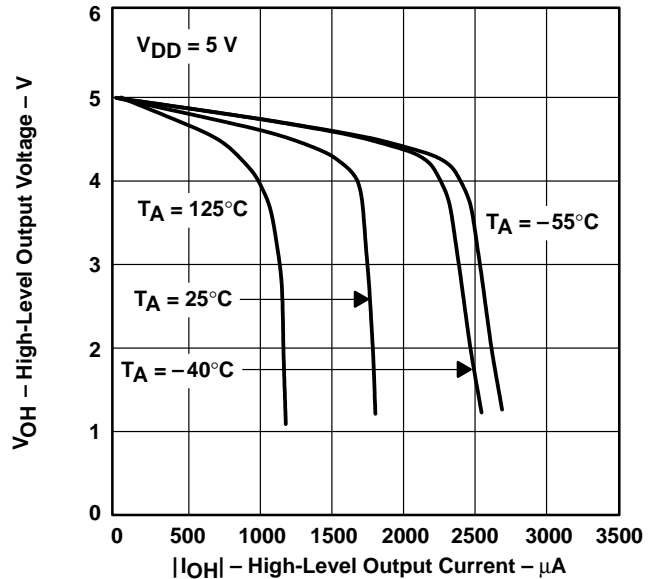


Figure 15

LOW-LEVEL OUTPUT VOLTAGE‡
 vs
 LOW-LEVEL OUTPUT CURRENT

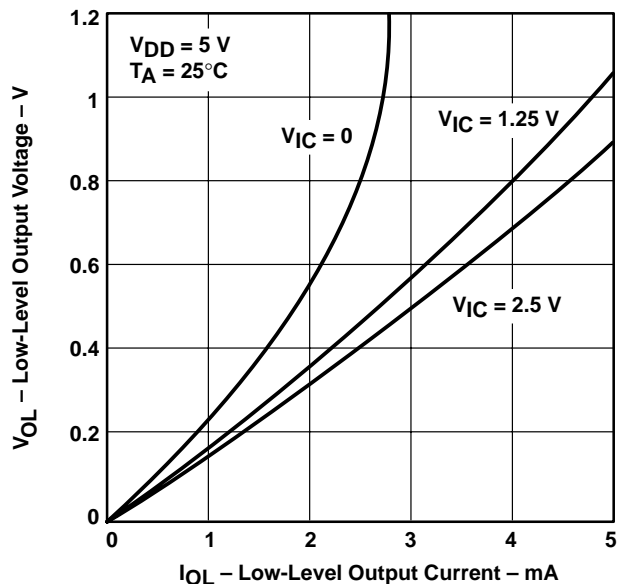


Figure 16

LOW-LEVEL OUTPUT VOLTAGE†‡
 vs
 LOW-LEVEL OUTPUT CURRENT

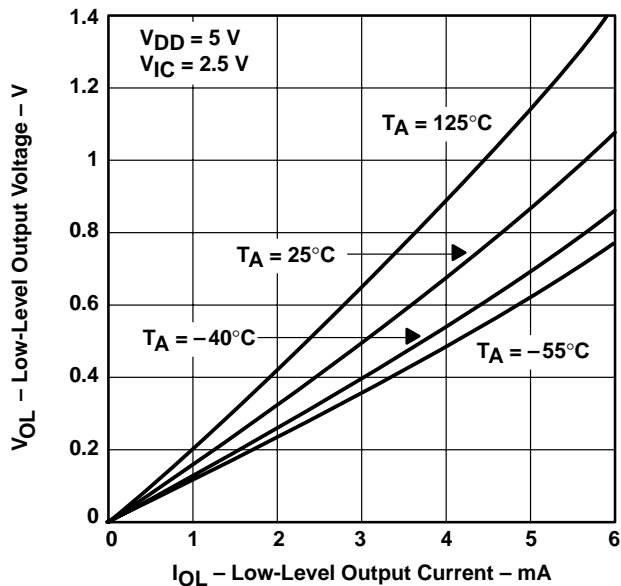


Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

MAXIMUM POSITIVE OUTPUT VOLTAGE†
 vs
 OUTPUT CURRENT

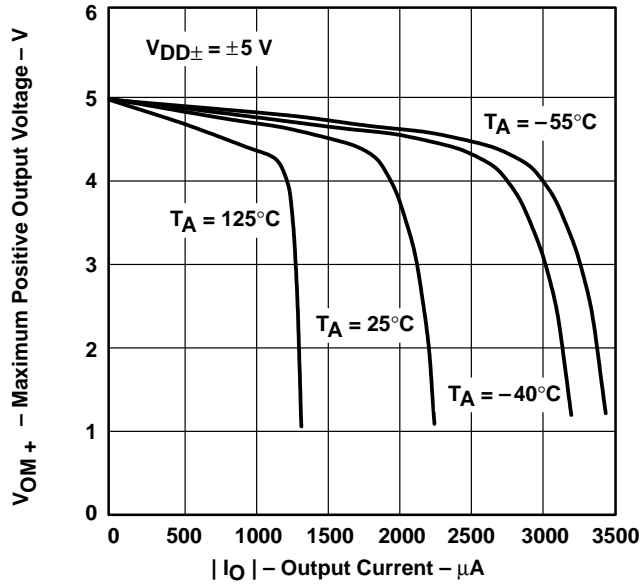


Figure 18

MAXIMUM NEGATIVE OUTPUT VOLTAGE†
 vs
 OUTPUT CURRENT

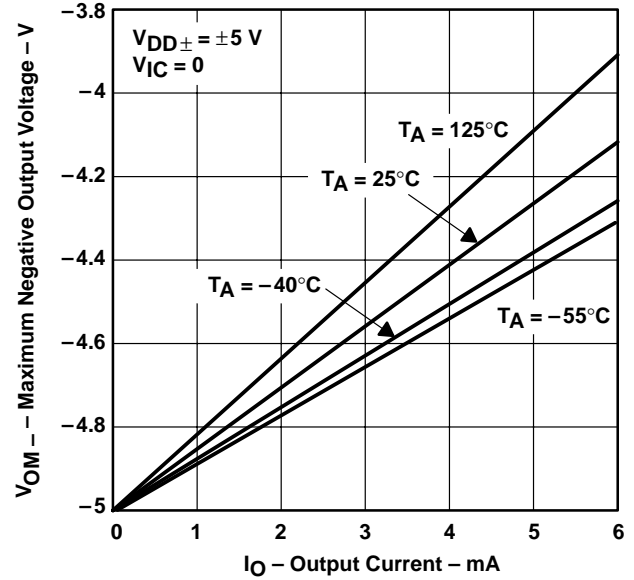


Figure 19

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE‡
 vs
 FREQUENCY

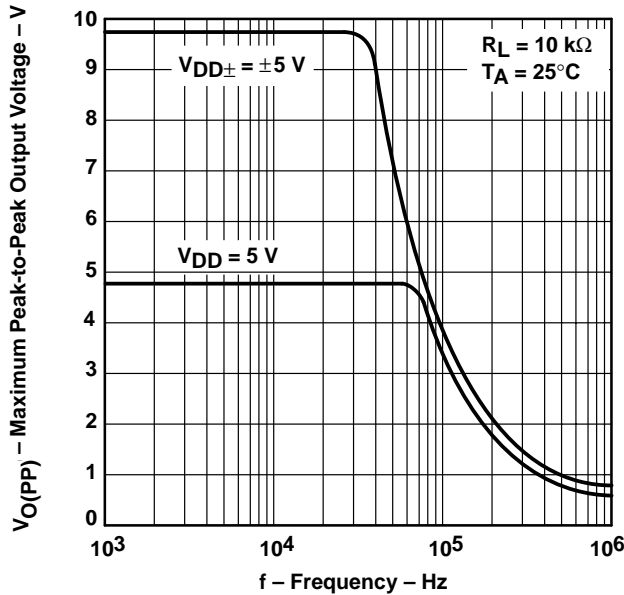


Figure 20

SHORT-CIRCUIT OUTPUT CURRENT
 vs
 SUPPLY VOLTAGE

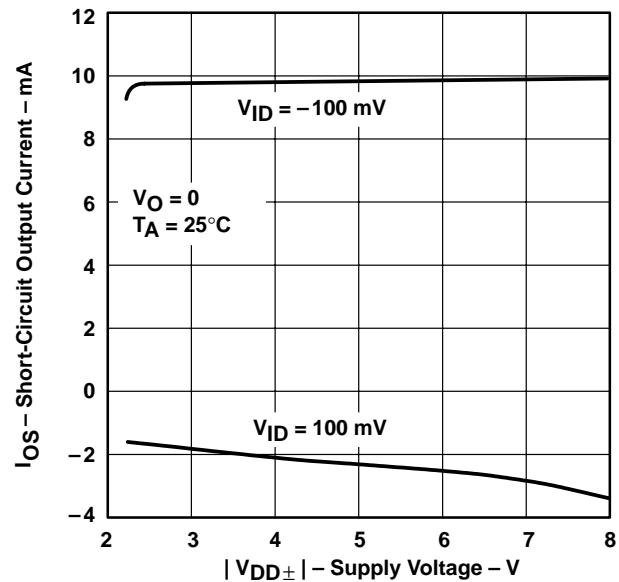


Figure 21

‡ For curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V.

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TLC226x, TLC226xA
Advanced LinCMOS™ RAIL-TO-RAIL
OPERATIONAL AMPLIFIERS

SLOS177D – FEBRUARY 1997 – REVISED MARCH 2001

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT †
vs
FREE-AIR TEMPERATURE

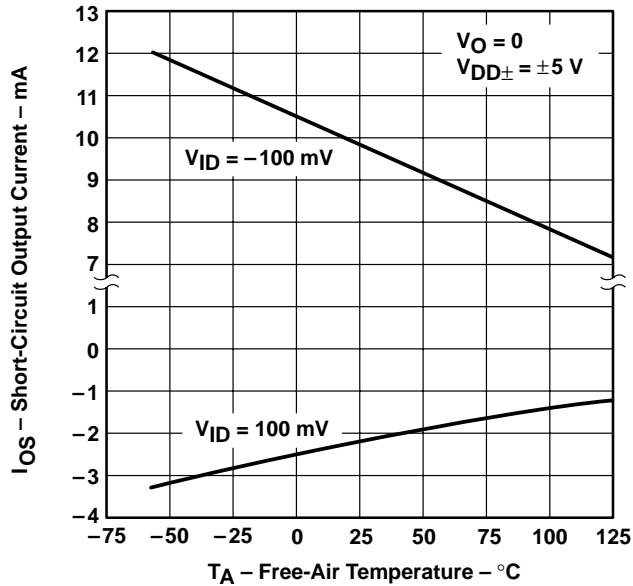


Figure 22

OUTPUT VOLTAGE ‡
vs
DIFFERENTIAL INPUT VOLTAGE

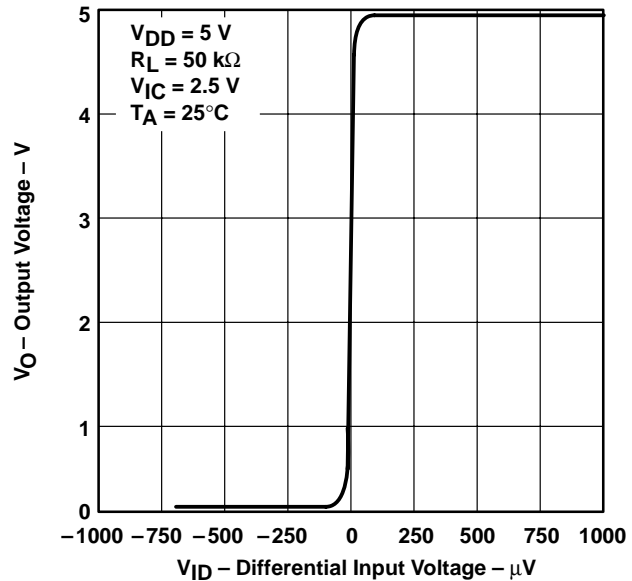


Figure 23

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

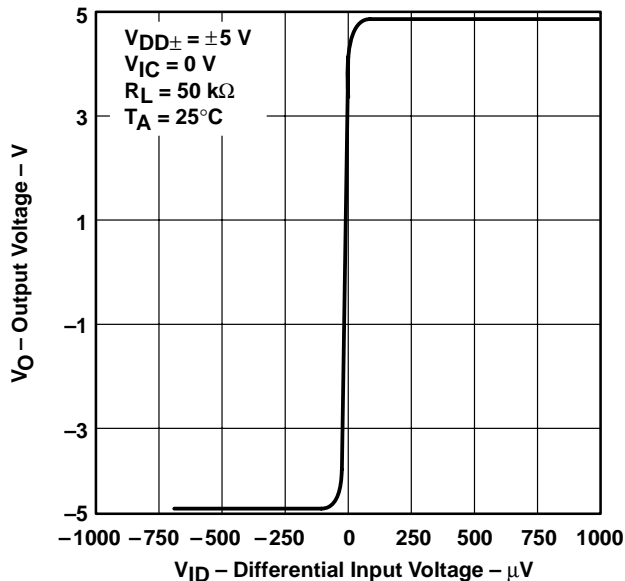


Figure 24

DIFFERENTIAL GAIN ‡
vs
LOAD RESISTANCE

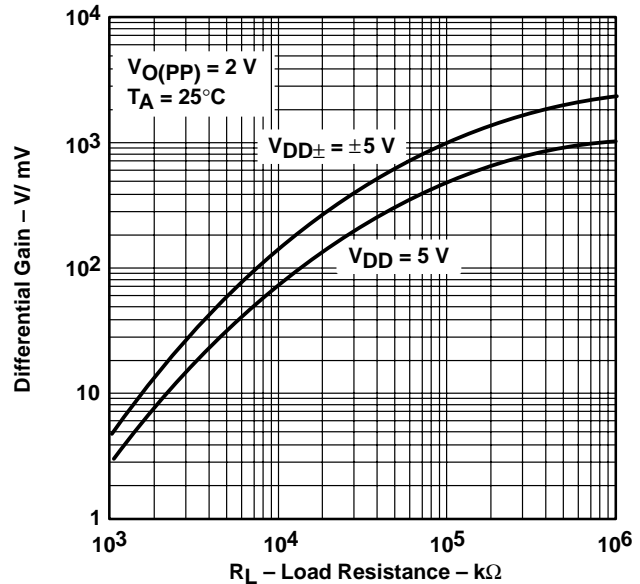


Figure 25

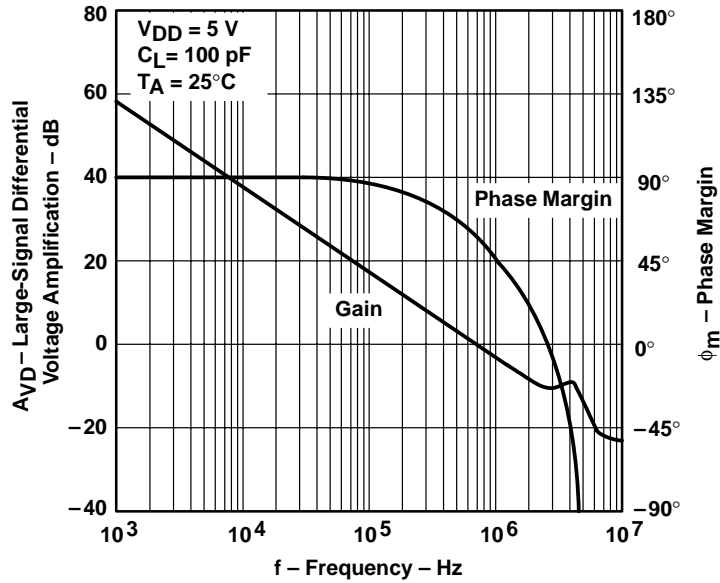
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.



TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE†
 AMPLIFICATION AND PHASE MARGIN
 VS
 FREQUENCY



† For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.

Figure 26

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
 AMPLIFICATION AND PHASE MARGIN
 VS
 FREQUENCY

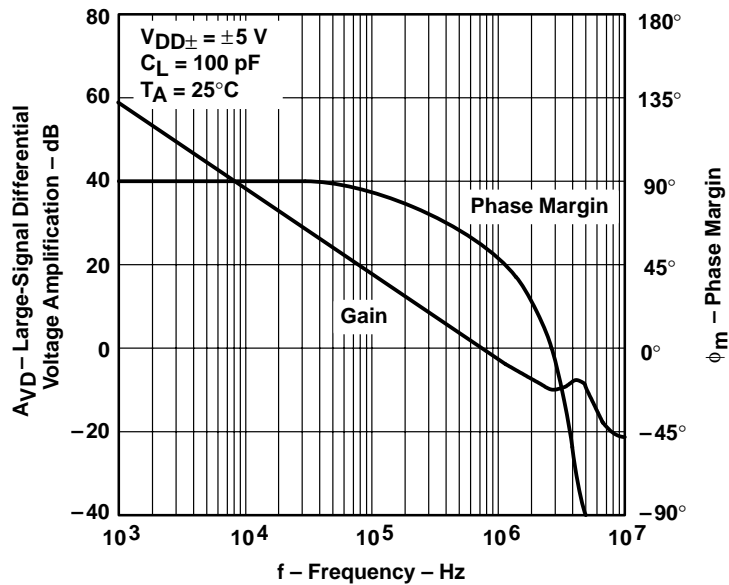


Figure 27

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION†‡
vs
FREE-AIR TEMPERATURE

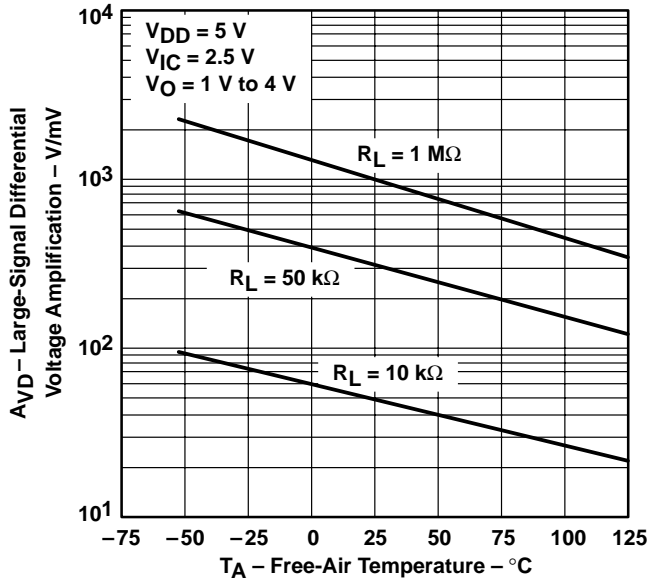


Figure 28

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION†
vs
FREE-AIR TEMPERATURE

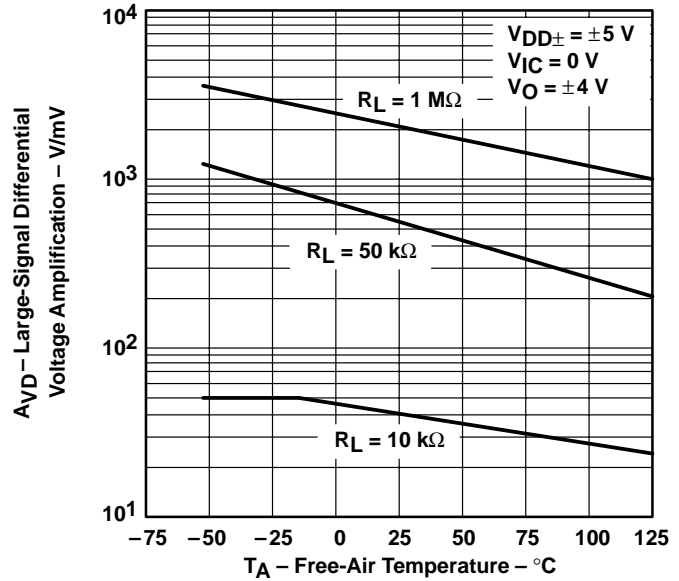


Figure 29

OUTPUT IMPEDANCE‡
vs
FREQUENCY

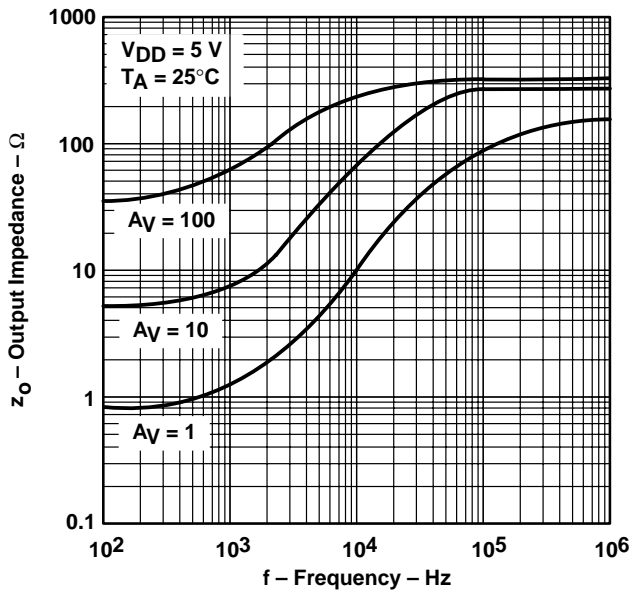


Figure 30

OUTPUT IMPEDANCE
vs
FREQUENCY

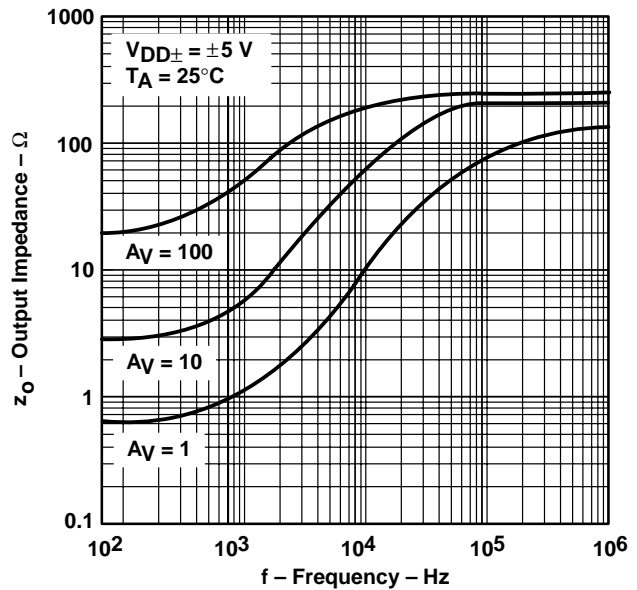


Figure 31

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

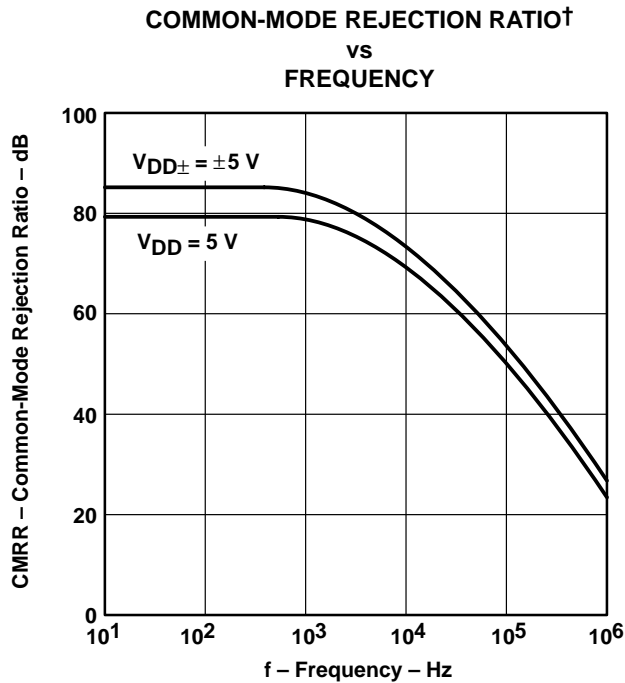


Figure 32

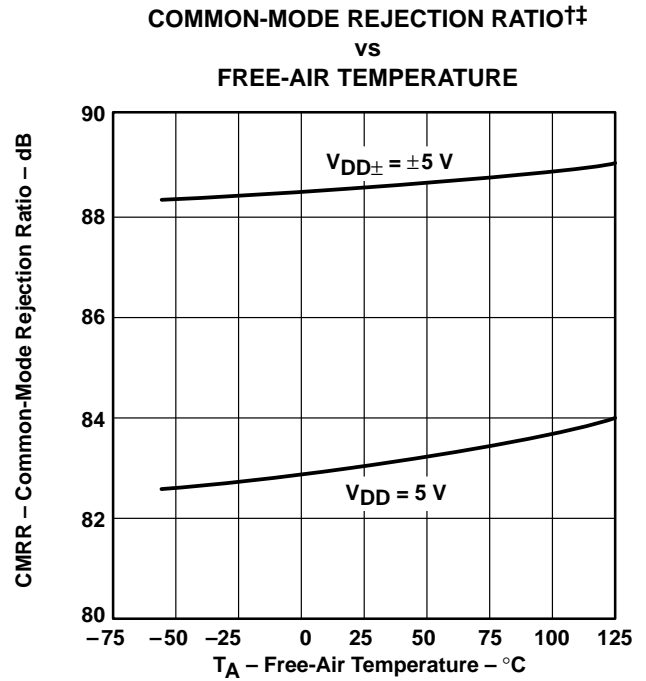


Figure 33

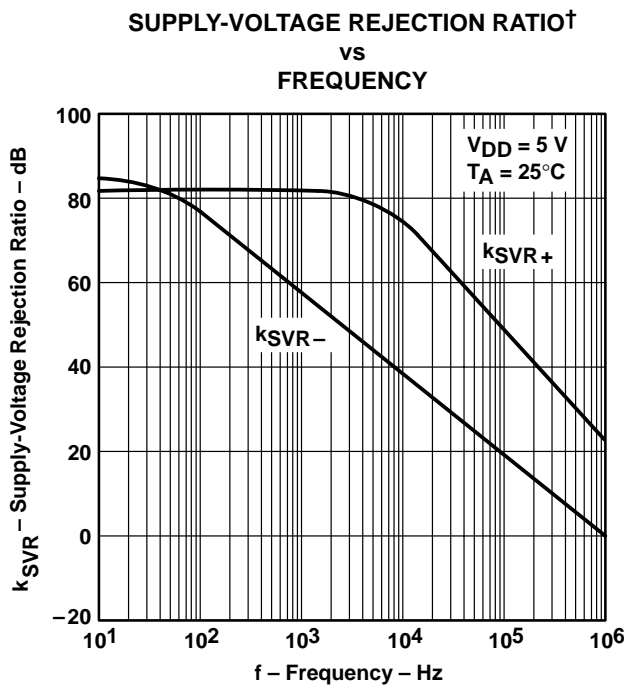


Figure 34

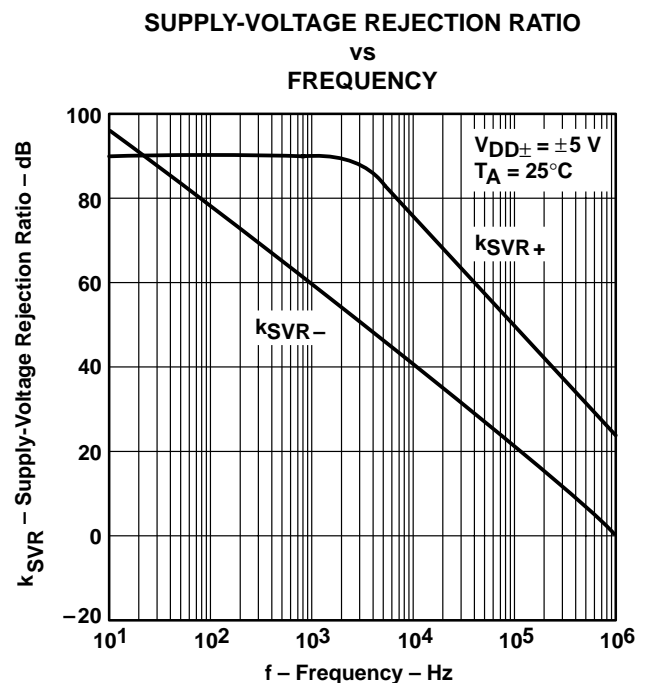


Figure 35

† For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V .

‡ Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

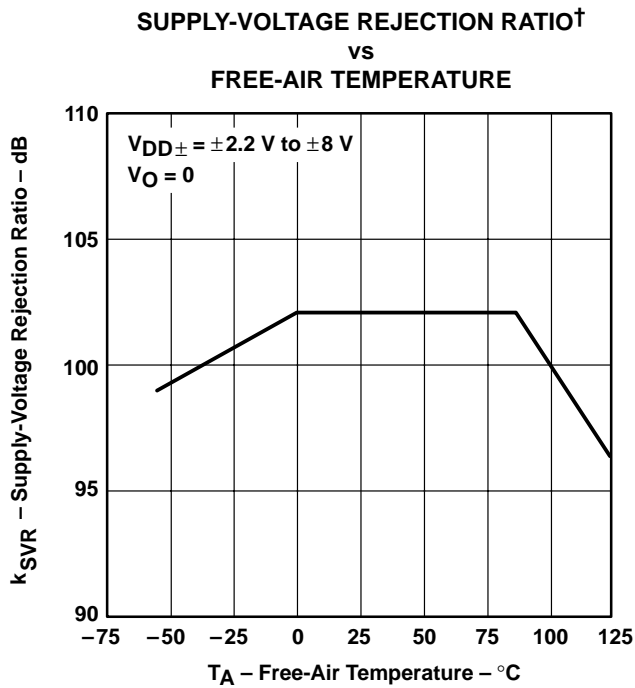


Figure 36

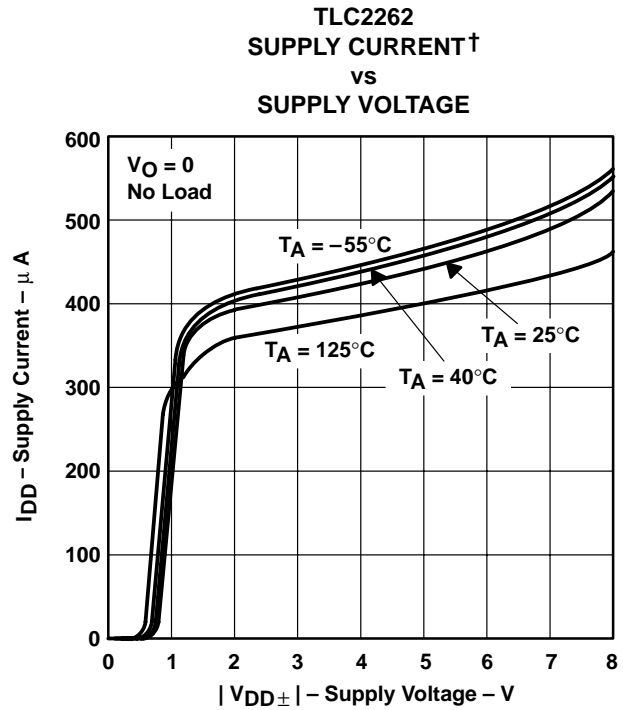


Figure 37

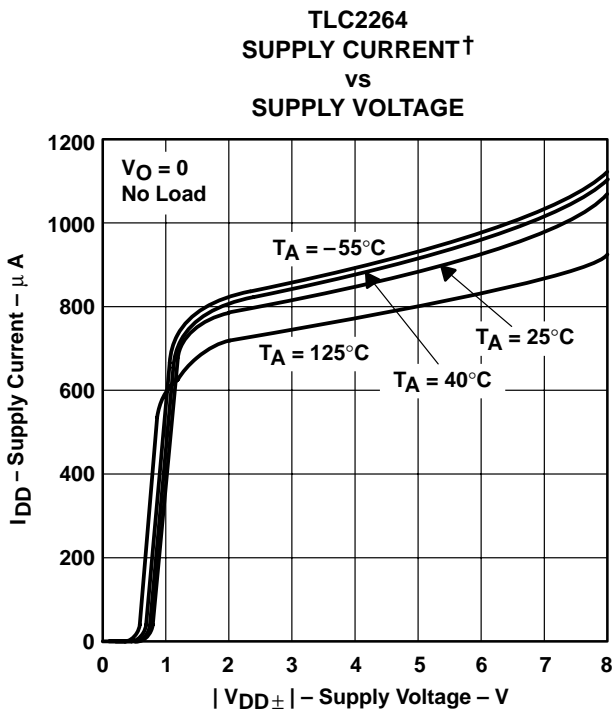


Figure 38

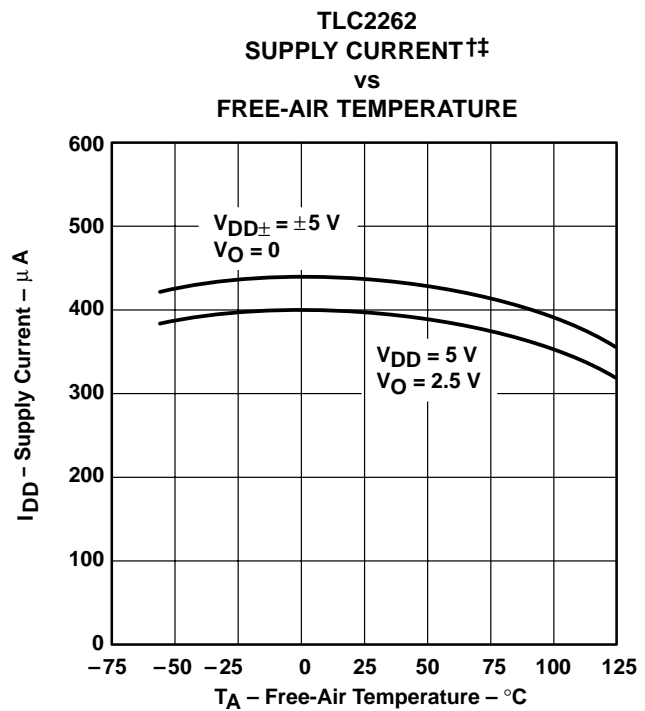
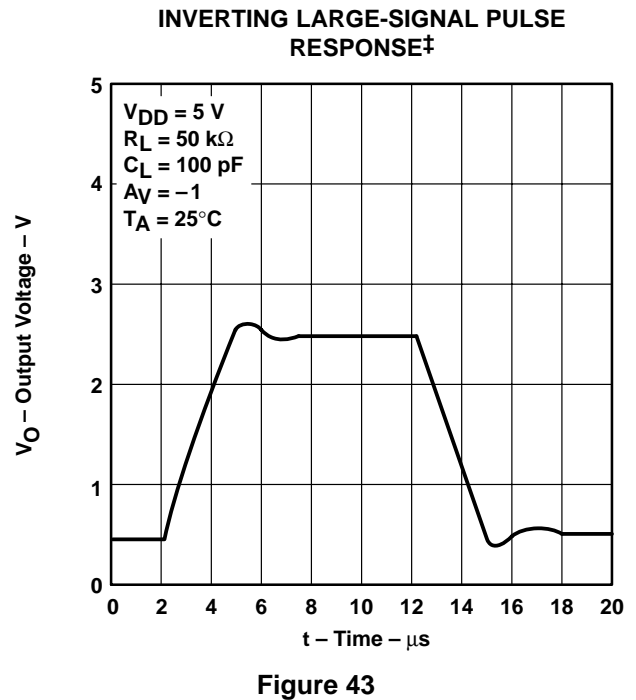
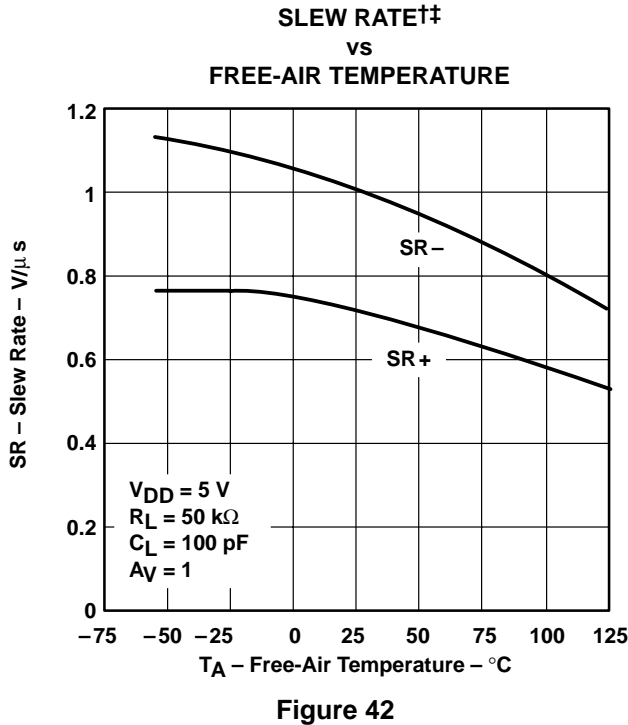
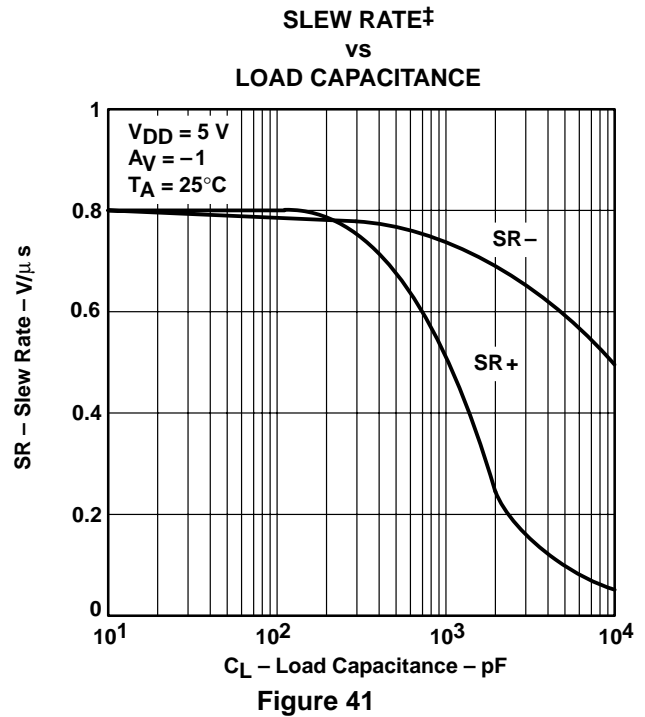
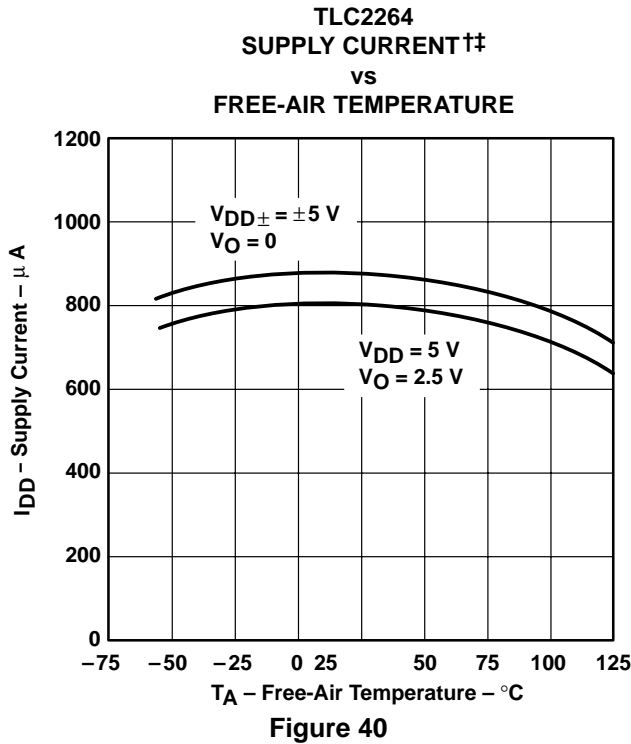


Figure 39

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

†† For curves where $V_{DD} = 5 \text{ V}$, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

INVERTING LARGE-SIGNAL PULSE RESPONSE

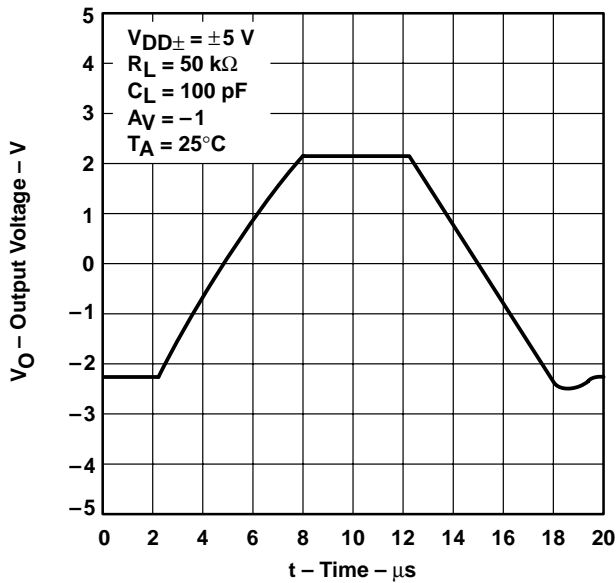


Figure 44

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE†

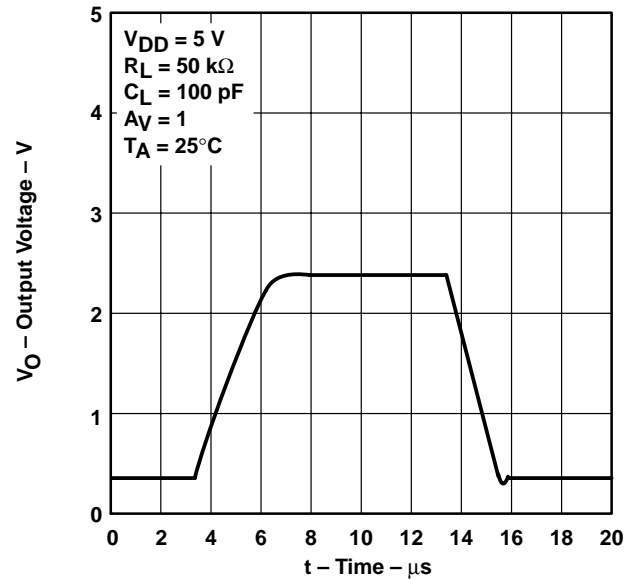


Figure 45

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

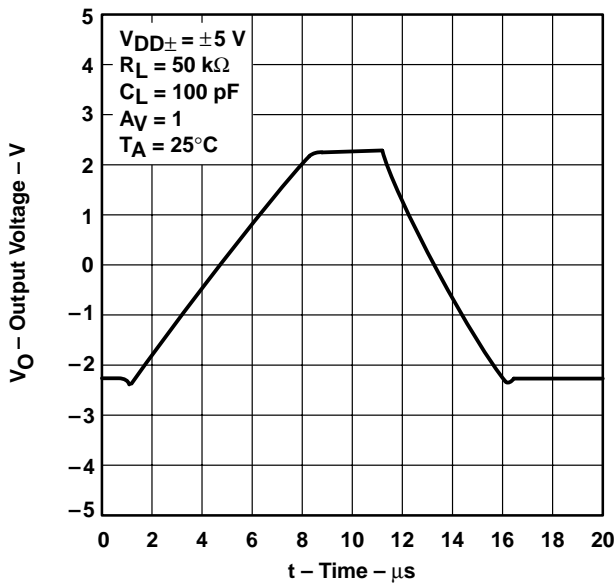


Figure 46

INVERTING SMALL-SIGNAL PULSE RESPONSE†

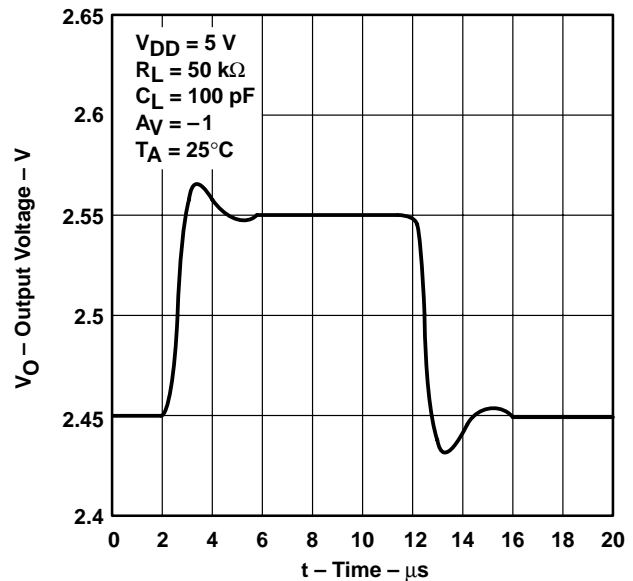


Figure 47

† For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

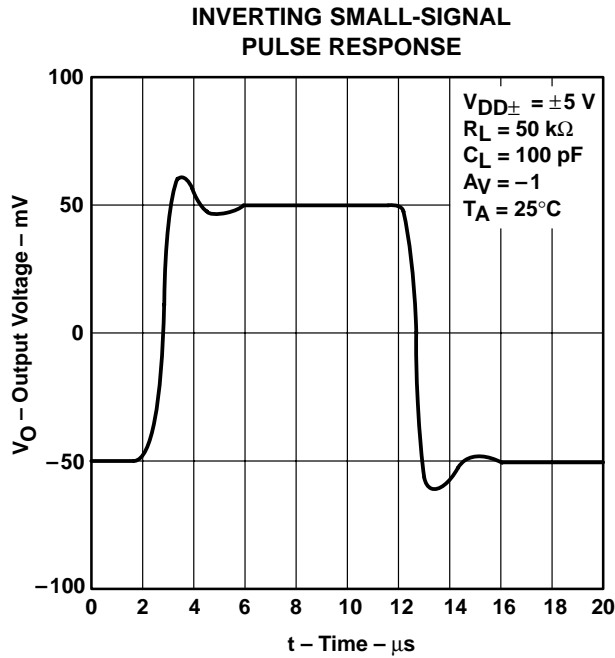


Figure 48

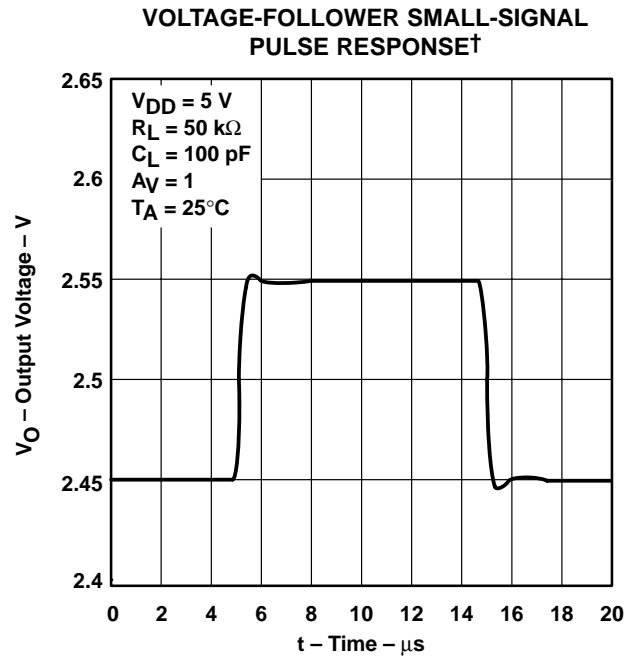


Figure 49

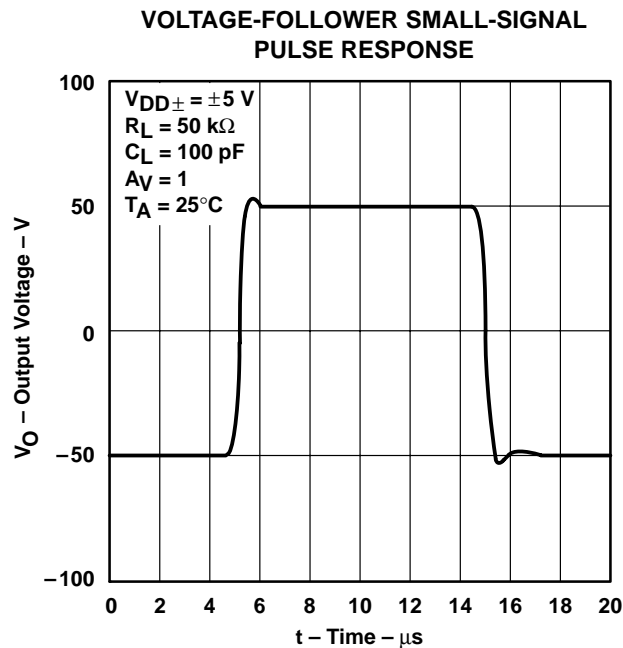


Figure 50

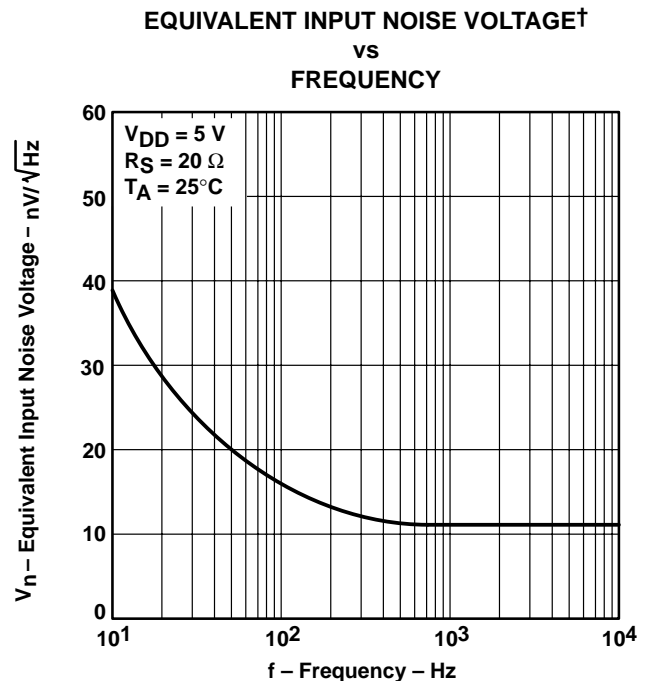


Figure 51

† For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE
 VS
 FREQUENCY

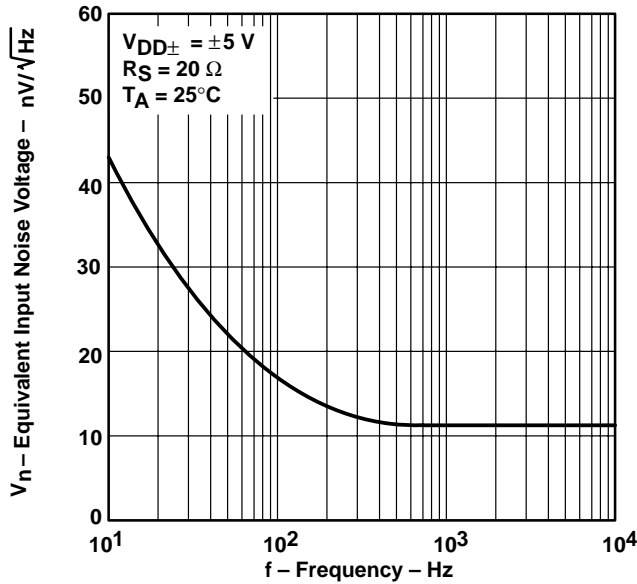


Figure 52

EQUIVALENT INPUT NOISE VOLTAGE OVER
 A 10-SECOND PERIOD†

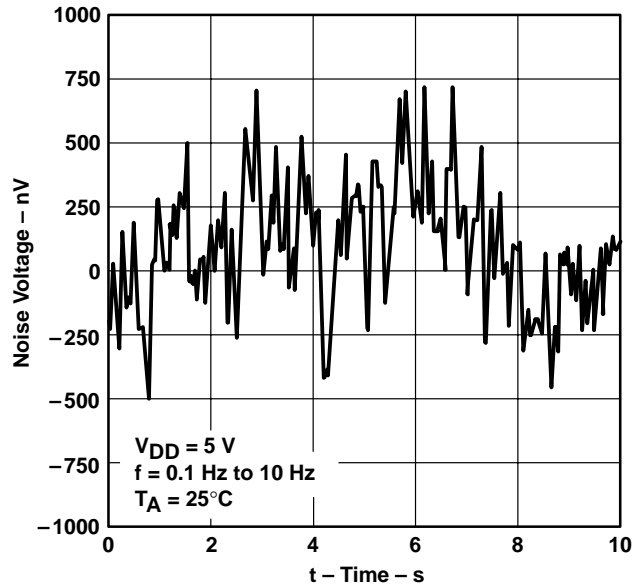


Figure 53

INTEGRATED NOISE VOLTAGE
 VS
 FREQUENCY

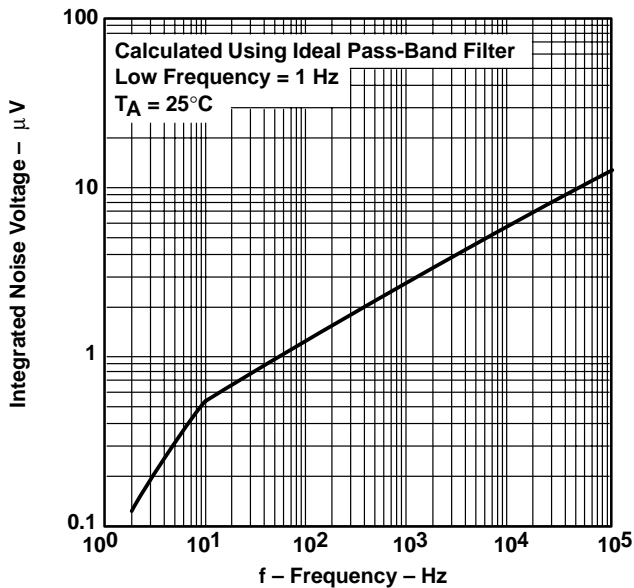


Figure 54

TOTAL HARMONIC DISTORTION PLUS NOISE†
 VS
 FREQUENCY

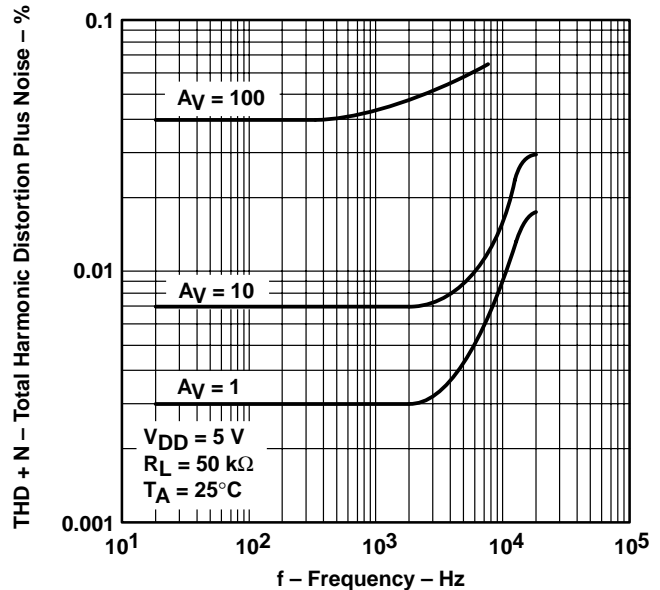


Figure 55

† For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

GAIN-BANDWIDTH PRODUCT
 vs
 SUPPLY VOLTAGE

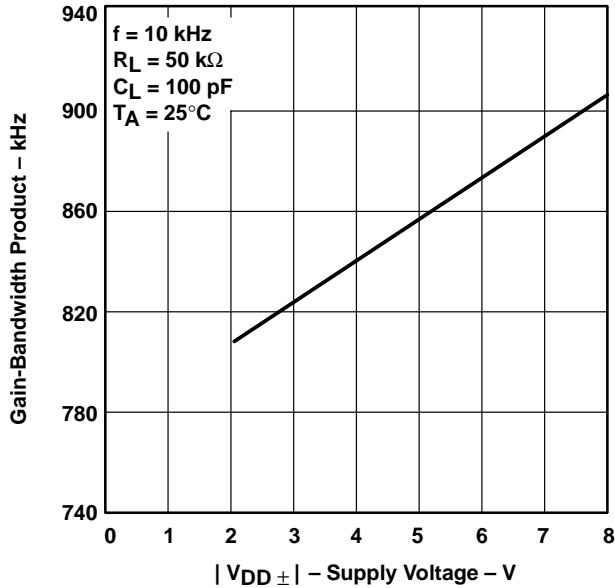


Figure 56

GAIN-BANDWIDTH PRODUCT†‡
 vs
 FREE-AIR TEMPERATURE

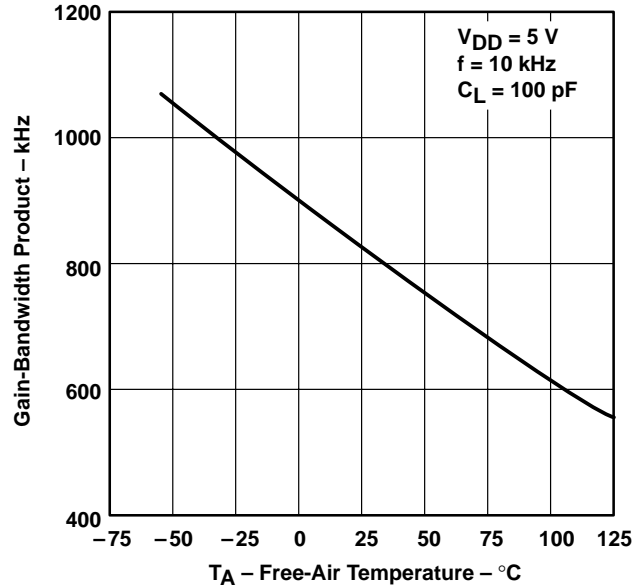


Figure 57

PHASE MARGIN
 vs
 LOAD CAPACITANCE

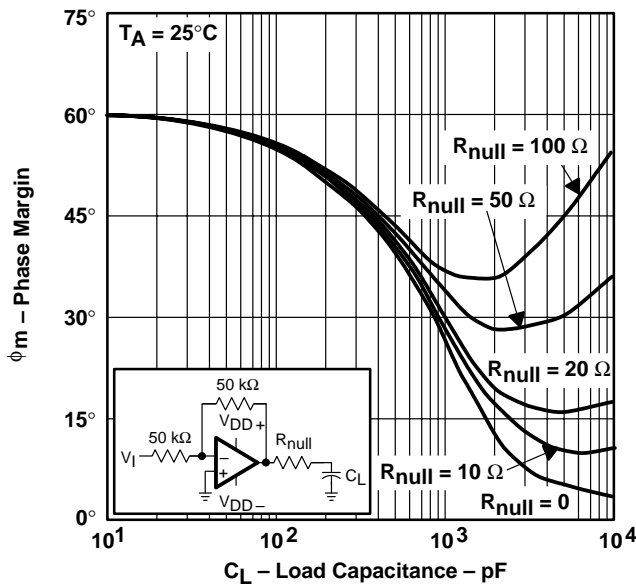


Figure 58

GAIN MARGIN
 vs
 LOAD CAPACITANCE

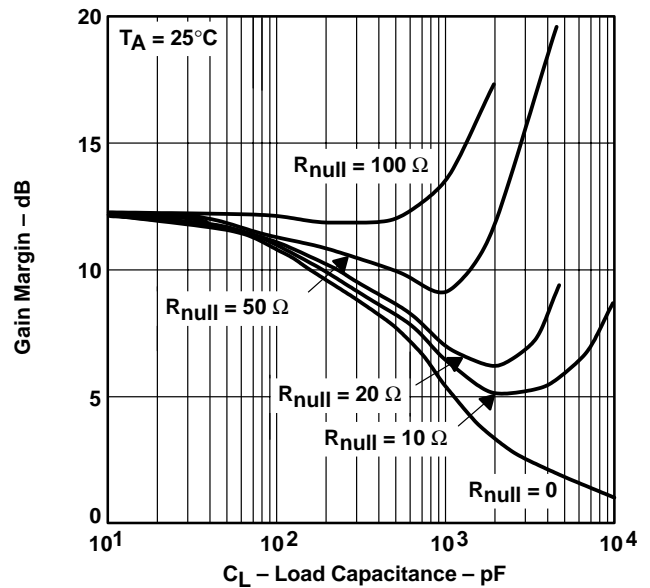


Figure 59

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

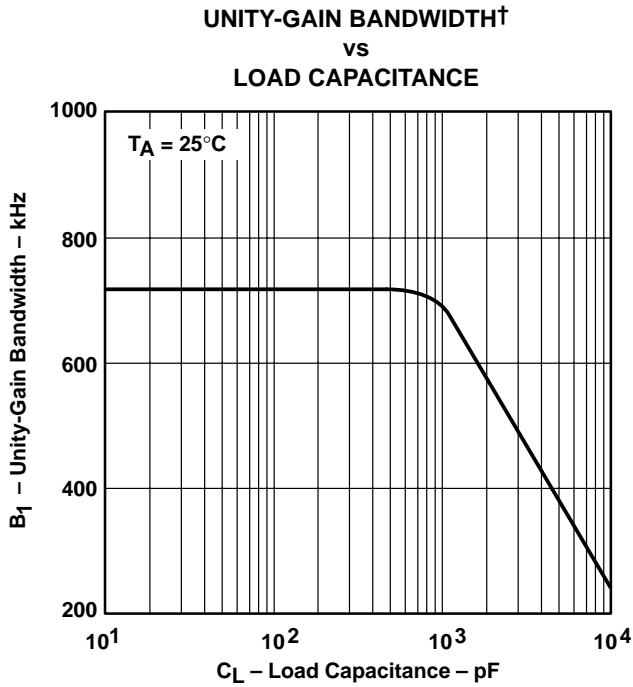


Figure 60

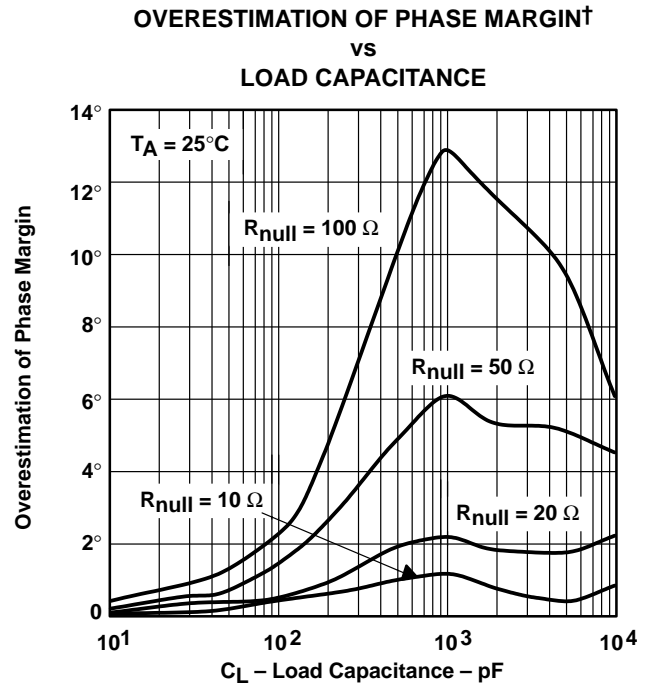


Figure 61

† See application information

APPLICATION INFORMATION

driving large capacitive loads

The TLC226x is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 58 and Figure 59 illustrate its ability to drive loads greater than 400 pF while maintaining good gain and phase margins ($R_{null} = 0$).

A smaller series resistor (R_{null}) at the output of the device (see Figure 62) improves the gain and phase margins when driving large capacitive loads. Figure 58 and Figure 59 show the effects of adding series resistances of 10 Ω , 20 Ω , 50 Ω , and 100 Ω . The addition of this series resistor has two effects: the first is that it adds a zero to the transfer function and the second is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, equation 1 can be used.

$$\Delta\theta_{m1} = \tan^{-1} \left(2 \times \pi \times \text{UGBW} \times R_{null} \times C_L \right) \quad (1)$$

Where :

- $\Delta\theta_{m1}$ = improvement in phase margin
- UGBW = unity-gain bandwidth frequency
- R_{null} = output series resistance
- C_L = load capacitance

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 60). To use equation 1, UGBW must be approximated from Figure 60.

Using equation 1 alone overestimates the improvement in phase margin, as illustrated in Figure 61. The overestimation is caused by the decrease in the frequency of the pole associated with the load, thus providing additional phase shift and reducing the overall improvement in phase margin. The pole associated with the load is reduced by the factor calculated in equation 2.

$$F = \frac{1}{1 + g_m \times R_{null}} \quad (2)$$

Where :

- F = factor reducing frequency of pole
- g_m = small-signal output transconductance (typically 4.83×10^{-3} mhos)
- R_{null} = output series resistance

For the TLC226x, the pole associated with the load is typically 7 MHz with 100-pF load capacitance. This value varies inversely with C_L : at $C_L = 10$ pF, use 70 MHz, at $C_L = 1000$ pF, use 700 kHz, and so on.

Reducing the pole associated with the load introduces phase shift, thereby reducing phase margin. This results in an error in the increase in phase margin expected by considering the zero alone (equation 1). Equation 3 approximates the reduction in phase margin due to the movement of the pole associated with the load. The result of this equation can be subtracted from the result of the equation in equation 1 to better approximate the improvement in phase margin.

APPLICATION INFORMATION

driving large capacitive loads (continued)

$$\Delta\theta_{m2} = \tan^{-1} \left[\frac{UGBW}{(F \times P_2)} \right] - \tan^{-1} \left(\frac{UGBW}{P_2} \right) \tag{3}$$

Where :

$\Delta\theta_{m2}$ = reduction in phase margin

UGBW = unity-gain bandwidth frequency

F = factor from equation 2

P_2 = unadjusted pole (70 MHz @10 pF, 7 MHz @100 pF, etc.)

Using these equations with Figure 60 and Figure 61 enables the designer to choose the appropriate output series resistance to optimize the design of circuits driving large capacitive loads.

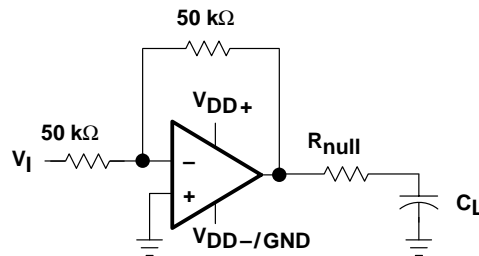


Figure 62. Series-Resistance Circuit

APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 5) and subcircuit in Figure 63 are generated using the TLC226x typical electrical and operating characteristics at $T_A = 25^\circ\text{C}$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

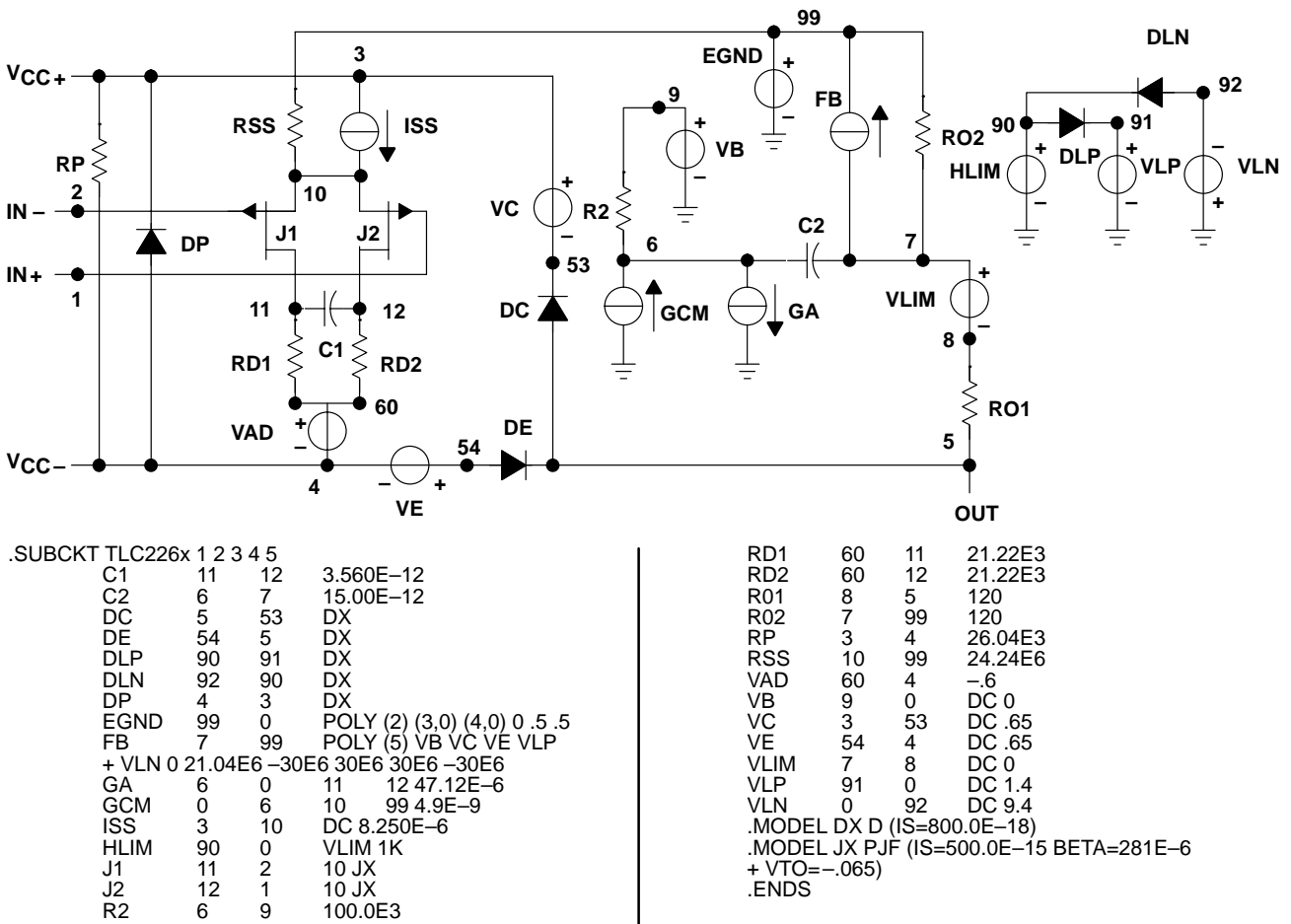


Figure 63. Boyle Macromodel and Subcircuit

PSpice and *Parts* are trademarks of MicroSim Corporation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9469201QHA	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	9469201QHA TLC2262M	Samples
5962-9469203QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9469203QPA TLC2262AM	Samples
5962-9469204Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9469204Q2A TLC2264 AMFKB	Samples
5962-9469204QCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9469204QC A TLC2264AMJB	Samples
TLC2262AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2262AI	Samples
TLC2262AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2262AI	Samples
TLC2262AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2262AI	Samples
TLC2262AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2262AI	Samples
TLC2262AIP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLC2262AI	Samples
TLC2262AIPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLC2262AI	Samples
TLC2262AIPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y2262A	Samples
TLC2262AIPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y2262A	Samples
TLC2262AIPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y2262A	Samples
TLC2262AIPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y2262A	Samples
TLC2262AMJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	TLC2262 AMJG	Samples
TLC2262AMJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9469203QPA TLC2262AM	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC2262AQD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C2262A	Samples
TLC2262CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2262C	Samples
TLC2262CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2262C	Samples
TLC2262CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2262C	Samples
TLC2262CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2262C	Samples
TLC2262CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLC2262CP	Samples
TLC2262CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLC2262CP	Samples
TLC2262CPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P2262	Samples
TLC2262CPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P2262	Samples
TLC2262CPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P2262	Samples
TLC2262CPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P2262	Samples
TLC2262ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2262I	Samples
TLC2262IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2262I	Samples
TLC2262IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2262I	Samples
TLC2262IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2262I	Samples
TLC2262IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC2262IP	Samples
TLC2262MUB	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	9469201QHA TLC2262M	Samples
TLC2262QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C2262Q	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC2262QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C2262Q	Samples
TLC2262QDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		C2262Q	Samples
TLC2264AID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2264AI	Samples
TLC2264AIDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2264AI	Samples
TLC2264AIDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2264AI	Samples
TLC2264AIDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2264AI	Samples
TLC2264AIN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLC2264AIN	Samples
TLC2264AINE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLC2264AIN	Samples
TLC2264AIPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y2264A	Samples
TLC2264AIPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y2264A	Samples
TLC2264AIPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y2264A	Samples
TLC2264AIPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y2264A	Samples
TLC2264AMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9469204Q2A TLC2264 AMFKB	Samples
TLC2264AMJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	TLC2264AMJ	Samples
TLC2264AMJB	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9469204QC A TLC2264AMJB	Samples
TLC2264AQD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2264AQ	Samples
TLC2264AQDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PJ2264A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC2264CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC2264C	Samples
TLC2264CDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC2264C	Samples
TLC2264CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC2264C	Samples
TLC2264CN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLC2264CN	Samples
TLC2264CNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLC2264CN	Samples
TLC2264CPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P2264	Samples
TLC2264CPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P2264	Samples
TLC2264CPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P2264	Samples
TLC2264CPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P2264	Samples
TLC2264ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC2264I	Samples
TLC2264IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC2264I	Samples
TLC2264IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC2264I	Samples
TLC2264IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC2264IN	Samples
TLC2264INE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC2264IN	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLC2262, TLC2262A, TLC2262AM, TLC2262M, TLC2264A, TLC2264AM :

- Catalog: [TLC2262A](#), [TLC2262](#), [TLC2264A](#)
- Automotive: [TLC2264A-Q1](#), [TLC2264A-Q1](#)
- Military: [TLC2262M](#), [TLC2262AM](#), [TLC2264AM](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC2262AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2262AIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC2262CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2262CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC2262IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2262QDR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TLC2264AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2264AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2264CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2264CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2264IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

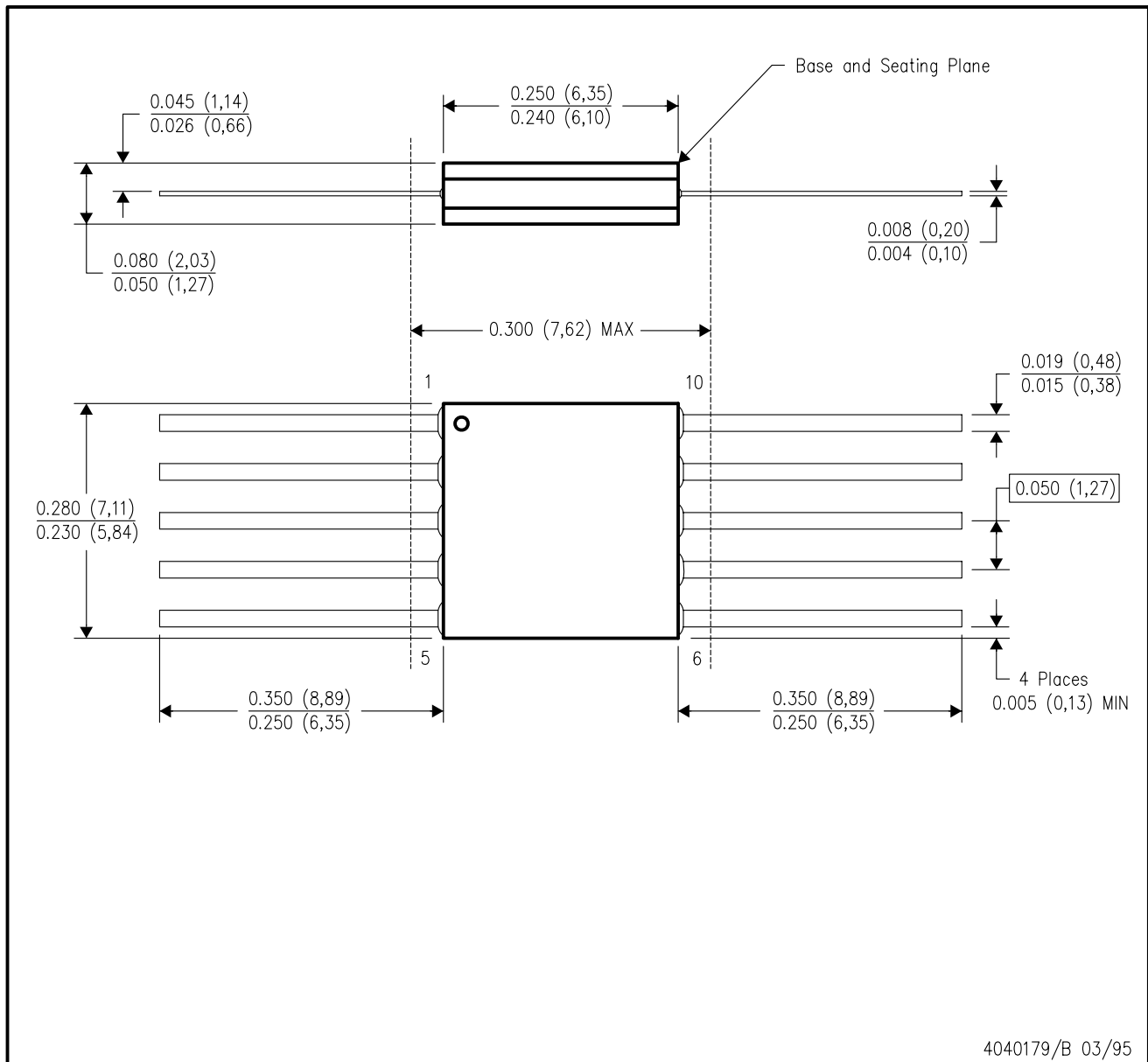
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC2262AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC2262AIPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TLC2262CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC2262CPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TLC2262IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC2262QDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC2264AIDR	SOIC	D	14	2500	333.2	345.9	28.6
TLC2264AIPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TLC2264CDR	SOIC	D	14	2500	333.2	345.9	28.6
TLC2264CPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TLC2264IDR	SOIC	D	14	2500	333.2	345.9	28.6

U (S-GDFP-F10)

CERAMIC DUAL FLATPACK



4040179/B 03/95

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F10 and JEDEC MO-092AA

J 14

GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G



J0014A

PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP1-T8

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

PW0008A



PACKAGE OUTLINE
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.