

REAC1251J

Low Input Offset Voltage $V_{IO} \leq 1\text{mV}$ (@ -40°C to $+125^{\circ}\text{C}$)

Single Power Supply Dual Operational Amplifiers

DESCRIPTION

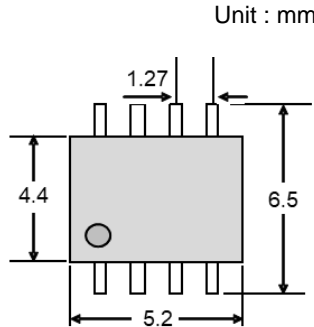
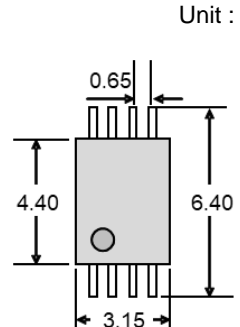
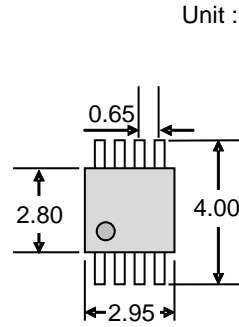
The REAC1251J is a single power and dual operational amplifiers which has features low input offset voltage $V_{IO} \leq \pm 1\text{mV}$ and low input offset voltage temperature drift in $T_a = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$. The features include low-voltage operation, a common-mode input voltage that range from V^- (GND) level, an output from a V^- (GND) level that is determined by the output stage of class C push-pull circuit and a $50\ \mu\text{A}$ (TYP.) constant current, and a low current consumption.

In addition to that, this amplifier can also operate in both positive and negative power supply and can be used extensively in various amplifier circuits.

Features

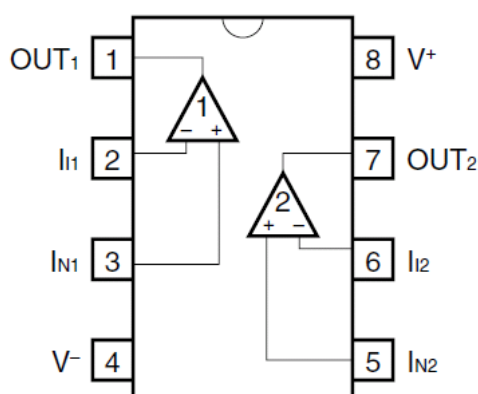
- Low input offset voltage $\pm 1\text{mV}$ (Max.) @ $T_a : -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
- Low input offset voltage temperature drift $\pm 1\ \mu\text{V}/^{\circ}\text{C}$ (Typ.)
- Qualified and characterized according to AEC-Q100
- The package line-up is MSOP

ORDERING INFORMATION

Package	Standard SOP	TSSOP	MSOP
Subject Part Number⁽¹⁾	REAC1251JSM#GCB REAC1251JSM#HCB	REAC1251JSP#GC1 REAC1251JSP#HC1	REAC1251JSN#GC1 REAC1251JSN#HC1
Product Type Quality Level	High Quality Level		
Outline Comparison	Unit : mm 	Unit : mm 	Unit : mm 
(Mounting Area Ratio)	(100 %)	(60 %)	(35 %)

(1) The taping directions are different between GC and HC. Please refer to the delivery specifications in detail.

PIN CONFIGURATION (Marking Side)



ABSOLUTE MAXIMUM RATINGS

<T_A= -40 °C to +125 °C>

Parameter	Symbol	REAC1251JSM	REAC1251JSP	REAC1251JSN	Unit
Power Supply Voltage ^{Note.1}	V ⁺ - V ⁻	-0.1 to +32			V
Differential Input Voltage	V _{ID}	±10			V
Input Voltage ^{Note.2}	V _I	V ⁻ -0.1 to V ⁻ +32			V
Output applied Voltage ^{Note.3}	V _O	V ⁻ -0.1 to V ⁺ +0.1			V
Total Power Dissipation ^{Note.4}	P _T	440			mW
Output Short Circuit Duration ^{Note.5}	t _s	Indefinite			s
Operating Ambient Temperature	T _A	-40 to +125			°C
Operating Junction Temperature	T _J	-40 to +150			°C
Storage Temperature	T _{stg}	-55 to +150			°C

Note

- Note that reverse connections of the power supply may damage ICs.
- The input voltage is allowed to input without damage or destruction independent of the magnitude of V⁺. Either input signal is not allowed to go negative by more than 0.1 V if the conditions are within absolute maximum ratings. This specification which includes the transition state such as electric power ON/OFF must be kept. In addition, the input voltage that operates normally as an operational amplifier is within the Common Mode Input Voltage range of an electrical characteristic.
- A range where input voltage can be applied to an output pin externally with no deterioration or damage to the feature (characteristic). The input voltage can be applied regardless of the electric supply voltage. This specification which includes the transition state such as electric power ON/OFF must be kept.
- This is the value of when the glass epoxy substrate (size: 100 mm x 100 mm, thickness: 1 mm, 15% of the substrate area where only one side is copper foiled is filling wired) is mounted. Note that restrictions will be made to the following conditions for each product, and the derating ratio depending on the operating ambient temperature.

REAC1251JSM Derate at -4.4 mW/°C when T_A > 50°C.

Junction ambient thermal resistance R_{th(J-A)}=227°C/W

REAC1251JSP Derate at -5.5 mW/°C when T_A > 69°C.

Junction ambient thermal resistance R_{th(J-A)}=183°C/W

REAC1251JSN Derate at -4.8 mW/°C when T_A > 58°C.

Junction ambient thermal resistance R_{th(J-A)}=208°C/W

- Short circuits from the output to V⁺ can cause destruction. Pay careful attention to the total power dissipation not to exceed the absolute maximum ratings, Note 4.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Power Supply Voltage (Split)	V^{\pm}	± 1.5		± 15	V
Power Supply Voltage ($V^- = \text{GND}$)	V^+	+3		+30	V

ELECTRICAL CHARACTERISTICS

< $V^+ = +5\text{V}$, $V^- = \text{GND}$, $T_A = 25^\circ\text{C}$ >

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Conditions
Input Offset Voltage	V_{IO}		± 0.2	± 1	mV	$V_{IN} = 1/2V_{CC}$, $R_S \leq 50\Omega$
Input Offset Current	I_{IO}		± 5	± 50	nA	
Input Bias Current ^{Note 6}	I_B		14	60	nA	
Large Signal Voltage Gain	A_V	25,000	100,000			$R_L \geq 2\text{k}\Omega$ (Connect to GND)
Supply Current ^{Note 7}	I_{CC}		0.7	1.4	mA	$R_L = \infty$, $I_O = 0\text{A}$
Common Mode Rejection Ratio	CMR	65	85		dB	
Supply Voltage Rejection Ratio	SVR	65	100		dB	
Common Mode Input Voltage Range	V_{ICM}	0		$V^+ - 1.5$	V	
Output Voltage Swing	V_O	0		$V^+ - 1.6$	V	$R_L = 2\text{k}\Omega$ (Connect to GND)
Output Current (Source)	$I_{O \text{ SOURCE}}$	20	40		mA	$V_{IN^+} = +1\text{V}$, $V_{IN^-} = 0\text{V}$
Output Current (Sink)	$I_{O \text{ SINK1}}$	10	20		mA	$V_{IN^-} = +1\text{V}$, $V_{IN^+} = 0\text{V}$
	$I_{O \text{ SINK2}}$	12	50		μA	$V_{IN^-} = +1\text{V}$, $V_{IN^+} = 0\text{V}$, $V_O = 200\text{mV}$
Channel Separation			120		dB	$f = 1\text{kHz}$ to 20kHz

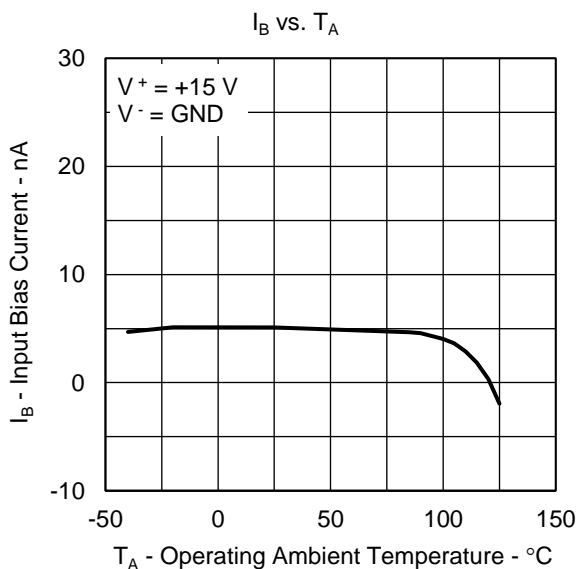
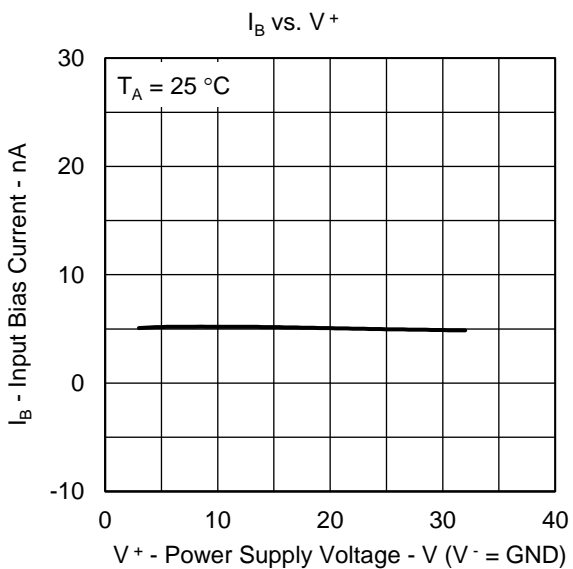
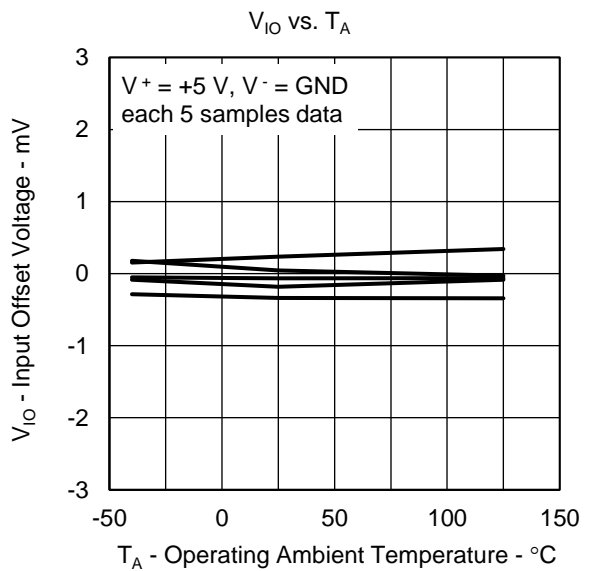
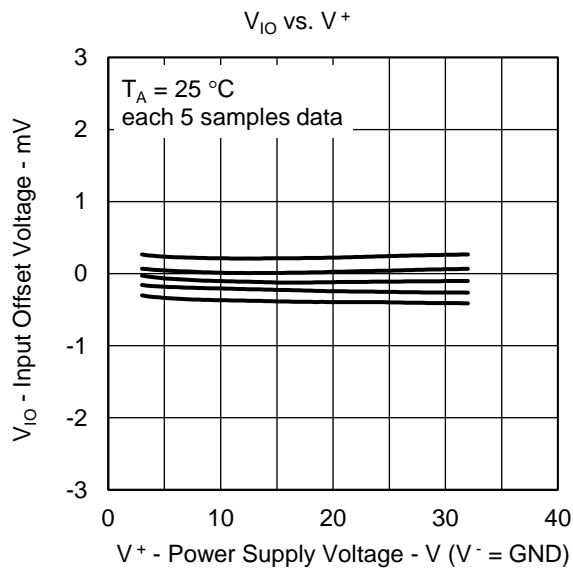
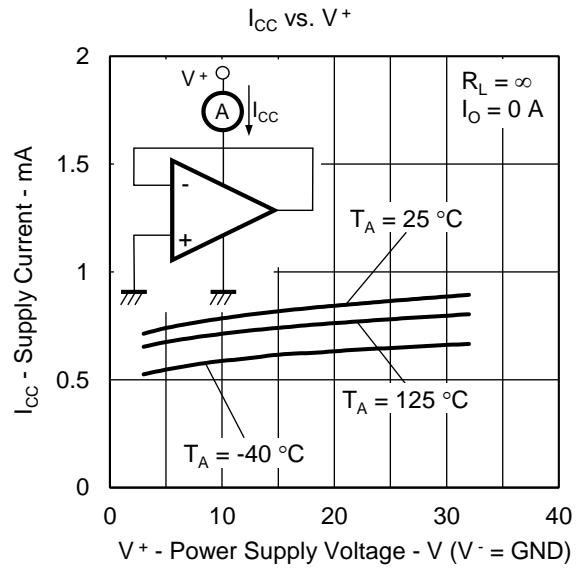
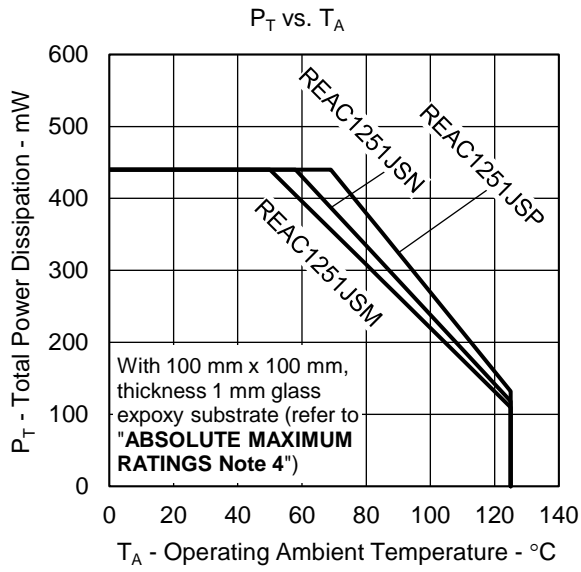
< $V^+ = +5\text{V}$, $V^- = \text{GND}$, $T_A = -40$ to $+125^\circ\text{C}$ >

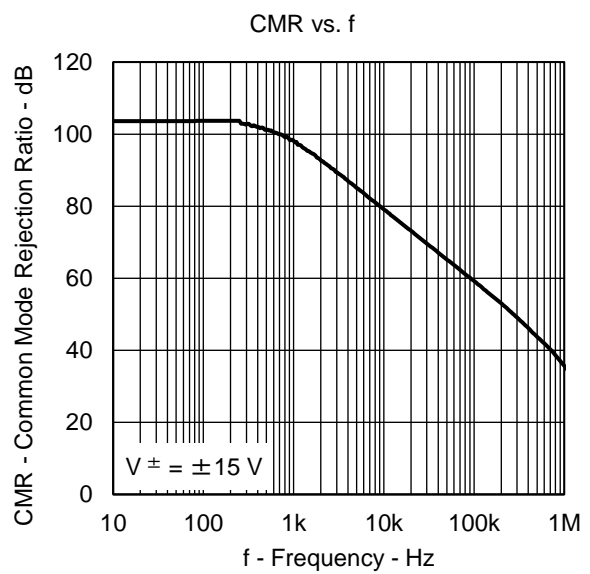
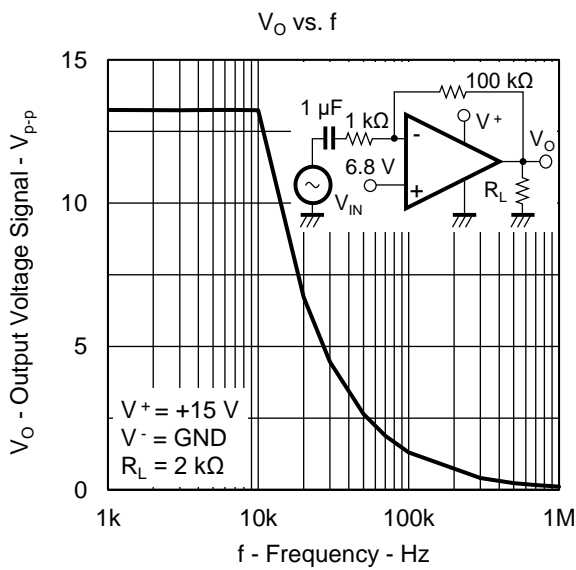
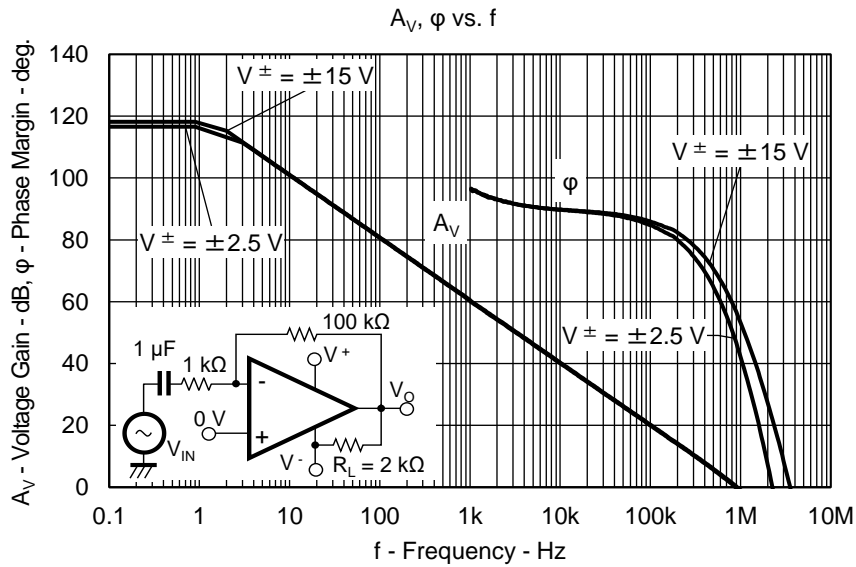
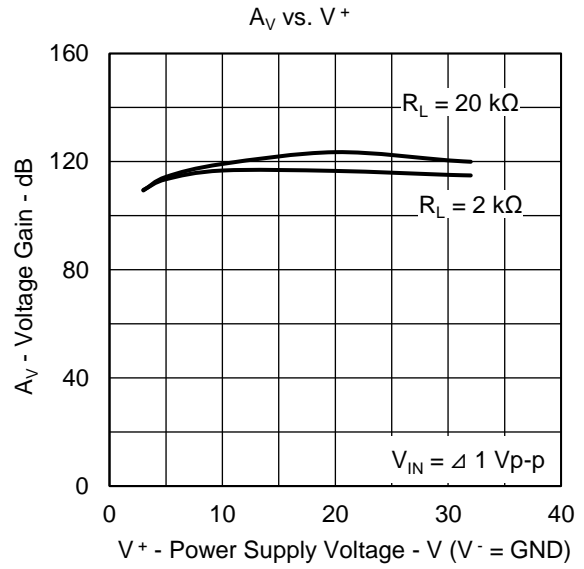
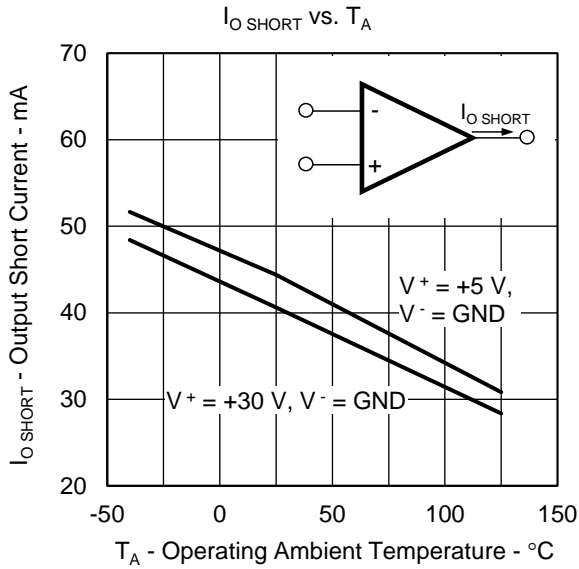
Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Conditions
Input Offset Voltage	V_{IO}		± 0.5	± 1	mV	$V_{IN} = 1/2V_{CC}$, $R_S \leq 50\Omega$
Input Offset Current	I_{IO}			± 100	nA	
Input Bias Current ^{Note 6}	I_B			100	nA	
Large Signal Voltage Gain	A_V	10,000				$R_L \geq 2\text{k}\Omega$ (Connect to GND)
Supply Current ^{Note 7}	I_{CC}			1.4	mA	$R_L = \infty$, $I_O = 0\text{A}$
Common Mode Rejection Ratio	CMR	50			dB	
Supply Voltage Rejection Ratio	SVR	50			dB	
Common Mode Input Voltage Range	V_{ICM}	0		$V^+ - 1.8$	V	
Output Voltage Swing	V_O	0		$V^+ - 1.8$	V	$R_L = 2\text{k}\Omega$ (Connect to GND)
Output Current (Source)	$I_{O \text{ SOURCE}}$	10			mA	$V_{IN^+} = +1\text{V}$, $V_{IN^-} = 0\text{V}$
Output Current (Sink)	$I_{O \text{ SINK1}}$	5			mA	$V_{IN^-} = +1\text{V}$, $V_{IN^+} = 0\text{V}$
	$I_{O \text{ SINK2}}$	5			μA	$V_{IN^-} = +1\text{V}$, $V_{IN^+} = 0\text{V}$, $V_O = 200\text{mV}$

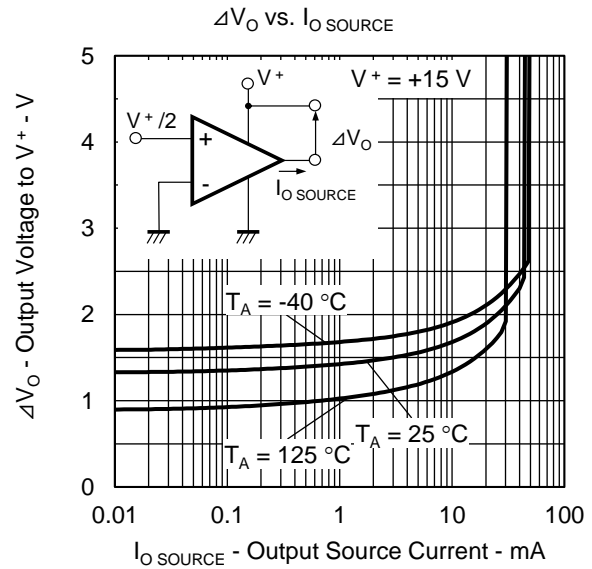
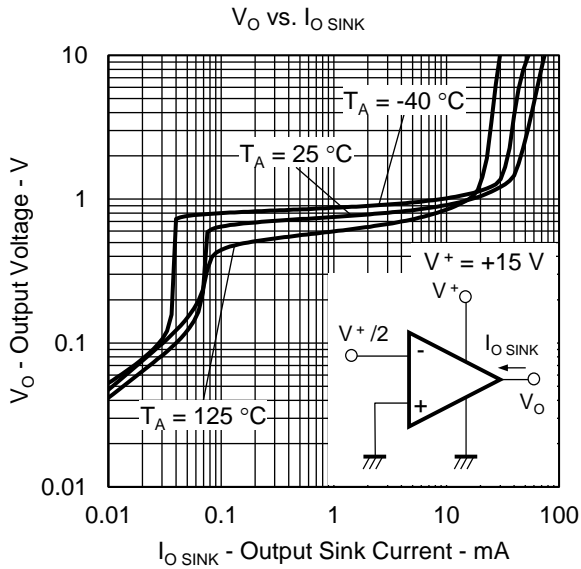
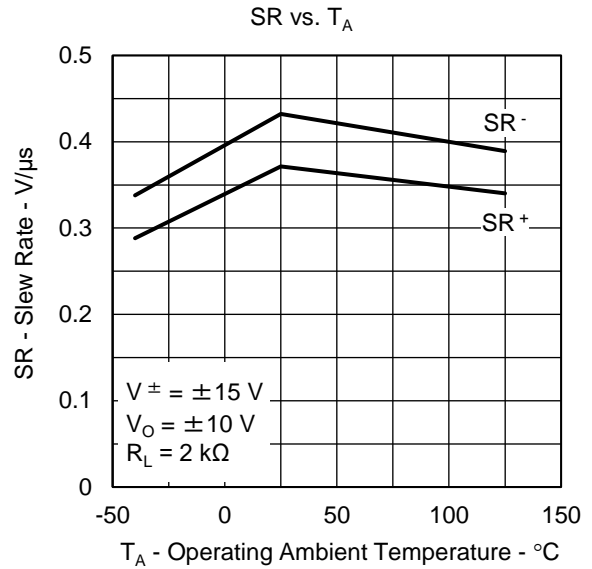
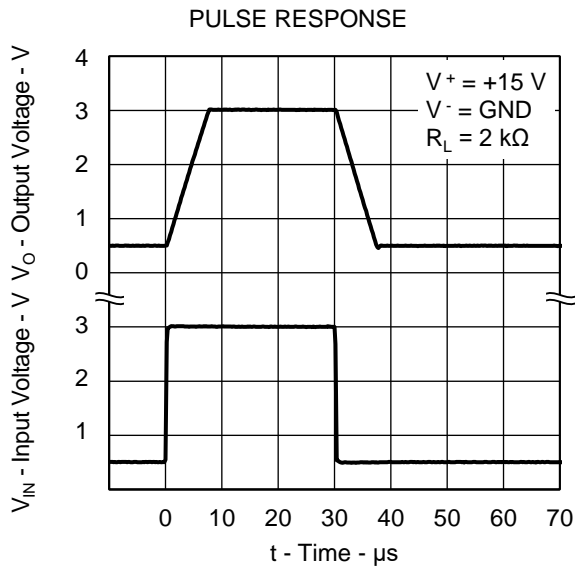
Note 6. The input bias current flows in the direction where the IC flows out because the first stage is configured with a PNP transistor.

7. This is a current that flows in the internal circuit. This current will flow irrespective of the channel used.

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25 °C, TYP.) (Reference value)



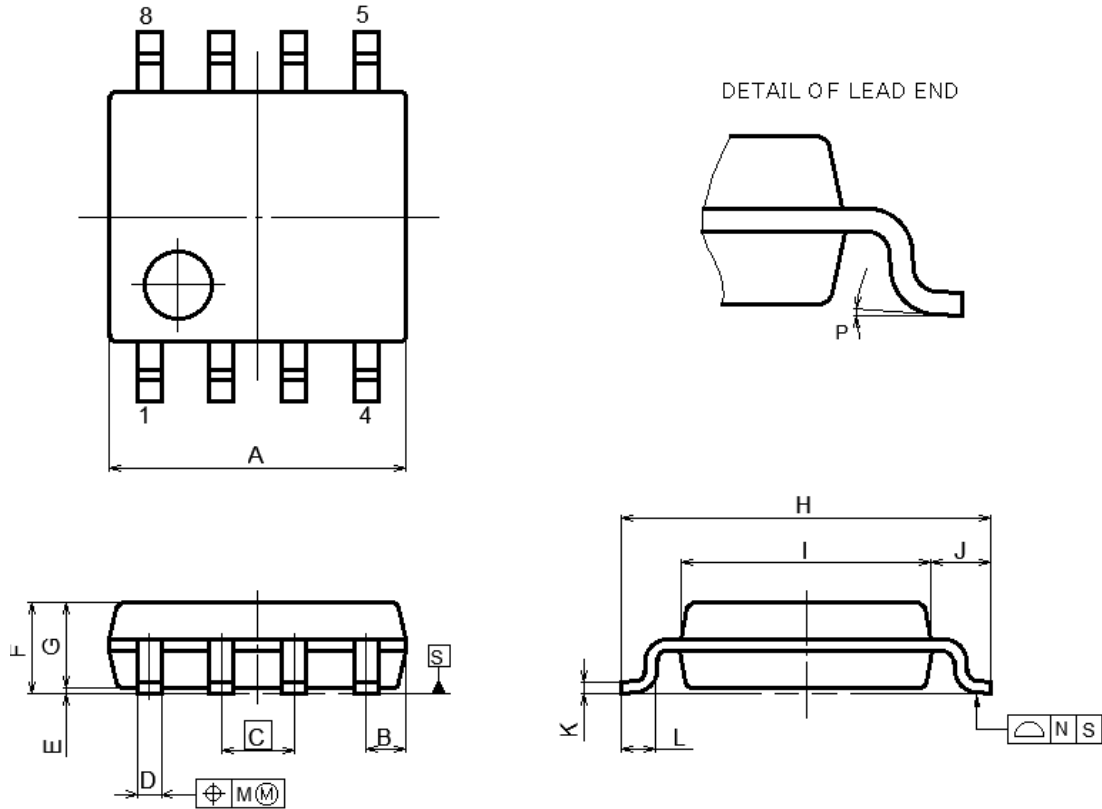




PACKAGE DRAWINGS

8-PIN PLASTIC SOP

JEITA Package code	RENESAS code	MASS (TYP.) [g]
P-LSOP8-4.4x5.2-1.27	PLSP0008DE-A	0.09[g]

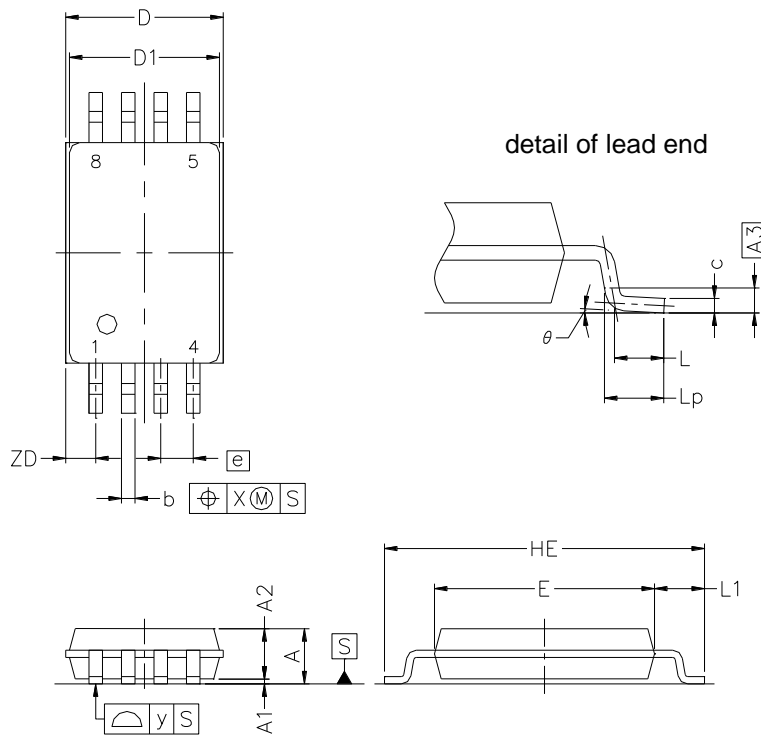


NOTE
 EACH LEAD CENTERLINE IS LOCATED WITHIN 0.12 MM OF ITS TRUE POSITION(T.P.) AT MAXIMUM MATERIAL CONDITION.

(UNIT:mm)	
ITEM	DIMENSIONS
A	5.2±0.17
B	0.78MAX
C	1.27(T.P)
D	0.40±0.05
E	0.1±0.1
F	1.59±0.21
G	1.49
H	6.5±0.3
I	4.4±0.1
J	1.05±0.15
K	0.2±0.07
L	0.6±0.20
M	0.1MAX
N	0.1MAX
P	4°±4°

8-PIN PLASTIC TSSOP

JEITA Package code	RENESAS code	Previous code	MASS(TYP.) [g]
P-TSSOP8-0225-0.65	PTSP0008JD-A	P8GR-65-9LG	—



(Unit : mm)

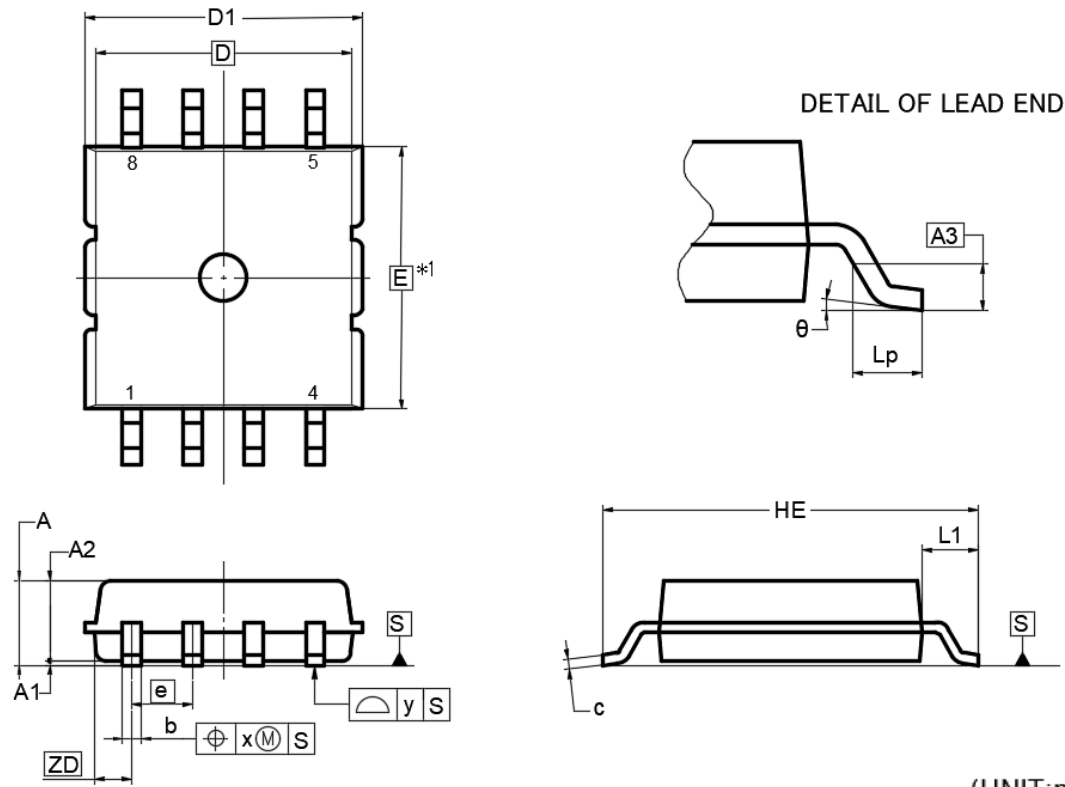
NOTE

Each lead centerline is located within 0.10 mm of its true position at maximum material condition.

ITEM	MILLIMETERS
D	3.15 ±0.15
D1	3.00 ±0.10
E	4.40 ±0.10
HE	6.40 ±0.20
A	1.20 MAX.
A1	0.10 ±0.05
A2	1.00 ±0.05
A3	0.25
b	0.24 ^{+0.06} _{-0.05}
c	0.145 ±0.055
L	0.5
Lp	0.60 ±0.15
L1	1.00 ±0.20
θ	3° ^{+5°} _{-3°}
e	0.65
x	0.10
y	0.10
ZD	0.60

8-PIN PLASTIC MSOP

JEITA Package Code	RENESAS Code	MASS (TYP.) [g]
P-VSSOP8-2.75x2.8-0.65	PVSP0008JA-A	0.02[g]



(UNIT:mm)

ITEM	DIMENSIONS
D	2.75
D1	2.95±0.20
E	2.80
HE	4.00±0.30
e	0.65
b	0.20 ^{+0.10} _{-0.05}
A	1.00MAX
A1	0.05±0.05
A2	0.85±0.10
A3	0.25
L1	0.60±0.20
c	0.13 ^{+0.10} _{-0.05}
Lp	0.37±0.12
x	0.10
y	0.10
θ	7±7°
ZD	0.50

NOTE)

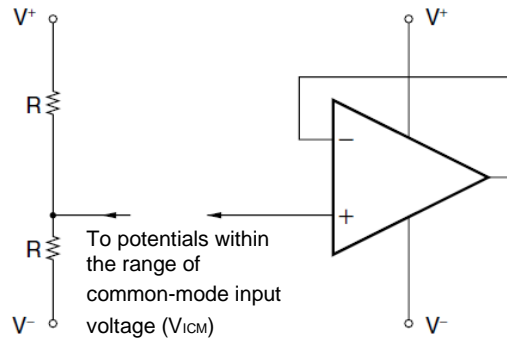
- 1.DIMENSIONS"*1"
DO NOT INCLUDE MOLD FLASH.
- 2.EACH LEAD CENTERLINE IS LOCATED WITHIN 0.10 MM OF
ITS TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

PRECAUTIONS FOR USE

○The process of unused circuits

If there is an unused circuit, the following connection is recommended.

Process example of unused circuits



Remark A midpoint potential of V^+ and V^- is applied to this example.

○Ratings of input/output pin voltage

When the voltage of input/output pin exceeds the absolute maximum rating, it may cause degradation of characteristics or damages, by a conduction of a parasitic diode within an IC. In addition, when the input pin may be lower than V^- , or the output pin may exceed the power supply voltage, it is recommended to make a clamp circuit by a diode whose forward voltage is low (e.g.: Schottky diode) for protection.

○Range of common-mode input voltage

When the supply voltage does not meet the condition of electrical characteristics, the range of common-mode input voltage is as follows.

$$V_{ICM} \text{ (TYP.)}: V^- \text{ to } V^+ - 1.5 \text{ (V)} \text{ (} T_A = 25^\circ\text{C)}.$$

During designing, do include some tolerance by considering temperature characteristics and etc.

○The maximum output voltage

The range of the TYP. value of the maximum output voltage when the supply voltage does not meet the condition of electrical characteristics is as follows:

$$V_{Om+} \text{ (TYP.)}: V^- - 1.6 \text{ [V]} \text{ (} T_A = 25^\circ\text{C)},$$

$$V_{Om-} \text{ (TYP.) (} I_{o \text{ SINK}} \leq 50 \mu\text{A)}: \text{Approx. } V^- \text{ (V)} \text{ (} T_A = 25^\circ\text{C)}$$

During designing, consider variations in characteristics and temperature characteristics for use with allowance. In addition, also note that the output voltage range ($V_{Om+} - V_{Om-}$) becomes narrow when an output current increases.

○Operation of output

This IC consist an output level of a class C push-pull. Therefore, when a load resistance is connected to the midpoint potential of V^+ , V^- , a crossover distortion occurs at the transition state of output current flow direction (source, sink).

○Handling of ICs

When stress is added to ICs due to warpage or bending of a board, the characteristic fluctuates due to piezoelectric effect. Therefore, pay attention to warpage or bending of a board.

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