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SSI 32F8130/8131
Low-Power Programmable Electronic Filter

January 1995

DESCRIPTION

The SSI 32F8130/8131 Programmable Electronic Filters are digitally controlled low pass filters with a normal low pass output and a time differentiated low pass output. The low pass filter is of a 7-pole / 2-zero 0.05° phase equiripple type, with flat group delay response beyond the passband.

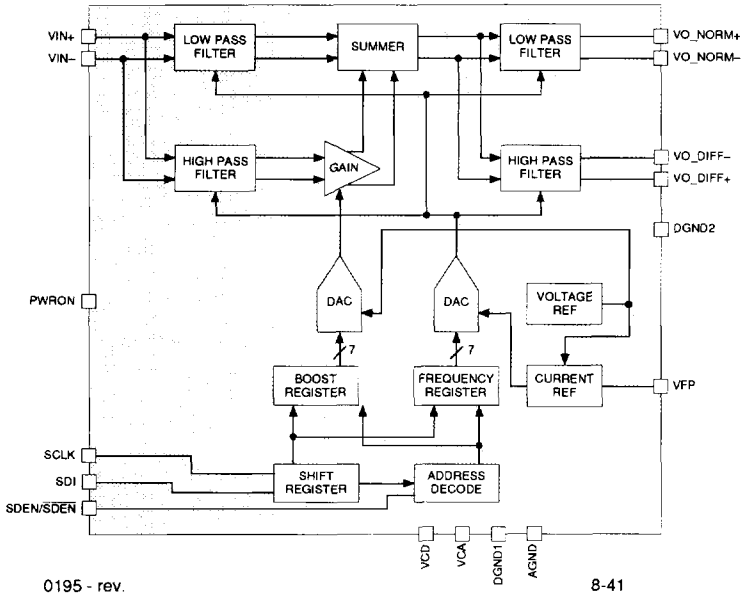
The SSI 32F8130/8131 bandwidth and boost are controlled by two on-chip 7-bit DACs, which are programmed via a 3-line serial interface. The SSI 32F8130 filter bandwidth is programmable from 285 kHz to 2.2 MHz. The SSI 32F8131 is programmable from 150 kHz to 1.4 MHz. The boost is programmable from 0 to 10 dB. Because the boost function is implemented as two zeros on the real axis with opposite sign, the flat group delay characteristic is not affected by the boost programming.

The SSI 32F8130/8131 are ideal for multi-rate, equalization applications. They require only a +5V supply and have a power down mode for minimal idle dissipation. The SSI 32F8130/8131 is available in a 16-lead SOL package.

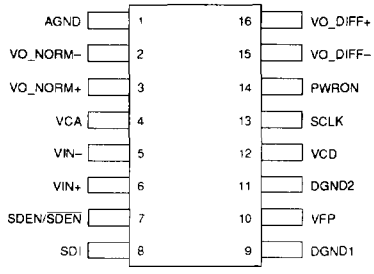
FEATURES

- **Programmable filter cutoff frequency (SSI 32F8130: fc = 0.285 to 2.2 MHz, SSI 32F8131: fc = 0.15 to 1.4 MHz) with no external components, serial data connections to minimize pin count**
- **Power down mode (<5 mW)**
- **Programmable pulse slimming equalization (0 to 10 dB boost at the filter cutoff frequency)**
- **Matched normal and differentiated low-pass outputs**
- **Differential filter inputs and outputs**
- **Programming via internal 7-bit DACs**
- **No external filter components required**
- **+5V only operation**
- **Supports constant density recording**

BLOCK DIAGRAM



PIN DIAGRAM



16-Lead SOL

SSI 32F8130: Lead 7 = SDEN
SSI 32F8131: Lead 7 = $\overline{\text{SDEN}}$

CAUTION: Use handling procedures necessary for a static sensitive component.

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SSI 32F8130/8131
Low-Power Programmable Electronic Filter

FUNCTIONAL DESCRIPTION

The SSI 32F8130/8131, a high performance programmable electronic filter, provides a 7-pole / 2-zero 0.05° equiripple linear phase low pass function with matched normal and time differentiated outputs. The device includes multiple biquads and first-order sections to accomplish the filter function, two 7-bit DACs for bandwidth and boost controls, a 3-line serial interface, and complete bias reference circuits. Only one external precision 8.25 kΩ resistor should be connected from the VFP pin to ground for operation. See Figure 1.

SERIAL INTERFACE

The SSI 32F8130/8131 allows easy digital controls of filter bandwidth and magnitude equalization via a 3-line serial interface. The three pins are SDI, SDEN and SCLK. SDI is the serial data input to an internal 8-bit shift register. SDEN is the shift register enable. SCLK is the shift register clock. Besides the 8-bit shift register which accepts data from the SDI input, there are four 4-bit registers which hold the filter bandwidth and boost controls. Two 4-bit registers are assigned to each control function, because a 7-bit binary control is required for each function.

The S-MSB register, whose address code is X000, holds the 3 MSBs of the boost control. The S-LSB register, whose address code is X001, holds the 4 LSBs of the boost control. The F-MSB register, whose address code is X010, holds the 4 MSBs of the cutoff frequency control. The F-LSB register, whose address code is X011, holds the 4 LSBs of the cutoff frequency control.

The serial interface consists of data packets, which are structured as 4-bit address decode followed by 4-bit data. Figure 2 shows the serial interface timing to successfully program the SSI 32F8130/8131.

CUTOFF FREQUENCY PROGRAMMING

The cutoff frequency, fc, is defined as the -3 dB bandwidth with no magnitude equalization applied, and is programmable from 285 kHz to 2.2 MHz for SSI 32F8130, and 150 kHz to 1.4 MHz for SSI 32F8131. While the fc is controlled by an on-chip 7-bit DAC, the cutoff frequency resolution is better than 20-kHz step.

Let F_Code be the decimal equivalent of the 7-bit control. The cutoff frequency can be determined by the following equations:

SSI 32F8130 fc (kHz) = 16.73 • F_Code + 84

SSI 32F8131 fc (kHz) = 10.81 • F_Code + 37

where $12 \leq F\_Code \leq 127$.

MAGNITUDE EQUALIZATION PROGRAMMING

The magnitude equalization, measured in dB, is the amount of high frequency peaking at the cutoff frequency relative to the original -3 dB point. For example, when 10 dB boost is applied, the magnitude response peaks up 7 dB above the DC gain. This equalization function is also controlled by an on-chip 7-bit DAC.

Let S_Code be the decimal equivalent of the 7-bit control. The magnitude equalization can be determined by the equation:

Boost (dB) = $20 \cdot \log_{10} [0.0145 \cdot S\_Code + 1]$ for 32F8130

Boost (dB) = $20 \cdot \log_{10} [0.01703 \cdot S\_Code + 1]$ for 32F8131

where $0 \leq S\_Code \leq 127$.

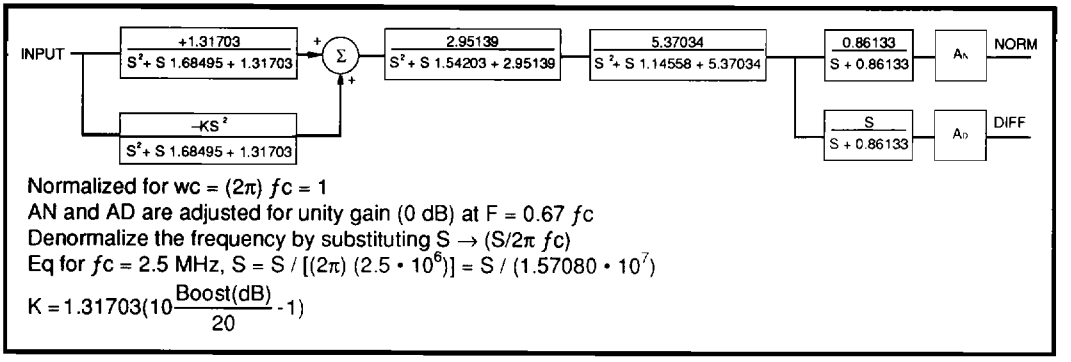

FIGURE 1: Normalized Transfer Function of the SSI 32F8130/8131

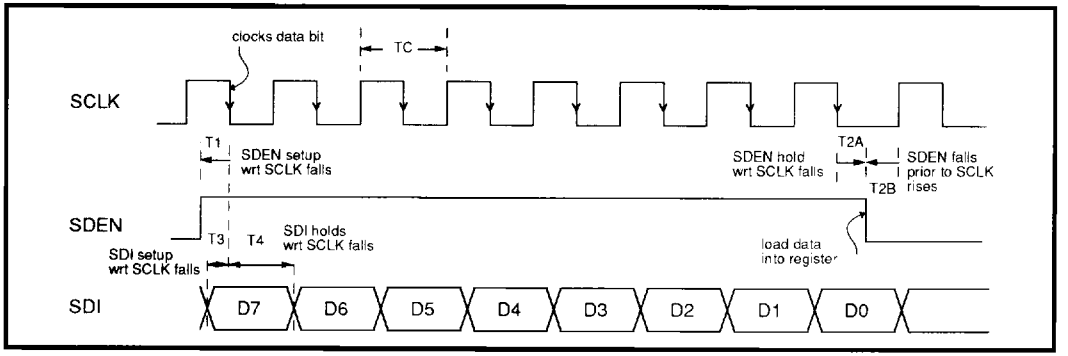

FIGURE 2: Serial Port Timing Relationship

Note:
The serial data enable function of the SSI 32F8130 and that of the SSI 32F8131 are of opposite polarity.

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TABLE 1: Data Packet Fields

	ADDRESS BITS				USAGE	DATA BITS			
	D7	D6	D5	D4		D3	D2	D1	D0
R0	X	0	0	0	S - MSB REGISTER	X	S6	S5	S4
R1	X	0	0	1	S - LSB REGISTER	S3	S2	S1	S0
R2	X	0	1	0	F - MSB REGISTER	X	F6	F5	F4
R3	X	0	1	1	F - LSB REGISTER	F3	F2	F1	F0

X = Don't care bit.

PIN DESCRIPTION

NAME	DESCRIPTION
VIN+, VIN–	DIFFERENTIAL FILTER INPUTS. The input signals must be AC coupled to these pins.
VO_NORM+, VO_NORM–	DIFFERENTIAL NORMAL OUTPUTS. The output signals must be AC coupled to the load.
VO_DIFF+ VO_DIFF–	DIFFERENTIAL DIFFERENTIATED OUTPUTS. These outputs should be AC coupled to the load.
PWR_ON	POWER ON. A TTL high logic level enables the chip. A low level or open circuit puts the chip into a low power state.
$\overline{\text{SDEN}}$ (8130) $\overline{\text{SDEN}}$ (8131)	SERIAL DATA ENABLE. An active level allows SCLK to clock data into the shift register via the SDI input. An inactive level latches the register data and issues the information to the appropriate circuitry. Active level for SSI 32F8130 is HIGH, for SSI 32F8131 is LOW.
SCLK	SERIAL CLOCK. Negative edge triggered clock input for serial register.
SDI	SERIAL DATA INPUT.
VCA	ANALOG +5 VOLT SUPPLY.
VCD	DIGITAL +5 VOLT SUPPLY.
AGND	ANALOG GROUND.
DGND1 DGND2	DIGITAL GROUND.
VFP	CUTOFF FREQUENCY PROGRAMMING REFERENCE. A resistor of 8.25 kΩ should be connected between this pin and AGND.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may permanently damage the device.

PARAMETER	RATING
Storage Temperature	-65 to +150°C
Junction Operating Temperature, Tj	+130°C
Supply Voltage, VCC	-0.5 to 7V
Voltage Applied to Inputs*	-0.5 to VCCV
T1 Lead Temperature (1/16" from case for 10 seconds)	260°C

* Analog input signals of this magnitude shall not cause any change or degradation in filter performance after signal has returned to normal operating range.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATING
Supply voltage, VCC	4.50 < VCC < 5.50V
Ambient Temperature	0 < Ta < 70°C
Tj Junction Temperature	0 < Tj < 130°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified recommended operating conditions apply. F_Code = 64, S_Code = 0.

PARAMETER		CONDITIONS		MIN	NOM	MAX	UNIT
Idle Mode Current						1	mA
Isupply					60	70	mA
Power Dissipation		PWR_ON ≤ 0.8V				6	mW
		PWR_ON ≥ 2.0V			303	385	mW
Idle to Active Mode Recovery Time						50	µs
Serial port program to output response time						50	µs
DC Characteristics							
VIH	High Level Input Voltage	TTL input		2			V
VIL	Low Level Input Voltage					0.8	V
IIH	High Level Input Current	VIH = 2.7V				25	µA
IIL	Low Level Input Current	VIL = 0.4V		-1.5			mA
Filter Characteristics							
fc	Filter Cutoff Frequency	12 < F_Code < 127					
		SSI 32F8130		0.285		2.2	MHz
		SSI 32F8131		0.15		1.4	MHz
FCA	Filter *fc* Accuracy	over *fc* range	32F8130	-12		+12	%
			32F8131	-10		+10	%
Cutoff Resolution		$\text{Resolution} = \frac{\text{Max fc}}{127}$	32F8130		17		kHz
			32F8131		11		kHz
AO	VO_NORM Diff Gain	F = 0.67 *fc*	32F8130	0.7		1.1	V/V
			32F8131	0.8		1.2	V/V
AD	VO_DIFF Diff Gain	F = 0.67*fc*	32F8130	0.8 AO		1.15 AO	V/V
			32F8131	1.0 AO		1.2 AO	V/V
FB	Frequency Boost at *fc* (32F8130)	FB(dB) = 20 log [0.0145 • S_Code + 1] 0 ≤ S_Code ≤ 127		0		9	dB
	(32F8131)	FB(dB) = 20 log [0.0173 • S_Code + 1] 0 ≤ S_Code ≤ 127		0		10	dB
FBA	Frequency Boost Accuracy	S_Code = 127		-1.5		+1.5	dB
TGD0	Group Delay Variation Without Boost	0.2 *fc* to *fc*	32F8130	-2.5		+2.5	%
			32F8131	-2		+2	%
		fc to 1.75 *fc*		-3		+3	%
TGDB	Group Delay Variation With Boost	0.2 *fc* to *fc*	32F8130	-2.5		+2.5	%
			32F8131	-2		+2	%
		fc to 1.75 *fc*		-3		+3	%
Boost Resolution				0.25			dB
VOF_N	Filter Output Dynamic Range	THD = 1% max, Normal Output		1			Vp-p

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ELECTRICAL CHARACTERISTICS (continued)
Unless otherwise specified recommended operating conditions apply. F_Code = 64, S_Code = 0.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Filter Characteristics (continued)					
VOF_D Filter Output Dynamic Range	THD = 1% max, Differentiated Output	1			Vp-p
RIN Filter Diff Input Resistance		3.0	4.0	5.0	kΩ
CIN Filter Input Capacitance			3.0		pF
EOUT Output Noise Voltage (VO_NORM)	BW = 100 MHz, 50Ω input, 0 dB Boost		1.2	1.9	mVRms
	fc = Max fc, max Boost		1.4	2.0	mVRms
EOUT Output Noise Voltage (VO_DIFF)	BW = 100 MHz, 50Ω input, 0 dB Boost		2.1	2.7	mVRms
	fc = Max fc, max Boost		2.5	3.4	mVRms
IO– Filter Output Sink Current		1.0			mA
IO+ Filter Output Source Current		3.0			mA
RO Filter Output Resistance (Single ended)	Output source current, IO+ = 1 mA		50	70	Ω
T1 SDEN Set-up WRT SCLK Falls		10		TC/2-10	ns
T2A SDEN Hold WRT SCLK Falls		10		TC/4	ns
T2B SDEN Falls (rises for 8131) prior to SCLK rises		25			ns
T3 SDI Set-up WRT SCLK Falls		25			ns
T4 SDI Hold WRT SCLK Falls		25			ns
SCLK Period, TC		100			ns
Power Supply Rejection Ratio VO_NORM	100 mVp-p from 10 kHz to 10 MHz on VCA, VCD	30	40		dB
Power Supply Rejection Ratio VO_DIFF		20	30		dB
Common Mode Rejection Ratio VO_NORM	Vin = 0VDC + 10 mVp-p from 10 kHz to 10 MHz	30	40		dB
Common Mode Rejection Ratio VO_DIFF		20	30		dB
Bias: VO_NORM±	VCC = 5V	2.40	2.75	3.10	V
Vin±		2.20	2.35	2.80	V
VO_DIFF±		2.40	2.75	3.10	V
Normal Output Offset Variation	F_Code switched from 12-127	-200		200	mV
Differentiated Output Offset Variation	F_Code switched from 12-127	-200		200	mV

TABLE 1: Calculations (Typical change in f-3 dB point with boost)

Boost (dB)	Gain@fc (dB)	Gain@ peak (dB)	$f$peak/fc	f-3dB/fc	K
0	-3	0.00	no peak	1.00	0
1	-2	0.00	no peak	1.21	0.16
2	-1	0.00	no peak	1.51	0.34
3	0	0.15	0.70	1.80	0.54
4	1	0.99	1.05	2.04	0.77
5	2	2.15	1.23	2.20	1.03
6	3	3.41	1.33	2.33	1.31
7	4	4.68	1.38	2.43	1.63
8	5	5.94	1.43	2.51	1.97
9	6	7.18	1.46	2.59	2.40
10	7	8.40	1.48	2.66	2.85

Notes: 1. fc is the original programmed cutoff frequency with no boost

2. f-3 dB is the new -3 dB value with boost implemented

3. $f$peak is the frequency where the amplitude reaches its maximum value with boost implemented

i.e., fc = 1 MHz when boost = 0 dB

if boost is programmed to 5 dB then f-3 dB = 2.20 MHz

$f$peak = 1.23 MHz

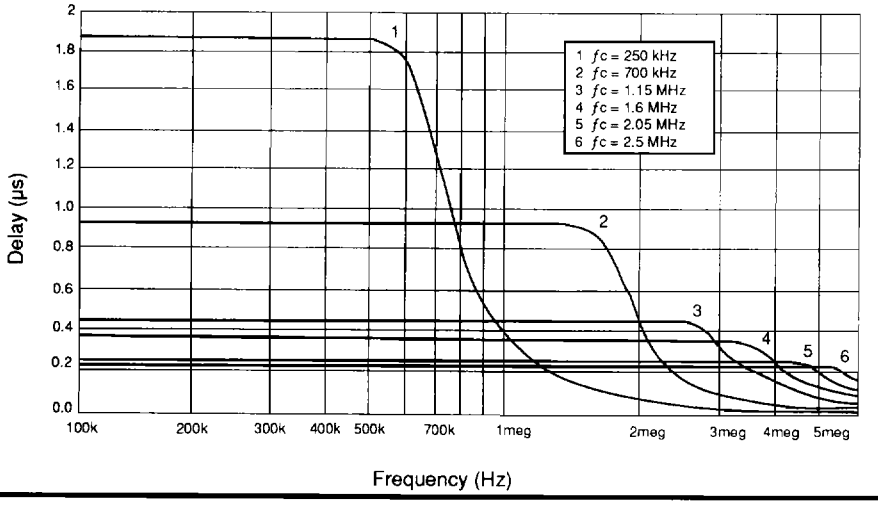

FIGURE 3: Typical Normal/Differentiated Output Group Delay Response

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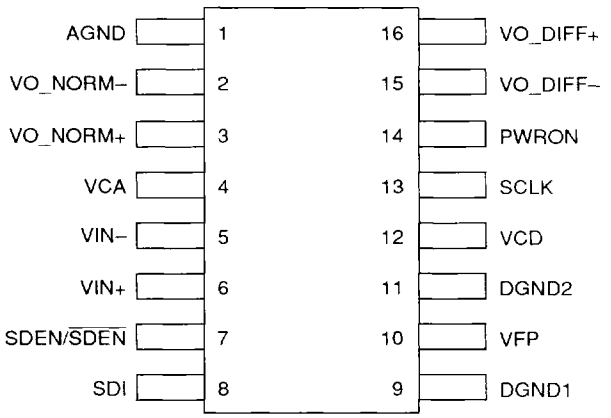
PACKAGE PIN DESIGNATIONS
(Top View)

THERMAL CHARACTERISTICS: θjA

16-Lead SOL	100° C/W



16-Lead SOL

SSI 32F8130: Lead 7 = SDEN
SSI 32F8131: Lead 7 = $\overline{SDEN}$

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32F8130 16-Lead SOL	32F8130-CL	32F8130-CL
SSI 32F8131 16-Lead SOL	32F8131-CL	32F8131-CL

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