2EL / 2DL M.2 Module Datasheet (EAR00409 / EAR00463 / EAR00464 / EAR00422 / EAR00480 / EAR00481)

- Wi-Fi 6, 802.11 a/b/g/n/ac/ax
- Bluetooth 5.3 BR/EDR/LE
- IEEE802.15.4
- SDIO 3.0 interface, SDR50@100MHz
- Chipset: NXP IW612

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Table of Contents

1 Document Information

This document applies to the following products.

Product Name	*Type Number*	*Murata Module*	*Chipset*	*Product Status*
2EL M.2 Module, rev A1	EAR00409 / EAR00463 / EAR00464	LBES5PL2EL-923	NXP IW612	Initial Production
2DL M.2 Module, rev A1	EAR00422 / EAR00480 / EAR00481	LBEE5PL2DL-921	NXP IW611	Initial Production

This table below lists the product differences. All products are not stocked. Consult Embedded Artists for availability and lead time.

Type Number	*Product Name*	*IEEE 802.15.4*	*Antenna*	*Packaging*
EAR00409	2EL M.2 Module	Yes	On-board antenna	Individual packing for evaluation
EAR00463	2EL M.2 Module	Yes	On-board antenna	Tray packing
EAR00464	2EL M.2 Module	Yes	External antenna via u.fl.connectors	Tray packing
EAR00422	2DL M.2 Module	No	On-board antenna	Individual packing for evaluation
EAR00480	2DL M.2 Module	No	On-board antenna	Tray packing
EAR00481	2DL M.2 Module	No	External antenna via u.fl.connectors	Tray packing

1.1 Revision History

Revision	*Date*	*Description*
PA1	2022-07-01	First version.
PA2	2023-03-03	Added information about orderable products.
PA3	2023-12-07	Adding 2DL M.2. Corrected spelling.
PA4	2024-08-05	Added version difference information. Minor corrections.

2 Introduction

This document is a datasheet that specifies and describes the *2EL / 2DL M.2 module* mainly from a hardware point of view.

The main component in the design is Murata's 2EL module (full part number: LBES5PL2EL-923) or 2DL module (full part number: LBEE5PL2DL-921), which in turn is based on the NXP IW612/IW611 chipset, respectively. The 2EL module enables Wi-Fi, Bluetooth, Bluetooth Low Energy (LE) and IEEE802.15.4 communication. The 2DL module has the same functionality except IEEE802.15.4, which has been removed.

There are multiple application areas for the 2EL / 2DL M.2 Module:

- Industrial and Buildings automation
- Asset management
- IoT applications
- Smart home: Voice assist device, smart printer, smart speaker, home automation gateway, and IP camera
- Retail/POS
- Healthcare and medical devices
- Smart city
- and many more…

2.1 Benefits of Using an M.2 Module to get Wireless Connectivity

There are several benefits to use an *M.2 module* to add connectivity to an embedded design:

- Drop-in, certified solution!
- Modular and flexible approach to evaluate different Wi-Fi / BT / 802.15.4 solutions - with different trade-offs around performance, cost, power consumption, longevity, etc.
- Access to maintained software drivers (Linux and SDK) with responsive support from Murata.
- Supported by Embedded Artists' Developer's Kits for i.MX RT/8/9 development, including advanced debugging support on carrier boards
- Futureproofing the design – easy to replace with a newer module in the future
- One component to buy, instead of 40+
- No RF expertise is required
- Developed in close collaboration with Murata

2.2 More M.2 Related Information

For more information about the M.2 standard and Embedded Artists' adaptation, see: M.2 Primer

For more general information about the M.2 standard, see: https://en.wikipedia.org/wiki/M.2

The official M.2 specification (PCI Express M.2 Specification) is available from: www.pcisig.com

2.3 ESD Precaution and Handling

Please note that the M.2 module come without any case/box and all components are exposed for finger touches – and therefore extra attention must be paid to ESD (electrostatic discharge) precaution, for example use of static-free workstation and grounding strap. Only qualified personnel shall handle the product.

Make it a habit always to first touch the mounting hole (which is grounded) for a few seconds with both hands before touching any other parts of the boards. That way, you will have the same potential as the board and therefore minimize the risk for ESD.

In general, touch as little as possible on the boards to minimize the risk of ESD damage. The only reasons to touch the board are when mounting/unmounting it on a carrier board.

Note that Embedded Artists does not replace modules that have been damaged by ESD.

2.4 Product Compliance

Visit Embedded Artists' website at http://www.embeddedartists.com/product_compliance for up-to-date information about product compliances such as CE, UKCA, RoHS2/3, Conflict Minerals, REACH, etc.

3 Specification

This chapter lists some of the more important characteristics of the M.2 module, but it is not a full specification of performance and timing. The main component in the design is NXP's 2EL / 2DL module (full part number: LBES5PL2EL-923 / LBEE5P2DL-921), which in turn is based around NXP's IW612/IW611 chipset.

For a detailed specification, see the LBES5PL2EL product page at Murata:
https://www.murata.com/products/connectivitymodule/wi-fi-bluetooth/overview/lineup/type2el
For a full specification, see Murata's 2EL Module (LBES5PL2EL) product page:
https://www.murata.com/products/productdata/8819414302750/TYPE2EL.pdf

For a detailed specification, see the LBEE5PL2DL product page at Murata:
https://www.murata.com/products/connectivitymodule/wi-fi-bluetooth/overview/lineup/type2dl
For a full specification, see Murata's 2DL Module (LBEE5PL2DL) product page:
https://www.murata.com/products/productdata/8821458370590/TYPE2DL.pdf

Module / Chipset	
Murata module	LBES5PL2EL-923 or LBEE5PL2DL-921
Chipset	NXP IW612 / IW611

Wi-Fi	
Standards	802.11a/b/g/n/ac/ax SISO, Wi-Fi 6
Network	uAP and STA dual mode
Frequency	2.4GHz and 5 GHz band
Data rates	601 Mbps
Host interface	SDIO 3.0, SDR12@24MHz, SDR25@50MHz, SDR50@100MHz, DDR50@50MHz

Bluetooth	
Standards	5.3 BR/EDR/LE, 2Mbps PHY
Power Class	Class 1.5
Host interface	4-wire UART@4MBaud
Audio interface	PCM for audio

IEEE802.15.4	**Only present on 2EL M.2**
Standards	IEEE 802.15.4-2015 compliant supporting Thread in 2.4 GHz band
PA	Integrated high power PA up to +20 dBm transmit power
Host interface	SPI

Powering			
Operating conditions on supply voltage to M.2 module	**Min**	**Typ**	**Max**
	0.0V minimum	3.3V	3.46V

		3.15V operating and RF specification
Absolute maximum rating on supply voltage to M.2 module **Note: Do not exceed minimum or maximum voltage. Module will be permanently damaged above this limit!**		**Min** 0.0V **Max** 3.63V
Peak current	1050 mA max	The power supply must be designed for this peak current, which typically happen during the startup calibration process.
Receive mode current (WLAN)	TBD mA typical max	Note that current consumption varies widely between different operational modes.
Transmit mode current (WLAN)	TBD mA typical max	Note that current consumption varies widely between different operational modes.

Environmental Specification	
Operational Temperature	-40 to +85 degrees Celsius
Storage Temperature	-40 to +85 degrees Celsius
Relative Humidity (RH), operating and storage	10 - 90% non-condensing

3.1 Power Up Sequence

The supply voltage shall not rise (10 - 90%) faster than 40 microseconds and not slower than 100 milliseconds.

Chipset signals PD_N (M.2 signal W_DISABLE1#) must be held low for at least 1 milliseconds after supply voltage has reached specification level before pulled high.

3.2 External Sleep Clock

The sleep clock signals can be applied to a powered and unpowered M.2 module.

Clock Specification	
Frequency	32.768 kHz
Frequency accuracy	±205 ppm including initial tolerance, aging, temperature, etc.
Duty cycle	20 - 80%
Phase noise requirement	-125 dBc/Hz typical (measured at 100kHz)
Clock jitter	1.5 ns typical (RMS)
Voltage level	3.3V logic, according to M.2 standard

3.3 Mechanical Dimensions

The M.2 module is of type: 2230-D5-E according to the M.2 nomenclature. This means width 22 mm, length 30mm (without trace antenna), top and bottom side component height 1.5 mm and key-E connector. The table below lists the different dimensions and weight.

M.2 Module Dimension	Value (±0.15 mm)	Unit
Width	22	mm
Height, with pcb trace antenna Height, without pcb trace antenna	44 30	mm mm
PCB thickness	0.8	mm
Maximum component height on top side	1.5	mm
Maximum component height on bottom side	1.5	mm
Ground hole diameter	3.5	mm
Plating around ground hole, diameter	5.5	mm
Module weight	1.5 ±0.5 gram	gram

Embedded Artists has added a non-standard feature to the 2230 M.2 modules designed together with Murata, NXP and Infineon (former Cypress). The pictures below illustrate the how the standard module size has been extended by 14 mm in the length direction to include a pcb trace antenna.

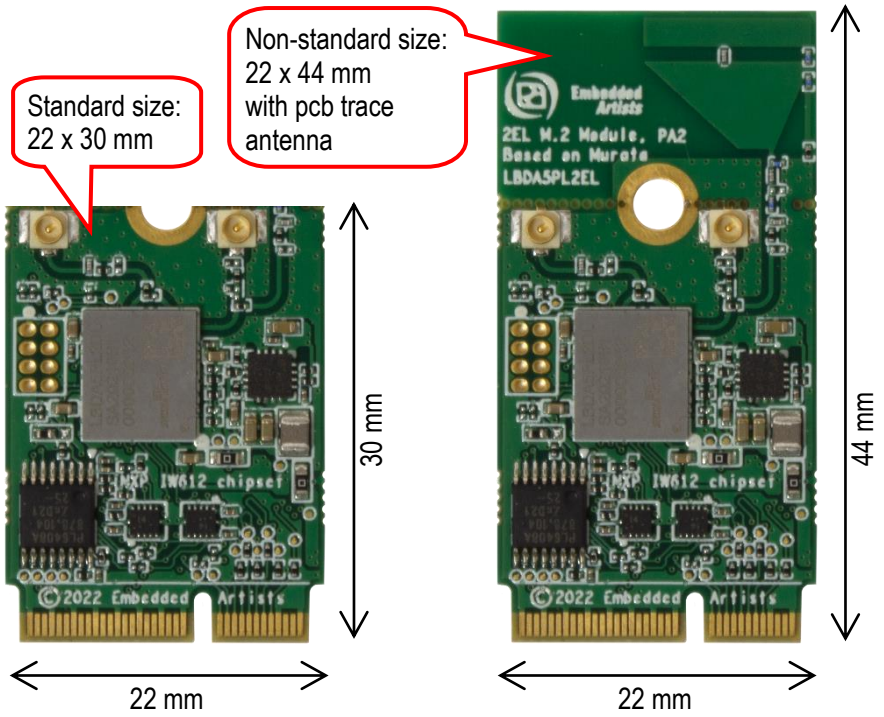


Figure 1 – M.2 Module with, and without, PCB Trace Antenna

The picture below gives dimensions for the grounded center (half) hole and the u.fl. antenna connector.

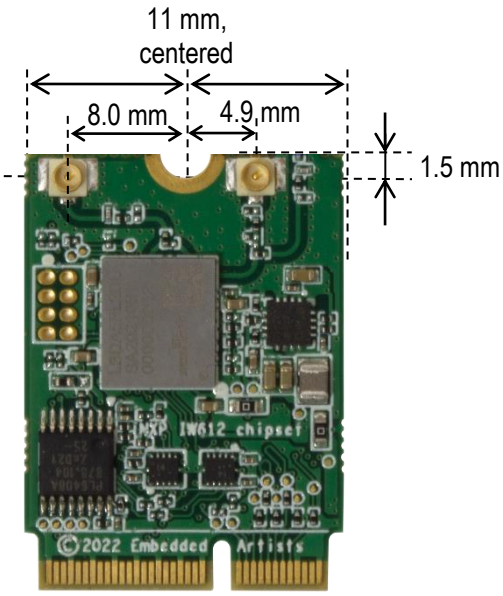


Figure 2 – M.2 Module Without Trace Antenna

3.4 M.2 Pinning

This section presents the pinning used for the M.2 module. It is essentially M.2 Key-E compliant with extensions to support the IEEE802.15.4 functionality (on the 2EL M:2, not the 2DL M.2). The pin assignment for specific control has been jointly defined by Embedded Artists, Murata, NXP and Infineon (former Cypress).

The picture below illustrates the edge pin numbering. It starts on the right edge and alternates between top and bottom side. The removed pads in the keying notch count (but are obviously non-existing).

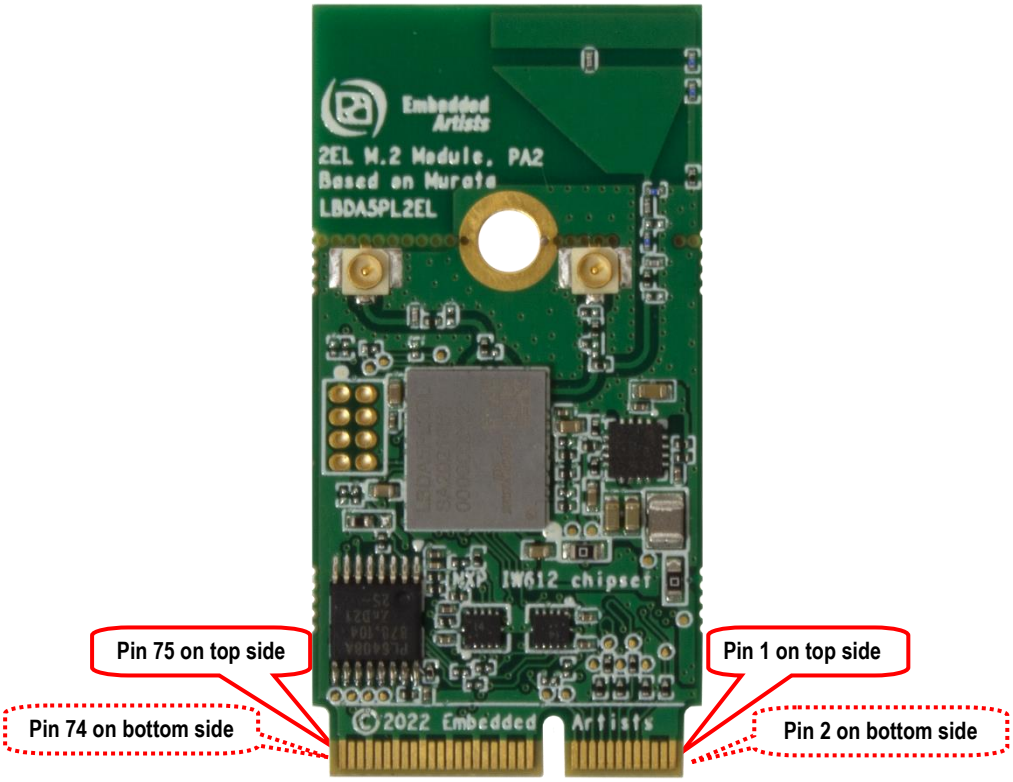


Figure 3 – M.2 Module Pin Numbering

The Wi-Fi interface use the SDIO interface. The Bluetooth interface use the UART interface for control and PCM interface for audio. The IEEE802.15.4 interface use a non-standard SPI interface. The table below lists the pin usage for the 2EL M.2 modules. The column "When is signal needed" signals four different categories:

- Always: These signals shall always be connected.
- Wi-Fi SDIO: These signals shall always be connected when the Wi-Fi interface is used.
- Bluetooth: These signals shall always be connected when the Bluetooth interface is used.
- IEEE802.15.4: These signals shall always be connected when the IEEE802.15.4 interface is used (on the 2EL M:2, not the 2DL M.2)
- Optional: These signals are optional to connect.

Pin #	Side of pcb	M.2 Name	Voltage Level and Signal Direction	When is signal needed	Note
1	Top	GND	GND	Always	Connect to ground
2	Bottom	3.3 V		Always	Power supply input. Connect to stable, low-noise 3.3V supply.
3	Top	USB_D+			Not connected.
4	Bottom	3.3 V		Always	Power supply input. Connect to stable, low-noise 3.3V supply.
5	Top	USB_D-			Not connected.
6	Bottom	LED_1#			Not connected.
7	Top	GND	GND	Always	Connect to ground.
8	Bottom	PCM_CLK	1.8V I/O	Bluetooth audio	For Bluetooth audio interface: PCM_CLK Connected to 2EL/2DL module, signal GPIO_4, pin 57
9	Top	SDIO CLK	1.8V Input to M.2	Wi-Fi	For Wi-Fi SDIO interface: SDIO_CLK Connected to 2EL/2DL module, signal SD_CLK, pin 44
10	Bottom	PCM_SYNC	1.8V I/O	Bluetooth audio	For Bluetooth audio interface: PCM_SYNC Connected to 2EL/2DL module, signal GPIO_7, pin 61
11	Top	SDIO CMD	1.8V I/O	Wi-Fi	For Wi-Fi SDIO interface: SDIO_CMD Connected to 2EL module, signal SD_CMD, pin 42 Note: Require an external 10-100K ohm pullup
12	Bottom	PCM_OUT	1.8V output from M.2	Bluetooth audio	For Bluetooth audio interface: PCM_OUT Connected to 2EL/2DL module, signal GPIO_5, pin 59
13	Top	SDIO DATA0	1.8V I/O	Wi-Fi	For Wi-Fi SDIO interface: SDIO_D0 Connected to 2EL/2DL module, signal SD_DATA_0, pin 48 Note: Require an external 10-100K ohm pullup
14	Bottom	PCM_IN	1.8V input to M.2	Bluetooth audio	For Bluetooth audio interface: PCM_IN Connected to 2EL module, signal GPIO_6, pin 60
15	Top	SDIO DATA1	1.8V I/O	Wi-Fi	For Wi-Fi SDIO interface: SDIO_D1 Connected to 2EL/2DL module, signal SD_DATA_1, pin 45 Note: Require an external 10-100K ohm pullup
16	Bottom	LED_2#			Not connected.
17	Top	SDIO DATA2	1.8V I/O	Wi-Fi	For Wi-Fi SDIO interface: SDIO_D2 Connected to 2EL/2DL module, signal SD_DATA_2, pin 47 Note: Require an external 10-100K ohm pullup
18	Bottom	GND		Always	Connect to ground.
19	Top	SDIO DATA3	1.8V I/O	Wi-Fi	For Wi-Fi SDIO interface: SDIO_D3 Connected to 2EL/2DL module, signal SD_DATA_3, pin 46 Note: Require an external 10-100K ohm pullup
20	Bottom	UART WAKE#	3.3V OD output from M.2	Bluetooth	For Bluetooth UART interface: BT15.4_WAKE_OUT Connected to 2EL/2DL module, via buffer, signal GPIO_19, pin 76 Require an external 10K pullup resistor to 3.3V.
21	Top	SDIO WAKE#	1.8V OD output from M.2	Wi-Fi	For Wi-Fi SDIO interface: WL_WAKE_OUT Connected to 2EL/2DL module, signal GPIO_17, pin 73 Note: Require an external 10K pullup resistor to 1.8V
22	Bottom	UART TXD	1.8V output from M.2	Bluetooth	For Bluetooth UART interface: UART_TXD

					Connected to 2EL/2DL module, signal GPIO11, pin 49
23	Top	SDIO RESET#	1.8V input to M.2	Wi-Fi	Independent reset signal for Wi-Fi functionality. Connected to 2EL/2DL module, signal GPIO_1, pin 63. SDIO RESET#: High = Wi-Fi part of module enabled/internally powered, Low = Wi-Fi disabled/powered down.
24	Key, non existing				
25	Key, non existing				
26	Key, non existing				
27	Key, non existing				
28	Key, non existing				
29	Key, non existing				
30	Key, non existing				
31	Key, non existing				
32	Bottom	UART_RXD	1.8V input to M.2	Bluetooth	For Bluetooth UART interface: BT_UART_RXD Connected to 2EL/2DL module, signal GPIO_10, pin 51
33	Top	GND		Always	Connect to ground.
34	Bottom	UART_RTS	1.8V output from M.2	Bluetooth	For Bluetooth UART interface: BT_UART_RTS Connected to 2EL/2DL module, signal GPIO_9, pin 52
35	Top	PERp0			Not connected.
36	Bottom	UART_CTS	1.8V input to M.2	Bluetooth	For Bluetooth UART interface: BT_UART_CTS Connected to 2EL/2DL module, signal GPIO_8, pin 50
37	Top	PERn0			Not connected.
38	Bottom	VENDOR DEFINED	1.8V input to M.2	IEEE802.15.4	SPI_MOSI, the SPI data signal (from host to M.2) for the IEEE802.15.4/SPI interface. Connected to 2EL module, via buffer, signal GPIO_14, pin 6. The buffer is only enabled if bit 0 of the on-board I2C GPIO expander is set to 1. Not used on 2DL module (but still connected to GPIO_14, pin 6).
39	Top	GND		Always	Connect to ground.
40	Bottom	VENDOR DEFINED	1.8V output from M.2	IEEE802.15.4	SPI_MISO, the SPI data signal (from M.2 to host) for the IEEE802.15.4/SPI interface. Connected to 2EL module, via buffer, signal GPIO_15, pin 7. The buffer is only enabled if bit 0 of the on-board I2C GPIO expander is set to 1. Not used on 2DL module (but still connected to GPIO_15, pin 7).
41	Top	PETp0			Not connected.
42	Bottom	VENDOR DEFINED	1.8V input to M.2	IEEE802.15.4	SPI_SCK, the SPI clock signal (from host to M.2) for the IEEE802.15.4/SPI interface. Connected to 2EL module, via buffer, signal GPIO_12, pin 8. The buffer is only enabled if bit 0 of the on-board I2C GPIO expander is set to 1. Not used on 2DL module (but still connected to GPIO_12, pin 8).
43	Top	PETn0			Not connected.
44	Bottom	COEX3	1.8V I/O	Optional	Connected to 2EL/2DL module, signal GPIO_30, pin 36.

					Note: Signal can be JTAG_TDI
45	Top	GND		Always	Connect to ground.
46	Bottom	COEX_TXD	1.8V I/O	Optional	Connected to 2EL/2DL module, signal GPIO_28, pin 35. Note: Signal can be JTAG_TCK
47	Top	REFCLKp0			Not connected.
48	Bottom	COEX_RXD	1.8V I/O	Optional	Connected to 2EL/2DL module, signal GPIO_29, pin 34. Note: Signal can be JTAG_TMS
49	Top	REFCLKn0			Not connected.
50	Bottom	SUSCLK	3.3V input to M.2	Always	External sleep clock input (32.768kHz) Connected to 2EL/2DL module, via buffer, signal SLP_CLK_IN, pin 3
51	Top	GND		Always	Connect to ground.
52	Bottom	PERST0#			Not connected.
53	Top	CLKREQ0#			Not connected.
54	Bottom	W_DISABLE2#	3.3V input to M.2	Always	Independent reset signal for Bluetooth functionality. Connected to 2EL/2DL module, via buffer, signal GPIO_2, pin 64. W_DISABLE#2: High = Bluetooth part of module enabled/internally powered, Low = Bluetooth disabled/powered down
55	Top	PEWAKE0#			Not connected.
56	Bottom	W_DISABLE1#	3.3V input to M.2	Always	Connected to 2EL/2DL module, via buffer, signal PD_N, pin 10 W_DISABLE1#: High = The module is enabled/internally powered, Low = The modules is disabled/powered down
57	Top	GND		Always	Connect to ground.
58	Bottom	I2C_SDA	1.8V I/O	Always	I2C data signal, connected to on-board GPIO expander, PCAL6408A
59	Top	Reserved			Not connected.
60	Bottom	I2C_CLK	1.8V input to M.2	Always	I2C clock signal, connected to on-board GPIO expander, PCAL6408A
61	Top	Reserved			Not connected.
62	Bottom	ALERT#	1.8V output from M.2	IEEE802.15.4	SPI_INT, interrupt signal from the IEEE802.15.4/SPI interface. Connected to 2EL module, signal GPIO_20, pin 5 Not used on 2DL module (but still connected to GPIO_20, pin 5).
63	Top	GND		Always	Connect to ground.
64	Bottom	RESERVED	1.8V input to M.2	IEEE802.15.4	SPI_SSEL, SPI select signal for the IEEE802.15.4/SPI interface. Connected to 2EL module, via buffer, signal GPIO_13, pin 4. The buffer is only enabled if bit 0 of the on-board I2C GPIO expander is set to 1. Not used on 2DL module (but still connected to GPIO_13, pin 4).
65	Top	Reserved			Not connected.
66	Bottom	UIM_SWP			Not connected.
67	Top	Reserved			Not connected.
68	Bottom	UIM_POWER_SNK			Not connected.

69	Top	GND	Always	Connect to ground.
70	Bottom	UIM_POWER_ SRC/GPIO_1		Not connected.
71	Top	Reserved		Not connected.
72	Bottom	3.3 V	Always	Power supply input. Connect to stable, low-noise 3.3V supply.
73	Top	Reserved		Not connected.
74	Bottom	3.3 V	Always	Power supply input. Connect to stable, low-noise 3.3V supply.
75	Top	GND	Always	Connect to ground.

3.5 On-board I2C GPIO Expander

The IW612 chipsets need several control signals and there is a limited number of available pins in the M.2 standard. To create four output signals and one input signal, there is an on-board I2C GPIO expander, PCAL6408A. It can be accessed at I2C address 0x20 (7-bit address) or 0x40/0x41 (8-bit address).

To maintain driver compatibility between the 2EL M.2 and 2DL M.2 boards, both designs have the same on-board I2C GPIO expander.

The table below lists the usage of the four output signals and one input signal.

Bit	Signal Name	Direction	Usage / Connection
0	SPI_ENABLE	output	0 = The SPI interface of the IW612 chipset is not connected to M.2 pins 38, 40, 42, and 64. The SPI interface can however be accessed via the expansion header, see section 3.10 for details. 1= Connect SPI interface of IW612 chipset to M.2 pins 38, 40, 42 and 64. Signal is not relevant for the 2DL module.
1	IND_RST_15_4	output	Independent reset signal for IEEE802.15.4 Connects to 2EL/2DL module, signal GPIO_24, pin 38 Signal is not relevant for the 2DL module.
2	IND_WAKE_WLAN	output	Wi-Fi wakeup signal from host to IW612/IW611 chipset WL_WAKE_IN Connects to 2EL/2DL module, signal GPIO_16, pin 74
3	IND_WAKE_BT15_4	output	Bluetooth and IEEE802.15.4 wakeup signal from host to IW612 chipset. Connects to 2EL/2DL module, signal GPIO_18, pin 75. Signal is not relevant for the 2DL module.
4	RST_IND	input	Reset indication signal (output) from IW612/IW611 chipset- Connects to 2EL/2DL module, signal GPIO_22, pin 37

3.6 Block Diagram

It can be difficult to understand the internal structure from just ready pin definitions. The block diagram below explains the 2EL M.2 internal structure with blocks instead. One of the I2C-GPIOs is used to control the buffer then enables/disables the SPI interface.

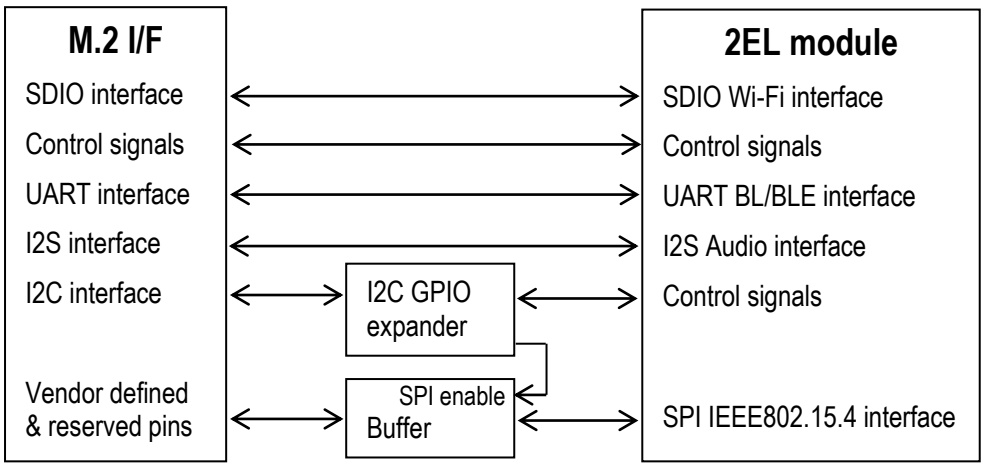


Figure 4 – 2EL M.2 Module Block Diagram

Similarly, the block diagram below explains the 2DL M.2 internal structure. The I2C GPIO expander connects to the same control signal as for the 2EL M.2 board, but the SPI buffer is not present.

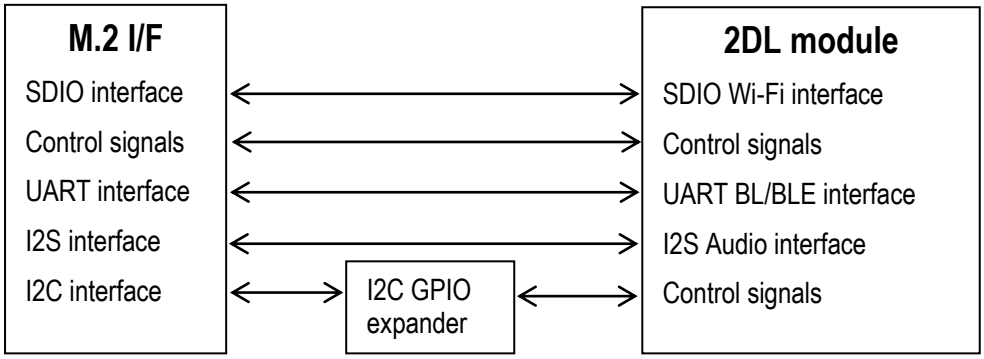


Figure 5 – 2DL M.2 Module Block Diagram

3.7 IEEE802.15.4 Interface (only relevant for 2EL M.2)

The IW612 chipset also implements an IEEE802.15.4 interface, which is a low-rate wireless personal area network (LR-WPAN) that was developed for low-data-rate monitor and control applications and extended-life low-power-consumption uses.

The IEEE802.15.4 functionality is accessed via an SPI interface. There is no standard SPI interface defined in the M.2 standard, but there are Vendor defined and reserved pins. These are used for the SPI interface. The 2EL M.2 module has a buffer that connects/disconnects the SPI interface IW612 chipset to the M.2 pins. This buffer is only enabled if bit 0 of the on-board I2C GPIO expander is set to 1.

Besides accessing the SPI interface with the M.2 pins, the SPI signals are also available via expansion connector JP1, see table below.

M.2 pin / name	JP1 pin	SPI signal	Direction	Connection
38 / VENDOR DEFINED	4	MOSI	Input to M.2	SPI_MOSI, the SPI data signal (from host to M.2) for the IEEE802.15.4/SPI interface.
40 / VENDOR DEFINED	5	MISO	Output from M.2	SPI_MISO, the SPI data signal (from M.2 to host) for the IEEE802.15.4/SPI interface.
42 / VENDOR DEFINED	2	CLK	Input to M.2	SPI_SCK, the SPI clock signal (from host to M.2) for the IEEE802.15.4/SPI interface.
62 / ALERT#	8	INT	Output from M.2	SPI_INT, the SPI interrupt signal (from M.2 to host) for the IEEE802.15.4/SPI interface.
64 / RESERVED	3	SSEL	Input to M.2	SPI_SSEL, SPI select signal for the IEEE802.15.4/SPI interface.

3.8 SDIO Interface

The SDIO interface conforms to the SDIO v3.0 specification, including the UHS-I modes, and is backward compatible with SDIO v2.0.

SDIO bus speed modes	Max SDIO clock frequency	Max bus speed	Signaling voltage according to M.2 specification
DS (Default speed)	25 MHz	12.5 MByte/s	1.8 V
HS (High speed)	50 MHz	25 MByte/s	1.8 V
SDR12	25 MHz	12.5 MByte/s	1.8 V
SDR25	50 MHz	25 MByte/s	1.8 V
SDR50	100 MHz	50 MByte/s	1.8 V
DDR50	50 MHz	50 MByte/s	1.8 V

3.9 Wi-Fi Interface Control

There are two interface configuration pins on the IW612/IW611 chipset. At the time of release, there is only one configuration defined (both pins pulled high); Wi-Fi interface via SDIO, Bluetooth interface via UART and 802.15.4 interface via SPI (802.15.4 only relevant for 2EL M.2). Future driver/firmware release may support other interface combinations. For future reference, the picture below illustrates the location of the controlling resistors.

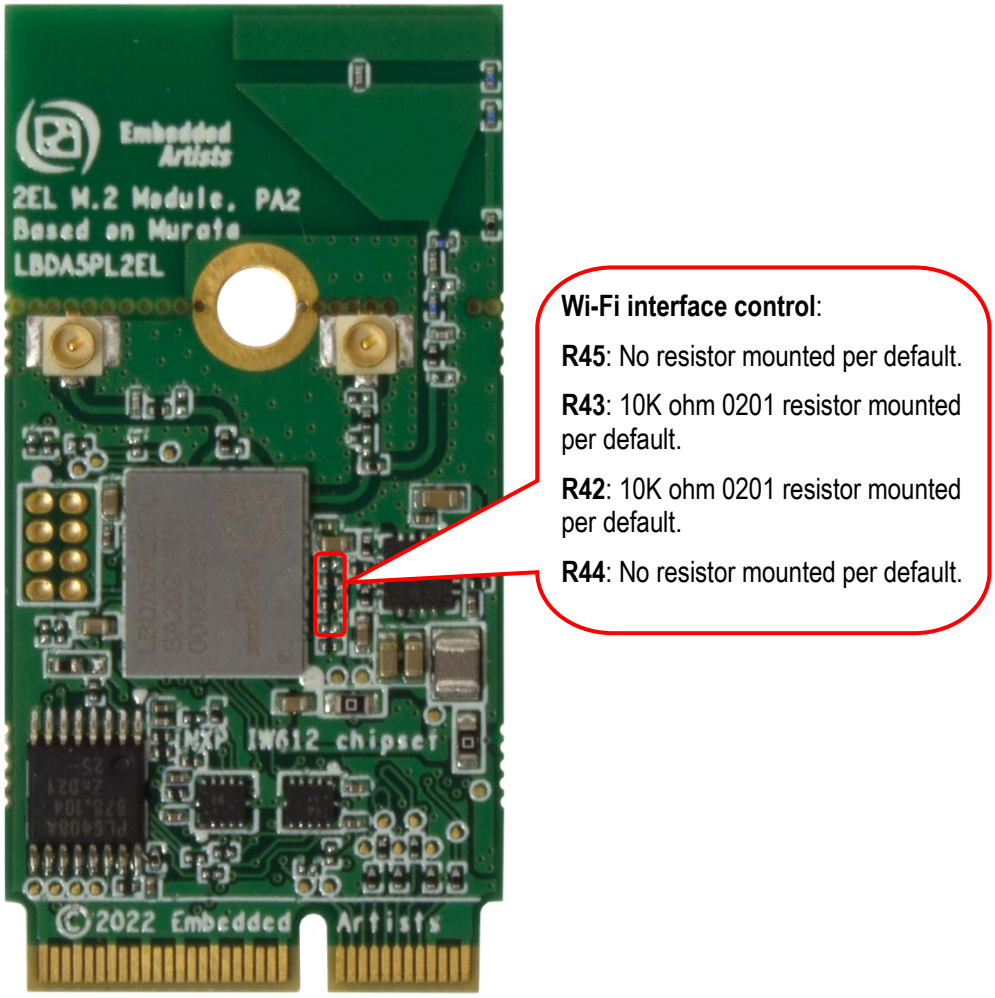


Figure 6 – 2EL/2DL M.2 Module Wi-Fi Interface Control

3.10 Test Points and Expansion Header

There are some test points that can be of interest to probe for SDIO debugging purposes, as illustrated in the picture below. Expansion connector, JP1, allows access to the SPI bus in case the M.2 interface does not support the (non-standard) SPI interface.

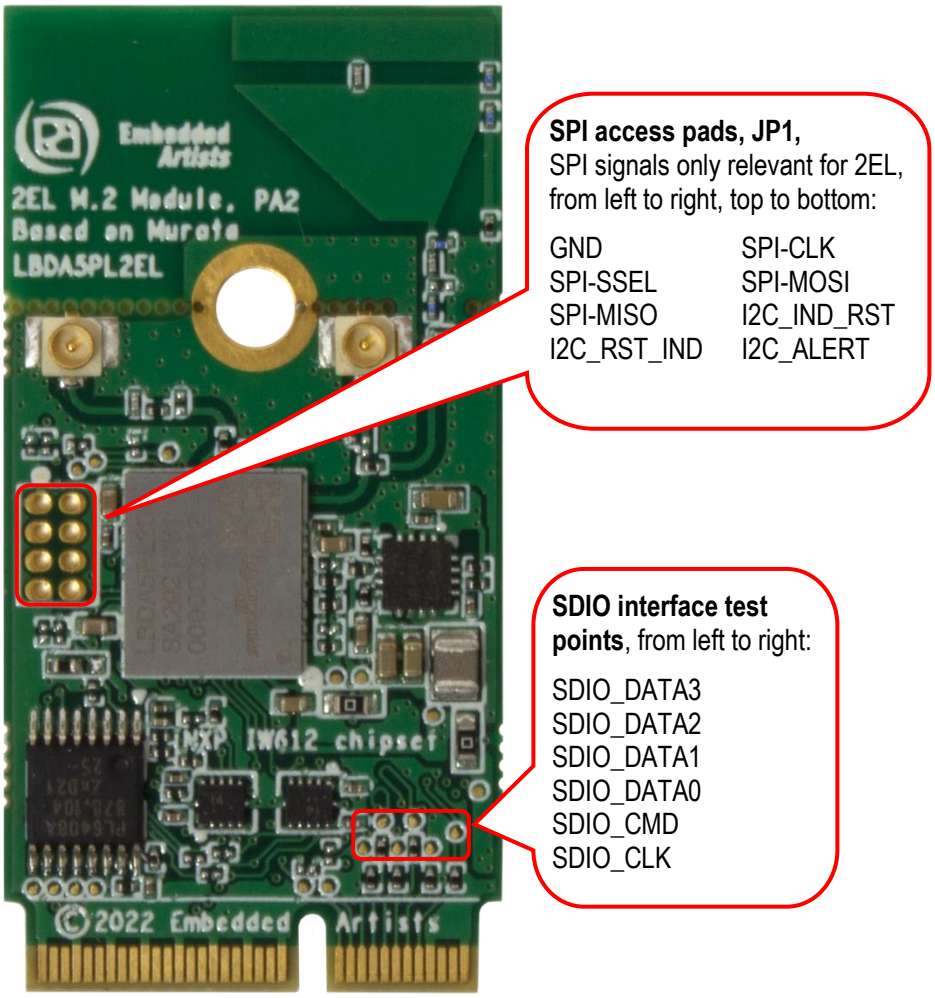


Figure 7 – 2EL/2DL M.2 Module Test Points

The table below lists the SPI signals that are available to access the SPI interface of the IW612 chipset via expansion connector JP1.

JP1 pin	SPI signal	Direction	Connection
1			GND
2	CLK	Input to JP1	SPI_SCK, the SPI clock signal (from host to IW612) for the IEEE802.15.4/SPI interface. Signal is not relevant for the 2DL M.2.
3	SSEL	Input to JP1	SPI_SSEL, SPI select signal for the IEEE802.15.4/SPI

			interface. Signal is not relevant for the 2DL M.2.
4	MOSI	Input to JP1	SPI_MOSI, the SPI data signal (from host to IW612) for the IEEE802.15.4/SPI interface. Signal is not relevant for the 2DL M.2.
5	MISO	Output from JP1	SPI_MISO, the SPI data signal (from IW612 to host) for the IEEE802.15.4/SPI interface. Signal is not relevant for the 2DL M.2.
6	RST	Input to JP1	Reset signal to the IW612/IW611 chipset. Note that the signal is connected to bit 1 of the on-board I2C GPIO expander. This pin must not be driven actively by the I2C GPIO expander. After reset/power cycle, all pins are high impedance, so it should not be a problem unless the I2C GPIO expanders registers are accessed.
7	RST_IND	Output from JP1	Signal from the IW612/IW611 chipset to indicate the reset state.
8	INT	Output from JP1	SPI_INT, the SPI interrupt signal (from IW612 to host) for the IEEE802.15.4/SPI interface. Signal is not relevant for the 2DL M.2.

3.11 Current Consumption Measurements

It is possible to measure the currents of the power supplies to the 2EL/2DL module, AVDD33 and VIO/SD_VIO/AVDD18. AVDD33 is the 3.3V that is supplied directly from the M.2 interface and VIO/SD_VIO/AVDD18 is an on-board generated 1.8V. VIO/SD_VIO/AVDD18 is generated from the supplied 3.3V via a buck dcdc converter. If the supply voltage (3.3V) to the M.2 module is measured it will be both the AVDD33 and VIO/SD_VIO/AVDD18 power consumption that are measured. By measuring currents at the illustrated points below it is possible to measure AVDD33 and VIO/SD_VIO/AVDD18 separately.

Note that zero-ohm resistors are mounted by default. Select a series resistor with as low resistance as possible to keep the voltage drop to a minimum. Keep the drop below 100mV. AVDD33 can be above 1 Amp in peak which means that maximum series resistance is 100 milliOhm for the AVDD33 resistor. The same applies for VIO/SD_VIO/AVDD18. The current can be over 1 Amp in peak, so a suitable resistor is also 100 milliOhm.

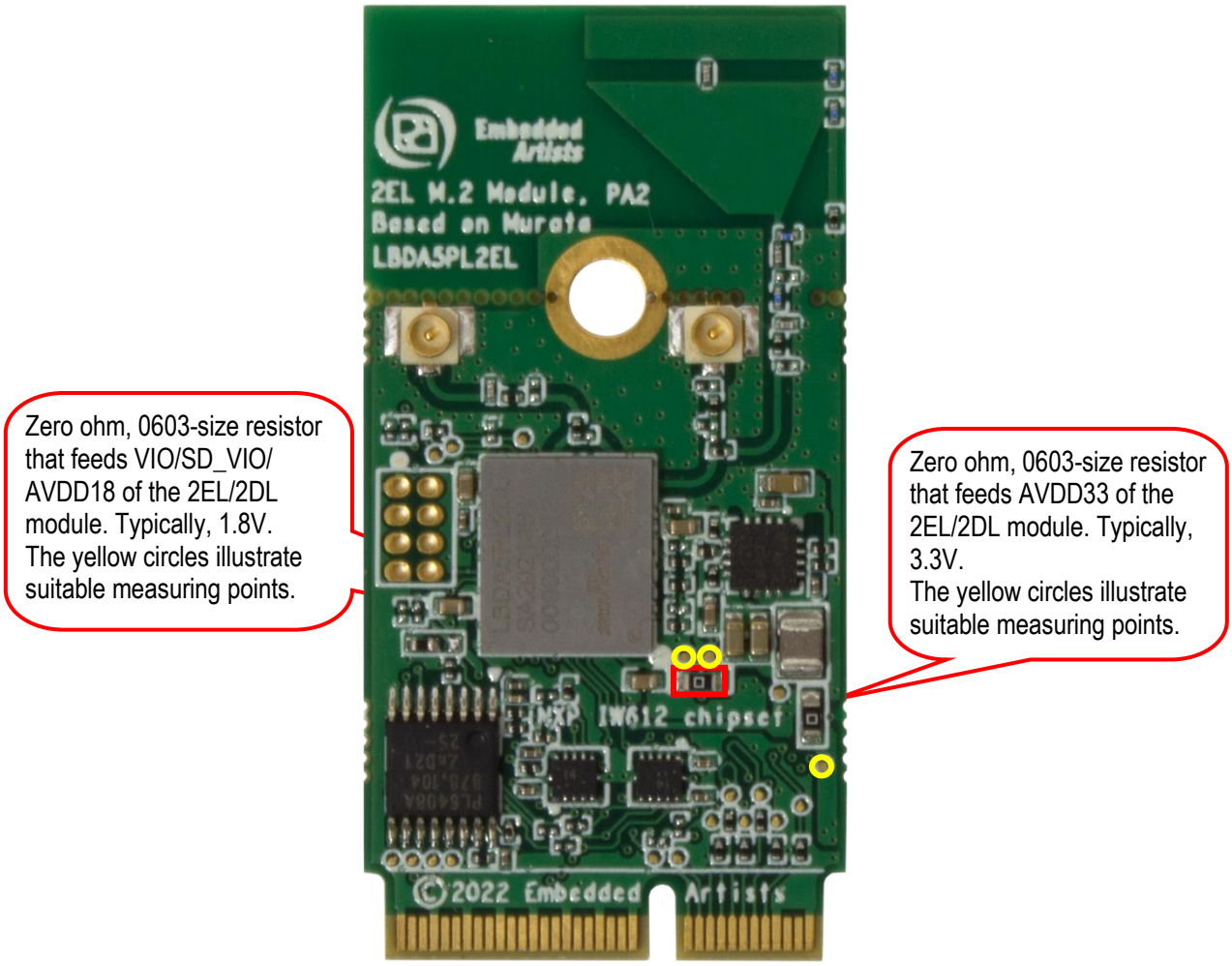


Figure 8 – Current Measurement

3.12 Differences between Revisions

There have been a couple of revisions on the 2EL / 2DL M.2 board design. The reason for this is that the board was used very early in the development cycle of the IW61x chipset, and some specifications have changed during the development. The latest rev A3 is expected to be the final version.

M.2 pin	M.2 pin definition	Board rev PA2	Board rev A	Board rev A1	Board rev A2	Board rev A3
56	W_DISABLE1#	Signal connected to a 3.3V to 1.8V voltage translator based on the NTB0104GU12	Signal connected to a 3.3V to 1.8V voltage translator based on the NTB0104GU12	Signal connected to a 3.3V to 1.8V voltage translator based on the 74AVC4TD245	Signal connected to a 3.3V to 1.8V voltage translator based on the 74AVC4TD245	Signal connected to a 3.3V to 1.8V voltage translator based on the 74AVC4TD245
54	W_DISABLE2#	Signal connected to a 3.3V to 1.8V voltage translator based on the NTB0104GU12	Signal connected to a 3.3V to 1.8V voltage translator based on the NTB0104GU12	Signal connected to a 3.3V to 1.8V voltage translator based on the 74AVC4TD245	Signal connected to a 3.3V to 1.8V voltage translator based on the 74AVC4TD245	Signal connected to a 3.3V to 1.8V voltage translator based on the 74AVC4TD245
50	SUSCLK	Connected to IW61x, pin SLP_CLK_IN	Connected to IW61x, pin SLP_CLK_IN	Connected to IW61x, pin SLP_CLK_IN	Not connected to the IW61x chipset. There is no 32.768KHz input to the chipset.	Not connected to the IW61x chipset. There is no 32.768KHz input to the chipset.
20	UARTWAKE#	Signal comes from IW61x pin GPIO19 via a 1.8V to 3.3V voltage translator (based on the NTB0104GU12)	Signal comes from IW61x pin GPIO19 via a 1.8V to 3.3V voltage translator (based on the NTB0104GU12)	Signal comes from IW61x pin GPIO19 via a 1.8V to 3.3V voltage translator (based on the 74AVC4TD245)	Signal comes from IW61x pin GPIO19 via a 1.8V to 3.3V voltage translator (based on the 74AVC4TD245)	Signal comes from IW61x pin GPIO19 via a 1.8V to 3.3V voltage translator (based on the 74AVC4TD245)
62	#ALERT	Push-pull output. Pin connected directly to IW61x, GPIO20	Push-pull output. Pin connected directly to IW61x, GPIO20	Push-pull output. Pin connected directly to IW61x, GPIO20	Push-pull output. Pin connected directly to IW61x, GPIO20	Open-drain output. There is an open-drain buffer between IW61x, GPIO20 and the M.2 pin
	Idle current when IW61x in power down mode	About 50mW (14.0mA@3.3V)	About 50mW (14.0mA@3.3V)	About 50mW (14.0mA@3.3V)	A few mW	A few mW
	CONFIG_HOST 0/1	0201 resistors	Larger 0603 pads on bottom side	Larger 0603 pads on bottom side	Larger 0603 pads on bottom side	Larger 0603 pads on bottom side
	Test pads				Test pads to access IW61x GPIO0 and GPIO23	Test pads to access IW61x GPIO0 and GPIO23

4 Antenna

This chapter addresses the antenna side of the module. There is an on-board, reference certified pcb trace antenna. This can be used for testing/evaluation purposes, but also for the final product. Also, for testing and evaluation purposes, it is possible to disconnect the on-board antenna and instead use a u.fl. connector to connect an external antenna.

4.1 Mounting and Clearance

Ideally, arrange the M.2 module so that the antenna is located at a corner of the product. Keep plastic case (i.e., non-metallic) away from the antenna area with at least 5 mm clearance (in all directions). Also keep any metal elements (e.g., connectors, battery, etc.) away from the antenna area with at least 5 mm clearance (in all directions). Keep a clearance area under and above the antenna area of at least 7.5 mm, both under and over the PCB.

Human hands or body parts should be kept away (in the normal use case) from the antenna area.

The ground hole in the middle shall be grounded. Use a metal stand-off according to M.2 standard (height suitable for selected M.2 connector) and use metal screw to create a proper ground connection.

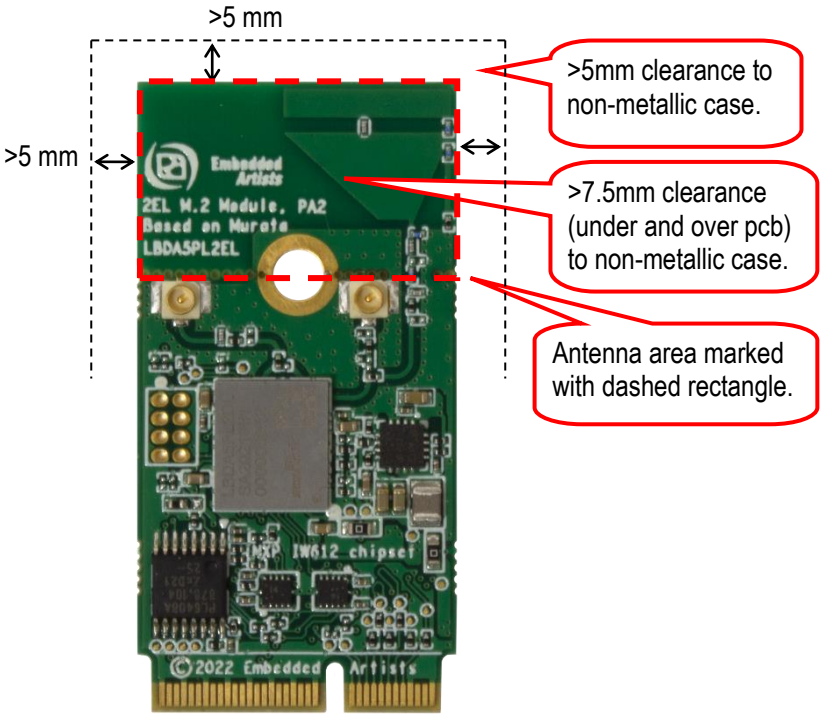


Figure 9 – M.2 Module Clearance Area

4.2 Antenna Connector

The M.2 standard specifies a 1.5 mm outer ring diameter male connector, which is compatible with the Murata MSC and IPEX MHF4 connector specifications. This connector is not used since our M.2 modules also target industrial users, where the Hirose U.FL. connector standard is more commonly used. U.FL. is compatible with the IPEX MHF1 connector specification.

4.3 Overriding on-board PCB Trace Antenna

Per default, the on-board PCB trace antenna is used for the Wi-Fi and Bluetooth interface. The antenna connection from the 2EL module can be redirected to the U.FL. connector by just moving one zero ohm 0201 series resistor, see illustration below. The on-board trace antenna can be left as-is, or the antenna part can be snapped-off.

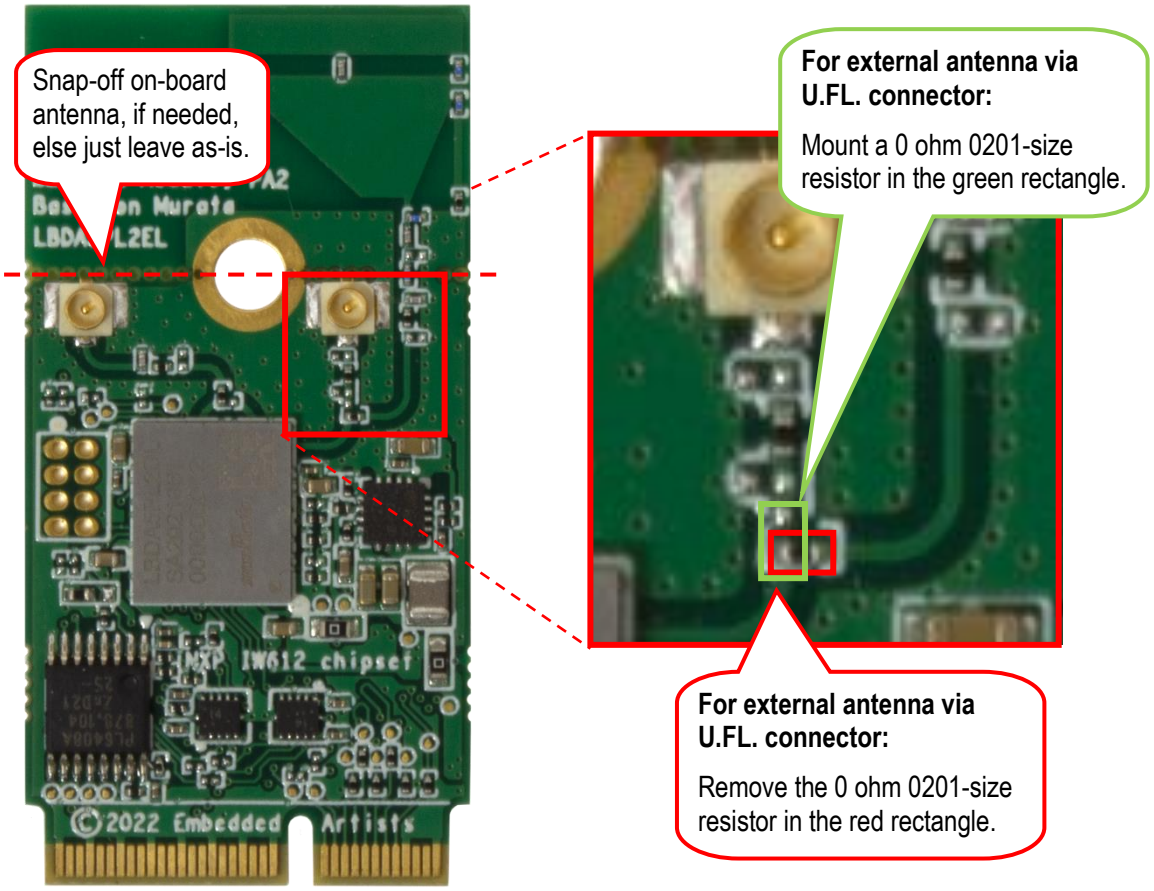


Figure 10 – Rework to Connect U.FL. Connector

4.4 On-board PCB Trace Antenna Performance

The on-board pcb trace antenna type is monopole, certified by Murata.

The table below lists total efficiency:

Measurement condition	Frequency MHz						Total Efficiency in dB		Total Efficiency in %	
	2400	2442	2484	5150	5500	5850	Average 2 GHz band	Average 5 GHz band	Average 2 GHz band	Average 5 GHz band
Certified trace antenna	**-1.0**	**-1.0**	**-0.9**	**-1.3**	**-1.6**	**-1.5**	**-1.0**	**-1.5**	**80.1**	**71.5**

The table below lists peak gain:

Measurement condition	Frequency MHz						Max dBi	
	2400	2442	2484	5150	5500	5850	Max 2 GHz band	Max 5 GHz band
Certified trace antenna	**2.6**	**2.4**	**2.5**	**3.5**	**3.6**	**3.5**	**2.6**	**3.64**

The pictures below illustrate the return loss and efficiency.

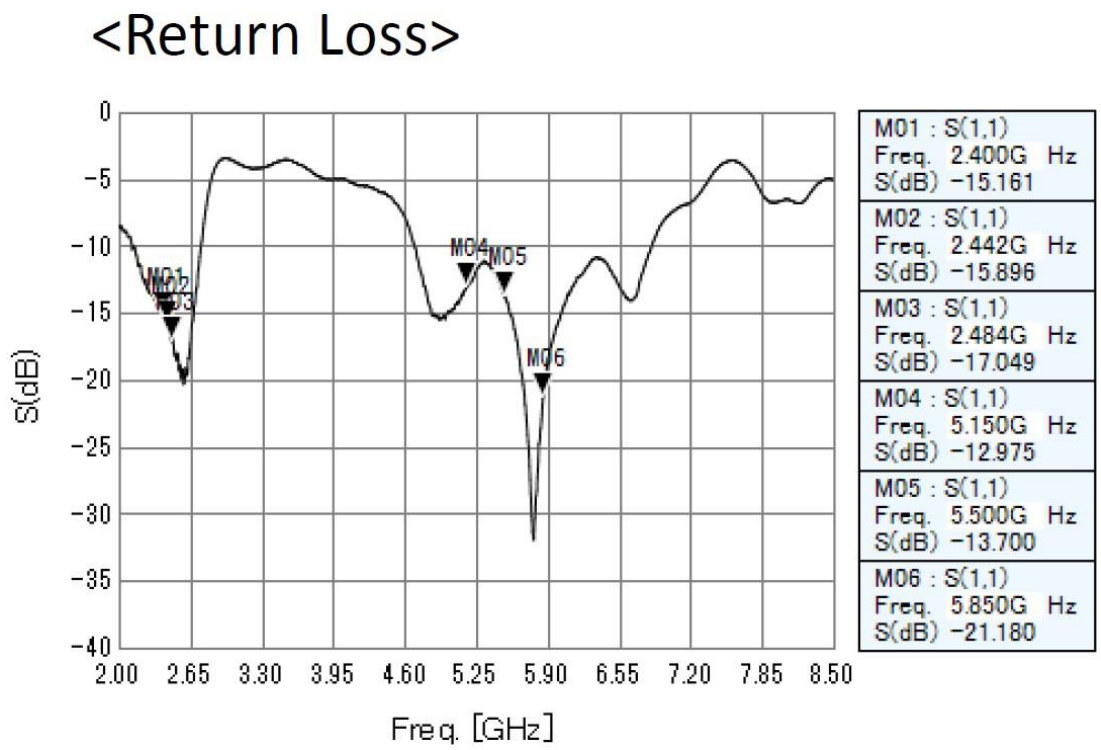


Figure 11 – Return Loss for Certified Trace Antenna

<Efficiency>

[dBi] [dB]

LINEAR POLARIZATION		XY-plane		YZ-plane		ZX-plane		Total Efficiency
		hor.	ver.	hor.	ver.	hor.	ver.	
2400 MHz	MAX.	-1.6	-0.9	2.6	-16.3	-2.2	1.0	
	AVE.	-4.9	-4.6	-2.0	-20.4	-8.3	-0.9	-1.0
2442 MHz	**MAX.**	**-1.6**	**-0.8**	**2.4**	**-15.0**	**-2.0**	**1.1**	
	AVE.	**-5.1**	**-4.6**	**-1.9**	**-19.5**	**-8.3**	**-0.7**	**-1.0**
2484 MHz	MAX.	-1.7	-0.7	2.5	-13.6	-1.7	1.6	
	AVE.	-5.2	-4.5	-1.6	-18.7	-8.2	-0.5	-0.9

[dBi] [dB]

LINEAR POLARIZATION		XY-plane		YZ-plane		ZX-plane		Total Efficiency
		hor.	ver.	hor.	ver.	hor.	ver.	
5150 MHz	MAX.	2.3	0.1	2.2	-11.4	3.5	-0.2	
	AVE.	-4.1	-4.5	-2.0	-19.2	-3.9	-3.9	-1.3
5500 MHz	**MAX.**	**2.3**	**-0.6**	**1.0**	**-12.7**	**3.6**	**-1.8**	
	AVE.	**-4.3**	**-5.0**	**-2.4**	**-20.0**	**-4.3**	**-5.1**	**-1.6**
5850 MHz	MAX.	2.3	-0.7	1.0	-12.9	3.5	-1.6	
	AVE.	-4.1	-5.4	-2.4	-19.8	-4.2	-5.5	-1.5

Figure 12 – Efficiency for Certified Trace Antenna

The directivity measurements are presented below for the 2 GHz and 5GHz bands with the orientation as illustrated below.

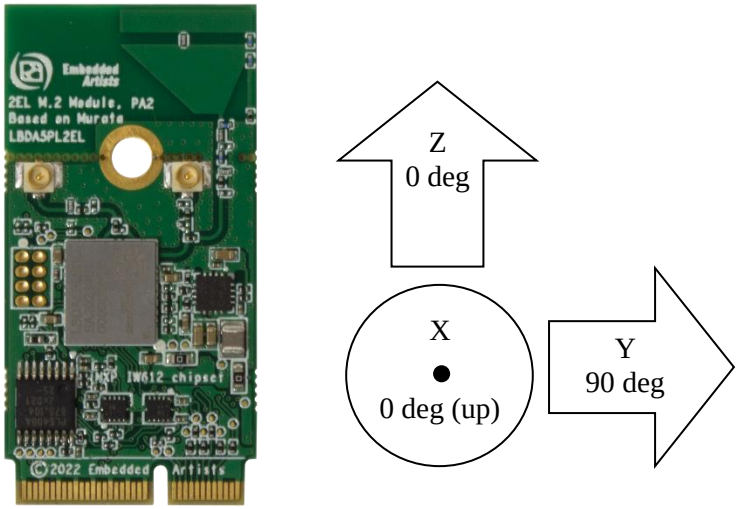
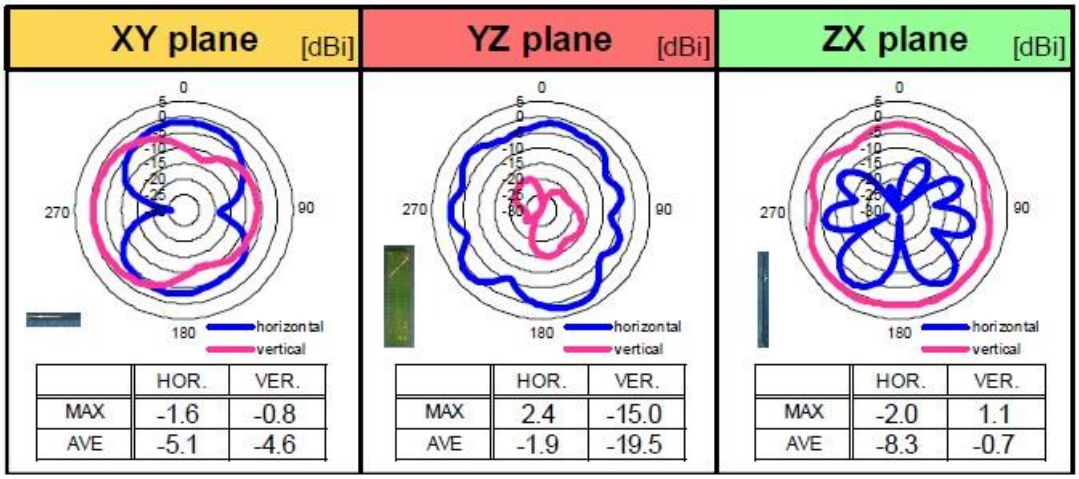


Figure 13 –Plane Orientations

<Directivity>

@2442MHz

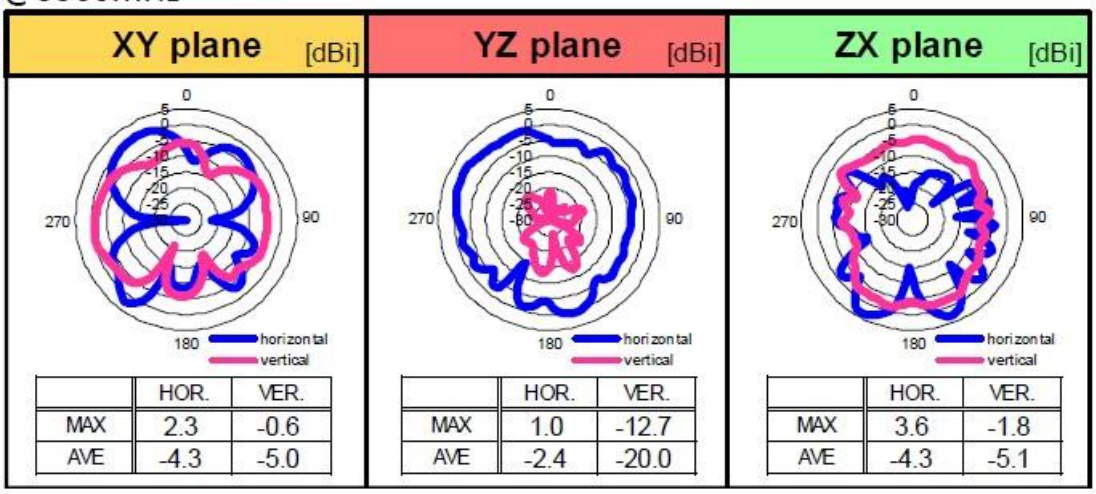


	HOR.	VER.
MAX	-1.6	-0.8
AVE	-5.1	-4.6

	HOR.	VER.
MAX	2.4	-15.0
AVE	-1.9	-19.5

	HOR.	VER.
MAX	-2.0	1.1
AVE	-8.3	-0.7

@5500MHz



	HOR.	VER.
MAX	2.3	-0.6
AVE	-4.3	-5.0

	HOR.	VER.
MAX	1.0	-12.7
AVE	-2.4	-20.0

	HOR.	VER.
MAX	3.6	-1.8
AVE	-4.3	-5.1

Figure 14 – Directivity for Certified Trace Antenna

5 Software and Support

This chapter contains information about software and support.

5.1 Software Driver

The IW612/IW611 chipset does not contain any persistent software. A firmware image must be downloaded by the host at start-up. This is the responsibility of the operating system driver.

There are three different cases, depending on which host processor is used:

1. **Embedded Artists' Computer-on-Modules, (u)COM, as host processor**
   Embedded Artists' Linux BSPs and SDKs for the different (u)COM board contains all drivers available and pre-configured. Everything has been tested and works out-of-the-box on the different iMX Developer's Kits.

iMX Developer's Kit	2EL/2DL M.2 (SDIO) support
iMX93 uCOM	Preliminary support in Linux BSP v6.1.1
iMX8M Mini uCOM	Preliminary support in Linux BSP v6.1.1 No direct IEEE802.15.4 support
iMX8M Nano uCOM	Preliminary support in Linux BSP v6.1.1 No direct IEEE802.15.4 support
iMX8M COM	No
iMX7 Dual COM	No
iMX7 Dual uCOM	No
iMX7ULP uCOM	No
iMX6 Quad COM	No
iMX6 DualLite COM	No
iMX6 SoloX COM	No
iMX6 UltraLite/ULL COM	No
iMX RT1176 uCOM	No
iMX RT1166 uCOM	No
iMX RT1064 uCOM	No
iMX RT1062 OEM	No

2. **Other i.MX based, for example NXP's EVKs**
   Murata has created documentation how to compile the Linux kernel for the NXP EVKs https://wireless.murata.com/products/rf-modules-1/wi-fi-bluetooth-for-nxp-i-mx.html#Linux

3. **Non-i.MX host processor**
   There is no ready-to-go driver exist. Contact Murata to check driver availability on the hardware platform used.

5.2 Support

Embedded Artists supports customers that use our M.2 module in combination with Embedded Artists' Computer-on-Modules, (u)COM, based on NXP's i.MX RT/8/9 families.

For other platforms, support is provided by Murata via their Community Support Forum:
https://community.murata.com/s/topic/0TO5F0000002TLWWA2/connectivity-modules

6 Regulatory

The Murata 2EL/2DL module is reference certified. See the LBES5PL2EL/ LBEE5PL2DL datasheets from Murata for details.

6.1 European Union Regulatory Compliance

EUROPEAN DECLARATION OF CONFORMITY (Simplified DoC per Article 10.9 of the Radio Equipment Directive 2014/53/EU)

This apparatus, namely 2EL/2DL M.2 module (pn EAR00409 / EAR00463 / EAR00464 / EAR00422 / EAR00480 / EAR00481) conforms to the Radio Equipment Directive (RED) 2014/53/EU. The full EU Declaration of Conformity for this apparatus can be found at this location: https://www.embeddedartists.com/products/2el-m-2-module/, see document *2EL M.2 module Declaration of Conformity*, or https://www.embeddedartists.com/products/2dl-m-2-module/, see document *2DL M.2 module Declaration of Conformity*.

The following information is provided per Article 10.8 of the Radio Equipment Directive 2014/53/EU:

(a) Frequency bands in which the equipment operates.

(b) The maximum RF power transmitted.

PN	RF Technology	(a) Frequency Ranges (EU)	(b) Max Transmitted Power
EAR00409 / EAR00463 / EAR00464 / EAR00422 / EAR00480 / EAR00481	Bluetooth BR/EDR/LE	2400 MHz – 2484 MHz	2.6 dBm
EAR00409 / EAR00463 / EAR00464 / EAR00422 / EAR00480 / EAR00481	Wi-Fi IEEE 802.11b/g/n	2400 MHz – 2484 MHz	2.6 dBm
EAR00409 / EAR00463 / EAR00464 / EAR00422 / EAR00480 / EAR00481	Wi-Fi IEEE 802.11a/n/ac/ax	5150 MHz – 5850 MHz	3.64 dBm

The 2EL/2DL M.2 module complies with the Directive 2011/65/EU (EU RoHS 2) and its amendment Directive (EU) 2015/863 (EU RoHS 3).

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