

# MOSFET – Power, Single N-Channel

60 V, 26 A, 24 mΩ

## NVMFS5826NL

### Features

- Small Footprint (5x6 mm) for Compact Design
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low  $Q_G$  and Capacitance to Minimize Driver Losses
- NVMFS5826NLWF – Wettable Flanks Product
- AEC-Q101 Qualified and PPAP Capable
- These are Pb-Free Devices and RoHS Compliant

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit	
$V_{DSS}$	Drain-to-Source Voltage	60	V	
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V	
$I_D$	Continuous Drain Current $R_{\Psi J-mb}$ (Notes 1, 2, 3, 4)	Steady State		
		$T_{mb} = 25^\circ\text{C}$	26	A
$P_D$	Power Dissipation $R_{\Psi J-mb}$ (Notes 1, 2, 3)	$T_{mb} = 100^\circ\text{C}$	19	
		$T_{mb} = 25^\circ\text{C}$	39	W
$I_D$	Continuous Drain Current $R_{\theta JA}$ (Notes 1, 3, 4)	Steady State		
		$T_A = 25^\circ\text{C}$	8.0	A
$P_D$	Power Dissipation $R_{\theta JA}$ (Notes 1 & 3)	$T_A = 100^\circ\text{C}$	6.0	
		$T_A = 25^\circ\text{C}$	3.6	W
$I_{DM}$	Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	130	A
$T_J, T_{stg}$	Operating Junction and Storage Temperature	-55 to +175	$^\circ\text{C}$	
$I_S$	Source Current (Body Diode)	32	A	
$E_{AS}$	Single Pulse Drain-to-Source Avalanche Energy ( $T_J = 25^\circ\text{C}, V_{DD} = 24 \text{ V}, V_{GS} = 10 \text{ V}, I_{L(pk)} = 20 \text{ A}, L = 0.1 \text{ mH}, R_G = 25 \Omega$ )	20	mJ	
$T_L$	Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	260	$^\circ\text{C}$	

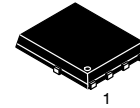
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE MAXIMUM RATINGS

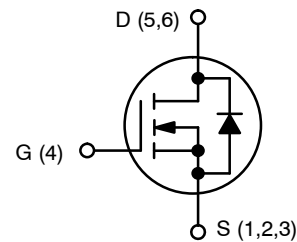
Symbol	Parameter	Value	Unit
$R_{\Psi J-mb}$	Junction-to-Mounting Board (top) – Steady State (Notes 2, 3)	3.9	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient – Steady State (Note 3)	42	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Psi ( $\Psi$ ) is used as required per JESD51-12 for packages in which substantially less than 100% of the heat flows to single case surface.
3. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
4. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(ON) MAX}$	$I_D MAX$
60 V	24 mΩ @ 10 V	26 A
	32 mΩ @ 4.5 V	

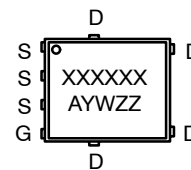


DFN5  
(SO-8FL)  
CASE 488AA  
STYLE 1



N-CHANNEL MOSFET

### MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 5.

# NVMFS5826NL

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	60			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 60 V		T <sub>J</sub> = 25°C		1.0
				T <sub>J</sub> = 125°C		10
I <sub>GSS</sub>	Gate-to-Source Leakage Current	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V			±100	nA

### ON CHARACTERISTICS (Note 5)

V <sub>GS(TH)</sub>	Gate Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	1.5		2.5	V
R <sub>DS(on)</sub>	Drain-to-Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A		18	24	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 10 A		24	32	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 5 A		8.0		S

### CHARGES AND CAPACITANCES

C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> = 0 V, f = 1 MHz, V <sub>DS</sub> = 25 V		850		pF
C <sub>oss</sub>	Output Capacitance			85		
C <sub>rss</sub>	Reverse Transfer Capacitance			50		
Q <sub>G(TOT)</sub>	Total Gate Charge	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 48 V, I <sub>D</sub> = 10 A		9.1		nC
Q <sub>G(TH)</sub>	Threshold Gate Charge			1.0		
Q <sub>GS</sub>	Gate-to-Source Charge			3.0		
Q <sub>GD</sub>	Gate-to-Drain Charge			4.0		
Q <sub>G(TOT)</sub>	Total Gate Charge	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 48 V, I <sub>D</sub> = 10 A		17		nC

### SWITCHING CHARACTERISTICS (Note 6)

t <sub>d(ON)</sub>	Turn-On Delay Time	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 48 V, I <sub>D</sub> = 10 A, R <sub>G</sub> = 2.5 Ω		9.0		ns
t <sub>r</sub>	Rise Time			32		
t <sub>d(OFF)</sub>	Turn-Off Delay Time			15		
t <sub>f</sub>	Fall Time			24		

### DRAIN-SOURCE DIODE CHARACTERISTICS

V <sub>SD</sub>	Forward Diode Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 10 A		T <sub>J</sub> = 25°C	0.8	1.2	V
				T <sub>J</sub> = 125°C	0.7		
t <sub>RR</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, dI <sub>S</sub> /dt = 100 A/μs, I <sub>S</sub> = 10 A			15		ns
t <sub>a</sub>	Charge Time				11		
t <sub>b</sub>	Discharge Time				4.0		
Q <sub>RR</sub>	Reverse Recovery Charge					11	

5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

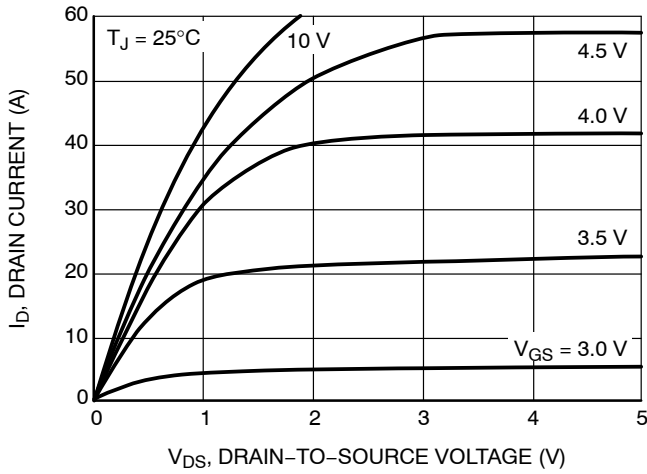


Figure 1. On-Region Characteristics

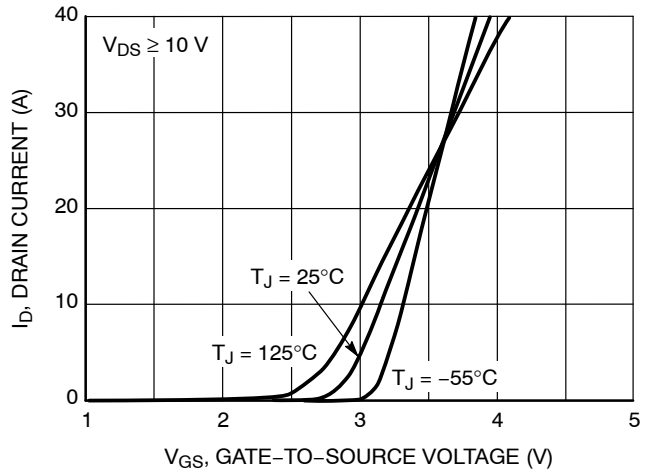


Figure 2. Transfer Characteristics

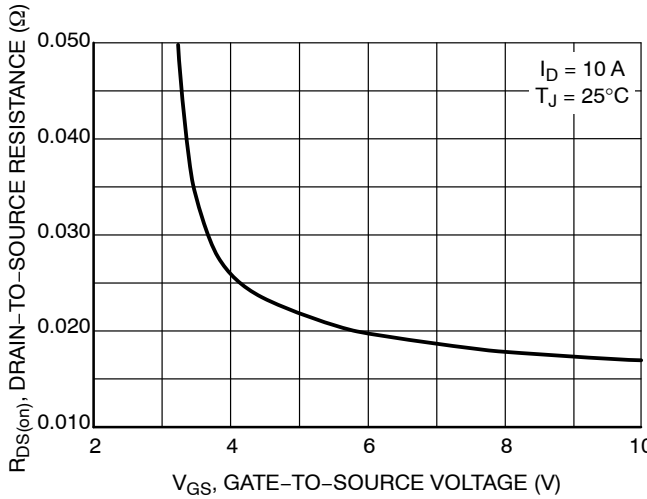


Figure 3. On-Resistance vs. Gate-to-Source Voltage

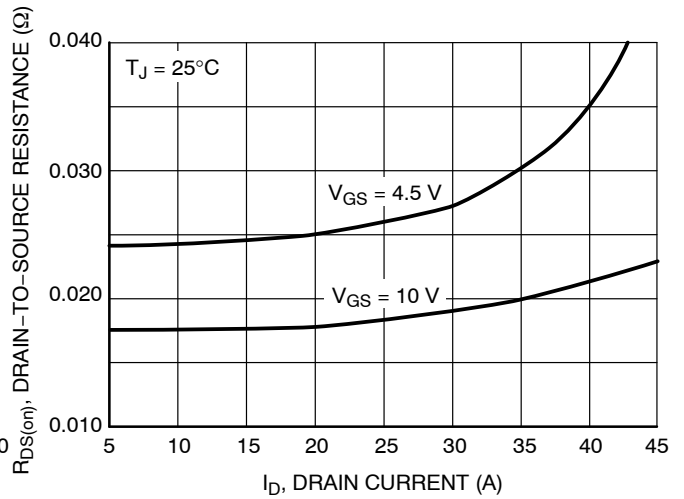


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

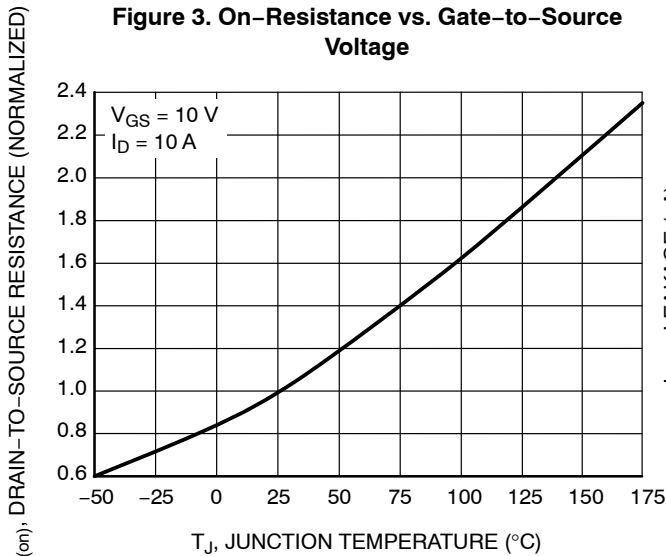


Figure 5. On-Resistance Variation with Temperature

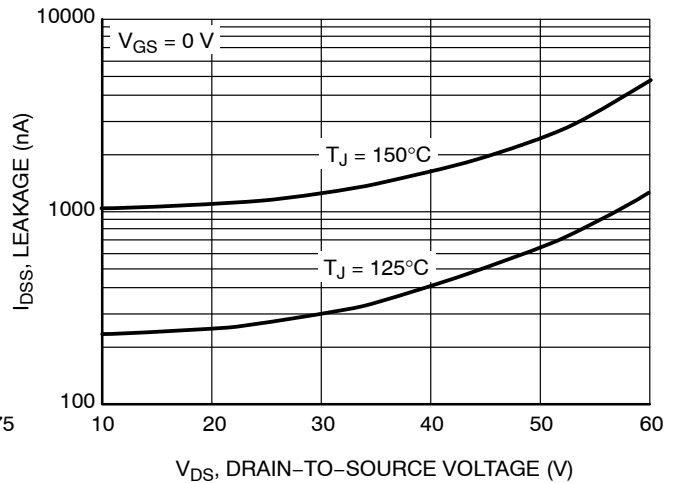


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS (continued)

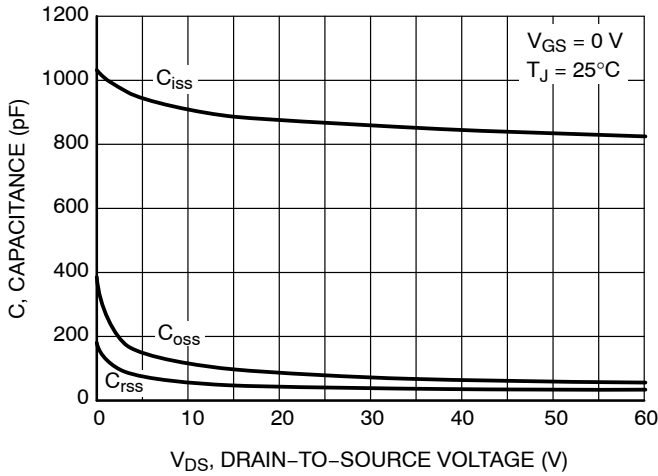


Figure 7. Capacitance Variation

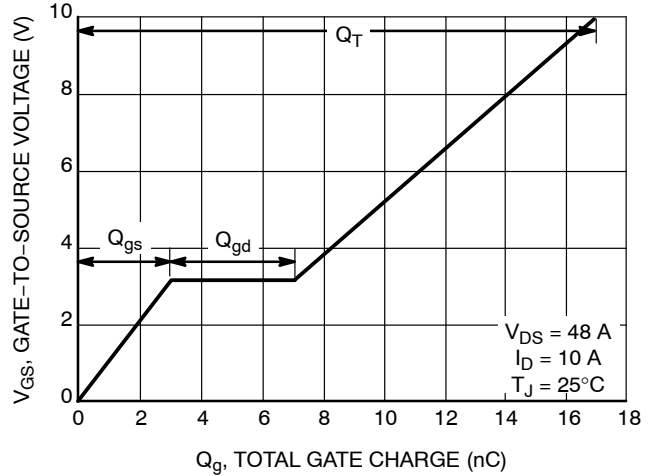


Figure 8. Gate-to-Source Voltage vs. Total Charge

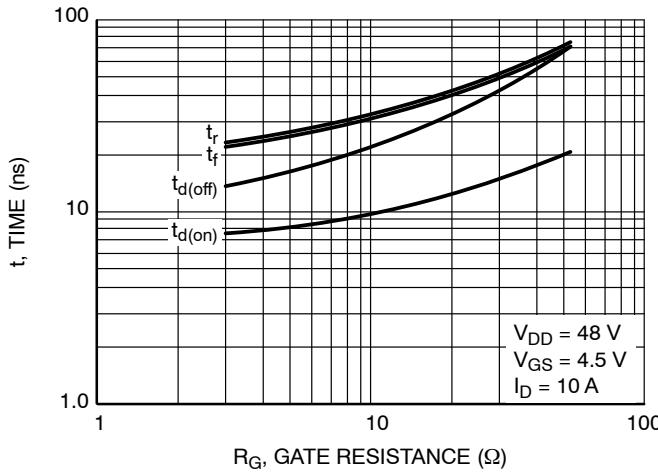


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

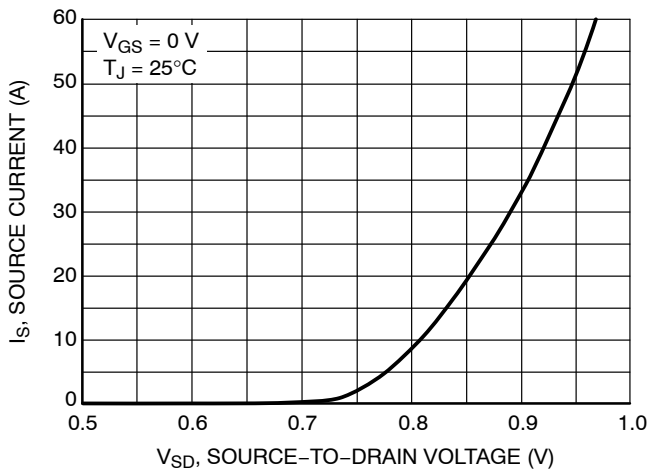


Figure 10. Diode Forward Voltage vs. Current

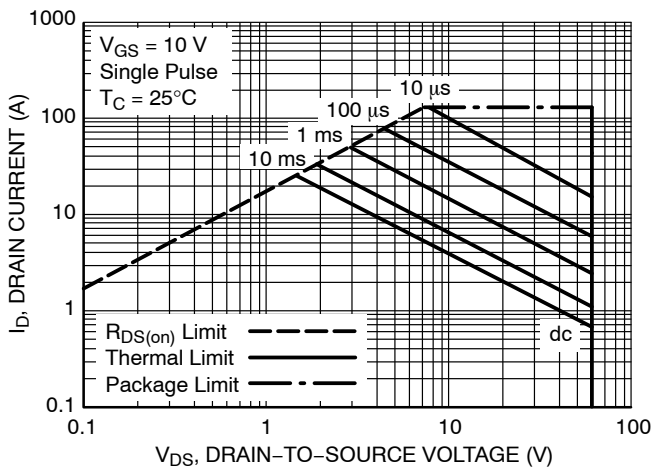


Figure 11. Maximum Rated Forward Biased Safe Operating Area

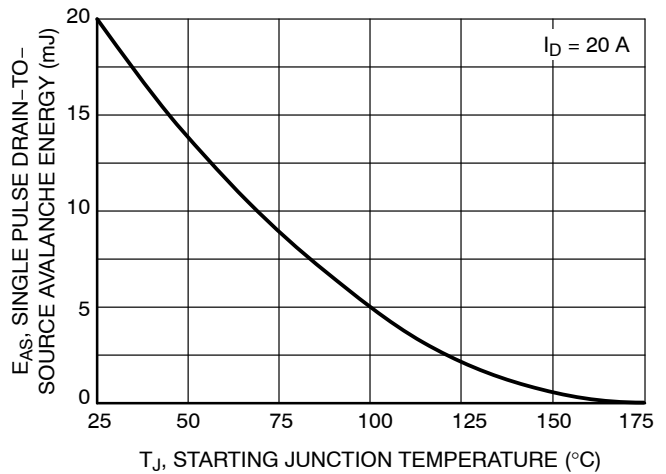
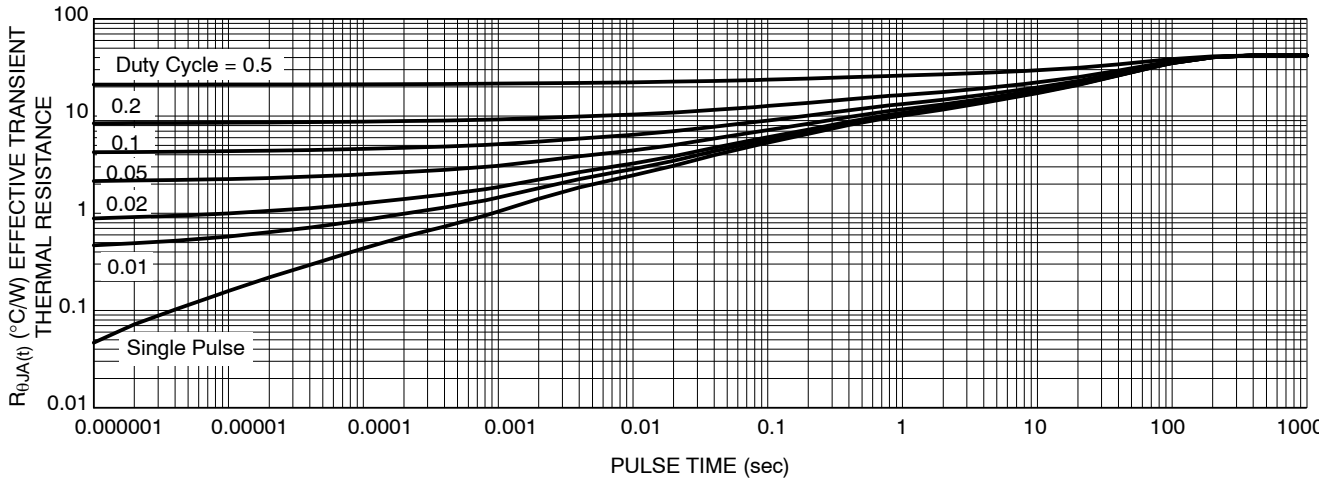


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

# NVMFS5826NL

## TYPICAL CHARACTERISTICS (continued)



**Figure 13. Thermal Response**

### DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NVMFS5826NLWFT1G	5826LW	DFN5 (Pb-Free)	1500 / Tape & Reel

### DISCONTINUED (Note 7)

NVMFS5826NLT1G	V5826L	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5826NLT3G	V5826L	DFN5 (Pb-Free)	5000 / Tape & Reel
NVMFS5826NLWFT3G	5826LW	DFN5 (Pb-Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

7. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on [www.onsemi.com](http://www.onsemi.com).

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS



1  
SCALE 2:1

DFN5 5x6, 1.27P  
(SO-8FL)  
CASE 488AA  
ISSUE N

DATE 25 JUN 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0°	---	12°

### GENERIC MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



- STYLE 1:  
PIN 1. SOURCE  
2. SOURCE  
3. SOURCE  
4. GATE  
5. DRAIN
- STYLE 2:  
PIN 1. ANODE  
2. ANODE  
3. ANODE  
4. NO CONNECT  
5. CATHODE

DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	DFN5 5x6, 1.27P (SO-8FL)	PAGE 1 OF 1

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