

TMS320F28003x Real-Time Microcontrollers

1 Features

- TMS320C28x 32-bit DSP core at 120 MHz
 - IEEE 754 Floating-Point Unit (FPU)
 - Support for Fast Integer Division (FINTDIV)
 - Trigonometric Math Unit (TMU)
 - Support for Nonlinear Proportional Integral Derivative (NLPID) control
 - CRC Engine and Instructions (VCRC)
 - Ten hardware breakpoints (with ERAD)
- Programmable Control Law Accelerator (CLA)
 - 120 MHz
 - IEEE 754 single-precision floating-point instructions
 - Executes code independently of main CPU
- On-chip memory
 - 384KB (192KW) of flash (ECC-protected) across three independent banks
 - 69KB (34.5KW) of RAM (ECC-protected)
 - Security
 - JTAGLOCK
 - Zero-pin boot
 - Dual-zone security
- Clock and system control
 - Two internal 10-MHz oscillators
 - Crystal oscillator or external clock input
 - Windowed watchdog timer module
 - Missing clock detection circuitry
 - Dual-clock Comparator (DCC)
- 3.3-V I/O design
 - Internal VREG generation allows for single-supply design
 - Brownout reset (BOR) circuit
- System peripherals
 - 6-channel Direct Memory Access (DMA) controller
 - 55 individually programmable multiplexed General-Purpose Input/Output (GPIO) pins
 - 23 digital inputs on analog pins
 - 2 digital inputs/outputs on analog pins (AGPIO)
 - Enhanced Peripheral Interrupt Expansion (ePIE)
 - Multiple low-power mode (LPM) support
 - Embedded Real-time Analysis and Diagnostic (ERAD)
 - Unique Identification (UID) number
- Communications peripherals
 - One Power-Management Bus (PMBus) interface
 - Two Inter-integrated Circuit (I2C) interfaces
 - One Controller Area Network (CAN/DCAN) bus port
 - One Controller Area Network with Flexible Data-Rate (CAN FD/MCAN) bus port
 - Two Serial Peripheral Interface (SPI) ports
 - Two UART-compatible Serial Communication Interface (SCI)
 - Two UART-compatible Local Interconnect Network (LIN) interfaces
 - Fast Serial Interface (FSI) with one transmitter and one receiver (up to 200Mbps)
- Analog system
 - Three 4-MSPS, 12-bit Analog-to-Digital Converters (ADCs)
 - Up to 23 external channels (includes the two gpdac outputs)
 - Four integrated Post-Processing Blocks (PPB) per ADC
 - Four windowed comparators (CMPSS) with 12-bit reference Digital-to-Analog Converters (DACs)
 - Digital glitch filters
 - Two 12-bit buffered DAC outputs
- Enhanced control peripherals
 - 16 ePWM channels with eight channels that have high-resolution capability (150-ps resolution)
 - Integrated dead-band support
 - Integrated hardware trip zones (TZs)
 - Three Enhanced Capture (eCAP) modules
 - High-resolution Capture (HRCAP) available on one of the three eCAP modules
 - Two Enhanced Quadrature Encoder Pulse (eQEP) modules with support for CW/CCW operation modes
 - Eight Sigma-Delta Filter Module (SDFM) input channels (two parallel filters per channel)
 - Standard SDFM data filtering
 - Comparator filter for fast action for overvalue or undervalue condition
 - Embedded Pattern Generator (EPG)
- Configurable Logic Block (CLB)
 - 4 tiles
 - Augments existing peripheral capability
 - Supports position manager solutions
- Host Interface Controller (HIC)
 - Access to internal memory from an external host
- Background CRC (BGCRC)
 - One cycle CRC computation on 32 bits of data
- Advanced Encryption Standard (AES) accelerator



- Live Firmware Update (LFU)
 - Fast context switching from old to new firmware
 - Flash bank erase time improvements
 - Diagnostic features
 - Memory Power On Self Test (MPOST)
 - Hardware Built-in Self Test (HWBIST)
 - **Functional Safety-Compliant** (PZ and Q100 PM packages only)
 - Developed for functional safety applications
 - Documentation available to aid ISO 26262 and IEC 61508 system design
 - [Systematic capability up to ASIL D and SIL 3](#)
 - [Hardware capability up to ASIL B and SIL 2](#)
 - Safety-related certification
 - [ISO 26262 certification up to ASIL B and SIL 2 by TÜV SÜD](#) (PZ and Q100 PM packages only)
 - Package options:
 - 100-pin Low-profile Quad Flatpack (LQFP) [PZ suffix]
 - 80-pin Low-profile Quad Flatpack (LQFP) [PN suffix]
 - 64-pin (LQFP) [PM suffix]
 - 48-pin (LQFP) [PT suffix]
 - Temperature options:
 - Free-air (T_A): -40°C to 125°C
 - Junction (T_J): -40°C to 150°C
- ## 2 Applications
- Appliances
 - [Air conditioner outdoor unit](#)
 - Building automation
 - [Door operator drive control](#)
 - Industrial machine & machine tools
 - [Automated sorting equipment](#)
 - [Textile machine](#)
 - AC inverter & VF drives
 - [AC drive control module](#)
 - [AC drive position feedback](#)
 - [AC drive power stage module](#)
 - Linear motor transport systems
 - [Linear motor power stage](#)
 - Single & multi axis servo drives
 - [Servo drive position feedback](#)
 - [Servo drive power stage module](#)
 - Speed controlled BLDC drives
 - [AC-input BLDC motor drive](#)
 - [DC-input BLDC motor drive](#)
 - Factory automation
 - [Robot servo drive](#)
 - [Mobile robot motor control](#)
 - [Position sensor](#)
 - Industrial power
 - [Industrial AC-DC](#)
 - UPS
 - [Three phase UPS](#)
 - [Single phase online UPS](#)
 - Telecom & server power
 - [Merchant DC/DC](#)
 - [Merchant network & server PSU](#)
 - [Merchant telecom rectifiers](#)
 - Hybrids, electric & powertrain systems
 - [DC/DC converter](#)
 - [Inverter & motor control](#)
 - [On-board \(OBC\) & wireless charger](#)
 - [Virtual engine sound system \(VESS\)](#)
 - [Engine fan](#)
 - [eTurbo/charger](#)
 - [Pump](#)
 - [Electric power steering \(EPS\)](#)
 - Infotainment and cluster
 - [Head-up display](#)
 - [Automotive head unit](#)
 - [Automotive external amplifier](#)
 - Body electronics & lighting
 - [Automotive HVAC compressor module](#)
 - [DC/AC inverter](#)
 - [Headlight](#)
 - ADAS
 - [Mechanically scanning LIDAR](#)
 - HEV/EV battery-management system (BMS)
 - [100-V battery pack-passive balancing](#)
 - [12- & 24-V battery pack-passive balancing](#)
 - [400-V battery pack-passive balancing](#)
 - [48-V battery pack-passive balancing](#)
 - EV charging infrastructure
 - [AC charging \(pile\) station](#)
 - [DC charging \(pile\) station](#)
 - [EV charging station power module](#)
 - [Wireless EV charging station](#)
 - Renewable energy storage
 - [Energy storage power conversion system \(PCS\)](#)
 - Solar energy
 - [Central inverter](#)
 - [Micro inverter](#)
 - [Solar power optimizer](#)
 - [Solar arc protection](#)
 - [Rapid shutdown](#)
 - [String inverter](#)

3 Description

The TMS320F28003x (F28003x) is a member of the C2000™ real-time microcontroller family of scalable, ultra-low latency devices designed for efficiency in power electronics, including but not limited to: high power density, high switching frequencies, and supporting the use of GaN and SiC technologies.

These include such [applications](#) as:

- [Motor drives](#)
- [Appliances](#)
- [Hybrid, electric & powertrain systems](#)
- [Solar & EV charging](#)
- [Digital power](#)
- [Body electronics & lighting](#)
- [Test & measurement](#)

The [real-time control subsystem](#) is based on TI's 32-bit C28x DSP core, which provides 120 MHz of signal-processing performance for floating- or fixed-point code running from either on-chip flash or SRAM. The C28x CPU is further boosted by the [Floating-Point Unit \(FPU\)](#), [Trigonometric Math Unit \(TMU\)](#), and [VCRC \(Cyclical Redundancy Check\) extended instruction sets](#), speeding up common algorithms key to real-time control systems.

The CLA allows significant offloading of common tasks from the main C28x CPU. The CLA is an independent 32-bit floating-point math accelerator that executes in parallel with the CPU. Additionally, the CLA has its own dedicated memory resources and it can directly access the key peripherals that are required in a typical control system. Support of a subset of ANSI C is standard, as are key features like hardware breakpoints and hardware task-switching.

The F28003x supports up to 384KB (192KW) of flash memory divided into three 128KB (64KW) banks, which enable programming and execution in parallel. Up to 69KB (34.5KW) of on-chip SRAM is also available to supplement the flash memory.

The Live Firmware Update hardware enhancements on F28003x allow fast context switching from the old firmware to the new firmware to minimize application downtime when updating the device firmware.

High-performance analog blocks are integrated on the F28003x real-time microcontroller (MCU) and are closely coupled with the processing and PWM units to provide optimal real-time signal chain performance. Sixteen PWM channels, all supporting frequency-independent resolution modes, enable control of various power stages from a 3-phase inverter to power factor correction and advanced multilevel power topologies.

The inclusion of the Configurable Logic Block (CLB) allows the user to add [custom logic](#) and potentially [integrate FPGA-like functions](#) into the C2000 real-time MCU.

Interfacing is supported through various industry-standard communication ports (such as SPI, SCI, I2C, PMBus, LIN, CAN and CAN FD) and offers [multiple pin-muxing options](#) for optimal signal placement. The [Fast Serial Interface \(FSI\)](#) enables up to 200Mbps of robust communications across an isolation boundary.

New to the C2000 platform is the [Host Interface Controller \(HIC\)](#), a high-throughput interface that allows an external host to access the resources of the TMS320F28003x directly.

Want to learn more about features that make C2000 Real-Time MCUs the right choice for your real-time control system? Check out [The Essential Guide for Developing With C2000™ Real-Time Microcontrollers](#) and visit the [C2000™ real-time control MCUs](#) page.

The [Getting Started With C2000™ Real-Time Control Microcontrollers \(MCUs\) Getting Started Guide](#) covers all aspects of development with C2000 devices from hardware to support resources. In addition to key reference documents, each section provides relevant links and resources to further expand on the information covered.

Ready to get started? Check out the [TMDSCNCD280039C](#) evaluation board and download [C2000Ware](#).

Package Information

| PART NUMBER | PACKAGE ⁽¹⁾ | PACKAGE SIZE ⁽²⁾ | BODY SIZE (NOM) |
|---------------------------------|------------------------|-----------------------------|-----------------|
| TMS320F280039C | PZ (LQFP, 100) | 16 mm × 16 mm | 14 mm × 14 mm |
| | PN (LQFP, 80) | 14 mm × 14 mm | 12 mm × 12 mm |
| | PM (LQFP, 64) | 12 mm × 12 mm | 10 mm × 10 mm |
| TMS320F280039C-Q1 | PZ (LQFP, 100) | 16 mm × 16 mm | 14 mm × 14 mm |
| | PN (LQFP, 80) | 14 mm × 14 mm | 12 mm × 12 mm |
| TMS320F280039 | PZ (LQFP, 100) | 16 mm × 16 mm | 14 mm × 14 mm |
| | PN (LQFP, 80) | 14 mm × 14 mm | 12 mm × 12 mm |
| | PM (LQFP, 64) | 12 mm × 12 mm | 10 mm × 10 mm |
| TMS320F280039-Q1 | PZ (LQFP, 100) | 16 mm × 16 mm | 14 mm × 14 mm |
| | PN (LQFP, 80) | 14 mm × 14 mm | 12 mm × 12 mm |
| TMS320F280038C-Q1 | PM (LQFP, 64) | 12 mm × 12 mm | 10 mm × 10 mm |
| TMS320F280038-Q1 | PM (LQFP, 64) | 12 mm × 12 mm | 10 mm × 10 mm |
| TMS320F280037C | PZ (LQFP, 100) | 16 mm × 16 mm | 14 mm × 14 mm |
| | PN (LQFP, 80) | 14 mm × 14 mm | 12 mm × 12 mm |
| | PM (LQFP, 64) | 12 mm × 12 mm | 10 mm × 10 mm |
| | PT (LQFP, 48) | 9 mm × 9 mm | 7 mm × 7 mm |
| TMS320F280037C-Q1 | PZ (LQFP, 100) | 16 mm × 16 mm | 14 mm × 14 mm |
| | PN (LQFP, 80) | 14 mm × 14 mm | 12 mm × 12 mm |
| | PT (LQFP, 48) | 9 mm × 9 mm | 7 mm × 7 mm |
| TMS320F280037 | PZ (LQFP, 100) | 16 mm × 16 mm | 14 mm × 14 mm |
| | PN (LQFP, 80) | 14 mm × 14 mm | 12 mm × 12 mm |
| | PM (LQFP, 64) | 12 mm × 12 mm | 10 mm × 10 mm |
| | PT (LQFP, 48) | 9 mm × 9 mm | 7 mm × 7 mm |
| TMS320F280037-Q1 | PZ (LQFP, 100) | 16 mm × 16 mm | 14 mm × 14 mm |
| | PT (LQFP, 48) | 9 mm × 9 mm | 7 mm × 7 mm |
| TMS320F280036C-Q1 | PM (LQFP, 64) | 12 mm × 12 mm | 10 mm × 10 mm |
| TMS320F280036-Q1 | PM (LQFP, 64) | 12 mm × 12 mm | 10 mm × 10 mm |
| TMS320F280034 | PZ (LQFP, 100) | 16 mm × 16 mm | 14 mm × 14 mm |
| | PN (LQFP, 80) | 14 mm × 14 mm | 12 mm × 12 mm |
| | PM (LQFP, 64) | 12 mm × 12 mm | 10 mm × 10 mm |
| | PT (LQFP, 48) | 9 mm × 9 mm | 7 mm × 7 mm |
| TMS320F280034-Q1 | PN (LQFP, 80) | 14 mm × 14 mm | 12 mm × 12 mm |
| | PT (LQFP, 48) | 9 mm × 9 mm | 7 mm × 7 mm |
| TMS320F280033 | PZ (LQFP, 100) | 16 mm × 16 mm | 14 mm × 14 mm |
| | PN (LQFP, 80) | 14 mm × 14 mm | 12 mm × 12 mm |
| | PM (LQFP, 64) | 12 mm × 12 mm | 10 mm × 10 mm |
| | PT (LQFP, 48) | 9 mm × 9 mm | 7 mm × 7 mm |
| TMS320F280033-Q1 ⁽³⁾ | PN (LQFP, 80) | 14 mm × 14 mm | 12 mm × 12 mm |

(1) For more information, see [Mechanical, Packaging, and Orderable Information](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.

(3) Preview information (not Production Data).

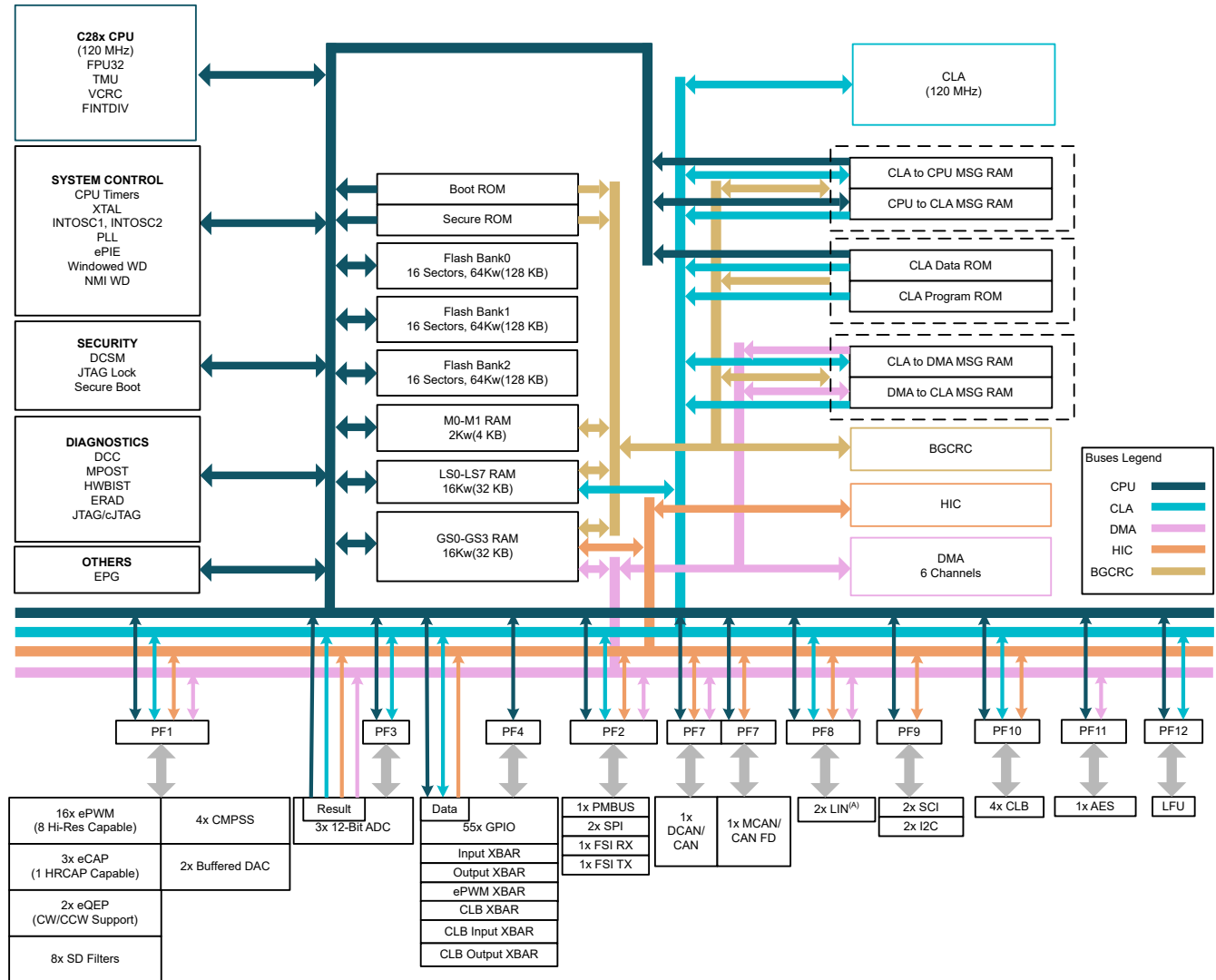
Device Information

| PART NUMBER ⁽¹⁾ | CONTROL LAW ACCELERATOR (CLA) | CONFIGURABLE LOGIC BLOCK (CLB) | FLASH SIZE |
|--|-------------------------------|--------------------------------|------------|
| TMS320F280039C-Q1 TMS320F280039C | Yes | 4 Tiles | 384KB |
| TMS320F280039-Q1 TMS320F280039 | Yes | – | |
| TMS320F280038C-Q1 | Yes | 4 Tiles | |
| TMS320F280038-Q1 | Yes | – | |
| TMS320F280037C-Q1 TMS320F280037C | Yes | 4 Tiles | 256KB |
| TMS320F280037-Q1 TMS320F280037 | Yes | – | |
| TMS320F280036C-Q1 | Yes | 4 Tiles | |
| TMS320F280036-Q1 | Yes | – | |
| TMS320F280034-Q1 TMS320F280034 | Yes | – | 128KB |
| TMS320F280033-Q1 ⁽²⁾ TMS320F280033 | No | – | 128KB |

- (1) For more information on these devices, see the [Device Comparison](#) table.
(2) Preview information (not Production Data).

3.1 Functional Block Diagram

The **Functional Block Diagram** shows the CPU system and associated peripherals.



A. The LIN module can also work as an SCI.

Figure 3-1. Functional Block Diagram

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4 Device Comparison

Table 4-1 lists the features of the TMS320F28003x devices.

Table 4-1. Device Comparison

| FEATURE ⁽¹⁾ | | F280039C F280039C-Q1 F280039 F280039-Q1 | F280038C-Q1 F280038-Q1 | F280037C F280037C-Q1 F280037 F280037-Q1 | F280036C-Q1 F280036-Q1 | F280034 F280034-Q1 | F280033 F280033-Q1 ⁽²⁾ |
|---|-----------------|---|---------------------------|--|---------------------------|-----------------------|--------------------------------------|
| Processor and Accelerators | | | | | | | |
| C28x | Frequency (MHz) | 120 | | | | | |
| | FPU | Yes (instructions for Fast Integer Division) | | | | | |
| | VCRC | Yes | | | | | |
| | TMU | Yes – Type 1 (instructions supporting NLPID) | | | | | |
| CLA – Type 2 | Available | Yes | | | | | No |
| | Frequency (MHz) | 120 | | | | | – |
| 6-Channel DMA – Type 0 | | Yes | | | | | |
| External interrupts | | 5 | | | | | |
| Memory | | | | | | | |
| Flash | | 384KB (192KW) | | 256KB (128KW) | | 128KB (64KW) | |
| Flash Banks | | 3 x 128KB | | 2 x 128KB | | 2 x 64KB | |
| RAM | Dedicated | 4KB (2KW) | | | | | |
| | Local Shared | 32KB (16KW) | | | | | |
| | Message | 1KB (0.5KW) | | | | | |
| | Global Shared | 32KB (16KW) | | | | | |
| | Total | 69KB (34.5KW) | | | | | |
| Message RAM Types | | 512B (256W) CPU-CLA 512B (256W) CLA-DMA | | | | | – |
| ECC | | FLASH, Mx, LSx, GSx, Message RAM | | | | | FLASH, Mx, LSx, GSx |
| Parity | | ROM, CAN RAM | | | | | |
| Security: JTAGLOCK, Zero-pin boot, Dual-zone security | | Yes | | | | | |
| System | | | | | | | |
| Configurable Logic Block (CLB) | | 4 Tiles on C Variants | | | | – | |
| Embedded Pattern Generator (EPG) | | Yes | | | | | |
| 32-bit CPU timers | | 3 | | | | | |
| Advance Encryption Standard (AES) | | Yes | | | | | |
| Background CRC (BGCRRC) | | Yes | | | | | |
| Live Firmware Update (LFU) Support | | Yes, with enhancements and flash bank erase time improvements | | | | | |
| Secure Boot | | Yes | | | | | |
| JTAG Lock | | Yes | | | | | |
| HWBIST | | Yes | | | | | |
| Nonmaskable Interrupt Watchdog (NMIWD) timers | | 1 | | | | | |
| Watchdog timers | | 1 | | | | | |
| Crystal oscillator/External clock input | | 1 | | | | | |
| Internal oscillator | | 2 | | | | | |

Table 4-1. Device Comparison (continued)

| FEATURE ⁽¹⁾ | | F280039C F280039C-Q1 F280039 F280039-Q1 | F280038C-Q1 F280038-Q1 | F280037C F280037C-Q1 F280037 F280037-Q1 | F280036C-Q1 F280036-Q1 | F280034 F280034-Q1 | F280033 F280033-Q1 ⁽²⁾ |
|--|---|--|---------------------------|--|---------------------------|-----------------------|--------------------------------------|
| Pins and Power Supply | | | | | | | |
| Internal 3.3-V to 1.2-V Voltage Regulator | VREG LDO | Yes | | | | | |
| GPIO pins | 100-pin PZ | 51 | – | 51 | – | 51 | |
| | 80-pin PN | 39 | – | 39 | – | 39 | |
| | 64-pin PM | 26 | 25 | 26 | 25 | 26 | |
| | 48-pin PT | – | – | 14 | – | 14 | |
| | Additional GPIO | 4 (2 from cJTAG and 2 from X1/X2) | | | | | |
| AIO (analog with digital inputs) | 100-pin PZ | 23 | – | 23 | – | 23 | |
| | 80-pin PN | 16 | – | 16 | – | 16 | |
| | 64-pin PM | 16 | 16 | 16 | 16 | 16 | |
| | 48-pin PT | – | – | 14 | – | 14 | |
| AGPIO (analog with digital inputs and outputs) | 100-pin PZ | 2 | – | 2 | – | 2 | |
| | 80-pin PN | 2 | – | 2 | – | 2 | |
| Analog Peripherals | | | | | | | |
| ADC 12-bit | Number of ADCs | 3 | | | | | |
| | MSPS | 4 | | | | | |
| | Conversion Time (ns) ⁽³⁾ | 250 | | | | | |
| ADC channels (single-ended) <i>(includes the two gpdac outputs)</i> | 100-pin PZ | 25 | – | 25 | – | 25 | |
| | 80-pin PN | 18 | – | 18 | – | 18 | |
| | 64-pin PM | 16 | 16 | 16 | 16 | 16 | |
| | 48-pin PT | – | – | 14 | – | 14 | |
| Temperature sensor | 1 | | | | | | |
| Buffered DAC | 2 | | | | | | |
| CMPSS (each CMPSS has two comparators and two internal DACs) | 4 | | | | | | |
| Control Peripherals ⁽⁴⁾ | | | | | | | |
| eCAP/HRCAP modules – Type 2 | 3 (1 - eCAP3 with HRCAP capability) | | | | | | |
| ePWM/HRPWM channels – Type 4 | 16 (8 - ePWM1 to ePWM4 with HRPWM capability) | | | | | | |
| eQEP modules – Type 2 | 2 | | | | | | |
| SDFM channels – Type 2 | 8 | | | | | | |
| Communication Peripherals ⁽⁴⁾ | | | | | | | |
| CAN (DCAN) – Type 0 | 1 | | | | | | |
| CAN FD (MCAN) – Type 1 | 1 | | | | | | |
| Fast Serial Interface (FSI) – Type 2 | 1 (1 RX and 1 TX) | | | | | | |
| I2C – Type 1 | 2 | | | | | | |
| LIN – Type 1 (UART-Compatible) | 2 | | | | | | |
| Host Interface Controller (HIC) – Type 1 | 1 | | | | | | |
| PMBus – Type 0 | 1 | | | | | | |
| SCI – Type 0 (UART-Compatible) | 2 | | | | | | |
| SPI – Type 2 | 2 | | | | | | |

Table 4-1. Device Comparison (continued)

| FEATURE ⁽¹⁾ | | F280039C F280039C-Q1 F280039 F280039-Q1 | F280038C-Q1 F280038-Q1 | F280037C F280037C-Q1 F280037 F280037-Q1 | F280036C-Q1 F280036-Q1 | F280034 F280034-Q1 | F280033 F280033-Q1 ⁽²⁾ |
|--|------------|--|---------------------------|--|---------------------------|-----------------------|--------------------------------------|
| Package Options, Temperature, and Qualification | | | | | | | |
| Junction temperature (T _J) | | –40°C to 150°C | | | | | |
| Free-Air temperature (T _A) | | –40°C to 125°C | | | | | |
| Package Options | 100-pin PZ | F280039C F280039 | – | F280037C F280037 | – | F280034 | F280033 |
| | 80-pin PN | F280039C F280039 | – | F280037C F280037 | – | F280034 | F280033 |
| | 64-pin PM | F280039C F280039 | – | F280037C F280037 | – | F280034 | F280033 |
| | 48-pin PT | – | – | F280037C F280037 | – | F280034 | F280033 |
| Package Options with AEC-Q100 Qualification available | 100-pin PZ | F280039C-Q1 F280039-Q1 | – | F280037C-Q1 F280037-Q1 | – | – | – |
| | 80-pin PN | F280039C-Q1 F280039-Q1 | – | F280037C-Q1 | – | F280034-Q1 | F280033-Q1 |
| | 64-pin PM | – | F280038C-Q1 F280038-Q1 | – | F280036C-Q1 F280036-Q1 | – | – |
| | 48-pin PT | – | – | F280037C-Q1 F280037-Q1 | – | F280034-Q1 | – |

- (1) A type change represents a major functional feature difference in a peripheral module. Within a peripheral type, there may be minor differences between devices that do not affect the basic functionality of the module.
- (2) Preview information (not Production Data).
- (3) Time between start of sample-and-hold window to start of sample-and-hold window of the next conversion.
- (4) For devices that are available in more than one package, the peripheral count listed in the smaller package is reduced because the smaller package has less device pins available. The number of peripherals internally present on the device is not reduced compared to the largest package offered within a part number. See [Section 5](#) to identify which peripheral instances are accessible on pins in the smaller package.

4.1 Related Products

[TMS320F2803x Real-Time Microcontrollers](#)

The F2803x series increases the pin-count and memory size options. The F2803x series also introduces the parallel control law accelerator (CLA) option.

[TMS320F2807x Real-Time Microcontrollers](#)

The F2807x series offers the most performance, largest pin counts, flash memory sizes, and peripheral options. The F2807x series includes the latest generation of accelerators, ePWM peripherals, and analog technology.

[TMS320F28004x Real-Time Microcontrollers](#)

The F28004x series is a reduced version of the F2807x series with the latest generational enhancements.

[TMS320F28002x Real-Time Microcontrollers](#)

The F28002x series is a reduced version of the F28004x series with the latest generational enhancements.

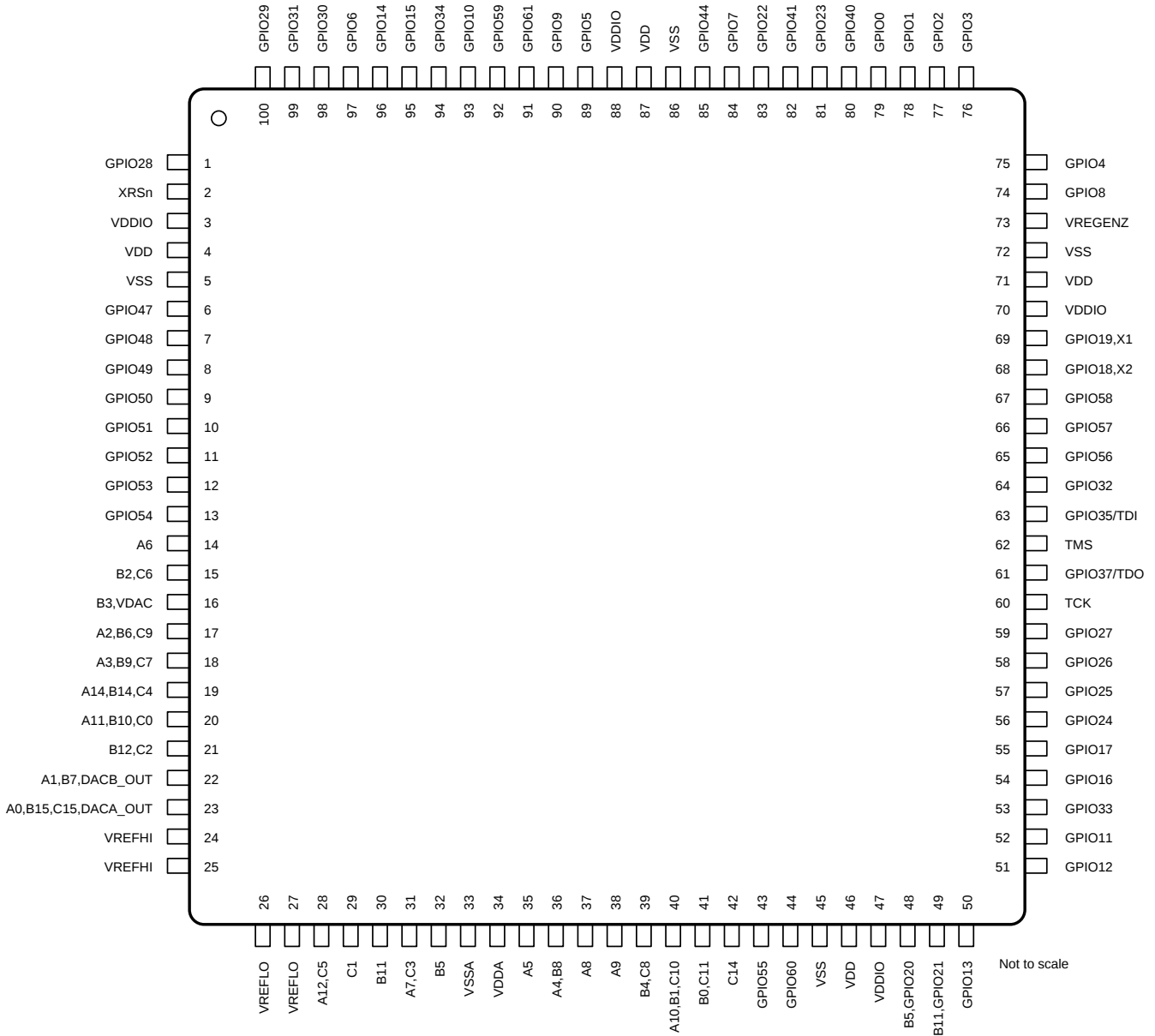
[TMS320F2838x Real-Time Microcontrollers](#)

The F2838x series offers more performance, larger pin counts, flash memory sizes, peripheral and wide variety of connectivity options. The F2838x series includes the latest generation of accelerators, ePWM peripherals, and analog technology.

5 Pin Configuration and Functions

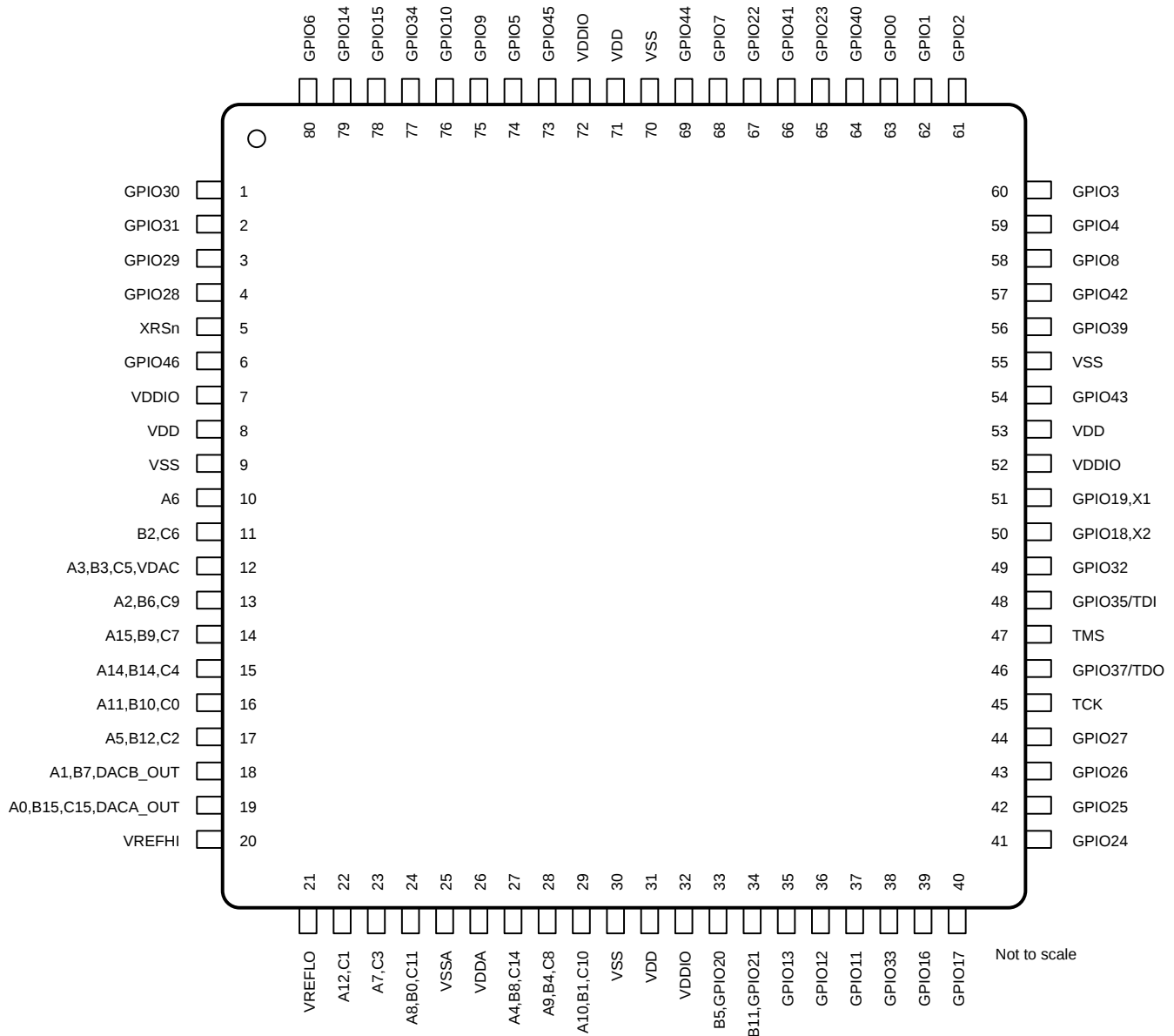
5.1 Pin Diagrams

Figure 5-1 shows the pin assignments on the 100-pin PZ low-profile quad flatpack; the Q and non-Q variant have the same pinout. Figure 5-2 shows the pin assignments on the 80-pin PN low-profile quad flatpack. Figure 5-3 shows the pin assignments on the 64-pin PM low-profile quad flatpack (Q temperature). Figure 5-4 shows the pin assignments on the 64-pin PM low-profile quad flatpack. Figure 5-5 shows the pin assignments on the 48-Pin PT low-profile quad flatpack; the Q and non-Q variant have the same pinout.



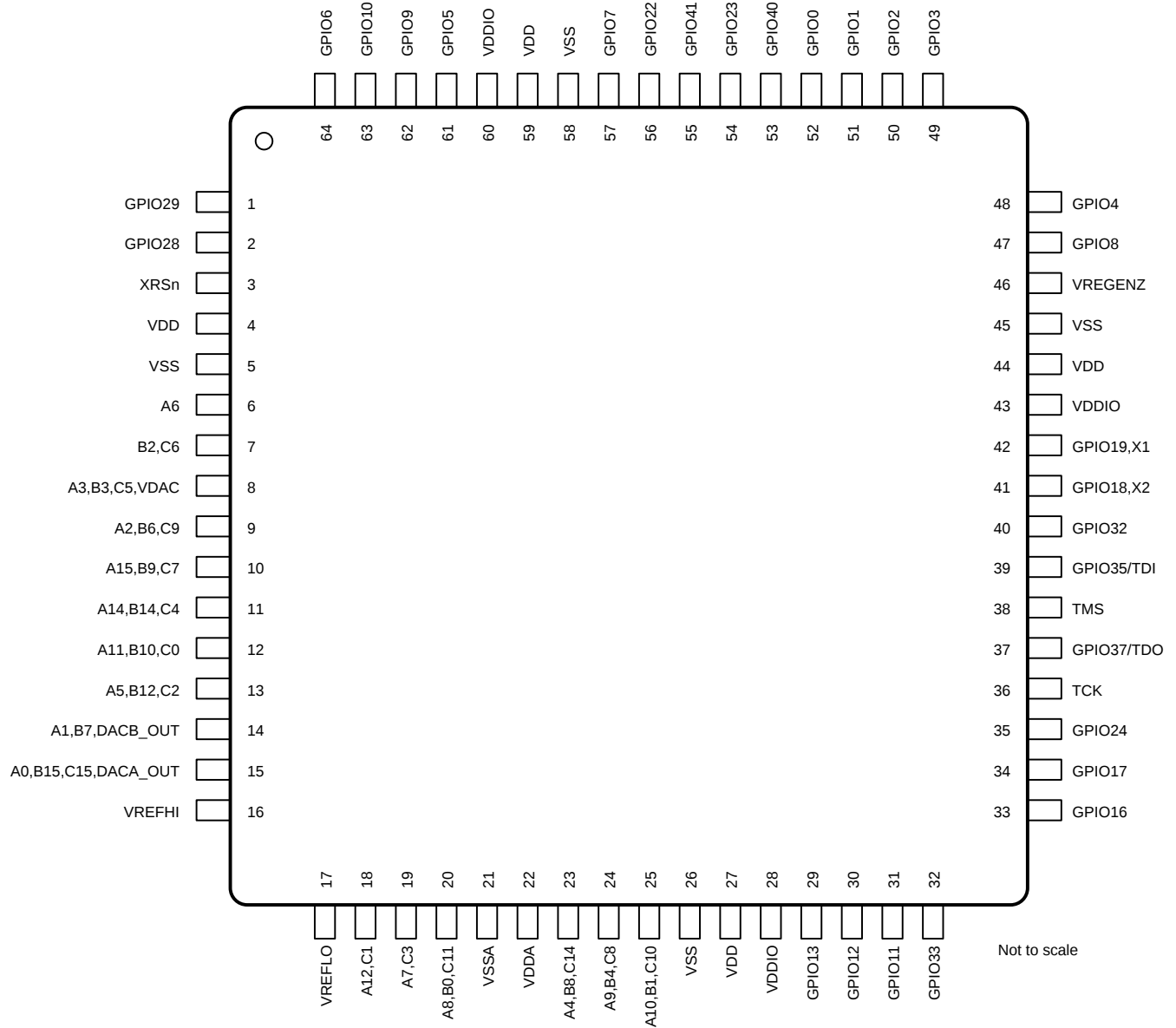
A. Only the GPIO function is shown on GPIO pins. See Section 5.2 for the complete, muxed signal name.

Figure 5-1. 100-Pin PZ Low-Profile Quad Flatpack (Top View)



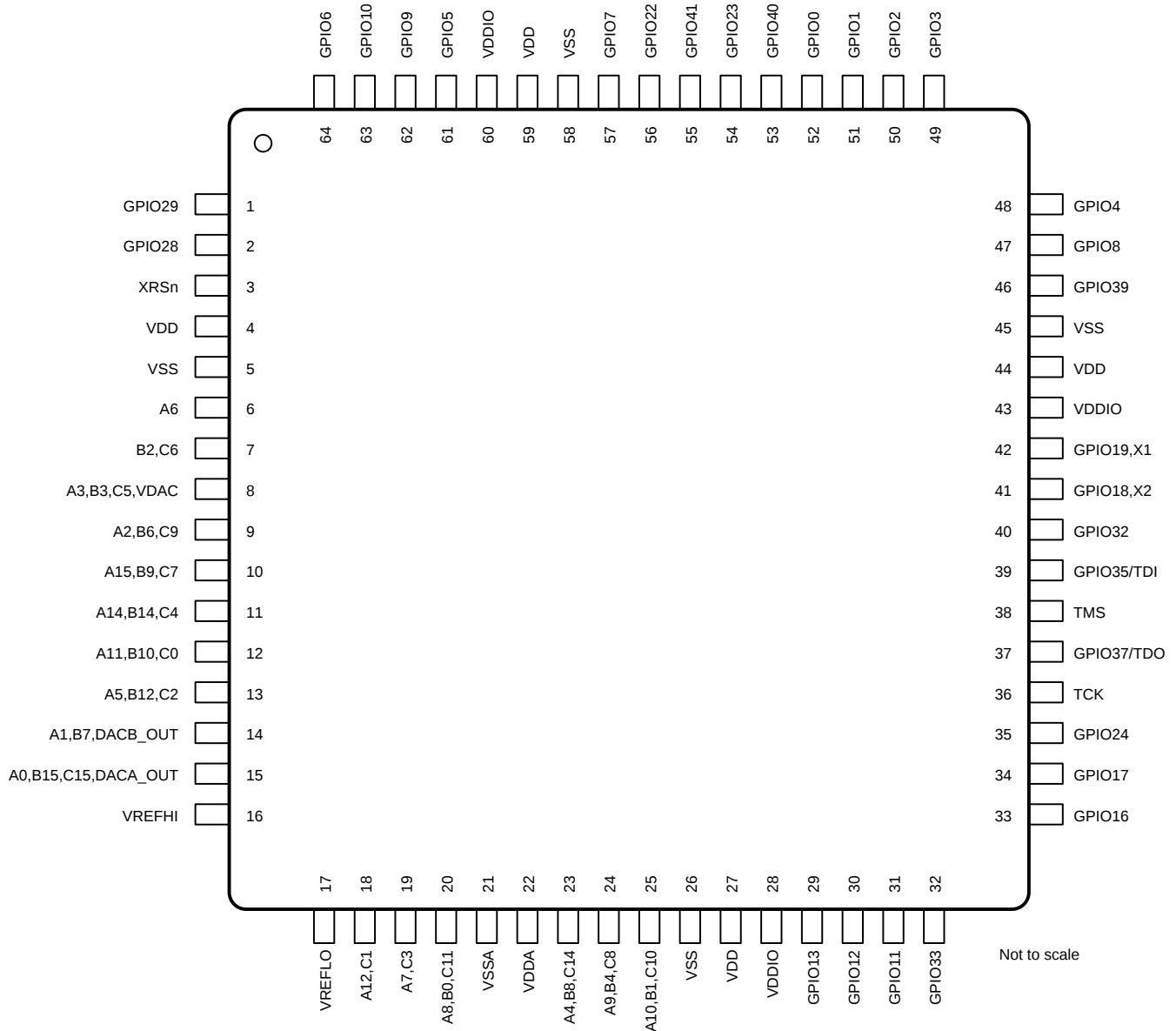
A. Only the GPIO function is shown on GPIO pins. See [Section 5.2](#) for the complete, muxed signal name.

Figure 5-2. 80-Pin PN Low-Profile Quad Flatpack (Top View)



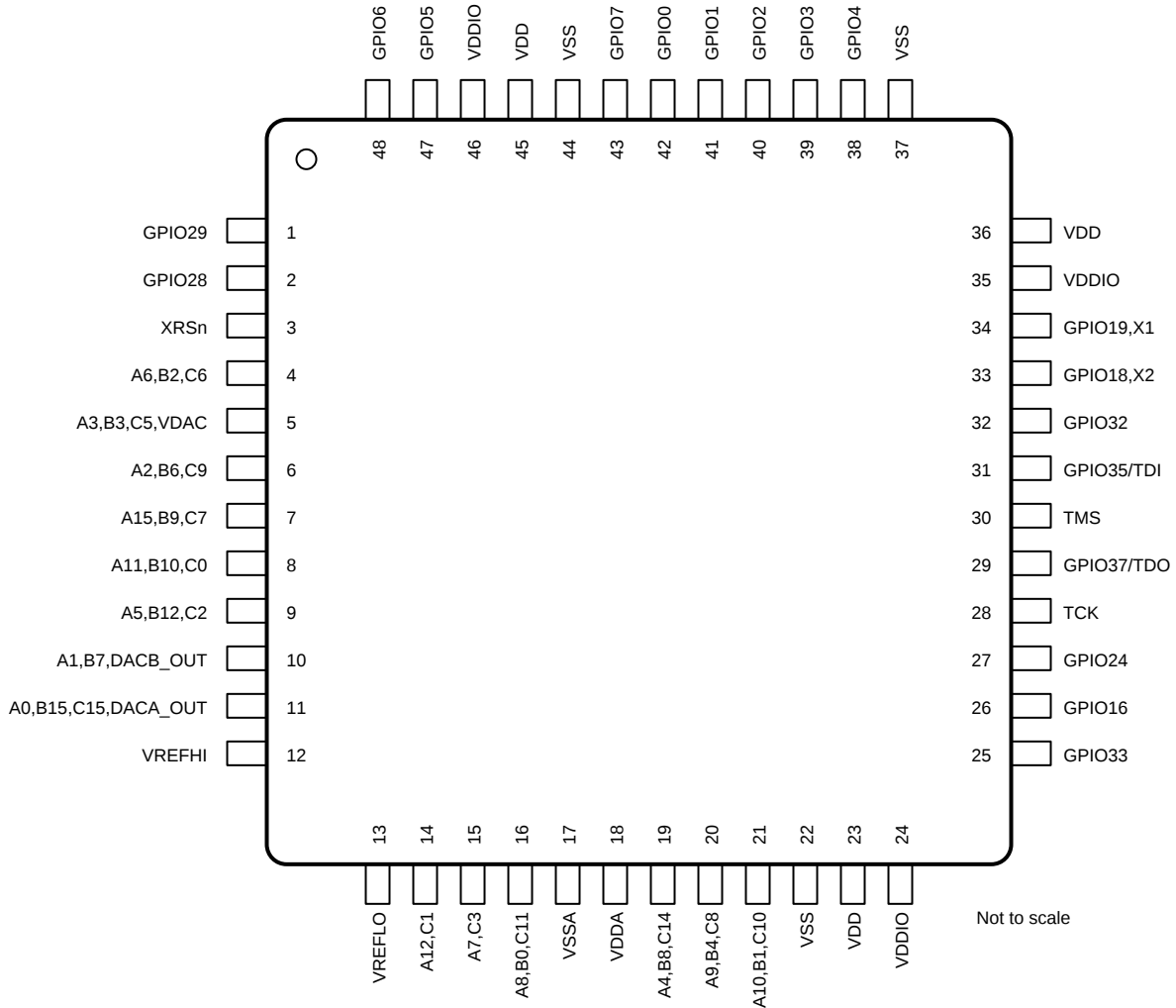
A. Only the GPIO function is shown on GPIO pins. See [Section 5.2](#) for the complete, muxed signal name.

Figure 5-3. 64-Pin PM Low-Profile Quad Flatpack - Q Temperature (Top View)



A. Only the GPIO function is shown on GPIO pins. See [Section 5.2](#) for the complete, muxed signal name.

Figure 5-4. 64-Pin PM Low-Profile Quad Flatpack (Top View)



A. Only the GPIO function is shown on GPIO pins. See [Section 5.2](#) for the complete, muxed signal name.

Figure 5-5. 48-Pin PT Low-Profile Quad Flatpack (Top View)

5.2 Pin Attributes

Table 5-1. Pin Attributes

| SIGNAL NAME | MUX POSITION | 100 PZ | 80 PN | 64 PMQ | 64 PM | 48 PT | PIN TYPE | DESCRIPTION |
|--|--------------|--------|-------|--------|-------|-------|---------------------------------|--|
| ANALOG | | | | | | | | |
| A0 B15 C15 CMP3_HP2 CMP3_LP2 DACA_OUT AIO231 | 0, 4, 8, 12 | 23 | 19 | 15 | 15 | 11 | I I I I I O I | ADC-A Input 0 ADC-B Input 15 ADC-C Input 15 CMPSS-3 High Comparator Positive Input 2 CMPSS-3 Low Comparator Positive Input 2 Buffered DAC-A Output. Analog Pin Used For Digital Input 231 This pin also has digital mux functions which are described in the GPIO section of this table. |
| A1 B7 CMP1_HP4 CMP1_LP4 DACB_OUT AIO232 | 0, 4, 8, 12 | 22 | 18 | 14 | 14 | 10 | I I I I O I | ADC-A Input 1 ADC-B Input 7 CMPSS-1 High Comparator Positive Input 4 CMPSS-1 Low Comparator Positive Input 4 Buffered DAC-B Output. Analog Pin Used For Digital Input 232 This pin also has digital mux functions which are described in the GPIO section of this table. |
| A2 B6 C9 CMP1_HP0 CMP1_LP0 AIO224 | 0, 4, 8, 12 | 17 | 13 | 9 | 9 | 6 | I I I I I I | ADC-A Input 2 ADC-B Input 6 ADC-C Input 9 CMPSS-1 High Comparator Positive Input 0 CMPSS-1 Low Comparator Positive Input 0 Analog Pin Used For Digital Input 224 This pin also has digital mux functions which are described in the GPIO section of this table. |
| A3 CMP3_HP5 CMP3_LP5 AIO229 | 0, 4, 8, 12 | 18 | | | | | I I I I | ADC-A Input 3 CMPSS-3 High Comparator Positive Input 5 CMPSS-3 Low Comparator Positive Input 5 Analog Pin Used For Digital Input 229 |
| A3 CMP3_HP5 CMP3_LP5 | | | 12 | 8 | 8 | 5 | I I I | ADC-A Input 3 CMPSS-3 High Comparator Positive Input 5 CMPSS-3 Low Comparator Positive Input 5 |
| A4 B8 CMP2_HP0 CMP2_LP0 AIO225 | 0, 4, 8, 12 | 36 | 27 | 23 | 23 | 19 | I I I I I | ADC-A Input 4 ADC-B Input 8 CMPSS-2 High Comparator Positive Input 0 CMPSS-2 Low Comparator Positive Input 0 Analog Pin Used For Digital Input 225 This pin also has digital mux functions which are described in the GPIO section of this table. |
| A5 CMP2_HP5 CMP2_LP5 AIO249 | 0, 4, 8, 12 | 35 | | | | | I I I I | ADC-A Input 5 CMPSS-2 High Comparator Positive Input 5 CMPSS-2 Low Comparator Positive Input 5 Analog Pin Used For Digital Input 249 |
| A5 CMP2_HP5 CMP2_LP5 | | | 17 | 13 | 13 | 9 | I I I | ADC-A Input 5 CMPSS-2 High Comparator Positive Input 5 CMPSS-2 Low Comparator Positive Input 5 |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 100 PZ | 80 PN | 64 PMQ | 64 PM | 48 PT | PIN TYPE | DESCRIPTION |
|--|--------------|--------|-------|--------|-------|-------|---|---|
| A6 CMP1_HP2 CMP1_LP2 AIO228 | 0, 4, 8, 12 | 14 | 10 | 6 | 6 | 4 | I I I I | ADC-A Input 6 CMPSS-1 High Comparator Positive Input 2 CMPSS-1 Low Comparator Positive Input 2 Analog Pin Used For Digital Input 228 This pin also has digital mux functions which are described in the GPIO section of this table. |
| A8 CMP4_HP4 CMP4_LP4 AIO240 | 0, 4, 8, 12 | 37 | | | | | I I I I | ADC-A Input 8 CMPSS-4 High Comparator Positive Input 4 CMPSS-4 Low Comparator Positive Input 4 Analog Pin Used For Digital Input 240 This pin also has digital mux functions which are described in the GPIO section of this table. |
| A8 CMP4_HP4 CMP4_LP4 AIO241 | 0, 4, 8, 12 | | 24 | 20 | 20 | 16 | I I I I | ADC-A Input 8 CMPSS-4 High Comparator Positive Input 4 CMPSS-4 Low Comparator Positive Input 4 Analog Pin Used For Digital Input 241 This pin also has digital mux functions which are described in the GPIO section of this table. |
| A9 CMP2_HP2 CMP2_LP2 AIO227 | 0, 4, 8, 12 | 38 | 28 | 24 | 24 | 20 | I I I I | ADC-A Input 9 CMPSS-2 High Comparator Positive Input 2 CMPSS-2 Low Comparator Positive Input 2 Analog Pin Used For Digital Input 227 This pin also has digital mux functions which are described in the GPIO section of this table. |
| A10 B1 C10 CMP2_HN0 CMP2_HP3 CMP2_LN0 CMP2_LP3 AIO230 | 0, 4, 8, 12 | 40 | 29 | 25 | 25 | 21 | I I I I I I I I I | ADC-A Input 10 ADC-B Input 1 ADC-C Input 10 CMPSS-2 High Comparator Negative Input 0 CMPSS-2 High Comparator Positive Input 3 CMPSS-2 Low Comparator Negative Input 0 CMPSS-2 Low Comparator Positive Input 3 Analog Pin Used For Digital Input 230 This pin also has digital mux functions which are described in the GPIO section of this table. |
| A11 B10 C0 CMP1_HN1 CMP1_HP1 CMP1_LN1 CMP1_LP1 AIO237 | 0, 4, 8, 12 | 20 | 16 | 12 | 12 | 8 | I I I I I I I I I | ADC-A Input 11 ADC-B Input 10 ADC-C Input 0 CMPSS-1 High Comparator Negative Input 1 CMPSS-1 High Comparator Positive Input 1 CMPSS-1 Low Comparator Negative Input 1 CMPSS-1 Low Comparator Positive Input 1 Analog Pin Used For Digital Input 237 This pin also has digital mux functions which are described in the GPIO section of this table. |
| A12 CMP2_HN1 CMP2_HP1 CMP2_LN1 CMP2_LP1 AIO238 | 0, 4, 8, 12 | 28 | 22 | 18 | 18 | 14 | I I I I I I | ADC-A Input 12 CMPSS-2 High Comparator Negative Input 1 CMPSS-2 High Comparator Positive Input 1 CMPSS-2 Low Comparator Negative Input 1 CMPSS-2 Low Comparator Positive Input 1 Analog Pin Used For Digital Input 238 This pin also has digital mux functions which are described in the GPIO section of this table. |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 100 PZ | 80 PN | 64 PMQ | 64 PM | 48 PT | PIN TYPE | DESCRIPTION |
|--|--------------|--------|-------|--------|-------|-------|----------|--|
| A14 B14 C4 CMP3_HP4 CMP3_LP4 AIO239 | 0, 4, 8, 12 | 19 | 15 | 11 | 11 | | I | ADC-A Input 14 ADC-B Input 14 ADC-C Input 4 CMPSS-3 High Comparator Positive Input 4 CMPSS-3 Low Comparator Positive Input 4 Analog Pin Used For Digital Input 239 This pin also has digital mux functions which are described in the GPIO section of this table. |
| A15 CMP1_HN0 CMP1_HP3 CMP1_LN0 CMP1_LP3 AIO233 | 0, 4, 8, 12 | | 14 | 10 | 10 | 7 | I | ADC-A Input 15 CMPSS-1 High Comparator Negative Input 0 CMPSS-1 High Comparator Positive Input 3 CMPSS-1 Low Comparator Negative Input 0 CMPSS-1 Low Comparator Positive Input 3 Analog Pin Used For Digital Input 233 This pin also has digital mux functions which are described in the GPIO section of this table. |
| B0 C11 CMP2_HP4 CMP2_LP4 AIO253 | 0, 4, 8, 12 | 41 | | | | | I | ADC-B Input 0 ADC-C Input 11 CMPSS-2 High Comparator Positive Input 4 CMPSS-2 Low Comparator Positive Input 4 Analog Pin Used For Digital Input 253 |
| B0 C11 CMP2_HP4 CMP2_LP4 | | | 24 | 20 | 20 | 16 | I | ADC-B Input 0 ADC-C Input 11 CMPSS-2 High Comparator Positive Input 4 CMPSS-2 Low Comparator Positive Input 4 |
| B2 C6 CMP3_HP0 CMP3_LP0 AIO226 | 0, 4, 8, 12 | 15 | 11 | 7 | 7 | 4 | I | ADC-B Input 2 ADC-C Input 6 CMPSS-3 High Comparator Positive Input 0 CMPSS-3 Low Comparator Positive Input 0 Analog Pin Used For Digital Input 226 This pin also has digital mux functions which are described in the GPIO section of this table. |
| B3 CMP3_HN0 CMP3_HP3 CMP3_LN0 CMP3_LP3 VDAC AIO242 | 0, 4, 8, 12 | 16 | 12 | 8 | 8 | 5 | I | ADC-B Input 3 CMPSS-3 High Comparator Negative Input 0 CMPSS-3 High Comparator Positive Input 3 CMPSS-3 Low Comparator Negative Input 0 CMPSS-3 Low Comparator Positive Input 3 Optional external reference voltage for on-chip DACs. Analog Pin Used For Digital Input 242 This pin also has digital mux functions which are described in the GPIO section of this table. |
| B4 C8 CMP4_HP0 CMP4_LP0 AIO236 | 0, 4, 8, 12 | 39 | 28 | 24 | 24 | 20 | I | ADC-B Input 4 ADC-C Input 8 CMPSS-4 High Comparator Positive Input 0 CMPSS-4 Low Comparator Positive Input 0 Analog Pin Used For Digital Input 236 |
| B5 CMP1_HP5 CMP1_LP5 AIO252 | 0, 4, 8, 12 | 32 | | | | | I | ADC-B Input 5 CMPSS-1 High Comparator Positive Input 5 CMPSS-1 Low Comparator Positive Input 5 Analog Pin Used For Digital Input 252 This pin also has digital mux functions which are described in the GPIO section of this table. |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 100 PZ | 80 PN | 64 PMQ | 64 PM | 48 PT | PIN TYPE | DESCRIPTION |
|---|--------------|--------|-------|--------|-------|-------|---------------------------------|---|
| B5 CMP1_HP5 CMP1_LP5 GPIO20 | | 48 | 33 | | | | I I I I/O | ADC-B Input 5 CMPSS-1 High Comparator Positive Input 5 CMPSS-1 Low Comparator Positive Input 5 General-Purpose Input Output 20 This pin also has digital mux functions which are described in the GPIO section of this table. |
| B11 CMP4_HP5 CMP4_LP5 AIO251 | 0, 4, 8, 12 | 30 | | | | | I I I I | ADC-B Input 11 CMPSS-4 High Comparator Positive Input 5 CMPSS-4 Low Comparator Positive Input 5 Analog Pin Used For Digital Input 251 |
| B11 CMP4_HP5 CMP4_LP5 GPIO21 | | 49 | 34 | | | | I I I I/O | ADC-B Input 11 CMPSS-4 High Comparator Positive Input 5 CMPSS-4 Low Comparator Positive Input 5 General-Purpose Input Output 21 This pin also has digital mux functions which are described in the GPIO section of this table. |
| C1 CMP4_HP2 CMP4_LP2 AIO248 | 0, 4, 8, 12 | 29 | 22 | 18 | 18 | 14 | I I I I | ADC-C Input 1 CMPSS-4 High Comparator Positive Input 2 CMPSS-4 Low Comparator Positive Input 2 Analog Pin Used For Digital Input 248 |
| AIO248 | | 29 | 22 | 18 | 18 | 14 | I | Analog Pin Used For Digital Input 248 |
| B12 C2 CMP3_HN1 CMP3_HP1 CMP3_LN1 CMP3_LP1 AIO244 | 0, 4, 8, 12 | 21 | 17 | 13 | 13 | 9 | I I I I I I I | ADC-B Input 12 ADC-C Input 2 CMPSS-3 High Comparator Negative Input 1 CMPSS-3 High Comparator Positive Input 1 CMPSS-3 Low Comparator Negative Input 1 CMPSS-3 Low Comparator Positive Input 1 Analog Pin Used For Digital Input 244 This pin also has digital mux functions which are described in the GPIO section of this table. |
| A7 C3 CMP4_HN1 CMP4_HP1 CMP4_LN1 CMP4_LP1 AIO245 | 0, 4, 8, 12 | 31 | 23 | 19 | 19 | 15 | I I I I I I I | ADC-A Input 7 ADC-C Input 3 CMPSS-4 High Comparator Negative Input 1 CMPSS-4 High Comparator Positive Input 1 CMPSS-4 Low Comparator Negative Input 1 CMPSS-4 Low Comparator Positive Input 1 Analog Pin Used For Digital Input 245 This pin also has digital mux functions which are described in the GPIO section of this table. |
| C5 | | 28 | 12 | 8 | 8 | 5 | I | ADC-C Input 5 |
| B9 C7 | | 18 | 14 | 10 | 10 | 7 | I I | ADC-B Input 9 ADC-C Input 7 |
| C14 CMP4_HN0 CMP4_HP3 CMP4_LN0 CMP4_LP3 AIO247 | 0, 4, 8, 12 | 42 | | | | | I I I I I I | ADC-C Input 14 CMPSS-4 High Comparator Negative Input 0 CMPSS-4 High Comparator Positive Input 3 CMPSS-4 Low Comparator Negative Input 0 CMPSS-4 Low Comparator Positive Input 3 Analog Pin Used For Digital Input 247 |
| C14 CMP4_HN0 CMP4_HP3 CMP4_LN0 CMP4_LP3 | | | 27 | 23 | 23 | 19 | I I I I | ADC-C Input 14 CMPSS-4 High Comparator Negative Input 0 CMPSS-4 High Comparator Positive Input 3 CMPSS-4 Low Comparator Negative Input 0 CMPSS-4 Low Comparator Positive Input 3 |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 100 PZ | 80 PN | 64 PMQ | 64 PM | 48 PT | PIN TYPE | DESCRIPTION |
|--------------|--------------|--------|-------|--------|-------|-------|----------|---|
| VREFHI | | 24, 25 | 20 | 16 | 16 | 12 | I | ADC High Reference. In external reference mode, externally drive the high reference voltage onto this pin. In internal reference mode, a voltage is driven onto this pin by the device. In either mode, place at least a 2.2- μ F capacitor on this pin. This capacitor should be placed as close to the device as possible between the VREFHI and VREFLO pins. |
| VREFLO | | 26, 27 | 21 | 17 | 17 | 13 | I | ADC Low Reference |
| GPIO | | | | | | | | |
| AIO231 | 0, 4, 8, 12 | 23 | 19 | 15 | 15 | 11 | I | Analog Pin Used For Digital Input 231 This pin also has analog functions which are described in the ANALOG section of this table. |
| SD1_C1 | 2 | | | | | | I | SDFM-1 Channel 1 Clock Input |
| HIC_BASESEL1 | 15 | | | | | | I | HIC Base address range select 1 |
| AIO232 | 0, 4, 8, 12 | 22 | 18 | 14 | 14 | 10 | I | Analog Pin Used For Digital Input 232 This pin also has analog functions which are described in the ANALOG section of this table. |
| SD1_D4 | 2 | | | | | | I | SDFM-1 Channel 4 Data Input |
| HIC_BASESEL0 | 15 | | | | | | I | HIC Base address range select 0 |
| AIO224 | 0, 4, 8, 12 | 17 | 13 | 9 | 9 | 6 | I | Analog Pin Used For Digital Input 224 This pin also has analog functions which are described in the ANALOG section of this table. |
| SD2_D3 | 2 | | | | | | I | SDFM-2 Channel 3 Data Input |
| HIC_A3 | 15 | | | | | | I | HIC Address 3 |
| AIO225 | 0, 4, 8, 12 | 36 | 27 | 23 | 23 | 19 | I | Analog Pin Used For Digital Input 225 This pin also has analog functions which are described in the ANALOG section of this table. |
| SD2_C2 | 2 | | | | | | I | SDFM-2 Channel 2 Clock Input |
| HIC_NWE | 15 | | | | | | I | HIC Data Write enable from host |
| AIO228 | 0, 4, 8, 12 | 14 | 10 | 6 | 6 | 4 | I | Analog Pin Used For Digital Input 228 This pin also has analog functions which are described in the ANALOG section of this table. |
| SD2_C1 | 2 | | | | | | I | SDFM-2 Channel 1 Clock Input |
| HIC_A0 | 15 | | | | | | I | HIC Address 0 |
| AIO240 | 0, 4, 8, 12 | 37 | | | | | I | Analog Pin Used For Digital Input 240 This pin also has analog functions which are described in the ANALOG section of this table. |
| SD2_C1 | 2 | | | | | | I | SDFM-2 Channel 1 Clock Input |
| HIC_NBE1 | 15 | | | | | | I | HIC Byte enable 1 |
| AIO241 | 0, 4, 8, 12 | | 24 | 20 | 20 | 16 | I | Analog Pin Used For Digital Input 241 This pin also has analog functions which are described in the ANALOG section of this table. |
| SD2_C1 | 2 | | | | | | I | SDFM-2 Channel 1 Clock Input |
| HIC_NBE1 | 15 | | | | | | I | HIC Byte enable 1 |
| AIO227 | 0, 4, 8, 12 | 38 | 28 | 24 | 24 | 20 | I | Analog Pin Used For Digital Input 227 This pin also has analog functions which are described in the ANALOG section of this table. |
| SD1_C3 | 2 | | | | | | I | SDFM-1 Channel 3 Clock Input |
| HIC_NBE0 | 15 | | | | | | I | HIC Byte enable 0 |
| AIO230 | 0, 4, 8, 12 | 40 | 29 | 25 | 25 | 21 | I | Analog Pin Used For Digital Input 230 This pin also has analog functions which are described in the ANALOG section of this table. |
| SD1_C4 | 2 | | | | | | I | SDFM-1 Channel 4 Clock Input |
| HIC_BASESEL2 | 15 | | | | | | I | HIC Base address range select 2 |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 100 PZ | 80 PN | 64 PMQ | 64 PM | 48 PT | PIN TYPE | DESCRIPTION |
|-----------------|--------------|--------|-------|--------|-------|-------|----------|---|
| AIO237 | 0, 4, 8, 12 | 20 | 16 | 12 | 12 | 8 | I | Analog Pin Used For Digital Input 237 This pin also has analog functions which are described in the ANALOG section of this table. |
| SD1_D2 | 2 | | | | | | I | SDFM-1 Channel 2 Data Input |
| HIC_A6 | 15 | | | | | | I | HIC Address 6 |
| AIO238 | 0, 4, 8, 12 | 28 | 22 | 18 | 18 | 14 | I | Analog Pin Used For Digital Input 238 This pin also has analog functions which are described in the ANALOG section of this table. |
| SD2_C3 | 2 | | | | | | I | SDFM-2 Channel 3 Clock Input |
| HIC_NCS | 15 | | | | | | I | HIC Chip select input |
| AIO239 | 0, 4, 8, 12 | 19 | 15 | 11 | 11 | | I | Analog Pin Used For Digital Input 239 This pin also has analog functions which are described in the ANALOG section of this table. |
| SD1_D1 | 2 | | | | | | I | SDFM-1 Channel 1 Data Input |
| HIC_A5 | 15 | | | | | | I | HIC Address 5 |
| AIO233 | 0, 4, 8, 12 | | 14 | 10 | 10 | 7 | I | Analog Pin Used For Digital Input 233 This pin also has analog functions which are described in the ANALOG section of this table. |
| SD2_D1 | 2 | | | | | | I | SDFM-2 Channel 1 Data Input |
| HIC_A4 | 15 | | | | | | I | HIC Address 4 |
| AIO226 | 0, 4, 8, 12 | 15 | 11 | 7 | 7 | 4 | I | Analog Pin Used For Digital Input 226 This pin also has analog functions which are described in the ANALOG section of this table. |
| SD2_D4 | 2 | | | | | | I | SDFM-2 Channel 4 Data Input |
| HIC_A1 | 15 | | | | | | I | HIC Address 1 |
| AIO242 | 0, 4, 8, 12 | 16 | 12 | 8 | 8 | 5 | I | Analog Pin Used For Digital Input 242 This pin also has analog functions which are described in the ANALOG section of this table. |
| SD2_D2 | 2 | | | | | | I | SDFM-2 Channel 2 Data Input |
| HIC_A2 | 15 | | | | | | I | HIC Address 2 |
| AIO252 | 0, 4, 8, 12 | 32 | | | | | I | Analog Pin Used For Digital Input 252 This pin also has analog functions which are described in the ANALOG section of this table. |
| SD2_C4 | 2 | | | | | | I | SDFM-2 Channel 4 Clock Input |
| AIO244 | 0, 4, 8, 12 | 21 | 17 | 13 | 13 | 9 | I | Analog Pin Used For Digital Input 244 This pin also has analog functions which are described in the ANALOG section of this table. |
| SD1_D3 | 2 | | | | | | I | SDFM-1 Channel 3 Data Input |
| HIC_A7 | 15 | | | | | | I | HIC Address 7 |
| AIO245 | 0, 4, 8, 12 | 31 | 23 | 19 | 19 | 15 | I | Analog Pin Used For Digital Input 245 This pin also has analog functions which are described in the ANALOG section of this table. |
| SD1_C2 | 2 | | | | | | I | SDFM-1 Channel 2 Clock Input |
| HIC_NOE | 15 | | | | | | O | HIC Output enable for data bus |
| GPIO0 | 0, 4, 8, 12 | 79 | 63 | 52 | 52 | 42 | I/O | General-Purpose Input Output 0 |
| EPWM1_A | 1 | | | | | | O | ePWM-1 Output A |
| I2CA_SDA | 6 | | | | | | I/OD | I2C-A Open-Drain Bidirectional Data |
| SPIA_STE | 7 | | | | | | I/O | SPI-A Slave Transmit Enable (STE) |
| FSIRXA_CLK | 9 | | | | | | I | FSIRX-A Input Clock |
| MCAN_RX | 10 | | | | | | I | CAN/CAN FD Receive |
| CLB_OUTPUTXBAR8 | 11 | | | | | | O | CLB Output X-BAR Output 8 |
| EQEP1_INDEX | 13 | | | | | | I/O | eQEP-1 Index |
| HIC_D7 | 14 | | | | | | I/O | HIC Data 7 |
| HIC_BASESEL1 | 15 | | | | | | I | HIC Base address range select 1 |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 100 PZ | 80 PN | 64 PMQ | 64 PM | 48 PT | PIN TYPE | DESCRIPTION |
|-----------------|--------------|--------|-------|--------|-------|-------|----------|---|
| GPIO1 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 1 |
| EPWM1_B | 1 | | | | | | O | ePWM-1 Output B |
| I2CA_SCL | 6 | | | | | | I/OD | I2C-A Open-Drain Bidirectional Clock |
| SPIA_SOMI | 7 | | | | | | I/O | SPI-A Slave Out, Master In (SOMI) |
| MCAN_TX | 10 | 78 | 62 | 51 | 51 | 41 | O | CAN/CAN FD Transmit |
| CLB_OUTPUTXBAR7 | 11 | | | | | | O | CLB Output X-BAR Output 7 |
| HIC_A2 | 13 | | | | | | I | HIC Address 2 |
| FSITXA_TDM_D1 | 14 | | | | | | I | FSITX-A Time Division Multiplexed Additional Data Input |
| HIC_D10 | 15 | | | | | | I/O | HIC Data 10 |
| GPIO2 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 2 |
| EPWM2_A | 1 | | | | | | O | ePWM-2 Output A |
| OUTPUTXBAR1 | 5 | | | | | | O | Output X-BAR Output 1 |
| PMBUSA_SDA | 6 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Data |
| SPIA_SIMO | 7 | | | | | | I/O | SPI-A Slave In, Master Out (SIMO) |
| SCIA_TX | 9 | 77 | 61 | 50 | 50 | 40 | O | SCI-A Transmit Data |
| FSIRXA_D1 | 10 | | | | | | I | FSIRX-A Optional Additional Data Input |
| I2CB_SDA | 11 | | | | | | I/OD | I2C-B Open-Drain Bidirectional Data |
| HIC_A1 | 13 | | | | | | I | HIC Address 1 |
| CANA_TX | 14 | | | | | | O | CAN-A Transmit |
| HIC_D9 | 15 | | | | | | I/O | HIC Data 9 |
| GPIO3 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 3 |
| EPWM2_B | 1 | | | | | | O | ePWM-2 Output B |
| OUTPUTXBAR2 | 2, 5 | | | | | | O | Output X-BAR Output 2 |
| PMBUSA_SCL | 6 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Clock |
| SPIA_CLK | 7 | | | | | | I/O | SPI-A Clock |
| SCIA_RX | 9 | 76 | 60 | 49 | 49 | 39 | I | SCI-A Receive Data |
| FSIRXA_D0 | 10 | | | | | | I | FSIRX-A Primary Data Input |
| I2CB_SCL | 11 | | | | | | I/OD | I2C-B Open-Drain Bidirectional Clock |
| HIC_NOE | 13 | | | | | | O | HIC Output enable for data bus |
| CANA_RX | 14 | | | | | | I | CAN-A Receive |
| HIC_D4 | 15 | | | | | | I/O | HIC Data 4 |
| GPIO4 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 4 |
| EPWM3_A | 1 | | | | | | O | ePWM-3 Output A |
| MCAN_TX | 3 | | | | | | O | CAN/CAN FD Transmit |
| OUTPUTXBAR3 | 5 | | | | | | O | Output X-BAR Output 3 |
| CANA_TX | 6 | | | | | | O | CAN-A Transmit |
| SPIB_CLK | 7 | 75 | 59 | 48 | 48 | 38 | I/O | SPI-B Clock |
| EQEP2_STROBE | 9 | | | | | | I/O | eQEP-2 Strobe |
| FSIRXA_CLK | 10 | | | | | | I | FSIRX-A Input Clock |
| CLB_OUTPUTXBAR6 | 11 | | | | | | O | CLB Output X-BAR Output 6 |
| HIC_BASESEL2 | 13 | | | | | | I | HIC Base address range select 2 |
| HIC_NWE | 15 | | | | | | I | HIC Data Write enable from host |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 100 PZ | 80 PN | 64 PMQ | 64 PM | 48 PT | PIN TYPE | DESCRIPTION |
|-----------------|--------------|--------|-------|--------|-------|-------|----------|---|
| GPIO5 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 5 |
| EPWM3_B | 1 | | | | | | O | ePWM-3 Output B |
| OUTPUTXBAR3 | 3 | | | | | | O | Output X-BAR Output 3 |
| MCAN_RX | 5 | | | | | | I | CAN/CAN FD Receive |
| CANA_RX | 6 | | | | | | I | CAN-A Receive |
| SPIA_STE | 7 | 89 | 74 | 61 | 61 | 47 | I/O | SPI-A Slave Transmit Enable (STE) |
| FSITXA_D1 | 9 | | | | | | O | FSITX-A Optional Additional Data Output |
| CLB_OUTPUTXBAR5 | 10 | | | | | | O | CLB Output X-BAR Output 5 |
| HIC_A7 | 13 | | | | | | I | HIC Address 7 |
| HIC_D4 | 14 | | | | | | I/O | HIC Data 4 |
| HIC_D15 | 15 | | | | | | I/O | HIC Data 15 |
| GPIO6 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 6 |
| EPWM4_A | 1 | | | | | | O | ePWM-4 Output A |
| OUTPUTXBAR4 | 2 | | | | | | O | Output X-BAR Output 4 |
| SYNCOU | 3 | | | | | | O | External ePWM Synchronization Pulse |
| EQEP1_A | 5 | | | | | | I | eQEP-1 Input A |
| SPIB_SOMI | 7 | 97 | 80 | 64 | 64 | 48 | I/O | SPI-B Slave Out, Master In (SOMI) |
| FSITXA_D0 | 9 | | | | | | O | FSITX-A Primary Data Output |
| FSITXA_D1 | 11 | | | | | | O | FSITX-A Optional Additional Data Output |
| HIC_NBE1 | 13 | | | | | | I | HIC Byte enable 1 |
| CLB_OUTPUTXBAR8 | 14 | | | | | | O | CLB Output X-BAR Output 8 |
| HIC_D14 | 15 | | | | | | I/O | HIC Data 14 |
| GPIO7 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 7 |
| EPWM4_B | 1 | | | | | | O | ePWM-4 Output B |
| OUTPUTXBAR5 | 3 | | | | | | O | Output X-BAR Output 5 |
| EQEP1_B | 5 | | | | | | I | eQEP-1 Input B |
| SPIB_SIMO | 7 | 84 | 68 | 57 | 57 | 43 | I/O | SPI-B Slave In, Master Out (SIMO) |
| FSITXA_CLK | 9 | | | | | | O | FSITX-A Output Clock |
| CLB_OUTPUTXBAR2 | 10 | | | | | | O | CLB Output X-BAR Output 2 |
| HIC_A6 | 13 | | | | | | I | HIC Address 6 |
| HIC_D14 | 15 | | | | | | I/O | HIC Data 14 |
| GPIO8 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 8 |
| EPWM5_A | 1 | | | | | | O | ePWM-5 Output A |
| ADCSOCAO | 3 | | | | | | O | ADC Start of Conversion A for External ADC |
| EQEP1_STROBE | 5 | | | | | | I/O | eQEP-1 Strobe |
| SCIA_TX | 6 | | | | | | O | SCI-A Transmit Data |
| SPIA_SIMO | 7 | | | | | | I/O | SPI-A Slave In, Master Out (SIMO) |
| I2CA_SCL | 9 | 74 | 58 | 47 | 47 | | I/OD | I2C-A Open-Drain Bidirectional Clock |
| FSITXA_D1 | 10 | | | | | | O | FSITX-A Optional Additional Data Output |
| CLB_OUTPUTXBAR5 | 11 | | | | | | O | CLB Output X-BAR Output 5 |
| HIC_A0 | 13 | | | | | | I | HIC Address 0 |
| FSITXA_TDM_CLK | 14 | | | | | | I | FSITX-A Time Division Multiplexed Clock Input |
| HIC_D8 | 15 | | | | | | I/O | HIC Data 8 |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 100 PZ | 80 PN | 64 PMQ | 64 PM | 48 PT | PIN TYPE | DESCRIPTION |
|-----------------|--------------|--------|-------|--------|-------|-------|----------|--|
| GPIO9 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 9 |
| EPWM5_B | 1 | | | | | | O | ePWM-5 Output B |
| SCIB_TX | 2 | | | | | | O | SCI-B Transmit Data |
| OUTPUTXBAR6 | 3 | | | | | | O | Output X-BAR Output 6 |
| EQEP1_INDEX | 5 | | | | | | I/O | eQEP-1 Index |
| SCIA_RX | 6 | 90 | 75 | 62 | 62 | | I | SCI-A Receive Data |
| SPIA_CLK | 7 | | | | | | I/O | SPI-A Clock |
| FSITXA_D0 | 10 | | | | | | O | FSITX-A Primary Data Output |
| LINB_RX | 11 | | | | | | I | LIN-B Receive |
| HIC_BASESEL0 | 13 | | | | | | I | HIC Base address range select 0 |
| I2CB_SCL | 14 | | | | | | I/OD | I2C-B Open-Drain Bidirectional Clock |
| HIC_NRDY | 15 | | | | | | O | HIC Ready from device to host |
| GPIO10 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 10 |
| EPWM6_A | 1 | | | | | | O | ePWM-6 Output A |
| ADCSOCBO | 3 | | | | | | O | ADC Start of Conversion B for External ADC |
| EQEP1_A | 5 | | | | | | I | eQEP-1 Input A |
| SCIB_TX | 6 | | | | | | O | SCI-B Transmit Data |
| SPIA_SOMI | 7 | 93 | 76 | 63 | 63 | | I/O | SPI-A Slave Out, Master In (SOMI) |
| I2CA_SDA | 9 | | | | | | I/OD | I2C-A Open-Drain Bidirectional Data |
| FSITXA_CLK | 10 | | | | | | O | FSITX-A Output Clock |
| LINB_TX | 11 | | | | | | O | LIN-B Transmit |
| HIC_NWE | 13 | | | | | | I | HIC Data Write enable from host |
| FSITXA_TDM_D0 | 14 | | | | | | I | FSITX-A Time Division Multiplexed Data Input |
| CLB_OUTPUTXBAR4 | 15 | | | | | | O | CLB Output X-BAR Output 4 |
| GPIO11 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 11 |
| EPWM6_B | 1 | | | | | | O | ePWM-6 Output B |
| OUTPUTXBAR7 | 3 | | | | | | O | Output X-BAR Output 7 |
| EQEP1_B | 5 | | | | | | I | eQEP-1 Input B |
| SCIB_RX | 6 | | | | | | I | SCI-B Receive Data |
| SPIA_STE | 7 | 52 | 37 | 31 | 31 | | I/O | SPI-A Slave Transmit Enable (STE) |
| FSIRXA_D1 | 9 | | | | | | I | FSIRX-A Optional Additional Data Input |
| LINB_RX | 10 | | | | | | I | LIN-B Receive |
| EQEP2_A | 11 | | | | | | I | eQEP-2 Input A |
| SPIA_SIMO | 13 | | | | | | I/O | SPI-A Slave In, Master Out (SIMO) |
| HIC_D6 | 14 | | | | | | I/O | HIC Data 6 |
| HIC_NBE0 | 15 | | | | | | I | HIC Byte enable 0 |
| GPIO12 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 12 |
| EPWM7_A | 1 | | | | | | O | ePWM-7 Output A |
| MCAN_RX | 3 | | | | | | I | CAN/CAN FD Receive |
| EQEP1_STROBE | 5 | | | | | | I/O | eQEP-1 Strobe |
| SCIB_TX | 6 | | | | | | O | SCI-B Transmit Data |
| PMBUSA_CTL | 7 | 51 | 36 | 30 | 30 | | I/O | PMBus-A Control Signal - Slave Input/Master Output |
| FSIRXA_D0 | 9 | | | | | | I | FSIRX-A Primary Data Input |
| LINB_TX | 10 | | | | | | O | LIN-B Transmit |
| SPIA_CLK | 11 | | | | | | I/O | SPI-A Clock |
| CANA_RX | 13 | | | | | | I | CAN-A Receive |
| HIC_D13 | 14 | | | | | | I/O | HIC Data 13 |
| HIC_INT | 15 | | | | | | O | HIC Device interrupt to host |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 100 PZ | 80 PN | 64 PMQ | 64 PM | 48 PT | PIN TYPE | DESCRIPTION |
|-----------------|--------------|--------|-------|--------|-------|-------|----------|---|
| GPIO13 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 13 |
| EPWM7_B | 1 | | | | | | O | ePWM-7 Output B |
| MCAN_TX | 3 | | | | | | O | CAN/CAN FD Transmit |
| EQEP1_INDEX | 5 | | | | | | I/O | eQEP-1 Index |
| SCIB_RX | 6 | | | | | | I | SCI-B Receive Data |
| PMBUSA_ALERT | 7 | 50 | 35 | 29 | 29 | | I/OD | PMBus-A Open-Drain Bidirectional Alert Signal |
| FSIRXA_CLK | 9 | | | | | | I | FSIRX-A Input Clock |
| LINB_RX | 10 | | | | | | I | LIN-B Receive |
| SPIA_SOMI | 11 | | | | | | I/O | SPI-A Slave Out, Master In (SOMI) |
| CANA_TX | 13 | | | | | | O | CAN-A Transmit |
| HIC_D11 | 14 | | | | | | I/O | HIC Data 11 |
| HIC_D5 | 15 | | | | | | I/O | HIC Data 5 |
| GPIO14 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 14 |
| EPWM8_A | 1 | | | | | | O | ePWM-8 Output A |
| SCIB_TX | 2 | | | | | | O | SCI-B Transmit Data |
| I2CB_SDA | 5 | | | | | | I/OD | I2C-B Open-Drain Bidirectional Data |
| OUTPUTXBAR3 | 6 | | | | | | O | Output X-BAR Output 3 |
| PMBUSA_SDA | 7 | 96 | 79 | | | | I/OD | PMBus-A Open-Drain Bidirectional Data |
| SPIB_CLK | 9 | | | | | | I/O | SPI-B Clock |
| EQEP2_A | 10 | | | | | | I | eQEP-2 Input A |
| LINB_TX | 11 | | | | | | O | LIN-B Transmit |
| EPWM3_A | 13 | | | | | | O | ePWM-3 Output A |
| CLB_OUTPUTXBAR7 | 14 | | | | | | O | CLB Output X-BAR Output 7 |
| HIC_D15 | 15 | | | | | | I/O | HIC Data 15 |
| GPIO15 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 15 |
| EPWM8_B | 1 | | | | | | O | ePWM-8 Output B |
| SCIB_RX | 2 | | | | | | I | SCI-B Receive Data |
| I2CB_SCL | 5 | | | | | | I/OD | I2C-B Open-Drain Bidirectional Clock |
| OUTPUTXBAR4 | 6 | | | | | | O | Output X-BAR Output 4 |
| PMBUSA_SCL | 7 | 95 | 78 | | | | I/OD | PMBus-A Open-Drain Bidirectional Clock |
| SPIB_STE | 9 | | | | | | I/O | SPI-B Slave Transmit Enable (STE) |
| EQEP2_B | 10 | | | | | | I | eQEP-2 Input B |
| LINB_RX | 11 | | | | | | I | LIN-B Receive |
| EPWM3_B | 13 | | | | | | O | ePWM-3 Output B |
| CLB_OUTPUTXBAR6 | 14 | | | | | | O | CLB Output X-BAR Output 6 |
| HIC_D12 | 15 | | | | | | I/O | HIC Data 12 |
| GPIO16 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 16 |
| SPIA_SIMO | 1 | | | | | | I/O | SPI-A Slave In, Master Out (SIMO) |
| OUTPUTXBAR7 | 3 | | | | | | O | Output X-BAR Output 7 |
| EPWM5_A | 5 | | | | | | O | ePWM-5 Output A |
| SCIA_TX | 6 | | | | | | O | SCI-A Transmit Data |
| SD1_D1 | 7 | | | | | | I | SDFM-1 Channel 1 Data Input |
| EQEP1_STROBE | 9 | 54 | 39 | 33 | 33 | 26 | I/O | eQEP-1 Strobe |
| PMBUSA_SCL | 10 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Clock |
| XCLKOUT | 11 | | | | | | O | External Clock Output. This pin outputs a divided-down version of a chosen clock signal from within the device. |
| EQEP2_B | 13 | | | | | | I | eQEP-2 Input B |
| SPIB_SOMI | 14 | | | | | | I/O | SPI-B Slave Out, Master In (SOMI) |
| HIC_D1 | 15 | | | | | | I/O | HIC Data 1 |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 100 PZ | 80 PN | 64 PMQ | 64 PM | 48 PT | PIN TYPE | DESCRIPTION |
|-----------------|--------------|--------|-------|--------|-------|-------|----------|---|
| GPIO17 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 17 |
| SPIA_SOMI | 1 | | | | | | I/O | SPI-A Slave Out, Master In (SOMI) |
| OUTPUTXBAR8 | 3 | | | | | | O | Output X-BAR Output 8 |
| EPWM5_B | 5 | | | | | | O | ePWM-5 Output B |
| SCIA_RX | 6 | 55 | 40 | 34 | 34 | | I | SCI-A Receive Data |
| SD1_C1 | 7 | | | | | | I | SDFM-1 Channel 1 Clock Input |
| EQEP1_INDEX | 9 | | | | | | I/O | eQEP-1 Index |
| PMBUSA_SDA | 10 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Data |
| CANA_TX | 11 | | | | | | O | CAN-A Transmit |
| HIC_D2 | 15 | | | | | | I/O | HIC Data 2 |
| GPIO18 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 18 |
| SPIA_CLK | 1 | | | | | | I/O | SPI-A Clock |
| SCIB_TX | 2 | | | | | | O | SCI-B Transmit Data |
| CANA_RX | 3 | | | | | | I | CAN-A Receive |
| EPWM6_A | 5 | | | | | | O | ePWM-6 Output A |
| I2CA_SCL | 6 | | | | | | I/OD | I2C-A Open-Drain Bidirectional Clock |
| SD1_D2 | 7 | | | | | | I | SDFM-1 Channel 2 Data Input |
| EQEP2_A | 9 | 68 | 50 | 41 | 41 | 33 | I | eQEP-2 Input A |
| PMBUSA_CTL | 10 | | | | | | I/O | PMBus-A Control Signal - Slave Input/Master Output |
| XCLKOUT | 11 | | | | | | O | External Clock Output. This pin outputs a divided-down version of a chosen clock signal from within the device. |
| LINB_TX | 13 | | | | | | O | LIN-B Transmit |
| FSITXA_TDM_CLK | 14 | | | | | | I | FSITX-A Time Division Multiplexed Clock Input |
| HIC_INT | 15 | | | | | | O | HIC Device interrupt to host |
| X2 | ALT | | | | | | I/O | Crystal oscillator output. |
| GPIO19 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 19 |
| SPIA_STE | 1 | | | | | | I/O | SPI-A Slave Transmit Enable (STE) |
| SCIB_RX | 2 | | | | | | I | SCI-B Receive Data |
| CANA_TX | 3 | | | | | | O | CAN-A Transmit |
| EPWM6_B | 5 | | | | | | O | ePWM-6 Output B |
| I2CA_SDA | 6 | | | | | | I/OD | I2C-A Open-Drain Bidirectional Data |
| SD1_C2 | 7 | | | | | | I | SDFM-1 Channel 2 Clock Input |
| EQEP2_B | 9 | | | | | | I | eQEP-2 Input B |
| PMBUSA_ALERT | 10 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Alert Signal |
| CLB_OUTPUTXBAR1 | 11 | 69 | 51 | 42 | 42 | 34 | O | CLB Output X-BAR Output 1 |
| LINB_RX | 13 | | | | | | I | LIN-B Receive |
| FSITXA_TDM_D0 | 14 | | | | | | I | FSITX-A Time Division Multiplexed Data Input |
| HIC_NBE0 | 15 | | | | | | I | HIC Byte enable 0 |
| X1 | ALT | | | | | | I/O | Crystal oscillator input or single-ended clock input. The device initialization software must configure this pin before the crystal oscillator is enabled. To use this oscillator, a quartz crystal circuit must be connected to X1 and X2. This pin can also be used to feed a single-ended 3.3-V level clock. See the XTAL section for usage details. |
| GPIO20 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 20 This pin also has analog functions which are described in the ANALOG section of this table. |
| EQEP1_A | 1 | 48 | 33 | | | | I | eQEP-1 Input A |
| SPIB_SIMO | 6 | | | | | | I/O | SPI-B Slave In, Master Out (SIMO) |
| SD1_D3 | 7 | | | | | | I | SDFM-1 Channel 3 Data Input |
| MCAN_TX | 9 | | | | | | O | CAN/CAN FD Transmit |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 100 PZ | 80 PN | 64 PMQ | 64 PM | 48 PT | PIN TYPE | DESCRIPTION |
|-----------------|--------------|--------|-------|--------|-------|-------|----------|---|
| GPIO21 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 21 This pin also has analog functions which are described in the ANALOG section of this table. |
| EQEP1_B | 1 | 49 | 34 | | | | I | eQEP-1 Input B |
| SPIB_SOMI | 6 | | | | | | I/O | SPI-B Slave Out, Master In (SOMI) |
| SD1_C3 | 7 | | | | | | I | SDFM-1 Channel 3 Clock Input |
| MCAN_RX | 9 | | | | | | I | CAN/CAN FD Receive |
| GPIO22 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 22 |
| EQEP1_STROBE | 1 | | | | | | I/O | eQEP-1 Strobe |
| SCIB_TX | 3 | | | | | | O | SCI-B Transmit Data |
| SPIB_CLK | 6 | | | | | | I/O | SPI-B Clock |
| SD1_D4 | 7 | | | | | | I | SDFM-1 Channel 4 Data Input |
| LINA_TX | 9 | 83 | 67 | 56 | 56 | | O | LIN-A Transmit |
| CLB_OUTPUTXBAR1 | 10 | | | | | | O | CLB Output X-BAR Output 1 |
| LINB_TX | 11 | | | | | | O | LIN-B Transmit |
| HIC_A5 | 13 | | | | | | I | HIC Address 5 |
| EPWM4_A | 14 | | | | | | O | ePWM-4 Output A |
| HIC_D13 | 15 | | | | | | I/O | HIC Data 13 |
| GPIO23 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 23 |
| EQEP1_INDEX | 1 | | | | | | I/O | eQEP-1 Index |
| SCIB_RX | 3 | | | | | | I | SCI-B Receive Data |
| SPIB_STE | 6 | | | | | | I/O | SPI-B Slave Transmit Enable (STE) |
| SD1_C4 | 7 | | | | | | I | SDFM-1 Channel 4 Clock Input |
| LINA_RX | 9 | 81 | 65 | 54 | 54 | | I | LIN-A Receive |
| CLB_OUTPUTXBAR3 | 10 | | | | | | O | CLB Output X-BAR Output 3 |
| LINB_RX | 11 | | | | | | I | LIN-B Receive |
| HIC_A3 | 13 | | | | | | I | HIC Address 3 |
| EPWM4_B | 14 | | | | | | O | ePWM-4 Output B |
| HIC_D11 | 15 | | | | | | I/O | HIC Data 11 |
| GPIO24 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 24 |
| OUTPUTXBAR1 | 1 | | | | | | O | Output X-BAR Output 1 |
| EQEP2_A | 2 | | | | | | I | eQEP-2 Input A |
| EPWM8_A | 5 | | | | | | O | ePWM-8 Output A |
| SPIB_SIMO | 6 | | | | | | I/O | SPI-B Slave In, Master Out (SIMO) |
| SD2_D1 | 7 | 56 | 41 | 35 | 35 | 27 | I | SDFM-2 Channel 1 Data Input |
| LINB_TX | 9 | | | | | | O | LIN-B Transmit |
| PMBUSA_SCL | 10 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Clock |
| SCIA_TX | 11 | | | | | | O | SCI-A Transmit Data |
| ERRORSTS | 13 | | | | | | O | Error Status Output. This signal requires an external pulldown. |
| HIC_D3 | 15 | | | | | | I/O | HIC Data 3 |
| GPIO25 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 25 |
| OUTPUTXBAR2 | 1 | | | | | | O | Output X-BAR Output 2 |
| EQEP2_B | 2 | | | | | | I | eQEP-2 Input B |
| EQEP1_A | 5 | | | | | | I | eQEP-1 Input A |
| SPIB_SOMI | 6 | | | | | | I/O | SPI-B Slave Out, Master In (SOMI) |
| SD2_C1 | 7 | 57 | 42 | | | | I | SDFM-2 Channel 1 Clock Input |
| FSITXA_D1 | 9 | | | | | | O | FSITX-A Optional Additional Data Output |
| PMBUSA_SDA | 10 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Data |
| SCIA_RX | 11 | | | | | | I | SCI-A Receive Data |
| HIC_BASESEL0 | 14 | | | | | | I | HIC Base address range select 0 |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 100 PZ | 80 PN | 64 PMQ | 64 PM | 48 PT | PIN TYPE | DESCRIPTION |
|--------------|--------------|--------|-------|--------|-------|-------|----------|--|
| GPIO26 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 26 |
| OUTPUTXBAR3 | 1, 5 | | | | | | O | Output X-BAR Output 3 |
| EQEP2_INDEX | 2 | | | | | | I/O | eQEP-2 Index |
| SPIB_CLK | 6 | | | | | | I/O | SPI-B Clock |
| SD2_D2 | 7 | 58 | 43 | | | | I | SDFM-2 Channel 2 Data Input |
| FSITXA_D0 | 9 | | | | | | O | FSITX-A Primary Data Output |
| PMBUSA_CTL | 10 | | | | | | I/O | PMBus-A Control Signal - Slave Input/Master Output |
| I2CA_SDA | 11 | | | | | | I/OD | I2C-A Open-Drain Bidirectional Data |
| HIC_D0 | 14 | | | | | | I/O | HIC Data 0 |
| HIC_A1 | 15 | | | | | | I | HIC Address 1 |
| GPIO27 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 27 |
| OUTPUTXBAR4 | 1, 5 | | | | | | O | Output X-BAR Output 4 |
| EQEP2_STROBE | 2 | | | | | | I/O | eQEP-2 Strobe |
| SPIB_STE | 6 | | | | | | I/O | SPI-B Slave Transmit Enable (STE) |
| SD2_C2 | 7 | 59 | 44 | | | | I | SDFM-2 Channel 2 Clock Input |
| FSITXA_CLK | 9 | | | | | | O | FSITX-A Output Clock |
| PMBUSA_ALERT | 10 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Alert Signal |
| I2CA_SCL | 11 | | | | | | I/OD | I2C-A Open-Drain Bidirectional Clock |
| HIC_D1 | 14 | | | | | | I/O | HIC Data 1 |
| HIC_A4 | 15 | | | | | | I | HIC Address 4 |
| GPIO28 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 28 |
| SCIA_RX | 1 | | | | | | I | SCI-A Receive Data |
| EPWM7_A | 3 | | | | | | O | ePWM-7 Output A |
| OUTPUTXBAR5 | 5 | | | | | | O | Output X-BAR Output 5 |
| EQEP1_A | 6 | | | | | | I | eQEP-1 Input A |
| SD2_D3 | 7 | | | | | | I | SDFM-2 Channel 3 Data Input |
| EQEP2_STROBE | 9 | 1 | 4 | 2 | 2 | 2 | I/O | eQEP-2 Strobe |
| LINA_TX | 10 | | | | | | O | LIN-A Transmit |
| SPIB_CLK | 11 | | | | | | I/O | SPI-B Clock |
| ERRORSTS | 13 | | | | | | O | Error Status Output. This signal requires an external pull-down. |
| I2CB_SDA | 14 | | | | | | I/OD | I2C-B Open-Drain Bidirectional Data |
| HIC_NOE | 15 | | | | | | O | HIC Output enable for data bus |
| GPIO29 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 29 |
| SCIA_TX | 1 | | | | | | O | SCI-A Transmit Data |
| EPWM7_B | 3 | | | | | | O | ePWM-7 Output B |
| OUTPUTXBAR6 | 5 | | | | | | O | Output X-BAR Output 6 |
| EQEP1_B | 6 | | | | | | I | eQEP-1 Input B |
| SD2_C3 | 7 | | | | | | I | SDFM-2 Channel 3 Clock Input |
| EQEP2_INDEX | 9 | 100 | 3 | 1 | 1 | 1 | I/O | eQEP-2 Index |
| LINA_RX | 10 | | | | | | I | LIN-A Receive |
| SPIB_STE | 11 | | | | | | I/O | SPI-B Slave Transmit Enable (STE) |
| ERRORSTS | 13 | | | | | | O | Error Status Output. This signal requires an external pull-down. |
| I2CB_SCL | 14 | | | | | | I/OD | I2C-B Open-Drain Bidirectional Clock |
| HIC_NCS | 15 | | | | | | I | HIC Chip select input |
| AUXCLKIN | ALT | | | | | | I | Auxiliary Clock Input |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 100 PZ | 80 PN | 64 PMQ | 64 PM | 48 PT | PIN TYPE | DESCRIPTION |
|--------------|--------------|--------|-------|--------|-------|-------|----------|--|
| GPIO30 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 30 |
| CANA_RX | 1 | | | | | | I | CAN-A Receive |
| SPIB_SIMO | 3 | | | | | | I/O | SPI-B Slave In, Master Out (SIMO) |
| OUTPUTXBAR7 | 5 | | | | | | O | Output X-BAR Output 7 |
| EQEP1_STROBE | 6 | 98 | 1 | | | | I/O | eQEP-1 Strobe |
| SD2_D4 | 7 | | | | | | I | SDFM-2 Channel 4 Data Input |
| FSIRXA_CLK | 9 | | | | | | I | FSIRX-A Input Clock |
| MCAN_RX | 10 | | | | | | I | CAN/CAN FD Receive |
| EPWM1_A | 11 | | | | | | O | ePWM-1 Output A |
| HIC_D8 | 14 | | | | | | I/O | HIC Data 8 |
| GPIO31 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 31 |
| CANA_TX | 1 | | | | | | O | CAN-A Transmit |
| SPIB_SOMI | 3 | | | | | | I/O | SPI-B Slave Out, Master In (SOMI) |
| OUTPUTXBAR8 | 5 | | | | | | O | Output X-BAR Output 8 |
| EQEP1_INDEX | 6 | 99 | 2 | | | | I/O | eQEP-1 Index |
| SD2_C4 | 7 | | | | | | I | SDFM-2 Channel 4 Clock Input |
| FSIRXA_D1 | 9 | | | | | | I | FSIRX-A Optional Additional Data Input |
| MCAN_TX | 10 | | | | | | O | CAN/CAN FD Transmit |
| EPWM1_B | 11 | | | | | | O | ePWM-1 Output B |
| HIC_D10 | 14 | | | | | | I/O | HIC Data 10 |
| GPIO32 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 32 |
| I2CA_SDA | 1 | | | | | | I/OD | I2C-A Open-Drain Bidirectional Data |
| SPIB_CLK | 3 | | | | | | I/O | SPI-B Clock |
| EPWM8_B | 5 | | | | | | O | ePWM-8 Output B |
| LINA_TX | 6 | | | | | | O | LIN-A Transmit |
| SD1_D2 | 7 | 64 | 49 | 40 | 40 | 32 | I | SDFM-1 Channel 2 Data Input |
| FSIRXA_D0 | 9 | | | | | | I | FSIRX-A Primary Data Input |
| CANA_TX | 10 | | | | | | O | CAN-A Transmit |
| PMBUSA_SDA | 11 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Data |
| ADCSOCBO | 13 | | | | | | O | ADC Start of Conversion B for External ADC |
| HIC_INT | 15 | | | | | | O | HIC Device interrupt to host |
| GPIO33 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 33 |
| I2CA_SCL | 1 | | | | | | I/OD | I2C-A Open-Drain Bidirectional Clock |
| SPIB_STE | 3 | | | | | | I/O | SPI-B Slave Transmit Enable (STE) |
| OUTPUTXBAR4 | 5 | | | | | | O | Output X-BAR Output 4 |
| LINA_RX | 6 | | | | | | I | LIN-A Receive |
| SD1_C2 | 7 | 53 | 38 | 32 | 32 | 25 | I | SDFM-1 Channel 2 Clock Input |
| FSIRXA_CLK | 9 | | | | | | I | FSIRX-A Input Clock |
| CANA_RX | 10 | | | | | | I | CAN-A Receive |
| EQEP2_B | 11 | | | | | | I | eQEP-2 Input B |
| ADCSOCAO | 13 | | | | | | O | ADC Start of Conversion A for External ADC |
| SD1_C1 | 14 | | | | | | I | SDFM-1 Channel 1 Clock Input |
| HIC_D0 | 15 | | | | | | I/O | HIC Data 0 |
| GPIO34 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 34 |
| OUTPUTXBAR1 | 1 | | | | | | O | Output X-BAR Output 1 |
| PMBUSA_SDA | 6 | 94 | 77 | | | | I/OD | PMBus-A Open-Drain Bidirectional Data |
| HIC_NBE1 | 13 | | | | | | I | HIC Byte enable 1 |
| I2CB_SDA | 14 | | | | | | I/OD | I2C-B Open-Drain Bidirectional Data |
| HIC_D9 | 15 | | | | | | I/O | HIC Data 9 |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 100 PZ | 80 PN | 64 PMQ | 64 PM | 48 PT | PIN TYPE | DESCRIPTION |
|-----------------|--------------|--------|-------|--------|-------|-------|----------|---|
| GPIO35 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 35 |
| SCIA_RX | 1 | | | | | | I | SCI-A Receive Data |
| I2CA_SDA | 3 | | | | | | I/OD | I2C-A Open-Drain Bidirectional Data |
| CANA_RX | 5 | | | | | | I | CAN-A Receive |
| PMBUSA_SCL | 6 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Clock |
| LINA_RX | 7 | | | | | | I | LIN-A Receive |
| EQEP1_A | 9 | | | | | | I | eQEP-1 Input A |
| PMBUSA_CTL | 10 | 63 | 48 | 39 | 39 | 31 | I/O | PMBus-A Control Signal - Slave Input/Master Output |
| EPWM5_B | 11 | | | | | | O | ePWM-5 Output B |
| SD2_C1 | 13 | | | | | | I | SDFM-2 Channel 1 Clock Input |
| HIC_NWE | 14 | | | | | | I | HIC Data Write enable from host |
| TDI | 15 | | | | | | I | JTAG Test Data Input (TDI) - TDI is the default mux selection for the pin. The internal pullup is disabled by default. The internal pullup should be enabled or an external pullup added on the board if this pin is used as JTAG TDI to avoid a floating input. |
| GPIO37 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 37 |
| OUTPUTXBAR2 | 1 | | | | | | O | Output X-BAR Output 2 |
| I2CA_SCL | 3 | | | | | | I/OD | I2C-A Open-Drain Bidirectional Clock |
| SCIA_TX | 5 | | | | | | O | SCI-A Transmit Data |
| CANA_TX | 6 | | | | | | O | CAN-A Transmit |
| LINA_TX | 7 | | | | | | O | LIN-A Transmit |
| EQEP1_B | 9 | | | | | | I | eQEP-1 Input B |
| PMBUSA_ALERT | 10 | 61 | 46 | 37 | 37 | 29 | I/OD | PMBus-A Open-Drain Bidirectional Alert Signal |
| HIC_NRDY | 14 | | | | | | O | HIC Ready from device to host |
| TDO | 15 | | | | | | O | JTAG Test Data Output (TDO) - TDO is the default mux selection for the pin. The internal pullup is disabled by default. The TDO function will be in a tri-state condition when there is no JTAG activity, leaving this pin floating; the internal pullup should be enabled or an external pullup added on the board to avoid a floating GPIO input. |
| GPIO39 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 39 |
| MCAN_RX | 6 | | | | | | I | CAN/CAN FD Receive |
| FSIRXA_CLK | 7 | | | | | | I | FSIRX-A Input Clock |
| EQEP2_INDEX | 9 | | 56 | | 46 | | I/O | eQEP-2 Index |
| CLB_OUTPUTXBAR2 | 11 | | | | | | O | CLB Output X-BAR Output 2 |
| SYNCOUT | 13 | | | | | | O | External ePWM Synchronization Pulse |
| EQEP1_INDEX | 14 | | | | | | I/O | eQEP-1 Index |
| HIC_D7 | 15 | | | | | | I/O | HIC Data 7 |
| GPIO40 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 40 |
| SPIB_SIMO | 1 | | | | | | I/O | SPI-B Slave In, Master Out (SIMO) |
| EPWM2_B | 5 | | | | | | O | ePWM-2 Output B |
| PMBUSA_SDA | 6 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Data |
| FSIRXA_D0 | 7 | | | | | | I | FSIRX-A Primary Data Input |
| SCIB_TX | 9 | 80 | 64 | 53 | 53 | | O | SCI-B Transmit Data |
| EQEP1_A | 10 | | | | | | I | eQEP-1 Input A |
| LINB_TX | 11 | | | | | | O | LIN-B Transmit |
| HIC_NBE1 | 14 | | | | | | I | HIC Byte enable 1 |
| HIC_D5 | 15 | | | | | | I/O | HIC Data 5 |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 100 PZ | 80 PN | 64 PMQ | 64 PM | 48 PT | PIN TYPE | DESCRIPTION |
|-----------------|--------------|--------|-------|--------|-------|-------|----------|--|
| GPIO41 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 41 |
| EPWM2_A | 5 | | | | | | O | ePWM-2 Output A |
| PMBUSA_SCL | 6 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Clock |
| FSIRXA_D1 | 7 | | | | | | I | FSIRX-A Optional Additional Data Input |
| SCIB_RX | 9 | 82 | 66 | 55 | 55 | | I | SCI-B Receive Data |
| EQEP1_B | 10 | | | | | | I | eQEP-1 Input B |
| LINB_RX | 11 | | | | | | I | LIN-B Receive |
| HIC_A4 | 13 | | | | | | I | HIC Address 4 |
| SPIB_SOMI | 14 | | | | | | I/O | SPI-B Slave Out, Master In (SOMI) |
| HIC_D12 | 15 | | | | | | I/O | HIC Data 12 |
| GPIO42 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 42 |
| LINA_RX | 2 | | | | | | I | LIN-A Receive |
| OUTPUTXBAR5 | 3 | | | | | | O | Output X-BAR Output 5 |
| PMBUSA_CTL | 5 | | | | | | I/O | PMBus-A Control Signal - Slave Input/Master Output |
| I2CA_SDA | 6 | | 57 | | | | I/OD | I2C-A Open-Drain Bidirectional Data |
| EQEP1_STROBE | 10 | | | | | | I/O | eQEP-1 Strobe |
| CLB_OUTPUTXBAR3 | 11 | | | | | | O | CLB Output X-BAR Output 3 |
| HIC_D2 | 14 | | | | | | I/O | HIC Data 2 |
| HIC_A6 | 15 | | | | | | I | HIC Address 6 |
| GPIO43 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 43 |
| OUTPUTXBAR6 | 3 | | | | | | O | Output X-BAR Output 6 |
| PMBUSA_ALERT | 5, 9 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Alert Signal |
| I2CA_SCL | 6 | | | | | | I/OD | I2C-A Open-Drain Bidirectional Clock |
| EQEP1_INDEX | 10 | | 54 | | | | I/O | eQEP-1 Index |
| CLB_OUTPUTXBAR4 | 11 | | | | | | O | CLB Output X-BAR Output 4 |
| SD2_D3 | 13 | | | | | | I | SDFM-2 Channel 3 Data Input |
| HIC_D3 | 14 | | | | | | I/O | HIC Data 3 |
| HIC_A7 | 15 | | | | | | I | HIC Address 7 |
| GPIO44 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 44 |
| OUTPUTXBAR7 | 3 | | | | | | O | Output X-BAR Output 7 |
| EQEP1_A | 5 | | | | | | I | eQEP-1 Input A |
| PMBUSA_SDA | 6 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Data |
| FSITXA_CLK | 7 | | | | | | O | FSITX-A Output Clock |
| PMBUSA_CTL | 9 | 85 | 69 | | | | I/O | PMBus-A Control Signal - Slave Input/Master Output |
| CLB_OUTPUTXBAR3 | 10 | | | | | | O | CLB Output X-BAR Output 3 |
| FSIRXA_D0 | 11 | | | | | | I | FSIRX-A Primary Data Input |
| HIC_D7 | 13 | | | | | | I/O | HIC Data 7 |
| LINB_TX | 14 | | | | | | O | LIN-B Transmit |
| HIC_D5 | 15 | | | | | | I/O | HIC Data 5 |
| GPIO45 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 45 |
| OUTPUTXBAR8 | 3 | | | | | | O | Output X-BAR Output 8 |
| FSITXA_D0 | 7 | | | | | | O | FSITX-A Primary Data Output |
| PMBUSA_ALERT | 9 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Alert Signal |
| CLB_OUTPUTXBAR4 | 10 | | | | | | O | CLB Output X-BAR Output 4 |
| SD2_C3 | 13 | | | | | | I | SDFM-2 Channel 3 Clock Input |
| HIC_D6 | 15 | | | | | | I/O | HIC Data 6 |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 100 PZ | 80 PN | 64 PMQ | 64 PM | 48 PT | PIN TYPE | DESCRIPTION |
|-----------------|--------------|--------|-------|--------|-------|-------|----------|---|
| GPIO46 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 46 |
| LINA_TX | 3 | | | | | | O | LIN-A Transmit |
| MCAN_TX | 5 | | | | | | O | CAN/CAN FD Transmit |
| FSITXA_D1 | 7 | | 6 | | | | O | FSITX-A Optional Additional Data Output |
| PMBUSA_SDA | 9 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Data |
| SD2_C4 | 13 | | | | | | I | SDFM-2 Channel 4 Clock Input |
| HIC_NWE | 15 | | | | | | I | HIC Data Write enable from host |
| GPIO47 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 47 |
| LINA_RX | 3 | | | | | | I | LIN-A Receive |
| MCAN_RX | 5 | | | | | | I | CAN/CAN FD Receive |
| CLB_OUTPUTXBAR2 | 7 | 6 | | | | | O | CLB Output X-BAR Output 2 |
| PMBUSA_SCL | 9 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Clock |
| SD2_D4 | 13 | | | | | | I | SDFM-2 Channel 4 Data Input |
| FSITXA_TDM_CLK | 14 | | | | | | I | FSITX-A Time Division Multiplexed Clock Input |
| HIC_A6 | 15 | | | | | | I | HIC Address 6 |
| GPIO48 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 48 |
| OUTPUTXBAR3 | 1 | | | | | | O | Output X-BAR Output 3 |
| CANA_TX | 3 | | | | | | O | CAN-A Transmit |
| SCIA_TX | 6 | 7 | | | | | O | SCI-A Transmit Data |
| SD1_D1 | 7 | | | | | | I | SDFM-1 Channel 1 Data Input |
| PMBUSA_SDA | 9 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Data |
| HIC_A7 | 15 | | | | | | I | HIC Address 7 |
| GPIO49 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 49 |
| OUTPUTXBAR4 | 1 | | | | | | O | Output X-BAR Output 4 |
| CANA_RX | 3 | | | | | | I | CAN-A Receive |
| SCIA_RX | 6 | | | | | | I | SCI-A Receive Data |
| SD1_C1 | 7 | 8 | | | | | I | SDFM-1 Channel 1 Clock Input |
| LINA_RX | 9 | | | | | | I | LIN-A Receive |
| SD2_D1 | 13 | | | | | | I | SDFM-2 Channel 1 Data Input |
| FSITXA_D0 | 14 | | | | | | O | FSITX-A Primary Data Output |
| HIC_D2 | 15 | | | | | | I/O | HIC Data 2 |
| GPIO50 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 50 |
| EQEP1_A | 1 | | | | | | I | eQEP-1 Input A |
| MCAN_TX | 5 | | | | | | O | CAN/CAN FD Transmit |
| SPIB_SIMO | 6 | | | | | | I/O | SPI-B Slave In, Master Out (SIMO) |
| SD1_D2 | 7 | 9 | | | | | I | SDFM-1 Channel 2 Data Input |
| I2CB_SDA | 9 | | | | | | I/OD | I2C-B Open-Drain Bidirectional Data |
| SD2_D2 | 13 | | | | | | I | SDFM-2 Channel 2 Data Input |
| FSITXA_D1 | 14 | | | | | | O | FSITX-A Optional Additional Data Output |
| HIC_D3 | 15 | | | | | | I/O | HIC Data 3 |
| GPIO51 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 51 |
| EQEP1_B | 1 | | | | | | I | eQEP-1 Input B |
| MCAN_RX | 5 | | | | | | I | CAN/CAN FD Receive |
| SPIB_SOMI | 6 | | | | | | I/O | SPI-B Slave Out, Master In (SOMI) |
| SD1_C2 | 7 | 10 | | | | | I | SDFM-1 Channel 2 Clock Input |
| I2CB_SCL | 9 | | | | | | I/OD | I2C-B Open-Drain Bidirectional Clock |
| SD2_D3 | 13 | | | | | | I | SDFM-2 Channel 3 Data Input |
| FSITXA_CLK | 14 | | | | | | O | FSITX-A Output Clock |
| HIC_D6 | 15 | | | | | | I/O | HIC Data 6 |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 100 PZ | 80 PN | 64 PMQ | 64 PM | 48 PT | PIN TYPE | DESCRIPTION |
|-----------------|--------------|--------|-------|--------|-------|-------|----------|--|
| GPIO52 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 52 |
| EQEP1_STROBE | 1 | | | | | | I/O | eQEP-1 Strobe |
| CLB_OUTPUTXBAR5 | 5 | | | | | | O | CLB Output X-BAR Output 5 |
| SPIB_CLK | 6 | | | | | | I/O | SPI-B Clock |
| SD1_D3 | 7 | 11 | | | | | I | SDFM-1 Channel 3 Data Input |
| SYNCOUT | 9 | | | | | | O | External ePWM Synchronization Pulse |
| SD2_D4 | 13 | | | | | | I | SDFM-2 Channel 4 Data Input |
| FSIRXA_D0 | 14 | | | | | | I | FSIRX-A Primary Data Input |
| HIC_NWE | 15 | | | | | | I | HIC Data Write enable from host |
| GPIO53 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 53 |
| EQEP1_INDEX | 1 | | | | | | I/O | eQEP-1 Index |
| CLB_OUTPUTXBAR6 | 5 | | | | | | O | CLB Output X-BAR Output 6 |
| SPIB_STE | 6 | | | | | | I/O | SPI-B Slave Transmit Enable (STE) |
| SD1_C3 | 7 | 12 | | | | | I | SDFM-1 Channel 3 Clock Input |
| ADCSOCAO | 9 | | | | | | O | ADC Start of Conversion A for External ADC |
| CANA_RX | 10 | | | | | | I | CAN-A Receive |
| SD1_C1 | 13 | | | | | | I | SDFM-1 Channel 1 Clock Input |
| FSIRXA_D1 | 14 | | | | | | I | FSIRX-A Optional Additional Data Input |
| GPIO54 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 54 |
| SPIA_SIMO | 1 | | | | | | I/O | SPI-A Slave In, Master Out (SIMO) |
| EQEP2_A | 5 | | | | | | I | eQEP-2 Input A |
| OUTPUTXBAR2 | 6 | | | | | | O | Output X-BAR Output 2 |
| SD1_D4 | 7 | | | | | | I | SDFM-1 Channel 4 Data Input |
| ADCSOCBO | 9 | 13 | | | | | O | ADC Start of Conversion B for External ADC |
| LINB_TX | 10 | | | | | | O | LIN-B Transmit |
| SD1_C2 | 13 | | | | | | I | SDFM-1 Channel 2 Clock Input |
| FSIRXA_CLK | 14 | | | | | | I | FSIRX-A Input Clock |
| FSITXA_TDM_D1 | 15 | | | | | | I | FSITX-A Time Division Multiplexed Additional Data Input |
| GPIO55 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 55 |
| SPIA_SOMI | 1 | | | | | | I/O | SPI-A Slave Out, Master In (SOMI) |
| EQEP2_B | 5 | | | | | | I | eQEP-2 Input B |
| OUTPUTXBAR3 | 6 | | | | | | O | Output X-BAR Output 3 |
| SD1_C4 | 7 | 43 | | | | | I | SDFM-1 Channel 4 Clock Input |
| ERRORSTS | 9 | | | | | | O | Error Status Output. This signal requires an external pull-down. |
| LINB_RX | 10 | | | | | | I | LIN-B Receive |
| SD1_C3 | 13 | | | | | | I | SDFM-1 Channel 3 Clock Input |
| HIC_A0 | 15 | | | | | | I | HIC Address 0 |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 100 PZ | 80 PN | 64 PMQ | 64 PM | 48 PT | PIN TYPE | DESCRIPTION |
|-----------------|--------------|--------|-------|--------|-------|-------|----------|---|
| GPIO56 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 56 |
| SPIA_CLK | 1 | | | | | | I/O | SPI-A Clock |
| CLB_OUTPUTXBAR7 | 2 | | | | | | O | CLB Output X-BAR Output 7 |
| MCAN_TX | 3 | | | | | | O | CAN/CAN FD Transmit |
| EQEP2_STROBE | 5 | | | | | | I/O | eQEP-2 Strobe |
| SCIB_TX | 6 | | | | | | O | SCI-B Transmit Data |
| SD2_D1 | 7 | 65 | | | | | I | SDFM-2 Channel 1 Data Input |
| SPIB_SIMO | 9 | | | | | | I/O | SPI-B Slave In, Master Out (SIMO) |
| I2CA_SDA | 10 | | | | | | I/OD | I2C-A Open-Drain Bidirectional Data |
| EQEP1_A | 11 | | | | | | I | eQEP-1 Input A |
| SD1_C4 | 13 | | | | | | I | SDFM-1 Channel 4 Clock Input |
| FSIRXA_D1 | 14 | | | | | | I | FSIRX-A Optional Additional Data Input |
| HIC_D6 | 15 | | | | | | I/O | HIC Data 6 |
| GPIO57 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 57 |
| SPIA_STE | 1 | | | | | | I/O | SPI-A Slave Transmit Enable (STE) |
| CLB_OUTPUTXBAR8 | 2 | | | | | | O | CLB Output X-BAR Output 8 |
| MCAN_RX | 3 | | | | | | I | CAN/CAN FD Receive |
| EQEP2_INDEX | 5 | | | | | | I/O | eQEP-2 Index |
| SCIB_RX | 6 | | | | | | I | SCI-B Receive Data |
| SD2_C1 | 7 | 66 | | | | | I | SDFM-2 Channel 1 Clock Input |
| SPIB_SOMI | 9 | | | | | | I/O | SPI-B Slave Out, Master In (SOMI) |
| I2CA_SCL | 10 | | | | | | I/OD | I2C-A Open-Drain Bidirectional Clock |
| EQEP1_B | 11 | | | | | | I | eQEP-1 Input B |
| FSIRXA_CLK | 14 | | | | | | I | FSIRX-A Input Clock |
| HIC_D4 | 15 | | | | | | I/O | HIC Data 4 |
| GPIO58 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 58 |
| OUTPUTXBAR1 | 5 | | | | | | O | Output X-BAR Output 1 |
| SPIB_CLK | 6 | | | | | | I/O | SPI-B Clock |
| SD2_D2 | 7 | | | | | | I | SDFM-2 Channel 2 Data Input |
| LINA_TX | 9 | | | | | | O | LIN-A Transmit |
| CANA_TX | 10 | | | | | | O | CAN-A Transmit |
| EQEP1_STROBE | 11 | | | | | | I/O | eQEP-1 Strobe |
| SD2_C2 | 13 | | | | | | I | SDFM-2 Channel 2 Clock Input |
| FSIRXA_D0 | 14 | | | | | | I | FSIRX-A Primary Data Input |
| HIC_NRDY | 15 | | | | | | O | HIC Ready from device to host |
| GPIO59 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 59 |
| OUTPUTXBAR2 | 5 | | | | | | O | Output X-BAR Output 2 |
| SPIB_STE | 6 | | | | | | I/O | SPI-B Slave Transmit Enable (STE) |
| SD2_C2 | 7 | | | | | | I | SDFM-2 Channel 2 Clock Input |
| LINA_RX | 9 | | | | | | I | LIN-A Receive |
| CANA_RX | 10 | | | | | | I | CAN-A Receive |
| EQEP1_INDEX | 11 | | | | | | I/O | eQEP-1 Index |
| SD2_C3 | 13 | | | | | | I | SDFM-2 Channel 3 Clock Input |
| FSITXA_TDM_D1 | 14 | | | | | | I | FSITX-A Time Division Multiplexed Additional Data Input |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 100 PZ | 80 PN | 64 PMQ | 64 PM | 48 PT | PIN TYPE | DESCRIPTION |
|------------------------------|--------------|---------------|---------------|---------------|---------------|------------|----------|---|
| GPIO60 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 60 |
| MCAN_TX | 3 | | | | | | O | CAN/CAN FD Transmit |
| OUTPUTXBAR3 | 5 | | | | | | O | Output X-BAR Output 3 |
| SPIB_SIMO | 6 | 44 | | | | | I/O | SPI-B Slave In, Master Out (SIMO) |
| SD2_D3 | 7 | | | | | | I | SDFM-2 Channel 3 Data Input |
| SD2_C4 | 13 | | | | | | I | SDFM-2 Channel 4 Clock Input |
| HIC_A0 | 15 | | | | | | I | HIC Address 0 |
| GPIO61 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 61 |
| MCAN_RX | 3 | | | | | | I | CAN/CAN FD Receive |
| OUTPUTXBAR4 | 5 | | | | | | O | Output X-BAR Output 4 |
| SPIB_SOMI | 6 | 91 | | | | | I/O | SPI-B Slave Out, Master In (SOMI) |
| SD2_C3 | 7 | | | | | | I | SDFM-2 Channel 3 Clock Input |
| CANA_RX | 14 | | | | | | I | CAN-A Receive |
| TEST, JTAG, AND RESET | | | | | | | | |
| TCK | | 60 | 45 | 36 | 36 | 28 | I | JTAG test clock with internal pullup. |
| TMS | | 62 | 47 | 38 | 38 | 30 | I/O | JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK. This device does not have a TRSTn pin. An external pullup resistor (recommended 2.2 kΩ) on the TMS pin to VDDIO should be placed on the board to keep JTAG in reset during normal operation. |
| XRSn | | 2 | 5 | 3 | 3 | 3 | I/OD | Device Reset (in) and Watchdog Reset (out). During a power-on condition, this pin is driven low by the device. An external circuit may also drive this pin to assert a device reset. This pin is also driven low by the MCU when a watchdog reset occurs. During watchdog reset, the XRSn pin is driven low for the watchdog reset duration of 512 OSCCLK cycles. A resistor between 2.2 kΩ and 10 kΩ should be placed between XRSn and VDDIO. If a capacitor is placed between XRSn and VSS for noise filtering, it should be 100 nF or smaller. These values will allow the watchdog to properly drive the XRSn pin to VOL within 512 OSCCLK cycles when the watchdog reset is asserted. This pin is an open-drain output with an internal pullup. If this pin is driven by an external device, it should be done using an open-drain device. |
| POWER AND GROUND | | | | | | | | |
| VDD | | 4, 46, 71, 87 | 8, 31, 53, 71 | 4, 27, 44, 59 | 4, 27, 44, 59 | 23, 36, 45 | | 1.2-V Digital Logic Power Pins. See the Power Management Module (PMM) section for usage details. |
| VDDA | | 34 | 26 | 22 | 22 | 18 | | 3.3-V Analog Power Pins. Place a minimum 2.2-μF decoupling capacitor on each pin. See the Power Management Module (PMM) section for usage details. |
| VDDIO | | 3, 47, 70, 88 | 7, 32, 52, 72 | 28, 43, 60 | 28, 43, 60 | 24, 35, 46 | | 3.3-V Digital I/O Power Pins. See the Power Management Module (PMM) section for usage details. |
| VREGENZ | | 73 | | 46 | | | I | Internal voltage regulator enable with internal pulldown. Tie low to VSS to enable internal VREG. Tie high to VDDIO to use an external supply. See the Power Management Module (PMM) section for usage details. |
| VSS | | 5, 45, 72, 86 | 9, 30, 55, 70 | 5, 26, 45, 58 | 5, 26, 45, 58 | 22, 37, 44 | | Digital Ground |
| VSSA | | 33 | 25 | 21 | 21 | 17 | | Analog Ground |

5.3 Signal Descriptions

5.3.1 Analog Signals

Table 5-2. Analog Signals

| SIGNAL NAME | PIN TYPE | DESCRIPTION | 100 PZ | 80 PN | 64 PMQ | 64 PM | 48 PT |
|-------------|----------|---------------------------------------|--------|-------|--------|-------|-------|
| A0 | I | ADC-A Input 0 | 23 | 19 | 15 | 15 | 11 |
| A1 | I | ADC-A Input 1 | 22 | 18 | 14 | 14 | 10 |
| A2 | I | ADC-A Input 2 | 17 | 13 | 9 | 9 | 6 |
| A3 | I | ADC-A Input 3 | 18 | 12 | 8 | 8 | 5 |
| A4 | I | ADC-A Input 4 | 36 | 27 | 23 | 23 | 19 |
| A5 | I | ADC-A Input 5 | 35 | 17 | 13 | 13 | 9 |
| A6 | I | ADC-A Input 6 | 14 | 10 | 6 | 6 | 4 |
| A7 | I | ADC-A Input 7 | 31 | 23 | 19 | 19 | 15 |
| A8 | I | ADC-A Input 8 | 37 | 24 | 20 | 20 | 16 |
| A9 | I | ADC-A Input 9 | 38 | 28 | 24 | 24 | 20 |
| A10 | I | ADC-A Input 10 | 40 | 29 | 25 | 25 | 21 |
| A11 | I | ADC-A Input 11 | 20 | 16 | 12 | 12 | 8 |
| A12 | I | ADC-A Input 12 | 28 | 22 | 18 | 18 | 14 |
| A14 | I | ADC-A Input 14 | 19 | 15 | 11 | 11 | |
| A15 | I | ADC-A Input 15 | | 14 | 10 | 10 | 7 |
| AIO224 | I | Analog Pin Used For Digital Input 224 | 17 | 13 | 9 | 9 | 6 |
| AIO225 | I | Analog Pin Used For Digital Input 225 | 36 | 27 | 23 | 23 | 19 |
| AIO226 | I | Analog Pin Used For Digital Input 226 | 15 | 11 | 7 | 7 | 4 |
| AIO227 | I | Analog Pin Used For Digital Input 227 | 38 | 28 | 24 | 24 | 20 |
| AIO228 | I | Analog Pin Used For Digital Input 228 | 14 | 10 | 6 | 6 | 4 |
| AIO229 | I | Analog Pin Used For Digital Input 229 | 18 | | | | |
| AIO230 | I | Analog Pin Used For Digital Input 230 | 40 | 29 | 25 | 25 | 21 |
| AIO231 | I | Analog Pin Used For Digital Input 231 | 23 | 19 | 15 | 15 | 11 |
| AIO232 | I | Analog Pin Used For Digital Input 232 | 22 | 18 | 14 | 14 | 10 |
| AIO233 | I | Analog Pin Used For Digital Input 233 | | 14 | 10 | 10 | 7 |
| AIO236 | I | Analog Pin Used For Digital Input 236 | 39 | 28 | 24 | 24 | 20 |
| AIO237 | I | Analog Pin Used For Digital Input 237 | 20 | 16 | 12 | 12 | 8 |
| AIO238 | I | Analog Pin Used For Digital Input 238 | 28 | 22 | 18 | 18 | 14 |
| AIO239 | I | Analog Pin Used For Digital Input 239 | 19 | 15 | 11 | 11 | |
| AIO240 | I | Analog Pin Used For Digital Input 240 | 37 | | | | |
| AIO241 | I | Analog Pin Used For Digital Input 241 | | 24 | 20 | 20 | 16 |
| AIO242 | I | Analog Pin Used For Digital Input 242 | 16 | 12 | 8 | 8 | 5 |
| AIO244 | I | Analog Pin Used For Digital Input 244 | 21 | 17 | 13 | 13 | 9 |
| AIO245 | I | Analog Pin Used For Digital Input 245 | 31 | 23 | 19 | 19 | 15 |
| AIO247 | I | Analog Pin Used For Digital Input 247 | 42 | | | | |
| AIO248 | I | Analog Pin Used For Digital Input 248 | 29 | 22 | 18 | 18 | 14 |
| AIO249 | I | Analog Pin Used For Digital Input 249 | 35 | | | | |
| AIO251 | I | Analog Pin Used For Digital Input 251 | 30 | | | | |
| AIO252 | I | Analog Pin Used For Digital Input 252 | 32 | | | | |
| AIO253 | I | Analog Pin Used For Digital Input 253 | 41 | | | | |
| B0 | I | ADC-B Input 0 | 41 | 24 | 20 | 20 | 16 |
| B1 | I | ADC-B Input 1 | 40 | 29 | 25 | 25 | 21 |

Table 5-2. Analog Signals (continued)

| SIGNAL NAME | PIN TYPE | DESCRIPTION | 100 PZ | 80 PN | 64 PMQ | 64 PM | 48 PT |
|-------------|----------|--|--------|-------|--------|-------|-------|
| B2 | I | ADC-B Input 2 | 15 | 11 | 7 | 7 | 4 |
| B3 | I | ADC-B Input 3 | 16 | 12 | 8 | 8 | 5 |
| B4 | I | ADC-B Input 4 | 39 | 28 | 24 | 24 | 20 |
| B5 | I | ADC-B Input 5 | 32, 48 | 33 | | | |
| B6 | I | ADC-B Input 6 | 17 | 13 | 9 | 9 | 6 |
| B7 | I | ADC-B Input 7 | 22 | 18 | 14 | 14 | 10 |
| B8 | I | ADC-B Input 8 | 36 | 27 | 23 | 23 | 19 |
| B9 | I | ADC-B Input 9 | 18 | 14 | 10 | 10 | 7 |
| B10 | I | ADC-B Input 10 | 20 | 16 | 12 | 12 | 8 |
| B11 | I | ADC-B Input 11 | 30, 49 | 34 | | | |
| B12 | I | ADC-B Input 12 | 21 | 17 | 13 | 13 | 9 |
| B14 | I | ADC-B Input 14 | 19 | 15 | 11 | 11 | |
| B15 | I | ADC-B Input 15 | 23 | 19 | 15 | 15 | 11 |
| C0 | I | ADC-C Input 0 | 20 | 16 | 12 | 12 | 8 |
| C1 | I | ADC-C Input 1 | 29 | 22 | 18 | 18 | 14 |
| C2 | I | ADC-C Input 2 | 21 | 17 | 13 | 13 | 9 |
| C3 | I | ADC-C Input 3 | 31 | 23 | 19 | 19 | 15 |
| C4 | I | ADC-C Input 4 | 19 | 15 | 11 | 11 | |
| C5 | I | ADC-C Input 5 | 28 | 12 | 8 | 8 | 5 |
| C6 | I | ADC-C Input 6 | 15 | 11 | 7 | 7 | 4 |
| C7 | I | ADC-C Input 7 | 18 | 14 | 10 | 10 | 7 |
| C8 | I | ADC-C Input 8 | 39 | 28 | 24 | 24 | 20 |
| C9 | I | ADC-C Input 9 | 17 | 13 | 9 | 9 | 6 |
| C10 | I | ADC-C Input 10 | 40 | 29 | 25 | 25 | 21 |
| C11 | I | ADC-C Input 11 | 41 | 24 | 20 | 20 | 16 |
| C14 | I | ADC-C Input 14 | 42 | 27 | 23 | 23 | 19 |
| C15 | I | ADC-C Input 15 | 23 | 19 | 15 | 15 | 11 |
| CMP1_HN0 | I | CMPSS-1 High Comparator Negative Input 0 | | 14 | 10 | 10 | 7 |
| CMP1_HN1 | I | CMPSS-1 High Comparator Negative Input 1 | 20 | 16 | 12 | 12 | 8 |
| CMP1_HP0 | I | CMPSS-1 High Comparator Positive Input 0 | 17 | 13 | 9 | 9 | 6 |
| CMP1_HP1 | I | CMPSS-1 High Comparator Positive Input 1 | 20 | 16 | 12 | 12 | 8 |
| CMP1_HP2 | I | CMPSS-1 High Comparator Positive Input 2 | 14 | 10 | 6 | 6 | 4 |
| CMP1_HP3 | I | CMPSS-1 High Comparator Positive Input 3 | | 14 | 10 | 10 | 7 |
| CMP1_HP4 | I | CMPSS-1 High Comparator Positive Input 4 | 22 | 18 | 14 | 14 | 10 |
| CMP1_HP5 | I | CMPSS-1 High Comparator Positive Input 5 | 32, 48 | 33 | | | |
| CMP1_LN0 | I | CMPSS-1 Low Comparator Negative Input 0 | | 14 | 10 | 10 | 7 |
| CMP1_LN1 | I | CMPSS-1 Low Comparator Negative Input 1 | 20 | 16 | 12 | 12 | 8 |

Table 5-2. Analog Signals (continued)

| SIGNAL NAME | PIN TYPE | DESCRIPTION | 100 PZ | 80 PN | 64 PMQ | 64 PM | 48 PT |
|-------------|----------|--|--------|-------|--------|-------|-------|
| CMP1_LP0 | I | CMPSS-1 Low Comparator Positive Input 0 | 17 | 13 | 9 | 9 | 6 |
| CMP1_LP1 | I | CMPSS-1 Low Comparator Positive Input 1 | 20 | 16 | 12 | 12 | 8 |
| CMP1_LP2 | I | CMPSS-1 Low Comparator Positive Input 2 | 14 | 10 | 6 | 6 | 4 |
| CMP1_LP3 | I | CMPSS-1 Low Comparator Positive Input 3 | | 14 | 10 | 10 | 7 |
| CMP1_LP4 | I | CMPSS-1 Low Comparator Positive Input 4 | 22 | 18 | 14 | 14 | 10 |
| CMP1_LP5 | I | CMPSS-1 Low Comparator Positive Input 5 | 32, 48 | 33 | | | |
| CMP2_HN0 | I | CMPSS-2 High Comparator Negative Input 0 | 40 | 29 | 25 | 25 | 21 |
| CMP2_HN1 | I | CMPSS-2 High Comparator Negative Input 1 | 28 | 22 | 18 | 18 | 14 |
| CMP2_HP0 | I | CMPSS-2 High Comparator Positive Input 0 | 36 | 27 | 23 | 23 | 19 |
| CMP2_HP1 | I | CMPSS-2 High Comparator Positive Input 1 | 28 | 22 | 18 | 18 | 14 |
| CMP2_HP2 | I | CMPSS-2 High Comparator Positive Input 2 | 38 | 28 | 24 | 24 | 20 |
| CMP2_HP3 | I | CMPSS-2 High Comparator Positive Input 3 | 40 | 29 | 25 | 25 | 21 |
| CMP2_HP4 | I | CMPSS-2 High Comparator Positive Input 4 | 41 | 24 | 20 | 20 | 16 |
| CMP2_HP5 | I | CMPSS-2 High Comparator Positive Input 5 | 35 | 17 | 13 | 13 | 9 |
| CMP2_LN0 | I | CMPSS-2 Low Comparator Negative Input 0 | 40 | 29 | 25 | 25 | 21 |
| CMP2_LN1 | I | CMPSS-2 Low Comparator Negative Input 1 | 28 | 22 | 18 | 18 | 14 |
| CMP2_LP0 | I | CMPSS-2 Low Comparator Positive Input 0 | 36 | 27 | 23 | 23 | 19 |
| CMP2_LP1 | I | CMPSS-2 Low Comparator Positive Input 1 | 28 | 22 | 18 | 18 | 14 |
| CMP2_LP2 | I | CMPSS-2 Low Comparator Positive Input 2 | 38 | 28 | 24 | 24 | 20 |
| CMP2_LP3 | I | CMPSS-2 Low Comparator Positive Input 3 | 40 | 29 | 25 | 25 | 21 |
| CMP2_LP4 | I | CMPSS-2 Low Comparator Positive Input 4 | 41 | 24 | 20 | 20 | 16 |
| CMP2_LP5 | I | CMPSS-2 Low Comparator Positive Input 5 | 35 | 17 | 13 | 13 | 9 |
| CMP3_HN0 | I | CMPSS-3 High Comparator Negative Input 0 | 16 | 12 | 8 | 8 | 5 |
| CMP3_HN1 | I | CMPSS-3 High Comparator Negative Input 1 | 21 | 17 | 13 | 13 | 9 |
| CMP3_HP0 | I | CMPSS-3 High Comparator Positive Input 0 | 15 | 11 | 7 | 7 | 4 |
| CMP3_HP1 | I | CMPSS-3 High Comparator Positive Input 1 | 21 | 17 | 13 | 13 | 9 |

Table 5-2. Analog Signals (continued)

| SIGNAL NAME | PIN TYPE | DESCRIPTION | 100 PZ | 80 PN | 64 PMQ | 64 PM | 48 PT |
|-------------|----------|--|--------|-------|--------|-------|-------|
| CMP3_HP2 | I | CMPSS-3 High Comparator Positive Input 2 | 23 | 19 | 15 | 15 | 11 |
| CMP3_HP3 | I | CMPSS-3 High Comparator Positive Input 3 | 16 | 12 | 8 | 8 | 5 |
| CMP3_HP4 | I | CMPSS-3 High Comparator Positive Input 4 | 19 | 15 | 11 | 11 | |
| CMP3_HP5 | I | CMPSS-3 High Comparator Positive Input 5 | 18 | 12 | 8 | 8 | 5 |
| CMP3_LN0 | I | CMPSS-3 Low Comparator Negative Input 0 | 16 | 12 | 8 | 8 | 5 |
| CMP3_LN1 | I | CMPSS-3 Low Comparator Negative Input 1 | 21 | 17 | 13 | 13 | 9 |
| CMP3_LP0 | I | CMPSS-3 Low Comparator Positive Input 0 | 15 | 11 | 7 | 7 | 4 |
| CMP3_LP1 | I | CMPSS-3 Low Comparator Positive Input 1 | 21 | 17 | 13 | 13 | 9 |
| CMP3_LP2 | I | CMPSS-3 Low Comparator Positive Input 2 | 23 | 19 | 15 | 15 | 11 |
| CMP3_LP3 | I | CMPSS-3 Low Comparator Positive Input 3 | 16 | 12 | 8 | 8 | 5 |
| CMP3_LP4 | I | CMPSS-3 Low Comparator Positive Input 4 | 19 | 15 | 11 | 11 | |
| CMP3_LP5 | I | CMPSS-3 Low Comparator Positive Input 5 | 18 | 12 | 8 | 8 | 5 |
| CMP4_HN0 | I | CMPSS-4 High Comparator Negative Input 0 | 42 | 27 | 23 | 23 | 19 |
| CMP4_HN1 | I | CMPSS-4 High Comparator Negative Input 1 | 31 | 23 | 19 | 19 | 15 |
| CMP4_HP0 | I | CMPSS-4 High Comparator Positive Input 0 | 39 | 28 | 24 | 24 | 20 |
| CMP4_HP1 | I | CMPSS-4 High Comparator Positive Input 1 | 31 | 23 | 19 | 19 | 15 |
| CMP4_HP2 | I | CMPSS-4 High Comparator Positive Input 2 | 29 | 22 | 18 | 18 | 14 |
| CMP4_HP3 | I | CMPSS-4 High Comparator Positive Input 3 | 42 | 27 | 23 | 23 | 19 |
| CMP4_HP4 | I | CMPSS-4 High Comparator Positive Input 4 | 37 | 24 | 20 | 20 | 16 |
| CMP4_HP5 | I | CMPSS-4 High Comparator Positive Input 5 | 30, 49 | 34 | | | |
| CMP4_LN0 | I | CMPSS-4 Low Comparator Negative Input 0 | 42 | 27 | 23 | 23 | 19 |
| CMP4_LN1 | I | CMPSS-4 Low Comparator Negative Input 1 | 31 | 23 | 19 | 19 | 15 |
| CMP4_LP0 | I | CMPSS-4 Low Comparator Positive Input 0 | 39 | 28 | 24 | 24 | 20 |
| CMP4_LP1 | I | CMPSS-4 Low Comparator Positive Input 1 | 31 | 23 | 19 | 19 | 15 |
| CMP4_LP2 | I | CMPSS-4 Low Comparator Positive Input 2 | 29 | 22 | 18 | 18 | 14 |
| CMP4_LP3 | I | CMPSS-4 Low Comparator Positive Input 3 | 42 | 27 | 23 | 23 | 19 |

Table 5-2. Analog Signals (continued)

| SIGNAL NAME | PIN TYPE | DESCRIPTION | 100 PZ | 80 PN | 64 PMQ | 64 PM | 48 PT |
|-------------|----------|---|--------|-------|--------|-------|-------|
| CMP4_LP4 | I | CMPSS-4 Low Comparator Positive Input 4 | 37 | 24 | 20 | 20 | 16 |
| CMP4_LP5 | I | CMPSS-4 Low Comparator Positive Input 5 | 30, 49 | 34 | | | |
| DACA_OUT | O | Buffered DAC-A Output. | 23 | 19 | 15 | 15 | 11 |
| DACB_OUT | O | Buffered DAC-B Output. | 22 | 18 | 14 | 14 | 10 |
| VDAC | I | Optional external reference voltage for on-chip DACs. | 16 | 12 | 8 | 8 | 5 |
| VREFHI | I | ADC High Reference. In external reference mode, externally drive the high reference voltage onto this pin. In internal reference mode, a voltage is driven onto this pin by the device. In either mode, place at least a 2.2- μ F capacitor on this pin. This capacitor should be placed as close to the device as possible between the VREFHI and VREFLO pins. | 24, 25 | 20 | 16 | 16 | 12 |
| VREFLO | I | ADC Low Reference | 26, 27 | 21 | 17 | 17 | 13 |

5.3.2 Digital Signals

Table 5-3. Digital Signals

| SIGNAL NAME | PIN TYPE | DESCRIPTION | GPIO | 100 PZ | 80 PN | 64 PMQ | 64 PM | 48 PT |
|-----------------|----------|---|--|---|-------------------------------|----------------------------|----------------------------|--------------------|
| ADCSOCAO | O | ADC Start of Conversion A for External ADC | 8, 33, 53 | 12, 53, 74 | 38, 58 | 32, 47 | 32, 47 | 25 |
| ADCSOCBO | O | ADC Start of Conversion B for External ADC | 10, 32, 54 | 13, 64, 93 | 49, 76 | 40, 63 | 40, 63 | 32 |
| AUXCLKIN | I | Auxiliary Clock Input | 29 | 100 | 3 | 1 | 1 | 1 |
| CANA_RX | I | CAN-A Receive | 3, 5, 12, 18, 30, 33, 35, 49, 53, 59, 61 | 8, 12, 51, 53, 63, 68, 76, 89, 91, 92, 98 | 1, 36, 38, 48, 50, 60, 74 | 30, 32, 39, 41, 49, 61 | 30, 32, 39, 41, 49, 61 | 25, 31, 33, 39, 47 |
| CANA_TX | O | CAN-A Transmit | 2, 4, 13, 17, 19, 31, 32, 37, 48, 58 | 7, 50, 55, 61, 64, 67, 69, 75, 77, 99 | 2, 35, 40, 46, 49, 51, 59, 61 | 29, 34, 37, 40, 42, 48, 50 | 29, 34, 37, 40, 42, 48, 50 | 29, 32, 34, 38, 40 |
| CLB_OUTPUTXBAR1 | O | CLB Output X-BAR Output 1 | 19, 22 | 69, 83 | 51, 67 | 42, 56 | 42, 56 | 34 |
| CLB_OUTPUTXBAR2 | O | CLB Output X-BAR Output 2 | 7, 39, 47 | 6, 84 | 56, 68 | 57 | 46, 57 | 43 |
| CLB_OUTPUTXBAR3 | O | CLB Output X-BAR Output 3 | 23, 42, 44 | 81, 85 | 57, 65, 69 | 54 | 54 | |
| CLB_OUTPUTXBAR4 | O | CLB Output X-BAR Output 4 | 10, 43, 45 | 93 | 54, 73, 76 | 63 | 63 | |
| CLB_OUTPUTXBAR5 | O | CLB Output X-BAR Output 5 | 5, 8, 52 | 11, 74, 89 | 58, 74 | 47, 61 | 47, 61 | 47 |
| CLB_OUTPUTXBAR6 | O | CLB Output X-BAR Output 6 | 4, 15, 53 | 12, 75, 95 | 59, 78 | 48 | 48 | 38 |
| CLB_OUTPUTXBAR7 | O | CLB Output X-BAR Output 7 | 1, 14, 56 | 65, 78, 96 | 62, 79 | 51 | 51 | 41 |
| CLB_OUTPUTXBAR8 | O | CLB Output X-BAR Output 8 | 0, 6, 57 | 66, 79, 97 | 63, 80 | 52, 64 | 52, 64 | 42, 48 |
| EPWM1_A | O | ePWM-1 Output A | 0, 30 | 79, 98 | 1, 63 | 52 | 52 | 42 |
| EPWM1_B | O | ePWM-1 Output B | 1, 31 | 78, 99 | 2, 62 | 51 | 51 | 41 |
| EPWM2_A | O | ePWM-2 Output A | 2, 41 | 77, 82 | 61, 66 | 50, 55 | 50, 55 | 40 |
| EPWM2_B | O | ePWM-2 Output B | 3, 40 | 76, 80 | 60, 64 | 49, 53 | 49, 53 | 39 |
| EPWM3_A | O | ePWM-3 Output A | 4, 14 | 75, 96 | 59, 79 | 48 | 48 | 38 |
| EPWM3_B | O | ePWM-3 Output B | 5, 15 | 89, 95 | 74, 78 | 61 | 61 | 47 |
| EPWM4_A | O | ePWM-4 Output A | 6, 22 | 83, 97 | 67, 80 | 56, 64 | 56, 64 | 48 |
| EPWM4_B | O | ePWM-4 Output B | 7, 23 | 81, 84 | 65, 68 | 54, 57 | 54, 57 | 43 |
| EPWM5_A | O | ePWM-5 Output A | 8, 16 | 54, 74 | 39, 58 | 33, 47 | 33, 47 | 26 |
| EPWM5_B | O | ePWM-5 Output B | 9, 17, 35 | 55, 63, 90 | 40, 48, 75 | 34, 39, 62 | 34, 39, 62 | 31 |
| EPWM6_A | O | ePWM-6 Output A | 10, 18 | 68, 93 | 50, 76 | 41, 63 | 41, 63 | 33 |
| EPWM6_B | O | ePWM-6 Output B | 11, 19 | 52, 69 | 37, 51 | 31, 42 | 31, 42 | 34 |
| EPWM7_A | O | ePWM-7 Output A | 12, 28 | 1, 51 | 4, 36 | 2, 30 | 2, 30 | 2 |
| EPWM7_B | O | ePWM-7 Output B | 13, 29 | 50, 100 | 3, 35 | 1, 29 | 1, 29 | 1 |
| EPWM8_A | O | ePWM-8 Output A | 14, 24 | 56, 96 | 41, 79 | 35 | 35 | 27 |
| EPWM8_B | O | ePWM-8 Output B | 15, 32 | 64, 95 | 49, 78 | 40 | 40 | 32 |
| EQEP1_A | I | eQEP-1 Input A | 6, 10, 20, 25, 28, 35, 40, 44, 50, 56 | 1, 9, 48, 57, 63, 65, 80, 85, 93, 97 | 4, 33, 42, 48, 64, 69, 76, 80 | 2, 39, 53, 63, 64 | 2, 39, 53, 63, 64 | 2, 31, 48 |
| EQEP1_B | I | eQEP-1 Input B | 7, 11, 21, 29, 37, 41, 51, 57 | 10, 49, 52, 61, 66, 82, 84, 100 | 3, 34, 37, 46, 66, 68 | 1, 31, 37, 55, 57 | 1, 31, 37, 55, 57 | 1, 29, 43 |
| EQEP1_INDEX | I/O | eQEP-1 Index | 0, 9, 13, 17, 23, 31, 39, 43, 53, 59 | 12, 50, 55, 79, 81, 90, 92, 99 | 2, 35, 40, 54, 56, 63, 65, 75 | 29, 34, 52, 54, 62 | 29, 34, 46, 52, 54, 62 | 42 |
| EQEP1_STROBE | I/O | eQEP-1 Strobe | 8, 12, 16, 22, 30, 42, 52, 58 | 11, 51, 54, 67, 74, 83, 98 | 1, 36, 39, 57, 58, 67 | 30, 33, 47, 56 | 30, 33, 47, 56 | 26 |
| EQEP2_A | I | eQEP-2 Input A | 11, 14, 18, 24, 54 | 13, 52, 56, 68, 96 | 37, 41, 50, 79 | 31, 35, 41 | 31, 35, 41 | 27, 33 |
| EQEP2_B | I | eQEP-2 Input B | 15, 16, 19, 25, 33, 55 | 43, 53, 54, 57, 69, 95 | 38, 39, 42, 51, 78 | 32, 33, 42 | 32, 33, 42 | 25, 26, 34 |
| EQEP2_INDEX | I/O | eQEP-2 Index | 26, 29, 39, 57 | 58, 66, 100 | 3, 43, 56 | 1 | 1, 46 | 1 |
| EQEP2_STROBE | I/O | eQEP-2 Strobe | 4, 27, 28, 56 | 1, 59, 65, 75 | 4, 44, 59 | 2, 48 | 2, 48 | 2, 38 |
| ERRORSTS | O | Error Status Output. This signal requires an external pulldown. | 24, 28, 29, 55 | 1, 43, 56, 100 | 3, 4, 41 | 1, 2, 35 | 1, 2, 35 | 1, 2, 27 |
| FSIRXA_CLK | I | FSIRX-A Input Clock | 0, 4, 13, 30, 33, 39, 54, 57 | 13, 50, 53, 66, 75, 79, 98 | 1, 35, 38, 56, 59, 63 | 29, 32, 48, 52 | 29, 32, 46, 48, 52 | 25, 38, 42 |
| FSIRXA_D0 | I | FSIRX-A Primary Data Input | 3, 12, 32, 40, 44, 52, 58 | 11, 51, 64, 67, 76, 80, 85 | 36, 49, 60, 64, 69 | 30, 40, 49, 53 | 30, 40, 49, 53 | 32, 39 |
| FSIRXA_D1 | I | FSIRX-A Optional Additional Data Input | 2, 11, 31, 41, 53, 56 | 12, 52, 65, 77, 82, 99 | 2, 37, 61, 66 | 31, 50, 55 | 31, 50, 55 | 40 |
| FSITXA_CLK | O | FSITX-A Output Clock | 7, 10, 27, 44, 51 | 10, 59, 84, 85, 93 | 44, 68, 69, 76 | 57, 63 | 57, 63 | 43 |
| FSITXA_D0 | O | FSITX-A Primary Data Output | 6, 9, 26, 45, 49 | 8, 58, 90, 97 | 43, 73, 75, 80 | 62, 64 | 62, 64 | 48 |
| FSITXA_D1 | O | FSITX-A Optional Additional Data Output | 5, 6, 8, 25, 46, 50 | 9, 57, 74, 89, 97 | 6, 42, 58, 74, 80 | 47, 61, 64 | 47, 61, 64 | 47, 48 |

Table 5-3. Digital Signals (continued)

| SIGNAL NAME | PIN TYPE | DESCRIPTION | GPIO | 100 PZ | 80 PN | 64 PMQ | 64 PM | 48 PT |
|----------------|----------|---|-----------|------------|--------|--------|--------|-------|
| FSITXA_TDM_CLK | I | FSITX-A Time Division Multiplexed Clock Input | 8, 18, 47 | 6, 68, 74 | 50, 58 | 41, 47 | 41, 47 | 33 |
| FSITXA_TDM_D0 | I | FSITX-A Time Division Multiplexed Data Input | 10, 19 | 69, 93 | 51, 76 | 42, 63 | 42, 63 | 34 |
| FSITXA_TDM_D1 | I | FSITX-A Time Division Multiplexed Additional Data Input | 1, 54, 59 | 13, 78, 92 | 62 | 51 | 51 | 41 |
| GPIO0 | I/O | General-Purpose Input Output 0 | 0 | 79 | 63 | 52 | 52 | 42 |
| GPIO1 | I/O | General-Purpose Input Output 1 | 1 | 78 | 62 | 51 | 51 | 41 |
| GPIO2 | I/O | General-Purpose Input Output 2 | 2 | 77 | 61 | 50 | 50 | 40 |
| GPIO3 | I/O | General-Purpose Input Output 3 | 3 | 76 | 60 | 49 | 49 | 39 |
| GPIO4 | I/O | General-Purpose Input Output 4 | 4 | 75 | 59 | 48 | 48 | 38 |
| GPIO5 | I/O | General-Purpose Input Output 5 | 5 | 89 | 74 | 61 | 61 | 47 |
| GPIO6 | I/O | General-Purpose Input Output 6 | 6 | 97 | 80 | 64 | 64 | 48 |
| GPIO7 | I/O | General-Purpose Input Output 7 | 7 | 84 | 68 | 57 | 57 | 43 |
| GPIO8 | I/O | General-Purpose Input Output 8 | 8 | 74 | 58 | 47 | 47 | |
| GPIO9 | I/O | General-Purpose Input Output 9 | 9 | 90 | 75 | 62 | 62 | |
| GPIO10 | I/O | General-Purpose Input Output 10 | 10 | 93 | 76 | 63 | 63 | |
| GPIO11 | I/O | General-Purpose Input Output 11 | 11 | 52 | 37 | 31 | 31 | |
| GPIO12 | I/O | General-Purpose Input Output 12 | 12 | 51 | 36 | 30 | 30 | |
| GPIO13 | I/O | General-Purpose Input Output 13 | 13 | 50 | 35 | 29 | 29 | |
| GPIO14 | I/O | General-Purpose Input Output 14 | 14 | 96 | 79 | | | |
| GPIO15 | I/O | General-Purpose Input Output 15 | 15 | 95 | 78 | | | |
| GPIO16 | I/O | General-Purpose Input Output 16 | 16 | 54 | 39 | 33 | 33 | 26 |
| GPIO17 | I/O | General-Purpose Input Output 17 | 17 | 55 | 40 | 34 | 34 | |
| GPIO18 | I/O | General-Purpose Input Output 18 | 18 | 68 | 50 | 41 | 41 | 33 |
| GPIO19 | I/O | General-Purpose Input Output 19 | 19 | 69 | 51 | 42 | 42 | 34 |
| GPIO20 | I/O | General-Purpose Input Output 20 | 20 | 48 | 33 | | | |
| GPIO21 | I/O | General-Purpose Input Output 21 | 21 | 49 | 34 | | | |
| GPIO22 | I/O | General-Purpose Input Output 22 | 22 | 83 | 67 | 56 | 56 | |
| GPIO23 | I/O | General-Purpose Input Output 23 | 23 | 81 | 65 | 54 | 54 | |
| GPIO24 | I/O | General-Purpose Input Output 24 | 24 | 56 | 41 | 35 | 35 | 27 |
| GPIO25 | I/O | General-Purpose Input Output 25 | 25 | 57 | 42 | | | |
| GPIO26 | I/O | General-Purpose Input Output 26 | 26 | 58 | 43 | | | |
| GPIO27 | I/O | General-Purpose Input Output 27 | 27 | 59 | 44 | | | |
| GPIO28 | I/O | General-Purpose Input Output 28 | 28 | 1 | 4 | 2 | 2 | 2 |
| GPIO29 | I/O | General-Purpose Input Output 29 | 29 | 100 | 3 | 1 | 1 | 1 |
| GPIO30 | I/O | General-Purpose Input Output 30 | 30 | 98 | 1 | | | |
| GPIO31 | I/O | General-Purpose Input Output 31 | 31 | 99 | 2 | | | |
| GPIO32 | I/O | General-Purpose Input Output 32 | 32 | 64 | 49 | 40 | 40 | 32 |
| GPIO33 | I/O | General-Purpose Input Output 33 | 33 | 53 | 38 | 32 | 32 | 25 |
| GPIO34 | I/O | General-Purpose Input Output 34 | 34 | 94 | 77 | | | |
| GPIO35 | I/O | General-Purpose Input Output 35 | 35 | 63 | 48 | 39 | 39 | 31 |
| GPIO37 | I/O | General-Purpose Input Output 37 | 37 | 61 | 46 | 37 | 37 | 29 |
| GPIO39 | I/O | General-Purpose Input Output 39 | 39 | | 56 | | 46 | |
| GPIO40 | I/O | General-Purpose Input Output 40 | 40 | 80 | 64 | 53 | 53 | |
| GPIO41 | I/O | General-Purpose Input Output 41 | 41 | 82 | 66 | 55 | 55 | |
| GPIO42 | I/O | General-Purpose Input Output 42 | 42 | | 57 | | | |
| GPIO43 | I/O | General-Purpose Input Output 43 | 43 | | 54 | | | |
| GPIO44 | I/O | General-Purpose Input Output 44 | 44 | 85 | 69 | | | |
| GPIO45 | I/O | General-Purpose Input Output 45 | 45 | | 73 | | | |
| GPIO46 | I/O | General-Purpose Input Output 46 | 46 | | 6 | | | |
| GPIO47 | I/O | General-Purpose Input Output 47 | 47 | 6 | | | | |
| GPIO48 | I/O | General-Purpose Input Output 48 | 48 | 7 | | | | |
| GPIO49 | I/O | General-Purpose Input Output 49 | 49 | 8 | | | | |
| GPIO50 | I/O | General-Purpose Input Output 50 | 50 | 9 | | | | |
| GPIO51 | I/O | General-Purpose Input Output 51 | 51 | 10 | | | | |
| GPIO52 | I/O | General-Purpose Input Output 52 | 52 | 11 | | | | |

Table 5-3. Digital Signals (continued)

| SIGNAL NAME | PIN TYPE | DESCRIPTION | GPIO | 100 PZ | 80 PN | 64 PMQ | 64 PM | 48 PT |
|--------------|----------|--------------------------------------|--------------------------------|----------------------------|----------------------------|--------------------|--------------------|----------------|
| GPIO53 | I/O | General-Purpose Input Output 53 | 53 | 12 | | | | |
| GPIO54 | I/O | General-Purpose Input Output 54 | 54 | 13 | | | | |
| GPIO55 | I/O | General-Purpose Input Output 55 | 55 | 43 | | | | |
| GPIO56 | I/O | General-Purpose Input Output 56 | 56 | 65 | | | | |
| GPIO57 | I/O | General-Purpose Input Output 57 | 57 | 66 | | | | |
| GPIO58 | I/O | General-Purpose Input Output 58 | 58 | 67 | | | | |
| GPIO59 | I/O | General-Purpose Input Output 59 | 59 | 92 | | | | |
| GPIO60 | I/O | General-Purpose Input Output 60 | 60 | 44 | | | | |
| GPIO61 | I/O | General-Purpose Input Output 61 | 61 | 91 | | | | |
| HIC_A0 | I | HIC Address 0 | 8, 55, 60 | 14, 43, 44, 74 | 10, 58 | 6, 47 | 6, 47 | 4 |
| HIC_A1 | I | HIC Address 1 | 2, 26 | 15, 58, 77 | 11, 43, 61 | 7, 50 | 7, 50 | 4, 40 |
| HIC_A2 | I | HIC Address 2 | 1 | 16, 78 | 12, 62 | 8, 51 | 8, 51 | 5, 41 |
| HIC_A3 | I | HIC Address 3 | 23 | 17, 81 | 13, 65 | 9, 54 | 9, 54 | 6 |
| HIC_A4 | I | HIC Address 4 | 27, 41 | 59, 82 | 14, 44, 66 | 10, 55 | 10, 55 | 7 |
| HIC_A5 | I | HIC Address 5 | 22 | 19, 83 | 15, 67 | 11, 56 | 11, 56 | |
| HIC_A6 | I | HIC Address 6 | 7, 42, 47 | 6, 20, 84 | 16, 57, 68 | 12, 57 | 12, 57 | 8, 43 |
| HIC_A7 | I | HIC Address 7 | 5, 43, 48 | 7, 21, 89 | 17, 54, 74 | 13, 61 | 13, 61 | 9, 47 |
| HIC_BASESEL0 | I | HIC Base address range select 0 | 9, 25 | 22, 57, 90 | 18, 42, 75 | 14, 62 | 14, 62 | 10 |
| HIC_BASESEL1 | I | HIC Base address range select 1 | 0 | 23, 79 | 19, 63 | 15, 52 | 15, 52 | 11, 42 |
| HIC_BASESEL2 | I | HIC Base address range select 2 | 4 | 40, 75 | 29, 59 | 25, 48 | 25, 48 | 21, 38 |
| HIC_D0 | I/O | HIC Data 0 | 26, 33 | 53, 58 | 38, 43 | 32 | 32 | 25 |
| HIC_D1 | I/O | HIC Data 1 | 16, 27 | 54, 59 | 39, 44 | 33 | 33 | 26 |
| HIC_D2 | I/O | HIC Data 2 | 17, 42, 49 | 8, 55 | 40, 57 | 34 | 34 | |
| HIC_D3 | I/O | HIC Data 3 | 24, 43, 50 | 9, 56 | 41, 54 | 35 | 35 | 27 |
| HIC_D4 | I/O | HIC Data 4 | 3, 5, 57 | 66, 76, 89 | 60, 74 | 49, 61 | 49, 61 | 39, 47 |
| HIC_D5 | I/O | HIC Data 5 | 13, 40, 44 | 50, 80, 85 | 35, 64, 69 | 29, 53 | 29, 53 | |
| HIC_D6 | I/O | HIC Data 6 | 11, 45, 51, 56 | 10, 52, 65 | 37, 73 | 31 | 31 | |
| HIC_D7 | I/O | HIC Data 7 | 0, 39, 44 | 79, 85 | 56, 63, 69 | 52 | 46, 52 | 42 |
| HIC_D8 | I/O | HIC Data 8 | 8, 30 | 74, 98 | 1, 58 | 47 | 47 | |
| HIC_D9 | I/O | HIC Data 9 | 2, 34 | 77, 94 | 61, 77 | 50 | 50 | 40 |
| HIC_D10 | I/O | HIC Data 10 | 1, 31 | 78, 99 | 2, 62 | 51 | 51 | 41 |
| HIC_D11 | I/O | HIC Data 11 | 13, 23 | 50, 81 | 35, 65 | 29, 54 | 29, 54 | |
| HIC_D12 | I/O | HIC Data 12 | 15, 41 | 82, 95 | 66, 78 | 55 | 55 | |
| HIC_D13 | I/O | HIC Data 13 | 12, 22 | 51, 83 | 36, 67 | 30, 56 | 30, 56 | |
| HIC_D14 | I/O | HIC Data 14 | 6, 7 | 84, 97 | 68, 80 | 57, 64 | 57, 64 | 43, 48 |
| HIC_D15 | I/O | HIC Data 15 | 5, 14 | 89, 96 | 74, 79 | 61 | 61 | 47 |
| HIC_INT | O | HIC Device interrupt to host | 12, 18, 32 | 51, 64, 68 | 36, 49, 50 | 30, 40, 41 | 30, 40, 41 | 32, 33 |
| HIC_NBE0 | I | HIC Byte enable 0 | 11, 19 | 38, 52, 69 | 28, 37, 51 | 24, 31, 42 | 24, 31, 42 | 20, 34 |
| HIC_NBE1 | I | HIC Byte enable 1 | 6, 34, 40 | 37, 80, 94, 97 | 24, 64, 77, 80 | 20, 53, 64 | 20, 53, 64 | 16, 48 |
| HIC_NCS | I | HIC Chip select input | 29 | 28, 100 | 3, 22 | 1, 18 | 1, 18 | 1, 14 |
| HIC_NOE | O | HIC Output enable for data bus | 3, 28 | 1, 31, 76 | 4, 23, 60 | 2, 19, 49 | 2, 19, 49 | 2, 15, 39 |
| HIC_NRDY | O | HIC Ready from device to host | 9, 37, 58 | 61, 67, 90 | 46, 75 | 37, 62 | 37, 62 | 29 |
| HIC_NWE | I | HIC Data Write enable from host | 4, 10, 35, 46, 52 | 11, 36, 63, 75, 93 | 6, 27, 48, 59, 76 | 23, 39, 48, 63 | 23, 39, 48, 63 | 19, 31, 38 |
| I2CA_SCL | I/OD | I2C-A Open-Drain Bidirectional Clock | 1, 8, 18, 27, 33, 37, 43, 57 | 53, 59, 61, 66, 68, 74, 78 | 38, 44, 46, 50, 54, 58, 62 | 32, 37, 41, 47, 51 | 32, 37, 41, 47, 51 | 25, 29, 33, 41 |
| I2CA_SDA | I/OD | I2C-A Open-Drain Bidirectional Data | 0, 10, 19, 26, 32, 35, 42, 56 | 58, 63, 64, 65, 69, 79, 93 | 43, 48, 49, 51, 57, 63, 76 | 39, 40, 42, 52, 63 | 39, 40, 42, 52, 63 | 31, 32, 34, 42 |
| I2CB_SCL | I/OD | I2C-B Open-Drain Bidirectional Clock | 3, 9, 15, 29, 51 | 10, 76, 90, 95, 100 | 3, 60, 75, 78 | 1, 49, 62 | 1, 49, 62 | 1, 39 |
| I2CB_SDA | I/OD | I2C-B Open-Drain Bidirectional Data | 2, 14, 28, 34, 50 | 1, 9, 77, 94, 96 | 4, 61, 77, 79 | 2, 50 | 2, 50 | 2, 40 |
| LINA_RX | I | LIN-A Receive | 23, 29, 33, 35, 42, 47, 49, 59 | 6, 8, 53, 63, 81, 92, 100 | 3, 38, 48, 57, 65 | 1, 32, 39, 54 | 1, 32, 39, 54 | 1, 25, 31 |
| LINA_TX | O | LIN-A Transmit | 22, 28, 32, 37, 46, 58 | 1, 61, 64, 67, 83 | 4, 6, 46, 49, 67 | 2, 37, 40, 56 | 2, 37, 40, 56 | 2, 29, 32 |

Table 5-3. Digital Signals (continued)

| SIGNAL NAME | PIN TYPE | DESCRIPTION | GPIO | 100 PZ | 80 PN | 64 PMQ | 64 PM | 48 PT |
|--------------|----------|--|---------------------------------------|------------------------------------|-----------------------------------|------------------------|------------------------|-------------------|
| LINB_RX | I | LIN-B Receive | 9, 11, 13, 15, 19, 23, 41, 55 | 43, 50, 52, 69, 81, 82, 90, 95 | 35, 37, 51, 65, 66, 75, 78 | 29, 31, 42, 54, 55, 62 | 29, 31, 42, 54, 55, 62 | 34 |
| LINB_TX | O | LIN-B Transmit | 10, 12, 14, 18, 22, 24, 40, 44, 54 | 13, 51, 56, 68, 80, 83, 85, 93, 96 | 36, 41, 50, 64, 67, 69, 76, 79 | 30, 35, 41, 53, 56, 63 | 30, 35, 41, 53, 56, 63 | 27, 33 |
| MCAN_RX | I | CAN/CAN FD Receive | 0, 5, 12, 21, 30, 39, 47, 51, 57, 61 | 6, 10, 49, 51, 66, 79, 89, 91, 98 | 1, 34, 36, 56, 63, 74 | 30, 52, 61 | 30, 46, 52, 61 | 42, 47 |
| MCAN_TX | O | CAN/CAN FD Transmit | 1, 4, 13, 20, 31, 46, 50, 56, 60 | 9, 44, 48, 50, 65, 75, 78, 99 | 2, 6, 33, 35, 59, 62 | 29, 48, 51 | 29, 48, 51 | 38, 41 |
| OUTPUTXBAR1 | O | Output X-BAR Output 1 | 2, 24, 34, 58 | 56, 67, 77, 94 | 41, 61, 77 | 35, 50 | 35, 50 | 27, 40 |
| OUTPUTXBAR2 | O | Output X-BAR Output 2 | 3, 25, 37, 54, 59 | 13, 57, 61, 76, 92 | 42, 46, 60 | 37, 49 | 37, 49 | 29, 39 |
| OUTPUTXBAR3 | O | Output X-BAR Output 3 | 4, 5, 14, 26, 48, 55, 60 | 7, 43, 44, 58, 75, 89, 96 | 43, 59, 74, 79 | 48, 61 | 48, 61 | 38, 47 |
| OUTPUTXBAR4 | O | Output X-BAR Output 4 | 6, 15, 27, 33, 49, 61 | 8, 53, 59, 91, 95, 97 | 38, 44, 78, 80 | 32, 64 | 32, 64 | 25, 48 |
| OUTPUTXBAR5 | O | Output X-BAR Output 5 | 7, 28, 42 | 1, 84 | 4, 57, 68 | 2, 57 | 2, 57 | 2, 43 |
| OUTPUTXBAR6 | O | Output X-BAR Output 6 | 9, 29, 43 | 90, 100 | 3, 54, 75 | 1, 62 | 1, 62 | 1 |
| OUTPUTXBAR7 | O | Output X-BAR Output 7 | 11, 16, 30, 44 | 52, 54, 85, 98 | 1, 37, 39, 69 | 31, 33 | 31, 33 | 26 |
| OUTPUTXBAR8 | O | Output X-BAR Output 8 | 17, 31, 45 | 55, 99 | 2, 40, 73 | 34 | 34 | |
| PMBUSA_ALERT | I/OD | PMBus-A Open-Drain Bidirectional Alert Signal | 13, 19, 27, 37, 43, 45 | 50, 59, 61, 69 | 35, 44, 46, 51, 54, 73 | 29, 37, 42 | 29, 37, 42 | 29, 34 |
| PMBUSA_CTL | I/O | PMBus-A Control Signal - Slave Input/Master Output | 12, 18, 26, 35, 42, 44 | 51, 58, 63, 68, 85 | 36, 43, 48, 50, 57, 69 | 30, 39, 41 | 30, 39, 41 | 31, 33 |
| PMBUSA_SCL | I/OD | PMBus-A Open-Drain Bidirectional Clock | 3, 15, 16, 24, 35, 41, 47 | 6, 54, 56, 63, 76, 82, 95 | 39, 41, 48, 60, 66, 78 | 33, 35, 39, 49, 55 | 33, 35, 39, 49, 55 | 26, 27, 31, 39 |
| PMBUSA_SDA | I/OD | PMBus-A Open-Drain Bidirectional Data | 2, 14, 17, 25, 32, 34, 40, 44, 46, 48 | 7, 55, 57, 64, 77, 80, 85, 94, 96 | 6, 40, 42, 49, 61, 64, 69, 77, 79 | 34, 40, 50, 53 | 34, 40, 50, 53 | 32, 40 |
| SCIA_RX | I | SCI-A Receive Data | 3, 9, 17, 25, 28, 35, 49 | 1, 8, 55, 57, 63, 76, 90 | 4, 40, 42, 48, 60, 75 | 2, 34, 39, 49, 62 | 2, 34, 39, 49, 62 | 2, 31, 39 |
| SCIA_TX | O | SCI-A Transmit Data | 2, 8, 16, 24, 29, 37, 48 | 7, 54, 56, 61, 74, 77, 100 | 3, 39, 41, 46, 58, 61 | 1, 33, 35, 37, 47, 50 | 1, 33, 35, 37, 47, 50 | 1, 26, 27, 29, 40 |
| SCIB_RX | I | SCI-B Receive Data | 11, 13, 15, 19, 23, 41, 57 | 50, 52, 66, 69, 81, 82, 95 | 35, 37, 51, 65, 66, 78 | 29, 31, 42, 54, 55 | 29, 31, 42, 54, 55 | 34 |
| SCIB_TX | O | SCI-B Transmit Data | 9, 10, 12, 14, 18, 22, 40, 56 | 51, 65, 68, 80, 83, 90, 93, 96 | 36, 50, 64, 67, 75, 76, 79 | 30, 41, 53, 56, 62, 63 | 30, 41, 53, 56, 62, 63 | 33 |
| SD1_C1 | I | SDFM-1 Channel 1 Clock Input | 17, 33, 49, 53 | 8, 12, 23, 53, 55 | 19, 38, 40 | 15, 32, 34 | 15, 32, 34 | 11, 25 |
| SD1_C2 | I | SDFM-1 Channel 2 Clock Input | 19, 33, 51, 54 | 10, 13, 31, 53, 69 | 23, 38, 51 | 19, 32, 42 | 19, 32, 42 | 15, 25, 34 |
| SD1_C3 | I | SDFM-1 Channel 3 Clock Input | 21, 53, 55 | 12, 38, 43, 49 | 28, 34 | 24 | 24 | 20 |
| SD1_C4 | I | SDFM-1 Channel 4 Clock Input | 23, 55, 56 | 40, 43, 65, 81 | 29, 65 | 25, 54 | 25, 54 | 21 |
| SD1_D1 | I | SDFM-1 Channel 1 Data Input | 16, 48 | 7, 19, 54 | 15, 39 | 11, 33 | 11, 33 | 26 |
| SD1_D2 | I | SDFM-1 Channel 2 Data Input | 18, 32, 50 | 9, 20, 64, 68 | 16, 49, 50 | 12, 40, 41 | 12, 40, 41 | 8, 32, 33 |
| SD1_D3 | I | SDFM-1 Channel 3 Data Input | 20, 52 | 11, 21, 48 | 17, 33 | 13 | 13 | 9 |
| SD1_D4 | I | SDFM-1 Channel 4 Data Input | 22, 54 | 13, 22, 83 | 18, 67 | 14, 56 | 14, 56 | 10 |
| SD2_C1 | I | SDFM-2 Channel 1 Clock Input | 25, 35, 57 | 14, 37, 57, 63, 66 | 10, 24, 42, 48 | 6, 20, 39 | 6, 20, 39 | 4, 16, 31 |
| SD2_C2 | I | SDFM-2 Channel 2 Clock Input | 27, 58, 59 | 36, 59, 67, 92 | 27, 44 | 23 | 23 | 19 |
| SD2_C3 | I | SDFM-2 Channel 3 Clock Input | 29, 45, 59, 61 | 28, 91, 92, 100 | 3, 22, 73 | 1, 18 | 1, 18 | 1, 14 |
| SD2_C4 | I | SDFM-2 Channel 4 Clock Input | 31, 46, 60 | 32, 44, 99 | 2, 6 | | | |
| SD2_D1 | I | SDFM-2 Channel 1 Data Input | 24, 49, 56 | 8, 56, 65 | 14, 41 | 10, 35 | 10, 35 | 7, 27 |
| SD2_D2 | I | SDFM-2 Channel 2 Data Input | 26, 50, 58 | 9, 16, 58, 67 | 12, 43 | 8 | 8 | 5 |
| SD2_D3 | I | SDFM-2 Channel 3 Data Input | 28, 43, 51, 60 | 1, 10, 17, 44 | 4, 13, 54 | 2, 9 | 2, 9 | 2, 6 |
| SD2_D4 | I | SDFM-2 Channel 4 Data Input | 30, 47, 52 | 6, 11, 15, 98 | 1, 11 | 7 | 7 | 4 |
| SPIA_CLK | I/O | SPI-A Clock | 3, 9, 12, 18, 56 | 51, 65, 68, 76, 90 | 36, 50, 60, 75 | 30, 41, 49, 62 | 30, 41, 49, 62 | 33, 39 |
| SPIA_SIMO | I/O | SPI-A Slave In, Master Out (SIMO) | 2, 8, 11, 16, 54 | 13, 52, 54, 74, 77 | 37, 39, 58, 61 | 31, 33, 47, 50 | 31, 33, 47, 50 | 26, 40 |
| SPIA_SOMI | I/O | SPI-A Slave Out, Master In (SOMI) | 1, 10, 13, 17, 55 | 43, 50, 55, 78, 93 | 35, 40, 62, 76 | 29, 34, 51, 63 | 29, 34, 51, 63 | 41 |
| SPIA_STE | I/O | SPI-A Slave Transmit Enable (STE) | 0, 5, 11, 19, 57 | 52, 66, 69, 79, 89 | 37, 51, 63, 74 | 31, 42, 52, 61 | 31, 42, 52, 61 | 34, 42, 47 |

Table 5-3. Digital Signals (continued)

| SIGNAL NAME | PIN TYPE | DESCRIPTION | GPIO | 100 PZ | 80 PN | 64 PMQ | 64 PM | 48 PT |
|-------------|----------|---|-----------------------------------|------------------------------------|-----------------------|---------------|---------------|-----------|
| SPIB_CLK | I/O | SPI-B Clock | 4, 14, 22, 26, 28, 32, 52, 58 | 1, 11, 58, 64, 67, 75, 83, 96 | 4, 43, 49, 59, 67, 79 | 2, 40, 48, 56 | 2, 40, 48, 56 | 2, 32, 38 |
| SPIB_SIMO | I/O | SPI-B Slave In, Master Out (SIMO) | 7, 20, 24, 30, 40, 50, 56, 60 | 9, 44, 48, 56, 65, 80, 84, 98 | 1, 33, 41, 64, 68 | 35, 53, 57 | 35, 53, 57 | 27, 43 |
| SPIB_SOMI | I/O | SPI-B Slave Out, Master In (SOMI) | 6, 16, 21, 25, 31, 41, 51, 57, 61 | 10, 49, 54, 57, 66, 82, 91, 97, 99 | 2, 34, 39, 42, 66, 80 | 33, 55, 64 | 33, 55, 64 | 26, 48 |
| SPIB_STE | I/O | SPI-B Slave Transmit Enable (STE) | 15, 23, 27, 29, 33, 53, 59 | 12, 53, 59, 81, 92, 95, 100 | 3, 38, 44, 65, 78 | 1, 32, 54 | 1, 32, 54 | 1, 25 |
| SYNCOUT | O | External ePWM Synchronization Pulse | 6, 39, 52 | 11, 97 | 56, 80 | 64 | 46, 64 | 48 |
| TDI | I | JTAG Test Data Input (TDI) - TDI is the default mux selection for the pin. The internal pullup is disabled by default. The internal pullup should be enabled or an external pullup added on the board if this pin is used as JTAG TDI to avoid a floating input. | 35 | 63 | 48 | 39 | 39 | 31 |
| TDO | O | JTAG Test Data Output (TDO) - TDO is the default mux selection for the pin. The internal pullup is disabled by default. The TDO function will be in a tri-state condition when there is no JTAG activity, leaving this pin floating; the internal pullup should be enabled or an external pullup added on the board to avoid a floating GPIO input. | 37 | 61 | 46 | 37 | 37 | 29 |
| X1 | I/O | Crystal oscillator input or single-ended clock input. The device initialization software must configure this pin before the crystal oscillator is enabled. To use this oscillator, a quartz crystal circuit must be connected to X1 and X2. This pin can also be used to feed a single-ended 3.3-V level clock. See the XTAL section for usage details. | 19 | 69 | 51 | 42 | 42 | 34 |
| X2 | I/O | Crystal oscillator output. | 18 | 68 | 50 | 41 | 41 | 33 |
| XCLKOUT | O | External Clock Output. This pin outputs a divided-down version of a chosen clock signal from within the device. | 16, 18 | 54, 68 | 39, 50 | 33, 41 | 33, 41 | 26, 33 |

5.3.3 Power and Ground

Table 5-4. Power and Ground

| SIGNAL NAME | PIN TYPE | DESCRIPTION | 100 PZ | 80 PN | 64 PMQ | 64 PM | 48 PT |
|-------------|----------|---|---------------|---------------|---------------|---------------|------------|
| VDD | | 1.2-V Digital Logic Power Pins. See the Power Management Module (PMM) section for usage details. | 4, 46, 71, 87 | 8, 31, 53, 71 | 4, 27, 44, 59 | 4, 27, 44, 59 | 23, 36, 45 |
| VDDA | | 3.3-V Analog Power Pins. Place a minimum 2.2- μ F decoupling capacitor on each pin. See the Power Management Module (PMM) section for usage details. | 34 | 26 | 22 | 22 | 18 |
| VDDIO | | 3.3-V Digital I/O Power Pins. See the Power Management Module (PMM) section for usage details. | 3, 47, 70, 88 | 7, 32, 52, 72 | 28, 43, 60 | 28, 43, 60 | 24, 35, 46 |
| VREGENZ | I | Internal voltage regulator enable with internal pulldown. Tie low to VSS to enable internal VREG. Tie high to VDDIO to use an external supply. See the Power Management Module (PMM) section for usage details. | 73 | | 46 | | |
| VSS | | Digital Ground | 5, 45, 72, 86 | 9, 30, 55, 70 | 5, 26, 45, 58 | 5, 26, 45, 58 | 22, 37, 44 |
| VSSA | | Analog Ground | 33 | 25 | 21 | 21 | 17 |

5.3.4 Test, JTAG, and Reset

Table 5-5. Test, JTAG, and Reset

| SIGNAL NAME | PIN TYPE | DESCRIPTION | 100 PZ | 80 PN | 64 PMQ | 64 PM | 48 PT |
|-------------|----------|---|--------|-------|--------|-------|-------|
| TCK | I | JTAG test clock with internal pullup. | 60 | 45 | 36 | 36 | 28 |
| TMS | I/O | JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK. This device does not have a TRSTn pin. An external pullup resistor (recommended 2.2 kΩ) on the TMS pin to VDDIO should be placed on the board to keep JTAG in reset during normal operation. | 62 | 47 | 38 | 38 | 30 |
| XRSn | I/OD | Device Reset (in) and Watchdog Reset (out). During a power-on condition, this pin is driven low by the device. An external circuit may also drive this pin to assert a device reset. This pin is also driven low by the MCU when a watchdog reset occurs. During watchdog reset, the XRSn pin is driven low for the watchdog reset duration of 512 OSCCLK cycles. A resistor between 2.2 kΩ and 10 kΩ should be placed between XRSn and VDDIO. If a capacitor is placed between XRSn and VSS for noise filtering, it should be 100 nF or smaller. These values will allow the watchdog to properly drive the XRSn pin to VOL within 512 OSCCLK cycles when the watchdog reset is asserted. This pin is an open-drain output with an internal pullup. If this pin is driven by an external device, it should be done using an open-drain device. | 2 | 5 | 3 | 3 | 3 |

5.4 Pin Multiplexing

5.4.1 GPIO Muxed Pins

Table 5-6 lists the GPIO muxed pins. The default mode for each GPIO pin is the GPIO function, except GPIO35 and GPIO37, which default to TDI and TDO, respectively. Secondary functions can be selected by setting both the GPyGMUXn.GPIOz and GPyMUXn.GPIOz register bits. The GPyGMUXn register should be configured before the GPyMUXn to avoid transient pulses on GPIOs from alternate mux selections. Columns that are not shown and blank cells are reserved GPIO Mux settings. GPIO ALT functions cannot be configured with the GPyMUXn and GPyGMUXn registers. These are special functions that need to be configured from the module.

Note

GPIO36 and GPIO38 do not exist on this device. GPIO62 to GPIO63 exist but are not pinned out on any packages. Boot ROM enables pullups on GPIO62 to GPIO63. For more details, see [Section 5.5](#).

5.4.1.1 GPIO Muxed Pins

Table 5-6. GPIO Muxed Pins

| 0, 4, 8, 12 | 1 | 2 | 3 | 5 | 6 | 7 | 9 | 10 | 11 | 13 | 14 | 15 | ALT |
|-------------|------------------|-------------|-------------|--------------|-------------|--------------|------------------|-----------------|-----------------|------------------|--------------------|-----------------|-----|
| GPIO0 | EPWM1_A | | | | I2CA_SDA | SPIA_STE | FSIRXA_CLK | MCAN_RX | CLB_OUTPUTXBAR8 | EQEP1_INDE X | HIC_D7 | HIC_BASESEL1 | |
| GPIO1 | EPWM1_B | | | | I2CA_SCL | SPIA_SOMI | | MCAN_TX | CLB_OUTPUTXBAR7 | HIC_A2 | FSITXA_TDM_D1 | HIC_D10 | |
| GPIO2 | EPWM2_A | | | OUTPUTXBAR1 | PMBUSA_SDA | SPIA_SIMO | SCIA_TX | FSIRXA_D1 | I2CB_SDA | HIC_A1 | CANA_TX | HIC_D9 | |
| GPIO3 | EPWM2_B | OUTPUTXBAR2 | | OUTPUTXBAR2 | PMBUSA_SCL | SPIA_CLK | SCIA_RX | FSIRXA_D0 | I2CB_SCL | HIC_NOE | CANA_RX | HIC_D4 | |
| GPIO4 | EPWM3_A | | MCAN_TX | OUTPUTXBAR3 | CANA_TX | SPIB_CLK | EQEP2_STRO BE | FSIRXA_CLK | CLB_OUTPUTXBAR6 | HIC_BASESEL 2 | | HIC_NWE | |
| GPIO5 | EPWM3_B | | OUTPUTXBAR3 | MCAN_RX | CANA_RX | SPIA_STE | FSITXA_D1 | CLB_OUTPUTXBAR5 | | HIC_A7 | HIC_D4 | HIC_D15 | |
| GPIO6 | EPWM4_A | OUTPUTXBAR4 | SYNCOU | EQEP1_A | | SPIB_SOMI | FSITXA_D0 | | FSITXA_D1 | HIC_NBE1 | CLB_OUTPUTXBAR8 | HIC_D14 | |
| GPIO7 | EPWM4_B | | OUTPUTXBAR5 | EQEP1_B | | SPIB_SIMO | FSITXA_CLK | CLB_OUTPUTXBAR2 | | HIC_A6 | | HIC_D14 | |
| GPIO8 | EPWM5_A | | ADCSOAO | EQEP1_STROBE | SCIA_TX | SPIA_SIMO | I2CA_SCL | FSITXA_D1 | CLB_OUTPUTXBAR5 | HIC_A0 | FSITXA_TDM_CL K | HIC_D8 | |
| GPIO9 | EPWM5_B | SCIB_TX | OUTPUTXBAR6 | EQEP1_INDEX | SCIA_RX | SPIA_CLK | | FSITXA_D0 | LINB_RX | HIC_BASESEL 0 | I2CB_SCL | HIC_NRDY | |
| GPIO10 | EPWM6_A | | ADCSOBO | EQEP1_A | SCIB_TX | SPIA_SOMI | I2CA_SDA | FSITXA_CLK | LINB_TX | HIC_NWE | FSITXA_TDM_D0 | CLB_OUTPUTXBAR4 | |
| GPIO11 | EPWM6_B | | OUTPUTXBAR7 | EQEP1_B | SCIB_RX | SPIA_STE | FSIRXA_D1 | LINB_RX | EQEP2_A | SPIA_SIMO | HIC_D6 | HIC_NBE0 | |
| GPIO12 | EPWM7_A | | MCAN_RX | EQEP1_STROBE | SCIB_TX | PMBUSA_CTL | FSIRXA_D0 | LINB_TX | SPIA_CLK | CANA_RX | HIC_D13 | HIC_INT | |
| GPIO13 | EPWM7_B | | MCAN_TX | EQEP1_INDEX | SCIB_RX | PMBUSA_ALERT | FSIRXA_CLK | LINB_RX | SPIA_SOMI | CANA_TX | HIC_D11 | HIC_D5 | |
| GPIO14 | EPWM8_A | SCIB_TX | | I2CB_SDA | OUTPUTXBAR3 | PMBUSA_SDA | SPIB_CLK | EQEP2_A | LINB_TX | EPWM3_A | CLB_OUTPUTXBAR7 | HIC_D15 | |
| GPIO15 | EPWM8_B | SCIB_RX | | I2CB_SCL | OUTPUTXBAR4 | PMBUSA_SCL | SPIB_STE | EQEP2_B | LINB_RX | EPWM3_B | CLB_OUTPUTXBAR6 | HIC_D12 | |
| GPIO16 | SPIA_SIMO | | OUTPUTXBAR7 | EPWM5_A | SCIA_TX | SD1_D1 | EQEP1_STRO BE | PMBUSA_SCL | XCLKOUT | EQEP2_B | SPIB_SOMI | HIC_D1 | |
| GPIO17 | SPIA_SOMI | | OUTPUTXBAR8 | EPWM5_B | SCIA_RX | SD1_C1 | EQEP1_INDE X | PMBUSA_SDA | CANA_TX | | | HIC_D2 | |
| GPIO18 | SPIA_CLK | SCIB_TX | CANA_RX | EPWM6_A | I2CA_SCL | SD1_D2 | EQEP2_A | PMBUSA_CTL | XCLKOUT | LINB_TX | FSITXA_TDM_CL K | HIC_INT | X2 |
| GPIO19 | SPIA_STE | SCIB_RX | CANA_TX | EPWM6_B | I2CA_SDA | SD1_C2 | EQEP2_B | PMBUSA_ALERT | CLB_OUTPUTXBAR1 | LINB_RX | FSITXA_TDM_D0 | HIC_NBE0 | X1 |
| GPIO20 | EQEP1_A | | | | SPIB_SIMO | SD1_D3 | MCAN_TX | | | | | | |
| GPIO21 | EQEP1_B | | | | SPIB_SOMI | SD1_C3 | MCAN_RX | | | | | | |
| GPIO22 | EQEP1_STRO BE | | SCIB_TX | | SPIB_CLK | SD1_D4 | LINA_TX | CLB_OUTPUTXBAR1 | LINB_TX | HIC_A5 | EPWM4_A | HIC_D13 | |
| GPIO23 | EQEP1_INDE X | | SCIB_RX | | SPIB_STE | SD1_C4 | LINA_RX | CLB_OUTPUTXBAR3 | LINB_RX | HIC_A3 | EPWM4_B | HIC_D11 | |
| GPIO24 | OUTPUTXBAR1 | EQEP2_A | | EPWM8_A | SPIB_SIMO | SD2_D1 | LINB_TX | PMBUSA_SCL | SCIA_TX | ERRORSTS | | HIC_D3 | |

Table 5-6. GPIO Muxed Pins (continued)

| 0, 4, 8, 12 | 1 | 2 | 3 | 5 | 6 | 7 | 9 | 10 | 11 | 13 | 14 | 15 | ALT |
|-------------|--------------|--------------|-------------|-----------------|--------------|-----------------|--------------|-----------------|-----------------|----------|----------------|---------|----------|
| GPIO25 | OUTPUTXBAR2 | EQEP2_B | | EQEP1_A | SPIB_SOMI | SD2_C1 | FSITXA_D1 | PMBUSA_SDA | SCIA_RX | | HIC_BASESEL0 | | |
| GPIO26 | OUTPUTXBAR3 | EQEP2_INDEX | | OUTPUTXBAR3 | SPIB_CLK | SD2_D2 | FSITXA_D0 | PMBUSA_CTL | I2CA_SDA | | HIC_D0 | HIC_A1 | |
| GPIO27 | OUTPUTXBAR4 | EQEP2_STROBE | | OUTPUTXBAR4 | SPIB_STE | SD2_C2 | FSITXA_CLK | PMBUSA_ALERT | I2CA_SCL | | HIC_D1 | HIC_A4 | |
| GPIO28 | SCIA_RX | | EPWM7_A | OUTPUTXBAR5 | EQEP1_A | SD2_D3 | EQEP2_STROBE | LINA_TX | SPIB_CLK | ERRORSTS | I2CB_SDA | HIC_NOE | |
| GPIO29 | SCIA_TX | | EPWM7_B | OUTPUTXBAR6 | EQEP1_B | SD2_C3 | EQEP2_INDEX | LINA_RX | SPIB_STE | ERRORSTS | I2CB_SCL | HIC_NCS | AUXCLKIN |
| GPIO30 | CANA_RX | | SPIB_SIMO | OUTPUTXBAR7 | EQEP1_STROBE | SD2_D4 | FSIRXA_CLK | MCAN_RX | EPWM1_A | | HIC_D8 | | |
| GPIO31 | CANA_TX | | SPIB_SOMI | OUTPUTXBAR8 | EQEP1_INDEX | SD2_C4 | FSIRXA_D1 | MCAN_TX | EPWM1_B | | HIC_D10 | | |
| GPIO32 | I2CA_SDA | | SPIB_CLK | EPWM8_B | LINA_TX | SD1_D2 | FSIRXA_D0 | CANA_TX | PMBUSA_SDA | ADCSOCBO | | HIC_INT | |
| GPIO33 | I2CA_SCL | | SPIB_STE | OUTPUTXBAR4 | LINA_RX | SD1_C2 | FSIRXA_CLK | CANA_RX | EQEP2_B | ADCSOCAO | SD1_C1 | HIC_D0 | |
| GPIO34 | OUTPUTXBAR1 | | | | PMBUSA_SDA | | | | | HIC_NBE1 | I2CB_SDA | HIC_D9 | |
| GPIO35 | SCIA_RX | | I2CA_SDA | CANA_RX | PMBUSA_SCL | LINA_RX | EQEP1_A | PMBUSA_CTL | EPWM5_B | SD2_C1 | HIC_NWE | TDI | |
| GPIO37 | OUTPUTXBAR2 | | I2CA_SCL | SCIA_TX | CANA_TX | LINA_TX | EQEP1_B | PMBUSA_ALERT | | | HIC_NRDY | TDO | |
| GPIO39 | | | | | MCAN_RX | FSIRXA_CLK | EQEP2_INDEX | | CLB_OUTPUTXBAR2 | SYNCOUT | EQEP1_INDEX | HIC_D7 | |
| GPIO40 | SPIB_SIMO | | | EPWM2_B | PMBUSA_SDA | FSIRXA_D0 | SCIB_TX | EQEP1_A | LINB_TX | | HIC_NBE1 | HIC_D5 | |
| GPIO41 | | | | EPWM2_A | PMBUSA_SCL | FSIRXA_D1 | SCIB_RX | EQEP1_B | LINB_RX | HIC_A4 | SPIB_SOMI | HIC_D12 | |
| GPIO42 | | LINA_RX | OUTPUTXBAR5 | PMBUSA_CTL | I2CA_SDA | | | EQEP1_STROBE | CLB_OUTPUTXBAR3 | | HIC_D2 | HIC_A6 | |
| GPIO43 | | | OUTPUTXBAR6 | PMBUSA_ALERT | I2CA_SCL | | PMBUSA_ALERT | EQEP1_INDEX | CLB_OUTPUTXBAR4 | SD2_D3 | HIC_D3 | HIC_A7 | |
| GPIO44 | | | OUTPUTXBAR7 | EQEP1_A | PMBUSA_SDA | FSITXA_CLK | PMBUSA_CTL | CLB_OUTPUTXBAR3 | FSIRXA_D0 | HIC_D7 | LINB_TX | HIC_D5 | |
| GPIO45 | | | OUTPUTXBAR8 | | | FSITXA_D0 | PMBUSA_ALERT | CLB_OUTPUTXBAR4 | | SD2_C3 | | HIC_D6 | |
| GPIO46 | | | LINA_TX | MCAN_TX | | FSITXA_D1 | PMBUSA_SDA | | | SD2_C4 | | HIC_NWE | |
| GPIO47 | | | LINA_RX | MCAN_RX | | CLB_OUTPUTXBAR2 | PMBUSA_SCL | | | SD2_D4 | FSITXA_TDM_CLK | HIC_A6 | |
| GPIO48 | OUTPUTXBAR3 | | CANA_TX | | SCIA_TX | SD1_D1 | PMBUSA_SDA | | | | | HIC_A7 | |
| GPIO49 | OUTPUTXBAR4 | | CANA_RX | | SCIA_RX | SD1_C1 | LINA_RX | | | SD2_D1 | FSITXA_D0 | HIC_D2 | |
| GPIO50 | EQEP1_A | | | MCAN_TX | SPIB_SIMO | SD1_D2 | I2CB_SDA | | | SD2_D2 | FSITXA_D1 | HIC_D3 | |
| GPIO51 | EQEP1_B | | | MCAN_RX | SPIB_SOMI | SD1_C2 | I2CB_SCL | | | SD2_D3 | FSITXA_CLK | HIC_D6 | |
| GPIO52 | EQEP1_STROBE | | | CLB_OUTPUTXBAR5 | SPIB_CLK | SD1_D3 | SYNCOUT | | | SD2_D4 | FSIRXA_D0 | HIC_NWE | |
| GPIO53 | EQEP1_INDEX | | | CLB_OUTPUTXBAR6 | SPIB_STE | SD1_C3 | ADCSOCAO | CANA_RX | | SD1_C1 | FSIRXA_D1 | | |

Table 5-6. GPIO Muxed Pins (continued)

| 0, 4, 8, 12 | 1 | 2 | 3 | 5 | 6 | 7 | 9 | 10 | 11 | 13 | 14 | 15 | ALT |
|-------------|-----------|-----------------|---------|--------------|-------------|--------|-----------|----------|--------------|--------|---------------|---------------|-----|
| GPIO54 | SPIA_SIMO | | | EQEP2_A | OUTPUTXBAR2 | SD1_D4 | ADCSOCBO | LINB_TX | | SD1_C2 | FSIRXA_CLK | FSITXA_TDM_D1 | |
| GPIO55 | SPIA_SOMI | | | EQEP2_B | OUTPUTXBAR3 | SD1_C4 | ERRORSTS | LINB_RX | | SD1_C3 | | HIC_A0 | |
| GPIO56 | SPIA_CLK | CLB_OUTPUTXBAR7 | MCAN_TX | EQEP2_STROBE | SCIB_TX | SD2_D1 | SPIB_SIMO | I2CA_SDA | EQEP1_A | SD1_C4 | FSIRXA_D1 | HIC_D6 | |
| GPIO57 | SPIA_STE | CLB_OUTPUTXBAR8 | MCAN_RX | EQEP2_INDEX | SCIB_RX | SD2_C1 | SPIB_SOMI | I2CA_SCL | EQEP1_B | | FSIRXA_CLK | HIC_D4 | |
| GPIO58 | | | | OUTPUTXBAR1 | SPIB_CLK | SD2_D2 | LINA_TX | CANA_TX | EQEP1_STROBE | SD2_C2 | FSIRXA_D0 | HIC_NRDY | |
| GPIO59 | | | | OUTPUTXBAR2 | SPIB_STE | SD2_C2 | LINA_RX | CANA_RX | EQEP1_INDEX | SD2_C3 | FSITXA_TDM_D1 | | |
| GPIO60 | | | MCAN_TX | OUTPUTXBAR3 | SPIB_SIMO | SD2_D3 | | | | SD2_C4 | | HIC_A0 | |
| GPIO61 | | | MCAN_RX | OUTPUTXBAR4 | SPIB_SOMI | SD2_C3 | | | | | CANA_RX | | |
| AIO224 | | SD2_D3 | | | | | | | | | | HIC_A3 | |
| AIO225 | | SD2_C2 | | | | | | | | | | HIC_NWE | |
| AIO226 | | SD2_D4 | | | | | | | | | | HIC_A1 | |
| AIO227 | | SD1_C3 | | | | | | | | | | HIC_NBE0 | |
| AIO228 | | SD2_C1 | | | | | | | | | | HIC_A0 | |
| AIO229 | | | | | | | | | | | | | |
| AIO230 | | SD1_C4 | | | | | | | | | | HIC_BASESEL2 | |
| AIO231 | | SD1_C1 | | | | | | | | | | HIC_BASESEL1 | |
| AIO232 | | SD1_D4 | | | | | | | | | | HIC_BASESEL0 | |
| AIO233 | | SD2_D1 | | | | | | | | | | HIC_A4 | |
| AIO236 | | | | | | | | | | | | | |
| AIO237 | | SD1_D2 | | | | | | | | | | HIC_A6 | |
| AIO238 | | SD2_C3 | | | | | | | | | | HIC_NCS | |
| AIO239 | | SD1_D1 | | | | | | | | | | HIC_A5 | |
| AIO240 | | SD2_C1 | | | | | | | | | | HIC_NBE1 | |
| AIO241 | | SD2_C1 | | | | | | | | | | HIC_NBE1 | |
| AIO242 | | SD2_D2 | | | | | | | | | | HIC_A2 | |
| AIO244 | | SD1_D3 | | | | | | | | | | HIC_A7 | |
| AIO245 | | SD1_C2 | | | | | | | | | | HIC_NOE | |
| AIO247 | | | | | | | | | | | | | |
| AIO248 | | | | | | | | | | | | | |
| AIO249 | | | | | | | | | | | | | |
| AIO251 | | | | | | | | | | | | | |
| AIO252 | | SD2_C4 | | | | | | | | | | | |
| AIO253 | | | | | | | | | | | | | |

5.4.2 Digital Inputs on ADC Pins (AIOs)

GPIOs on port H (GPIO224–GPIO253) are multiplexed with analog pins. These are also referred to as AIOs. These pins can only function in input mode. By default, these pins will function as analog pins and the GPIOs are in a high-Z state. The GPHAMSEL register is used to configure these pins for digital or analog operation.

Note

If digital signals with sharp edges (high dv/dt) are connected to the AIOs, cross-talk can occur with adjacent analog signals. The user should therefore limit the edge rate of signals connected to AIOs if adjacent channels are being used for analog functions.

5.4.3 Digital Inputs and Outputs on ADC Pins (AGPIOs)

Some GPIOs on this device are multiplexed with analog pins. These are also referred to as AGPIOs. Unlike AIOs, AGPIOs have full input and output capability. This device has two GPIOs (GPIO20, GPIO21) that offer this feature on the 100-Pin PZ and 80-Pin PN packages.

100-Pin PZ: On this package, there are dedicated pins for B5 (pin 32) and B11 (pin 30) which respectively also have AIO252 and AIO251 functionality. In addition, GPIO20 (pin 48) and GPIO21 (pin 49) are also available as B5 and B11 respectively. Since B5 and B11 are dedicated pins on this package, it is recommended to use them instead of the ones on GPIO20/21.

80-Pin PN: On this package, GPIO20 (pin 33) and GPIO21 (pin 34) are also available as B5 and B11 respectively. There are no dedicated pin for B5 and B11.

By default the AGPIOs are not connected and have to be configured. [Table 5-7](#) truth table shows how to configure the AGPIOs using B5 (pin 32) and GPIO20 (pin 48) on the 100-Pin PZ as an example.

Table 5-7. AGPIO Configuration

| AGPIOTRLA.bit.GPIO20 | GPAAMSEL.bit.GPIO20 | GPHAMSEL.bit.GPIO252 | B5 CONNECTED TO | | | GPIO20 CONNECTED TO | | |
|----------------------|---------------------|----------------------|-----------------|--------|--------|---------------------|--------|--------|
| | | | ADC | GPIO20 | AIO252 | ADC | GPIO20 | AIO252 |
| 0 | 0 | 1 | Yes | - | - | - | Yes | - |
| 0 | 1 | 1 | Yes | - | - | - | - | - |
| 1 | 0 | 1 | Yes | - | - | - | Yes | - |
| 1 | 1 | 1 | - | - | - | Yes | - | - |
| 0 | 0 | 0 | Yes | - | Yes | - | Yes | - |
| 0 | 1 | 0 | Yes | - | Yes | - | - | - |
| 1 | 0 | 0 | Yes | - | Yes | - | Yes | - |
| 1 | 1 | 0 | - | - | Yes | Yes | - | - |

Note

If digital signals with sharp edges (high dv/dt) are connected to the AGPIOs, cross-talk can occur with adjacent analog signals. The user should therefore limit the edge rate of signals connected to AGPIOs if adjacent channels are being used for analog functions.

5.4.4 GPIO Input X-BAR

The Input X-BAR is used to route signals from a GPIO to many different IP blocks such as the ADCs, eCAPs, ePWMs, and external interrupts (see [Figure 5-6](#)). [Table 5-8](#) lists the input X-BAR destinations.

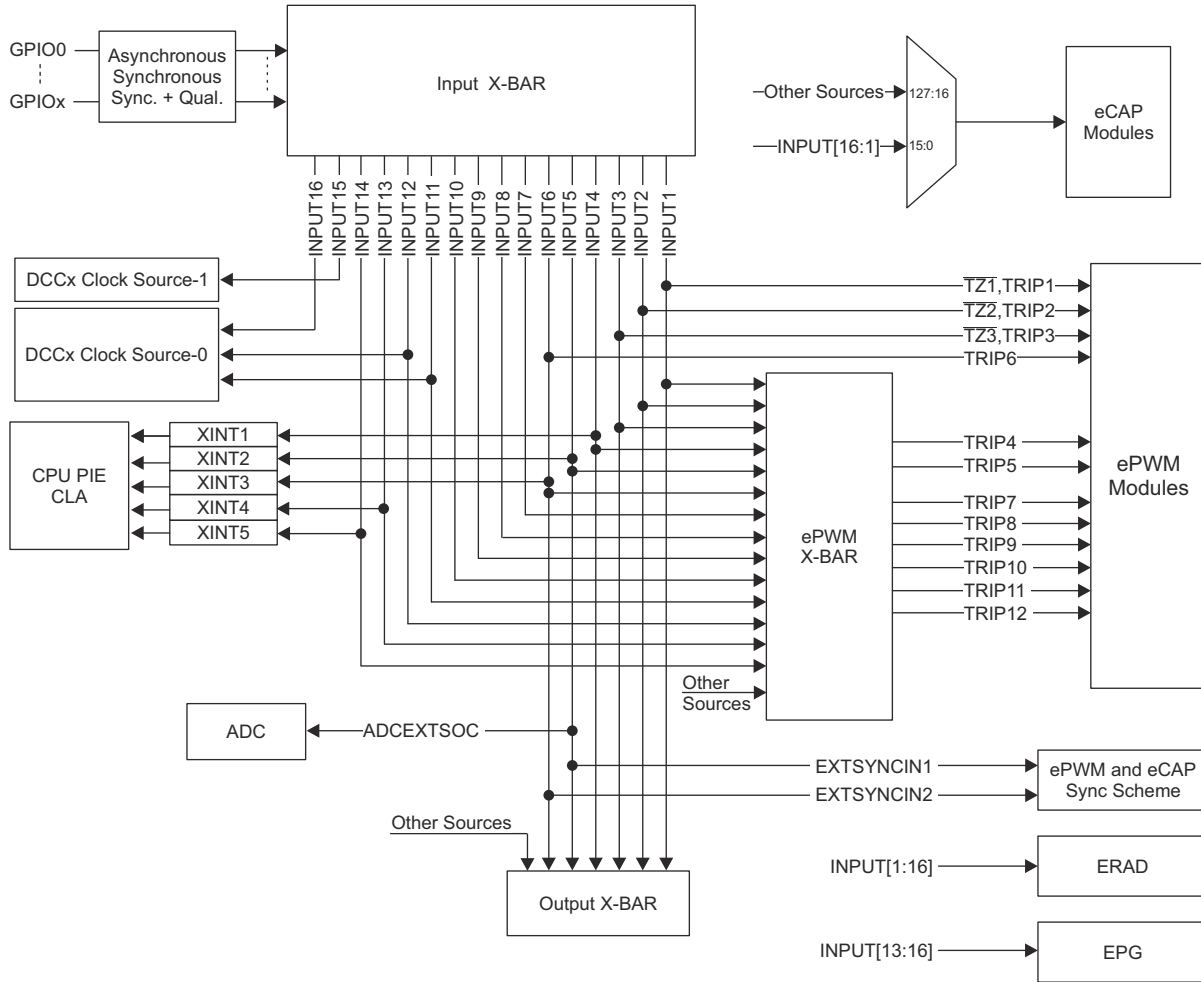


Figure 5-6. Input X-BAR

Table 5-8. Input X-BAR Destinations

| INPUT | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
|-------------------------|------------|------------|------------|-------|------------|------------|-----|-----|-----|-----|------|------|----------|----------|----------|----------|
| ECAP / HRCAP | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| EPWM X-BAR | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | | |
| CLB X-BAR | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | | |
| OUTPUT X-BAR | Yes | Yes | Yes | Yes | Yes | Yes | | | | | | | | | | |
| CPU XINT | | | | XINT1 | XINT2 | XINT3 | | | | | | | XINT4 | XINT5 | | |
| EPWM TRIP | TZ1, TRIP1 | TZ2, TRIP2 | TZ3, TRIP3 | | | TRIP6 | | | | | | | | | | |
| ADC START OF CONVERSION | | | | | ADCEXTSOC | | | | | | | | | | | |
| EPWM / ECAP SYNC | | | | | EXTSYNCIN1 | EXTSYNCIN2 | | | | | | | | | | |
| DCCx | | | | | | | | | | | CLK0 | CLK0 | | | CLK1 | CLK0 |
| EPG | | | | | | | | | | | | | EPG1 IN1 | EPG1 IN2 | EPG1 IN3 | EPG1 IN4 |
| ERAD | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |

5.4.5 GPIO Output X-BAR, CLB X-BAR, CLB Output X-BAR, and ePWM X-BAR

The Output X-BAR has eight outputs that can be selected on the GPIO mux as OUTPUTXBARx. The CLB X-BAR has eight outputs that are connected to the CLB global mux as AUXSIGx. The CLB Output X-BAR has eight outputs that can be selected on the GPIO mux as CLB_OUTPUTXBARx. The ePWM X-BAR has eight outputs that are connected to the TRIPx inputs of the ePWM. The sources for the Output X-BAR, CLB X-BAR, CLB Output X-BAR, and ePWM X-BAR are shown in [Figure 5-7](#).

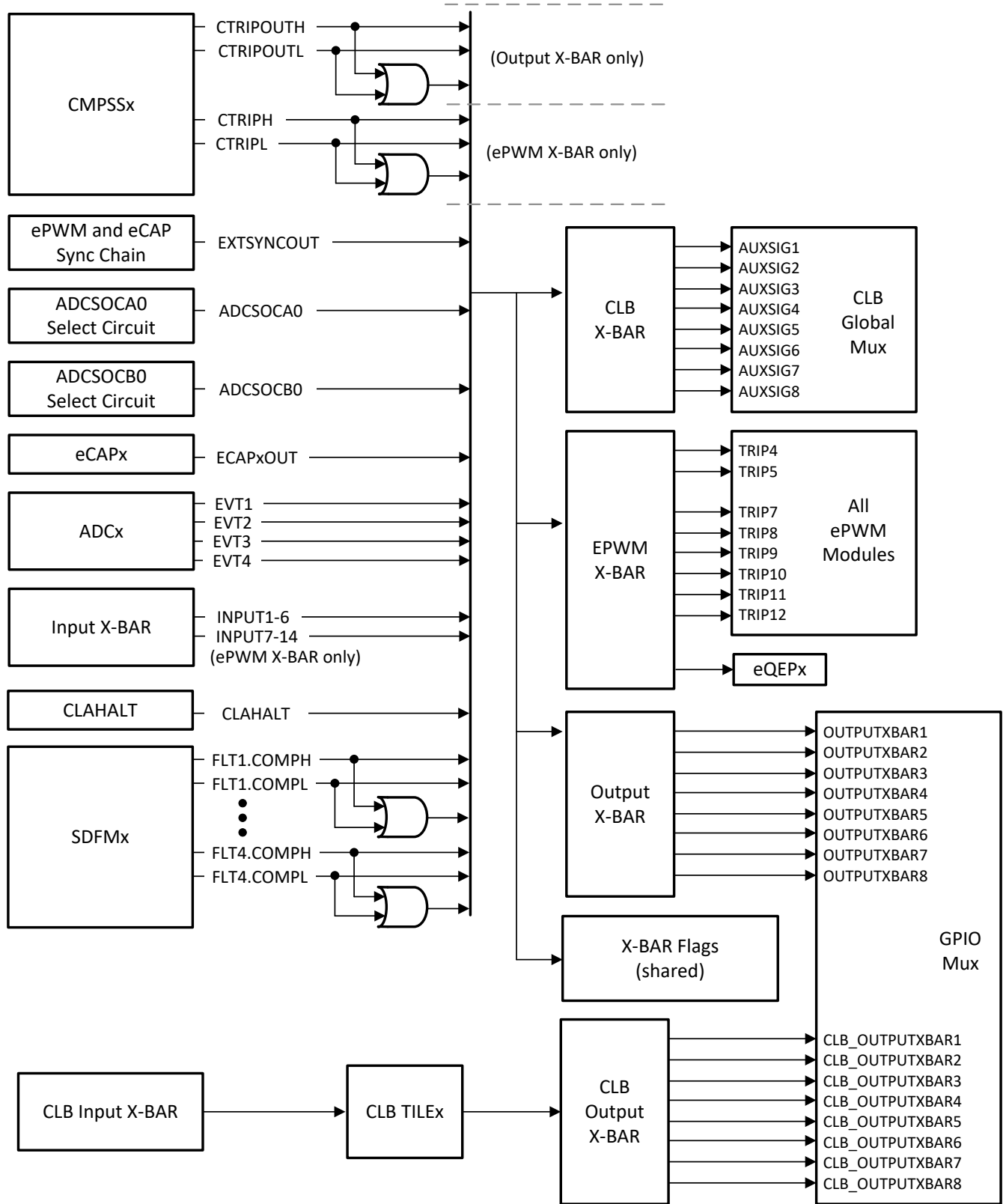


Figure 5-7. Output X-BAR, CLB X-BAR, CLB Output X-BAR, and ePWM X-BAR Sources

5.5 Pins With Internal Pullup and Pulldown

Some pins on the device have internal pullups or pulldowns. [Table 5-9](#) lists the pull direction and when it is active. The pullups on GPIO pins are disabled by default and can be enabled through software. To avoid any floating unbonded inputs, the Boot ROM will enable internal pullups on GPIO pins that are not bonded out in a particular package. Other pins noted in [Table 5-9](#) with pullups and pulldowns are always on and cannot be disabled.

Table 5-9. Pins With Internal Pullup and Pulldown

| PIN | RESET (XRSn = 0) | DEVICE BOOT | APPLICATION |
|-----------------------------|-------------------------------|--------------------------------|---------------------|
| GPIOx | Pullup disabled | Pullup disabled ⁽¹⁾ | Application defined |
| GPIO35/TDI | Pullup disabled | | Application defined |
| GPIO37/TDO | Pullup disabled | | Application defined |
| AGPIOx | Pullup disabled | Pullup disabled | Application defined |
| TCK | Pullup active | | |
| TMS | Pullup active | | |
| XRSn | Pullup active | | |
| Other pins (including AIOs) | No pullup or pulldown present | | |

(1) Pins not bonded out in a given package will have the internal pullups enabled by the Boot ROM.

5.6 Connections for Unused Pins

For applications that do not need to use all functions of the device, [Table 5-10](#) lists acceptable conditioning for any unused pins. When multiple options are listed in [Table 5-10](#), any option is acceptable. Pins not listed in [Table 5-10](#) must be connected according to [Section 5](#).

Table 5-10. Connections for Unused Pins

| SIGNAL NAME | ACCEPTABLE PRACTICE |
|--|--|
| ANALOG | |
| VREFHI | Tie to VDDA (applies only if ADC is not used in the application) |
| VREFLO | Tie to VSSA |
| Analog input pins with DACx_OUT | <ul style="list-style-type: none"> No Connect Tie to VSSA through 4.7-kΩ or larger resistor |
| Analog input pins (except DACx_OUT) | <ul style="list-style-type: none"> No Connect Tie to VSSA Tie to VSSA through resistor |
| Analog input pins (shared with GPIOs) ⁽¹⁾ | <ul style="list-style-type: none"> No connection (digital input mode with internal pullup enabled) No connection (digital output mode with internal pullup disabled) Pullup or pulldown resistor (any value resistor, digital input mode, and with internal pullup disabled) |
| DIGITAL | |
| GPIOx | <ul style="list-style-type: none"> No connection (input mode with internal pullup enabled) No connection (output mode with internal pullup disabled) Pullup or pulldown resistor (any value resistor, input mode, and with internal pullup disabled) |
| GPIO35/TDI | When TDI mux option is selected (default), the GPIO is in Input mode. <ul style="list-style-type: none"> Internal pullup enabled External pullup resistor |
| GPIO37/TDO | When TDO mux option is selected (default), the GPIO is in Output mode only during JTAG activity; otherwise, it is in a tri-state condition. The pin must be biased to avoid extra current on the input buffer. <ul style="list-style-type: none"> Internal pullup enabled External pullup resistor |
| TCK | <ul style="list-style-type: none"> No Connect Pullup resistor |
| TMS | Pullup resistor |
| GPIO19/X1 | Turn XTAL off and: <ul style="list-style-type: none"> Input mode with internal pullup enabled Input mode with external pullup or pulldown resistor Output mode with internal pullup disabled |
| GPIO18/X2 | Turn XTAL off and: <ul style="list-style-type: none"> Input mode with internal pullup enabled Input mode with external pullup or pulldown resistor Output mode with internal pullup disabled |
| POWER AND GROUND | |
| VDD | All VDD pins must be connected per Section 5.3 . Pins should not be used to bias any external circuits. |
| VDDA | If a dedicated analog supply is not used, tie to VDDIO. |
| VDDIO | All VDDIO pins must be connected per Section 5.3 . |
| VSS | All VSS pins must be connected to board ground. |

Table 5-10. Connections for Unused Pins (continued)

| SIGNAL NAME | ACCEPTABLE PRACTICE |
|-------------|--|
| VSSA | If an analog ground is not used, tie to VSS. |

- (1) AGPIO pins share analog and digital functionality. The actions here only apply if these pins are also not being used for analog functions.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾ ⁽²⁾

| | | MIN | MAX | UNIT |
|------------------------------------|---|------|-----|------|
| Supply voltage | VDDIO with respect to VSS | -0.3 | 4.6 | V |
| | VDDA with respect to VSSA | -0.3 | 4.6 | |
| | VDD with respect to VSS | -0.3 | 1.5 | |
| Input voltage | V _{IN} (3.3 V) | -0.3 | 4.6 | V |
| Output voltage | V _O | -0.3 | 4.6 | V |
| Input clamp current | Digital/analog input (per pin), I _{IK} (V _{IN} < VSS/VSSA or V _{IN} > VDDIO/VDDA) ⁽⁴⁾ | -20 | 20 | mA |
| | Total for all inputs, I _{IKTOTAL} (V _{IN} < VSS/VSSA or V _{IN} > VDDIO/VDDA) | -20 | 20 | |
| Output current | Digital output (per pin), I _{OUT} | -20 | 20 | mA |
| Free-Air temperature | T _A | -40 | 125 | °C |
| Operating junction temperature | T _J | -40 | 150 | °C |
| Storage temperature ⁽³⁾ | T _{stg} | -65 | 150 | °C |

- Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- All voltage values are with respect to VSS, unless otherwise noted.
- Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life. For additional information, see the [Semiconductor and IC Package Thermal Metrics Application Report](#).
- Continuous clamp current per pin is ±2 mA. Do not operate in this condition continuously as V_{DDIO}/V_{DDA} voltage may internally rise and impact other electrical specifications.

6.2 ESD Ratings – Commercial

| | | | VALUE | UNIT | |
|--|-------------------------------|---|---|------|------|
| F280039C, F280039, F280037C, F280037, F280034, F280033 in 100-pin PZ package | | | | | |
| V _(ESD) | Electrostatic discharge (ESD) | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 | V | |
| | | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾ | All pins | | ±500 |
| | | | Corner pins on 100-pin PZ: 1, 25, 26, 50, 51, 75, 76, 100 | | ±750 |
| F280039C, F280039, F280037C, F280037, F280034, F280033 in 80-pin PN package | | | | | |
| V _(ESD) | Electrostatic discharge (ESD) | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 | V | |
| | | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾ | All pins | | ±500 |
| | | | Corner pins on 80-pin PN: 1, 20, 21, 40, 41, 60, 61, 80 | | ±750 |
| F280039C, F280039, F280037C, F280037, F280034, F280033 in 64-pin PM package | | | | | |
| V _(ESD) | Electrostatic discharge (ESD) | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 | V | |
| | | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾ | All pins | | ±500 |
| | | | Corner pins on 64-pin PM: 1, 16, 17, 32, 33, 48, 49, 64 | | ±750 |
| F280037C, F280037, F280034, F280033 in 48-pin PT package | | | | | |
| V _(ESD) | Electrostatic discharge (ESD) | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 | V | |
| | | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾ | All pins | | ±500 |
| | | | Corner pins on 48-pin PT: 1, 12, 13, 24, 25, 36, 37, 48 | | ±750 |

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings – Automotive

| | | | VALUE | UNIT | |
|---|-------------------------|---|--|-------|---|
| F280039C-Q1, F280039-Q1, F280037C-Q1, F280037-Q1 in 100-pin PZ package | | | | | |
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 ⁽¹⁾ | All pins | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 | All pins | ±500 | |
| | | | Corner pins on 100-pin PZ: 1, 25, 26, 50, 51, 75, 76, 100 | ±750 | |
| F280039C-Q1, F280039-Q1, F280037C-Q1, F280034-Q1, F280033-Q1 in 80-pin PN package | | | | | |
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 ⁽¹⁾ | All pins | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 | All pins | ±500 | |
| | | | Corner pins on 80-pin PN: 1, 20, 21, 40, 41, 60, 61, 80 | ±750 | |
| F280038C-Q1, F280038-Q1, F280036C-Q1, F280036-Q1 in 64-pin PM package | | | | | |
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 ⁽¹⁾ | All pins | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 | All pins | ±500 | |
| | | | Corner pins on 64-pin PM: 1, 16, 17, 32, 33, 48, 49, 64 | ±750 | |
| F280037C-Q1, F280037-Q1, F280034-Q1 in 48-pin PT package | | | | | |
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 ⁽¹⁾ | All pins | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 | All pins | ±500 | |
| | | | Corner pins on 48-pin PT: 1, 12, 13, 24, 25, 36, 37, 48 | ±750 | |

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.4 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT | |
|---|-------------------------------------|---|-----|-------------|------|---|
| Device supply voltage, VDDIO and VDDA | Internal BOR enabled ⁽³⁾ | V _{BOR-VDDIO} (MAX) + V _{BOR-VDDIO-GB} ⁽²⁾ | | 3.3 | 3.63 | V |
| | Internal BOR disabled | 2.8 | 3.3 | 3.63 | | |
| Device supply voltage, VDD | | 1.14 | 1.2 | 1.32 | V | |
| Device ground, VSS | | | 0 | | V | |
| Analog ground, VSSA | | | 0 | | V | |
| SR _{SUPPLY} | Supply ramp rate ⁽⁴⁾ | | | | | |
| V _{IN} | Digital input voltage | VSS – 0.3 | | VDDIO + 0.3 | | V |
| | Analog input voltage | VSSA – 0.3 | | VDDA + 0.3 | | V |
| Junction temperature, T _J ⁽¹⁾ | | –40 | | 150 | °C | |
| Free-Air temperature, T _A | | –40 | | 125 | °C | |

(1) Operation above T_J = 105°C for extended duration will reduce the lifetime of the device. See [Calculating Useful Lifetimes of Embedded Processors](#) for more information.

(2) See the *Power Management Module (PMM)* section.

(3) Internal BOR is enabled by default.

(4) See the *Power Management Module Operating Conditions* table.

6.5 Power Consumption Summary

Current values listed in this section are representative for the test conditions given and not the absolute maximum possible. The actual device currents in an application will vary with application code and pin configurations. [Section 6.5.1](#) lists the system current consumption values. [Section 6.5.2](#) lists the system current consumption with VREG disabled.

6.5.1 System Current Consumption

over operating free-air temperature range (unless otherwise noted).

TYP : V_{nom} , 30°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|---|--|-----|------|------|------|
| OPERATING MODE | | | | | | |
| I_{DDIO} | VDDIO current consumption during operational usage | This is an estimation of current for a typical heavily loaded application. Actual currents will vary depending on system activity, I/O electrical loading and switching frequency. This includes Core supply current with Internal Vreg Enabled. - CPU is running from RAM - Flash is powered up - X1/X2 crystal is powered up - PLL is enabled, SYSCLK=Max Device frequency - Analog modules are powered up - Outputs are static without DC Load - Inputs are static high or low | | 80 | 108 | mA |
| I_{DDA} | VDDA current consumption during operational usage | | | 8 | 17.5 | mA |
| IDLE MODE | | | | | | |
| I_{DDIO} | VDDIO current consumption while device is in Idle mode | - CPU is in IDLE mode - Flash is powered down | | 30 | 58 | mA |
| I_{DDA} | VDDA current consumption while device is in Idle mode | - PLL is Enabled, SYSCLK=Max Device Frequency, CPUCLK is gated - X1/X2 crystal is powered up - Analog Modules are powered down - Outputs are static without DC Load - Inputs are static high or low | | 0.01 | 0.1 | mA |
| STANDBY MODE | | | | | | |
| I_{DDIO} | VDDIO current consumption while device is in Standby mode | - CPU is in STANDBY mode - Flash is powered down | | 16.5 | 41 | mA |
| I_{DDA} | VDDA current consumption while device is in Standby mode | - PLL is Enabled, SYSCLK & CPUCLK are gated - X1/X2 crystal is powered down - Analog Modules are powered down - Outputs are static without DC Load - Inputs are static high or low | | 0.01 | 0.1 | mA |

6.5.1 System Current Consumption (continued)

over operating free-air temperature range (unless otherwise noted).

TYP : V_{nom} , 30°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------|---|---|-----|------|-----|------|
| HALT MODE | | | | | | |
| I_{DDIO} | VDDIO current consumption while device is in Halt mode | - CPU is in HALT mode - Flash is powered down | | 12.5 | 36 | mA |
| I_{DDA} | VDDA current consumption while device is in Halt mode | - PLL is Disabled, SYSCLK & CPUCLK are gated - X1/X2 crystal is powered down - Analog Modules are powered down - Outputs are static without DC Load - Inputs are static high or low | | 0.01 | 0.1 | mA |
| FLASH ERASE/PROGRAM | | | | | | |
| I_{DDIO} | VDDIO current consumption during Erase/Program cycle ⁽¹⁾ | - CPU is running from RAM - Flash going through continuous Program/Erase operation | | 72 | 106 | mA |
| I_{DDA} | VDDA current consumption during Erase/Program cycle | - PLL is enabled, SYSCLK at 120 MHz. - Peripheral clocks are turned OFF. - X1/X2 crystal is powered up - Analog is powered down - Outputs are static without DC Load - Inputs are static high or low | | 0.1 | 2.5 | mA |
| RESET MODE | | | | | | |
| I_{DDIO} | VDDIO current consumption while reset is active ⁽²⁾ | | | 5.8 | | mA |
| I_{DDA} | VDDA current consumption while reset is active ⁽²⁾ | | | 0.1 | | mA |

(1) Brownout events during flash programming can corrupt flash data and permanently lock the device. Programming environments using alternate power sources (such as a USB programmer) must be capable of supplying the rated current for the device and other system components with sufficient margin to avoid supply brownout conditions.

(2) This is the current consumption while reset is active, that is XRSn is low.

6.5.2 System Current Consumption - VREG Disable - External Supply

over operating free-air temperature range (unless otherwise noted).

TYP : V_{nom} , 30°C

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|-----|------|-------|------|
| OPERATING MODE | | | | | |
| I_{DD} | VDD current consumption during operational usage | | 73 | 103.5 | mA |
| I_{DDIO} | VDDIO current consumption during operational usage | | 4 | 4.7 | mA |
| I_{DDA} | VDDA current consumption during operational usage | | 8 | 17.5 | mA |
| This is an estimation of current for a typical heavily loaded application. Actual currents will vary depending on system activity, I/O electrical loading and switching frequency. - CPU is running from RAM - Flash is powered up - X1/X2 crystal is powered up - PLL is enabled, SYSCLK=Max Device frequency - Analog modules are powered up - Outputs are static without DC Load - Inputs are static high or low | | | | | |
| IDLE MODE | | | | | |
| I_{DD} | VDD current consumption while device is in Idle mode | | 25 | 48 | mA |
| I_{DDIO} | VDDIO current consumption while device is in Idle mode | | 1.7 | 2.2 | mA |
| I_{DDA} | VDDA current consumption while device is in Idle mode | | 0.01 | 0.1 | mA |
| - CPU is in IDLE mode - Flash is powered down - PLL is Enabled, SYSCLK=Max Device Frequency, CPUCLK is gated - X1/X2 crystal is powered up - Analog Modules are powered down - Outputs are static without DC Load - Inputs are static high or low | | | | | |
| STANDBY MODE | | | | | |
| I_{DD} | VDD current consumption while device is in Standby mode | | 11.6 | 35 | mA |
| I_{DDIO} | VDDIO current consumption while device is in Standby mode | | 1.7 | 2.3 | mA |
| I_{DDA} | VDDA current consumption while device is in Standby mode | | 0.01 | 0.1 | mA |
| - CPU is in STANDBY mode - Flash is powered down - PLL is Enabled, SYSCLK & CPUCLK are gated - X1/X2 crystal is powered down - Analog Modules are powered down - Outputs are static without DC Load - Inputs are static high or low | | | | | |
| HALT MODE | | | | | |
| I_{DD} | VDD current consumption while device is in Halt mode | | 8.5 | 31 | mA |
| I_{DDIO} | VDDIO current consumption while device is in Halt mode | | 0.8 | 1.2 | mA |
| I_{DDA} | VDDA current consumption while device is in Halt mode | | 0.01 | 0.1 | mA |
| - CPU is in HALT mode - Flash is powered down - PLL is Disabled, SYSCLK & CPUCLK are gated - X1/X2 crystal is powered down - Analog Modules are powered down - Outputs are static without DC Load - Inputs are static high or low | | | | | |

6.5.2 System Current Consumption - VREG Disable - External Supply (continued)

over operating free-air temperature range (unless otherwise noted).

TYP : V_{nom} , 30°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------|---|---|-----|-----|------|------|
| FLASH ERASE/PROGRAM | | | | | | |
| I_{DD} | VDD Current consumption during Erase/Program cycle ⁽¹⁾ | - CPU is running from RAM - Flash going through continuous Program/Erase operation | | 41 | 60.5 | mA |
| I_{DDIO} | VDDIO Current consumption during Erase/Program cycle ⁽¹⁾ | - PLL is enabled, SYSCLK at 120 MHz. | | 31 | 45.5 | mA |
| I_{DDA} | VDDA Current consumption during Erase/Program cycle | - Peripheral clocks are turned OFF. - X1/X2 crystal is powered up - Analog is powered down - Outputs are static without DC Load - Inputs are static high or low | | 0.1 | 2.5 | mA |
| RESET MODE | | | | | | |
| I_{DD} | VDD current consumption while reset is active ⁽²⁾ | | | 3.3 | | mA |
| I_{DDIO} | VDDIO current consumption while reset is active ⁽²⁾ | | | 2.2 | | mA |
| I_{DDA} | VDDA current consumption while reset is active ⁽²⁾ | | | 0.1 | | mA |

- (1) Brownout events during flash programming can corrupt flash data and permanently lock the device. Programming environments using alternate power sources (such as a USB programmer) must be capable of supplying the rated current for the device and other system components with sufficient margin to avoid supply brownout conditions.
- (2) This is the current consumption while reset is active, that is XRSn is low.

6.5.3 Operating Mode Test Description

Section 6.5.1 and Section 6.5.5.1 list the current consumption values for the operational mode of the device. The operational mode provides an estimation of what an application might encounter. The test condition for these measurements has the following properties:

- Code is executing from RAM.
- FLASH is read and kept in active state.
- No external components are driven by I/O pins.
- All peripherals have clocks enabled.
- The CPU is actively executing code.
- All analog peripherals are powered up. ADCs and DACs are periodically converting.

6.5.4 Current Consumption Graphs

The below graphs show a typical representation of the relationship between frequency, temperature, supply(VREG Enabled), and current consumption on the device. Actual results will vary based on the system implementation and conditions.

Figure 6-2 shows the typical operating current profile across temperature and core supply voltage. Figure 6-3 shows the typical idle current profile across temperature and core supply voltage. Figure 6-4 shows the typical standby current profile across temperature and core supply voltage. Figure 6-5 shows the typical halt current profile across temperature and core supply voltage.

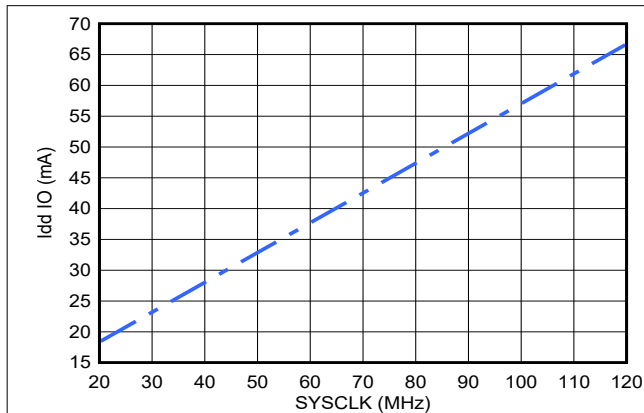


Figure 6-1. Operating Current Versus Frequency

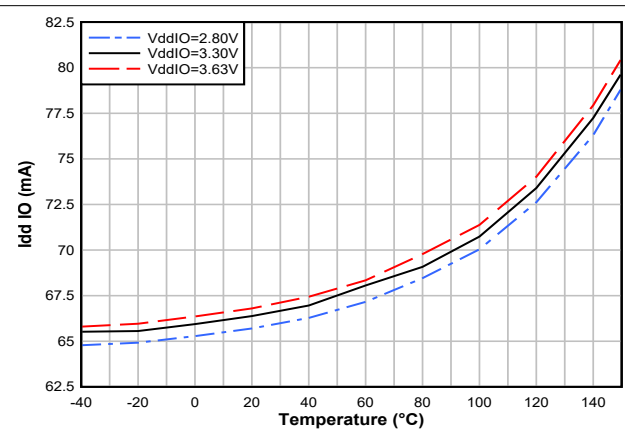


Figure 6-2. Operating Current Versus Temperature

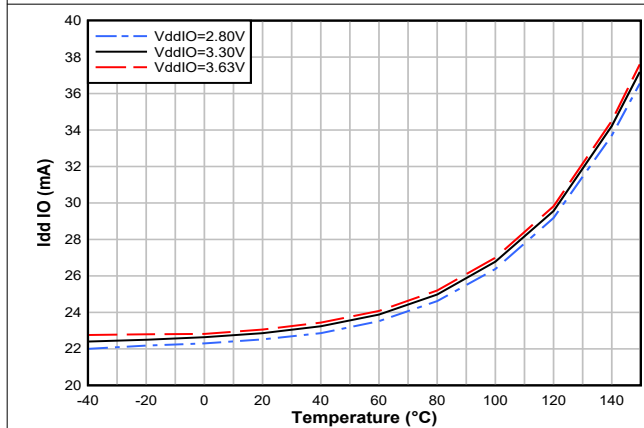


Figure 6-3. Current Versus Temperature – IDLE Mode

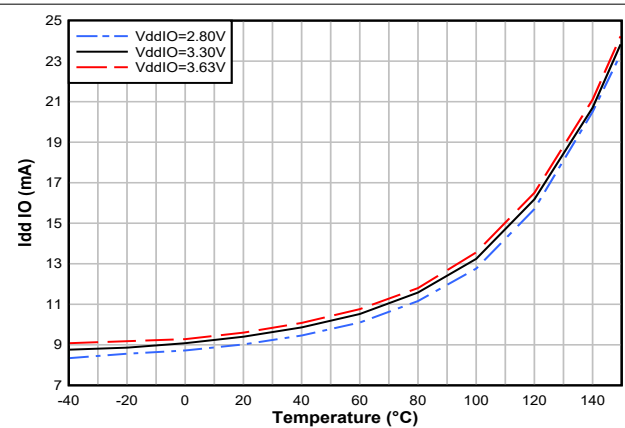


Figure 6-4. Current Versus Temperature – STANDBY Mode

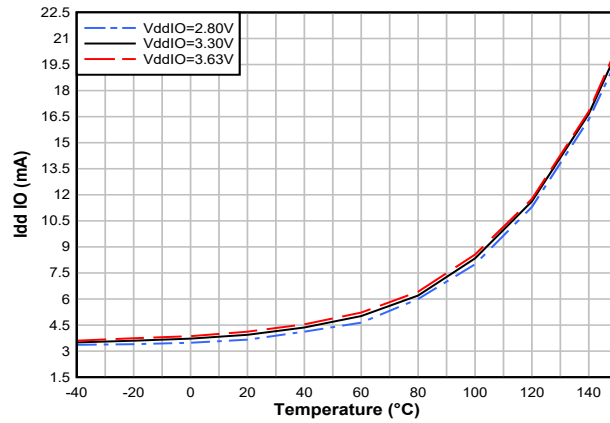


Figure 6-5. Current Versus Temperature – HALT Mode

6.5.5 Reducing Current Consumption

The F28003x devices provide some methods to reduce the device current consumption:

- One of the two low-power modes—IDLE or STANDBY—could be entered during idle periods in the application.
- The flash module may be powered down if the code is run from RAM.
- Disable the pullups on pins that assume an output function.
- Each peripheral has an individual clock-enable bit (PCLKCRx). Reduced current consumption may be achieved by turning off the clock to any peripheral that is not used in a given application. [Section 6.5.5.1](#) lists the typical current reduction that may be achieved by disabling the clocks using the PCLKCRx register.
- To realize the lowest VDDA current consumption in an LPM, see the Analog-to-Digital Converter (ADC) chapter of the [TMS320F28003x Real-Time Microcontrollers Technical Reference Manual](#) to ensure each module is powered down as well.

6.5.5.1 Typical Current Reduction per Disabled Peripheral

| PERIPHERAL | I _{DD} CURRENT REDUCTION (mA) |
|-------------------------------|--|
| ADC ⁽¹⁾ | 0.73 |
| CLA | 0.56 |
| CLA BGCRC | 0.42 |
| CLB | 1.41 |
| CMPSS ⁽¹⁾ | 0.33 |
| CPU BGCRC | 0.25 |
| CPU TIMER | 0.04 |
| GPDAC | 0.12 |
| DCAN | 1.28 |
| DCC | 0.12 |
| DMA | 0.57 |
| eCAP1 and eCAP2 | 0.08 |
| eCAP3 ⁽²⁾ | 0.29 |
| ePWM1 to ePWM4 ⁽³⁾ | 0.95 |
| ePWM5 to ePWM8 | 0.78 |
| ERAD | 1.56 |
| eQEP | 0.1 |
| FSI RX | 0.34 |
| FSI TX | 0.27 |
| HIC | 0.17 |
| I2C | 0.26 |
| LIN | 0.35 |
| MCAN (CAN FD) | 1.01 |
| PMBUS | 0.28 |
| SCI | 0.16 |
| SDFM | 1.83 |
| SPI | 0.08 |

(1) This current represents the current drawn by the digital portion of the each module.

(2) eCAP3 can also be configured as HRCAP.

(3) ePWM1 to ePWM4 can also be configured as HRPWM.

6.6 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------|--|---|---|-----|------------|------|
| Digital and Analog IO | | | | | | |
| V _{OH} | High-level output voltage | I _{OH} = I _{OH} MIN | VDDIO * 0.8 | | | V |
| | | I _{OH} = -100 µA | VDDIO - 0.2 | | | |
| V _{OL} | Low-level output voltage | I _{OL} = I _{OL} MAX | | | 0.4 | V |
| | | I _{OL} = 100 µA | | | 0.2 | |
| I _{OH} | High-level output source current for all output pins | | -4 | | | mA |
| I _{OL} | Low-level output sink current for all output pins | | | | 4 | mA |
| R _{OH} | High-level output impedance for all output pins | V _{OH} =VDDIO-0.4V | 50 | 66 | 96 | Ω |
| R _{OL} | Low-level output impedance for all output pins | V _{OL} =0.4V | 48 | 60 | 84 | Ω |
| V _{IH} | High-level input voltage | | 2.0 | | | V |
| V _{IL} | Low-level input voltage | | | | 0.8 | V |
| V _{HYSTERESIS} | Input hysteresis | | 125 | | | mV |
| I _{PULLDOWN} | Input current | Pins with pulldown | VDDIO = 3.3 V V _{IN} = VDDIO | | 120 | µA |
| I _{PULLUP} | Input current | Digital inputs with pullup enabled ⁽¹⁾ | VDDIO = 3.3 V V _{IN} = 0 V | | 160 | µA |
| R _{PULLDOWN} | Weak pulldown resistance | | 22 | 31 | 62 | kΩ |
| R _{PULLUP} | Weak pullup resistance | | 19 | 30 | 54 | kΩ |
| I _{LEAK} | Pin leakage | Digital inputs | Pullups and outputs disabled 0 V ≤ V _{IN} ≤ VDDIO | | 0.1 | µA |
| | | Analog pins (except ADCINB3/VDAC) | Analog drivers disabled | | 0.1 | |
| | | ADCINB3/VDAC | 0 V ≤ V _{IN} ≤ VDDA | | 0.2 4.4 | |
| C _I | Input capacitance | Digital inputs | | | 2 | pF |
| | | Analog pins ⁽²⁾ | | | | |
| VREG, POR and BOR | | | | | | |
| VREG, POR, BOR ⁽³⁾ | | | | | | |

(1) See [Pins With Internal Pullup and Pulldown](#) table for a list of pins with a pullup or pulldown.

(2) The analog pins are specified separately; see the Per-Channel Parasitic Capacitance tables that are in the ADC Input Model section.

(3) See the [Power Management Module \(PMM\)](#) section.

6.7 Thermal Resistance Characteristics for PZ Package

| | | °C/W ⁽¹⁾ | AIR FLOW (lfm) ⁽²⁾ |
|-------------------------------|---|---------------------|-------------------------------|
| RO _{JC} | Junction-to-case thermal resistance | 7.6 | N/A |
| RO _{JB} | Junction-to-board thermal resistance | 24.2 | N/A |
| RO _{JA} (High k PCB) | Junction-to-free air thermal resistance | 46.1 | 0 |
| RO _{JMA} | Junction-to-moving air thermal resistance | 37.3 | 150 |
| | | 34.8 | 250 |
| | | 32.6 | 500 |
| Psi _{JT} | Junction-to-package top | 0.2 | 0 |
| | | 0.4 | 150 |
| | | 0.4 | 250 |
| | | 0.6 | 500 |
| Psi _{JB} | Junction-to-board | 23.8 | 0 |
| | | 22.8 | 150 |
| | | 22.4 | 250 |
| | | 21.9 | 500 |

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [RO_{JC}] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(2) lfm = linear feet per minute

6.8 Thermal Resistance Characteristics for PN Package

| | | °C/W ⁽¹⁾ | AIR FLOW (lfm) ⁽²⁾ |
|------------------------------|---|---------------------|-------------------------------|
| R θ_{JC} | Junction-to-case thermal resistance | 14.2 | N/A |
| R θ_{JB} | Junction-to-board thermal resistance | 21.9 | N/A |
| R θ_{JA} (High k PCB) | Junction-to-free air thermal resistance | 49.9 | 0 |
| | | 38.3 | 150 |
| | | 36.7 | 250 |
| | | 34.4 | 500 |
| Psi $_{JT}$ | Junction-to-package top | 0.8 | 0 |
| | | 1.18 | 150 |
| | | 1.34 | 250 |
| | | 1.62 | 500 |
| Psi $_{JB}$ | Junction-to-board | 21.6 | 0 |
| | | 20.7 | 150 |
| | | 20.5 | 250 |
| | | 20.1 | 500 |

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [R θ_{JC}] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(2) lfm = linear feet per minute

6.9 Thermal Resistance Characteristics for PM Package

| | | °C/W ⁽¹⁾ | AIR FLOW (lfm) ⁽²⁾ |
|-------------------------------|---|---------------------|-------------------------------|
| RO _{JC} | Junction-to-case thermal resistance | 12.4 | N/A |
| RO _{JB} | Junction-to-board thermal resistance | 25.6 | N/A |
| RO _{JA} (High k PCB) | Junction-to-free air thermal resistance | 51.8 | 0 |
| RO _{JMA} | Junction-to-moving air thermal resistance | 42.2 | 150 |
| | | 39.4 | 250 |
| | | 36.5 | 500 |
| Psi _{JT} | Junction-to-package top | 0.5 | 0 |
| | | 0.9 | 150 |
| | | 1.1 | 250 |
| | | 1.4 | 500 |
| Psi _{JB} | Junction-to-board | 25.1 | 0 |
| | | 23.8 | 150 |
| | | 23.4 | 250 |
| | | 22.7 | 500 |

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [RO_{JC}] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(2) lfm = linear feet per minute

6.10 Thermal Resistance Characteristics for PT Package

| | | °C/W ⁽¹⁾ | AIR FLOW (lfm) ⁽²⁾ |
|-------------------------------|---|---------------------|-------------------------------|
| RO _{JC} | Junction-to-case thermal resistance | 16.2 | N/A |
| RO _{JB} | Junction-to-board thermal resistance | 22.3 | N/A |
| RO _{JA} (High k PCB) | Junction-to-free air thermal resistance | 56.7 | 0 |
| | | 50.4 | 150 |
| | | 48.2 | 250 |
| | | 45 | 500 |
| Psi _{JT} | Junction-to-package top | 0.7 | 0 |
| | | 0.94 | 150 |
| | | 1.1 | 250 |
| | | 1.38 | 500 |
| Psi _{JB} | Junction-to-board | 22 | 0 |
| | | 28.7 | 150 |
| | | 28.4 | 250 |
| | | 28 | 500 |

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [RO_{JC}] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(2) lfm = linear feet per minute

6.11 Thermal Design Considerations

Based on the end application design and operational profile, the I_{DD} and I_{DDIO} currents could vary. Systems that exceed the recommended maximum power dissipation in the end product may require additional thermal enhancements. Ambient temperature (T_A) varies with the end application and product design. The critical factor that affects reliability and functionality is T_J, the junction temperature, not the ambient temperature. Hence, care should be taken to keep T_J within the specified limits. T_{case} should be measured to estimate the operating junction temperature T_J. T_{case} is normally measured at the center of the package top-side surface. The thermal application report [Semiconductor and IC Package Thermal Metrics](#) helps to understand the thermal metrics and definitions.

6.12 System

6.12.1 Power Management Module (PMM)

6.12.1.1 Introduction

The Power Management Module (PMM) handles all the power management functions required for device operation.

6.12.1.2 Overview

The block diagram of the PMM is shown in Figure 6-6. As can be seen, the PMM comprises of various subcomponents, which are described in the subsequent sections.

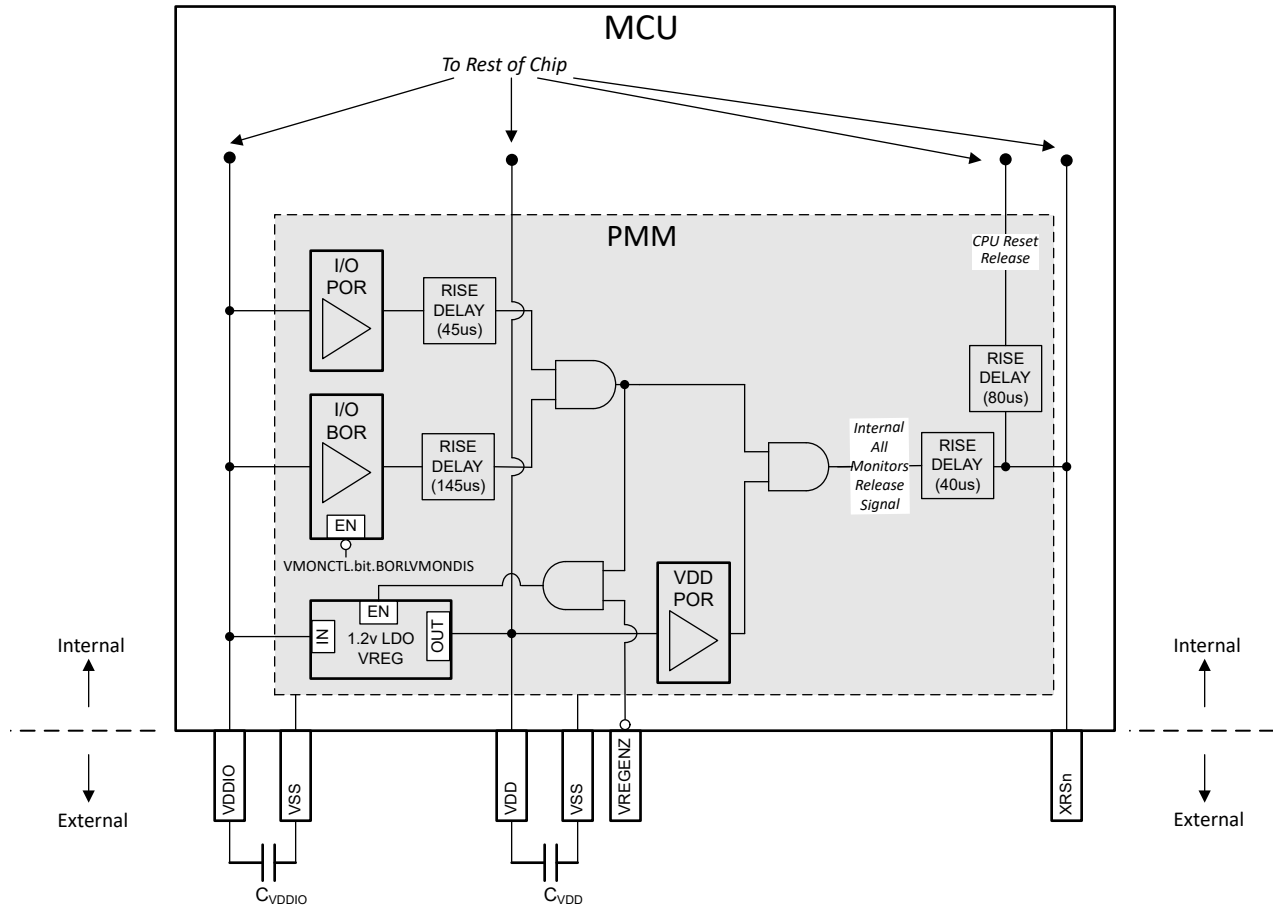


Figure 6-6. PMM Block Diagram

6.12.1.2.1 Power Rail Monitors

The PMM has voltage monitors on the supply rails that release the XRSn signal high once the voltages cross the set threshold during power up. They also function to trip the XRSn signal low if any of the voltages drop below the programmed levels. The various voltage monitors are described in subsequent sections.

Note

Not all the voltage monitors are supported for device operation in an application after boot up. In the case where a voltage monitor is not supported, an external supervisor is recommended if the device needs supply voltage monitoring while the application is running.

The three voltage monitors (I/O POR, I/O BOR, VDD POR) all have to release their respective outputs before the device begins operation (that is, XRSn goes high). However, if any of the voltage monitors trips, XRSn is driven low. The I/Os are held in high impedance when any of the voltage monitors trip.

6.12.1.2.1.1 I/O POR (Power-On Reset) Monitor

The I/O POR monitor supervises the VDDIO rail. During power up, this is the first monitor to release (that is, first to untrip) on VDDIO.

6.12.1.2.1.2 I/O BOR (Brown-Out Reset) Monitor

The I/O BOR monitor also supervises the VDDIO rail. During power up, this is the second monitor to release (that is, second to untrip) on VDDIO. This monitor has a tighter tolerance compared to the I/O POR.

Any drop in voltage below the recommended operating voltages will trip the I/O BOR and reset the device but this can be disabled by setting VMONCTL.bit.BORLVMONDIS to 1. The I/O BOR can only be disabled after the device has fully booted up. If the I/O BOR is disabled, the I/O POR will reset the device for voltage drops.

Note

The level at which the I/O POR trips is well below the minimum recommended voltage for VDDIO, and therefore should not be used for device supervision.

Figure 6-7 shows the operating region of the I/O BOR.

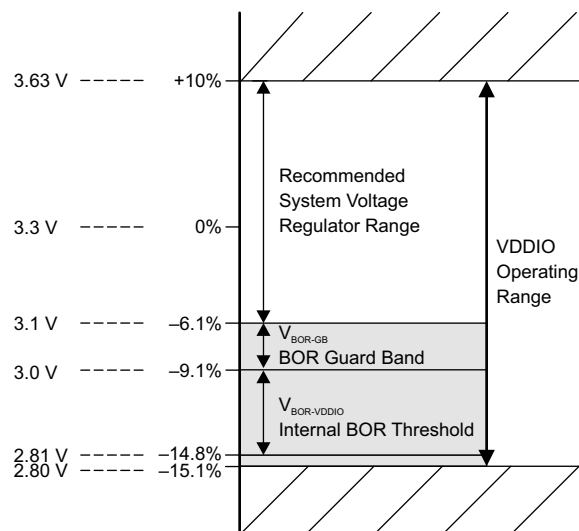


Figure 6-7. I/O BOR Operating Region

6.12.1.2.1.3 VDD POR (Power-On Reset) Monitor

The VDD POR monitor supervises the VDD rail. During power up, this monitor releases (that is, untrips) once the voltage crosses the programmed trip level on VDD.

Note

VDD POR is programmed at a level below the minimum recommended voltage for VDD, and therefore it should not be relied upon for VDD supervision if that is required in the application.

6.12.1.2.2 External Supervisor Usage

VDDIO Monitoring: The I/O BOR is supported for application use, so an external supervisor is not required to monitor the I/O rail.

VDD Monitoring:

- VDD supplied from the internal VREG: The VDD supply is derived from the VDDIO supply. The VREG is designed in such a way that a valid VDDIO supply(monitored by the IO BOR) implies a valid VDD supply.
- VDD supplied from an external supply: The VDD POR is not supported for application use. If VDD monitoring is required by the application, an external supervisor can be used to monitor the VDD rail.

Note

The use of an external supervisor with the internal VREG is not supported.If VDD monitoring is required by the application, a package with a VREGENZ pin must be used to power VDD externally.

6.12.1.2.3 Delay Blocks

The delay blocks in the path of the voltage monitors work together to delay the release time between the voltage monitors and XRSn. These delays are designed to make sure that the voltages are stable when XRSn releases in external VREG mode. The delay blocks are only active during power up (that is, when VDDIO and VDD are ramping up).

The delay blocks contribute to the minimum slew rates specified in [Power Management Module Electrical Data and Timing](#) for the power rails.

Note

The delay numbers specified in the block diagram are typical numbers.

6.12.1.2.4 Internal 1.2-V LDO Voltage Regulator (VREG)

The internal VREG is supplied by the VDDIO rail and can generate the 1.2 V required to power the VDD pins. It is enabled by tying the VREGENZ pin low. Although the internal VREG eliminates the need to use an external supply for VDD, decoupling capacitors are still required on the VDD pins for VREG stability and transients. See the *VDD Decoupling* section for details.

6.12.1.2.5 VREGENZ

The VREGENZ (VREG disable) pin controls the state of the internal VREG. To enable the internal VREG, connect the VREGENZ pin to a logic low voltage. For applications supplying VDD externally (external VREG), disable the internal VREG by tying the VREGENZ pin high.

Note

Not all device packages have VREGENZ pinned out. For packages without VREGENZ, external VREG mode is not supported.

6.12.1.3 External Components

6.12.1.3.1 Decoupling Capacitors

VDDIO and VDD require decoupling capacitors for correct operation. The requirements are outlined in subsequent sections.

6.12.1.3.1.1 VDDIO Decoupling

Place a minimum amount of decoupling capacitance on VDDIO. See the C_{VDDIO} parameter in [Power Management Module Electrical Data and Timing](#). The actual amount of decoupling capacitance to use is a requirement of the power supply driving VDDIO. Either of the configurations outlined below is acceptable:

- **Configuration 1:** Place a decoupling capacitor on each VDDIO pin per the C_{VDDIO} parameter.
- **Configuration 2:** Install a single decoupling capacitor that is the equivalent of $C_{VDDIO} * VDDIO$ pins.

Note

Having the decoupling capacitor or capacitors close to the device pins is critical.

6.12.1.3.1.2 VDD Decoupling

Place a minimum amount of decoupling capacitance on VDD. See the C_{VDD} TOTAL parameter in [Power Management Module Electrical Data and Timing](#).

In external VREG mode, the actual amount of decoupling capacitance to use is a requirement of the power supply driving VDD.

Either of the configurations outlined below is acceptable:

- **Configuration 1:** Divide C_{VDD} TOTAL across the VDD pins.
- **Configuration 2:** Install a single decoupling capacitor with value of C_{VDD} TOTAL.

Note

Having the decoupling capacitor or capacitors close to the device pins is critical.

6.12.1.4 Power Sequencing

6.12.1.4.1 Supply Pins Ganging

Connecting all 3.3-V rails together and supplying from a single source are strongly recommended. This list includes:

- VDDIO
- VDDA

In addition, connect all power pins to avoid leaving any unconnected.

In external VREG mode, the VDD pins should be tied together and supplied from a single source.

In internal VREG mode, tying the VDD pins together is optional as long as each VDD pin has a capacitor connected to pin. See the *VDD Decoupling* section for VDD decoupling configurations.

The analog modules on the device have fairly high PSRR; therefore, in most cases, noise on VDDA will have to exceed the recommended operating conditions of the supply rails before the analog modules see performance degradation. Therefore, supplying VDDA separately typically offers minimal benefits. Nevertheless, for the purposes of noise improvement, placing a pi filter between VDDIO and VDDA is acceptable.

Note

All the supply pins per rail are tied together internally. For example, all VDDIO pins are tied together internally, all VDD pins are tied together internally, and so forth.

6.12.1.4.2 Signal Pins Power Sequence

Before powering the device, do not apply voltage larger than 0.3 V above VDDIO or 0.3 V below VSS to any digital pin and 0.3 V above VDDA or 0.3 V below VSSA to any analog pin (including VREFHI and VDAC). Simply, the signal pins should only be driven after XRSn goes high, provided all the 3.3-V rails are tied together. This sequencing is still required even if VDDIO and VDDA are not tied together.

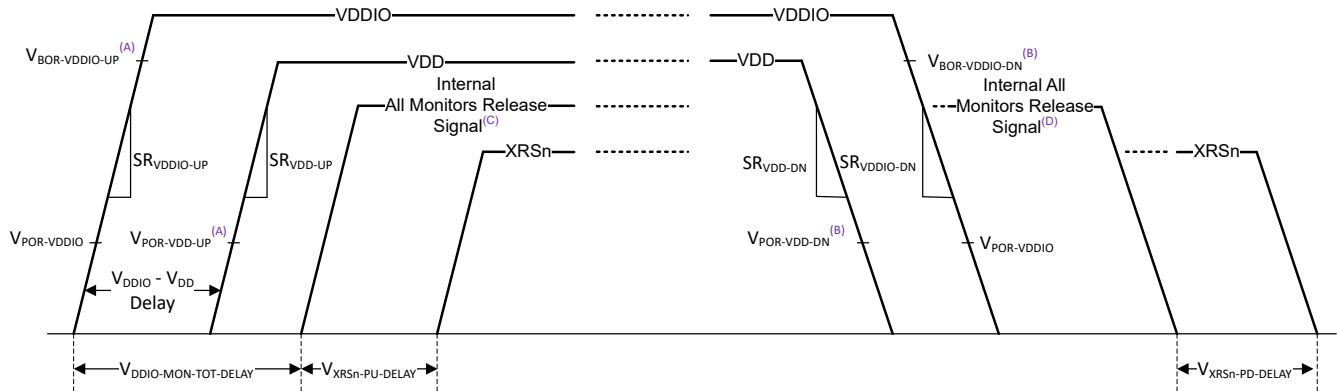
CAUTION

If the above sequence is violated, device malfunction and possibly damage can occur as current will flow through unintended parasitic paths in the device.

6.12.1.4.3 Supply Pins Power Sequence

6.12.1.4.3.1 External VREG/VDD Mode Sequence

Figure 6-8 depicts the power sequencing requirements for external VREG mode. The values for all the parameters indicated can be found in [Power Management Module Electrical Data and Timing](#).



- This trip point is the trip point before XRSn releases. See the Power Management Module Characteristics table.
- This trip point is the trip point after XRSn releases. See the Power Management Module Characteristics table.
- During power up, the All Monitors Release Signal goes high after all POR and BOR monitors are released. See the PMM Block Diagram.
- During power down, the All Monitors Release Signal goes low if any of the POR or BOR monitors are tripped. See the PMM Block Diagram.

Figure 6-8. External VREG Power Up Sequence

For Power Up:

- VDDIO (that is, the 3.3-V rail) should come up first with the minimum slew rate specified.
- VDD (that is, the 1.2-V rail) should come up next with the minimum slew rate specified.
- The time delta between the VDDIO rail coming up and when the VDD rail can come up is also specified.
- After the times specified by $V_{DDIO-MON-TOT-DELAY}$ and $V_{XRSN-PD-DELAY}$, XRSn will be released and the device starts the boot-up sequence.

There is an additional delay between XRSn releasing (that is, going high) and the boot-up sequence starting. See [Figure 6-6](#).

- The I/O BOR monitor has different release points during power up and power down.
- During power up, both VDDIO and VDD rails have to be up before XRSn releases.

For Power Down:

- There is no requirement between VDDIO and VDD on which should power down first; however, there is a minimum slew rate specification.
- The I/O BOR monitor has different release points during power up and power down.
- Any of the POR or BOR monitors that trips during power down will cause XRSn to go low after $V_{XRSN-PD-DELAY}$.

Note

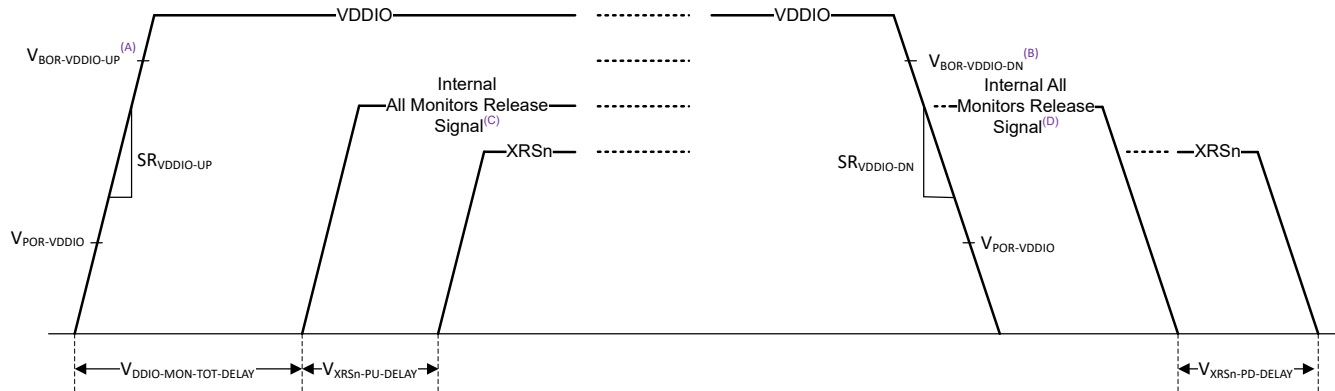
The *All Monitors Release Signal* is an internal signal.

Note

If there is an external circuit driving XRSn (for example, a supervisor), the boot-up sequence does not start until the XRSn pin is released by all internal and external sources.

6.12.1.4.3.2 Internal VREG/VDD Mode Sequence

[Figure 6-9](#) depicts the power sequencing requirements for internal VREG mode. The values for all the parameters indicated can be found in [Power Management Module Electrical Data and Timing](#).



- A. This trip point is the trip point before XRSn releases. See the Power Management Module Characteristics table.
- B. This trip point is the trip point after XRSn releases. See the Power Management Module Characteristics table.
- C. During power up, the All Monitors Release Signal goes high after all POR and BOR monitors are released. See the PMM Block Diagram.
- D. During power down, the All Monitors Release Signal goes low if any of the POR or BOR monitors are tripped. See the PMM Block Diagram.

Figure 6-9. Internal VREG Power Up Sequence

For Power Up:

- VDDIO (that is, the 3.3-V rail) should come up with the minimum slew rate specified.
- The Internal VREG powers up after the I/O monitors (I/O POR and I/O BOR) are released.
- After the times specified by $V_{DDIO-MON-TOT-DELAY}$ and $V_{XRSn-PU-DELAY}$, XRSn will be released and the device starts the boot-up sequence.

There is an additional delay between XRSn releasing (that is, going high) and the boot-up sequence starting. See [Figure 6-6](#).

- The I/O BOR monitor has different release points during power up and power down.

For Power Down:

- The only requirement on VDDIO during power down is the slew rate.
- The I/O BOR monitor has different release points during power up and power down.
- The I/O BOR tripping will cause XRSn to go low after $V_{XRSn-PD-DELAY}$ and also power down the Internal VREG.

Note

The *All Monitors Release Signal* is an internal signal.

Note

If there is an external circuit driving XRSn (for example, a supervisor), the boot-up sequence does not start until the XRSn pin is released by all internal and external sources.

6.12.1.4.3.3 Supply Sequencing Summary and Effects of Violations

The acceptable power-up sequence for the rails is summarized below. "Power up" here means the rail in question has reached the minimum recommended operating voltage.

CAUTION
Non-acceptable sequences leads to reliability concerns and possibly damage.

For simplicity, connecting all 3.3-V rails together and following the descriptions in [Supply Pins Power Sequence](#) is recommended.

Table 6-1. External VREG Sequence Summary

| CASE | RAILS POWER-UP ORDER | | | ACCEPTABLE |
|------|----------------------|------|-----|------------|
| | VDDIO | VDDA | VDD | |
| A | 1 | 2 | 3 | Yes |
| B | 1 | 3 | 2 | Yes |
| C | 2 | 1 | 3 | - |
| D | 2 | 3 | 1 | - |
| E | 3 | 2 | 1 | - |
| F | 3 | 1 | 2 | - |
| G | 1 | 1 | 2 | Yes |
| H | 2 | 2 | 1 | - |

Table 6-2. Internal VREG Sequence Summary

| CASE | RAILS POWER-UP ORDER | | ACCEPTABLE |
|------|----------------------|------|------------|
| | VDDIO | VDDA | |
| A | 1 | 2 | Yes |
| B | 2 | 1 | - |
| C | 1 | 1 | Yes |

Note

The analog modules on the device should only be powered after VDDA has reached the minimum recommended operating voltage.

6.12.1.4.3.4 Supply Slew Rate

VDDIO has a minimum slew rate requirement. If the minimum slew rate is not met, XRSn might toggle a few times until VDDIO crosses the I/O BOR region.

Note

The toggling on XRSn has no adverse effect on the device as boot only starts once XRSn is steadily high. However if XRSn from the device is used to gate the reset signal of other ICs, then the slew rate requirement should be met to prevent this toggling.

VDD has a minimum slew rate requirement in external VREG mode. If the minimum slew rate is not met, the VDD POR may release before the VDD operational minimum voltage is met and the device may not start in a properly reset state.

6.12.1.5 Power Management Module Electrical Data and Timing

6.12.1.5.1 Power Management Module Operating Conditions

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|-----------------|-----|-----|-----------------|-------------------|
| General | | | | | | |
| C_{VDDIO} (1) (2) | VDDIO Capacitance Per Pin ⁽⁷⁾ | | 0.1 | | | μF |
| C_{VDDA} (1) (2) | VDDA Capacitance Per Pin ⁽⁷⁾ | | 2.2 | | | μF |
| $SR_{VDDIO-UP}$ (3) | Supply Ramp Up Rate of 3.3V Rail (VDDIO) | | 8 | | 100 | mV/ μs |
| $SR_{VDDIO-DN}$ (3) | Supply Ramp Down Rate of 3.3V Rail (VDDIO) | | 20 | | 100 | mV/ μs |
| $V_{BOR-VDDIO-GB}$ (5) | VDDIO Brown Out Reset Voltage Guardband | | | 0.1 | | V |
| External VREG | | | | | | |
| C_{VDD} TOTAL (1) (4) | Total VDD Capacitance ⁽⁷⁾ | | 10 | | | μF |
| SR_{VDD-UP} (3) | Supply Ramp Up Rate of 1.2V Rail (VDD) | | 3.5 | | 100 | mV/ μs |
| SR_{VDD-DN} (3) | Supply Ramp Down Rate of 1.2V Rail (VDD) | | 10 | | 100 | mV/ μs |
| $V_{DDIO} - V_{DD}$ Delay ⁽⁶⁾ | Ramp Delay Between VDDIO and VDD | | 0 | | No Restrictions | μs |
| Internal VREG | | | | | | |
| C_{VDD} TOTAL (4) | Total VDD Capacitance ⁽⁷⁾ | | 10 | | 26.8 | μF |

- (1) The exact value of the decoupling capacitance depends on the system voltage regulation solution that is supplying these pins.
- (2) It is recommended to tie the 3.3V rails (VDDIO, VDDA) together and supply them from a single source.
- (3) See the *Supply Slew Rate* section. Supply ramp rate faster than the maximum can trigger the on-chip ESD protection.
- (4) See the *Power Management Module (PMM)* section on possible configurations for the total decoupling capacitance.
- (5) TI recommends $V_{BOR-VDDIO-GB}$ to avoid BOR-VDDIO resets due to normal supply noise or load-transient events on the 3.3-V VDDIO system regulator. Good system regulator design and decoupling capacitance (following the system regulator specifications) are important to prevent activation of the BOR-VDDIO during normal device operation. The value of $V_{BOR-VDDIO-GB}$ is a system-level design consideration; the voltage listed here is typical for many applications.
- (6) Delay between when the 3.3-V rail ramps up and when the 1.2-V rail ramps up. See the *VREG Sequence Summary* table for the allowable supply ramp sequences.
- (7) Max capacitor tolerance should be 20%.

6.12.1.5.2 Power Management Module Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|--|-------------------------------|------|-----|------|---------------|
| V_{VREG} | Internal Voltage Regulator Output | | 1.14 | 1.2 | 1.32 | V |
| $V_{VREG-PU}$ | Internal Voltage Regulator Power Up Time | | | | 350 | μs |
| $V_{VREG-INRUSH}$ (5) | Internal Voltage Regulator Inrush Current | | | 650 | | mA |
| $V_{POR-VDDIO}$ | VDDIO Power on Reset Voltage | Before and After XRSn Release | | 2.3 | | V |
| $V_{BOR-VDDIO-UP}$ (1) | VDDIO Brown Out Reset Voltage on Ramp Up | Before XRSn Release | | 2.7 | | V |
| $V_{BOR-VDDIO-DN}$ (1) | VDDIO Brown Out Reset Voltage on Ramp Down | After XRSn Release | 2.81 | | 3.0 | V |

6.12.1.5.2 Power Management Module Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------------|--|---------------------------------|-----|-----|-----|------|
| $V_{POR-VDD-UP}$ ⁽²⁾ | VDD Power on Reset Voltage on Ramp Up | Before XRSn Release | | 1 | | V |
| $V_{POR-VDD-DN}$ ⁽²⁾ | VDD Power on Reset Voltage on Ramp Down | After XRSn Release | | 1 | | V |
| $V_{XRSn-PU-DELAY}$ ⁽³⁾ | XRSn Release Delay after Supplies are Ramped Up During Power Up | This is the final delay | | 40 | | μs |
| $V_{XRSn-PD-DELAY}$ ⁽⁴⁾ | XRSn Trip Delay after Supplies are Ramped Down During Power Down | | | 2 | | μs |
| $V_{DDIO-MON-TOT-DELAY}$ | Total Delays in Path of VDDIO Monitors (POR, BOR) | | | 145 | | μs |
| $V_{XRSn-MON-RELEASE-DELAY}$ | XRSn Release Delay after a VDD POR Event | Supplies Within Operating Range | | 40 | | μs |
| | XRSn Release Delay after a VDDIO BOR | | | 140 | | μs |
| | XRSn Release Delay after a VDDIO POR Event | | | 185 | | μs |

- (1) See the *Supply Voltages* figure.
- (2) $V_{POR-VDD}$ is not supported and it is set to trip at a level below the recommended operating conditions. If monitoring of VDD is needed, an external supervisor is required.
- (3) Supplies are considered fully ramped up after they cross the minimum recommended operating conditions for the respective rail. All POR and BOR monitors need to be released before this delay takes effect. RC network delay will add to this.
- (4) On power down, any of the POR or BOR monitors that trips will immediately trip XRSn. This delay is the time between any of the POR, BOR monitors tripping and XRSn going low. It is variable and depends on the ramp down rate of the supply. RC network delay will add to this.
- (5) This is the transient current drawn on the VDDIO rail when the internal VREG turns on. Due to this, there might be some voltage drops on the VDDIO rail when the VREG turns on which could cause the VREG to ramp up in steps. There is no detriment to the device from this but the effect can be reduced if desired by using sufficient decoupling capacitors on VDDIO or picking an LDO/DC-DC that can supply this transient current.

Supply Voltages

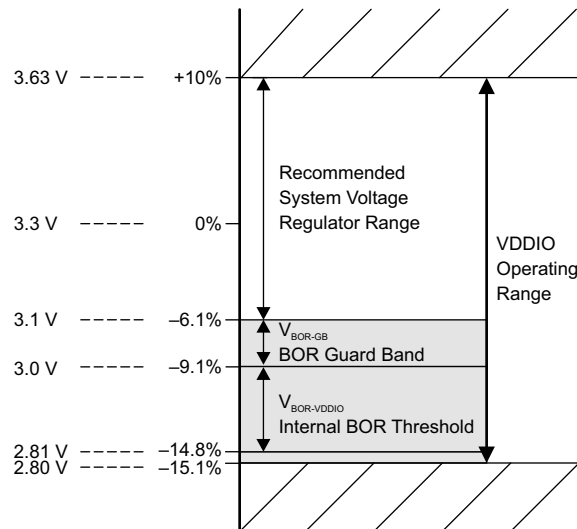


Figure 6-10. Supply Voltages

6.12.2 Reset Timing

XRSn is the device reset pin. It functions as an input and open-drain output. The device has a built-in power-on reset (POR) and brown-out reset (BOR) monitors. During power up, the monitor circuits keep the XRSn pin low. For more details, see the *Power Management Module (PMM)* section. A watchdog or NMI watchdog reset will also drive the pin low. An external open-drain circuit may drive the pin to assert a device reset.

A resistor with a value from 2.2 k Ω to 10 k Ω should be placed between XRSn and VDDIO. A capacitor should be placed between XRSn and VSS for noise filtering, it should be 100 nF or smaller. These values will allow the watchdog to properly drive the XRSn pin to V_{OL} within 512 OSCCLK cycles when the watchdog reset is asserted. Figure 6-11 shows the recommended reset circuit.

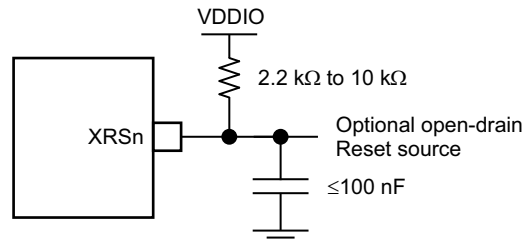


Figure 6-11. Reset Circuit

6.12.2.1 Reset Sources

The Reset Signals table summarizes the various reset signals and their effect on the device.

Table 6-3. Reset Signals

| Reset Source | CPU Core Reset (C28x, FPU, TMU) | Peripherals Reset | JTAG / Debug Logic Reset | IOs | XRS Output |
|--------------------------------------|---------------------------------|-------------------|--------------------------|------|------------|
| POR | Yes | Yes | Yes | Hi-Z | Yes |
| BOR | Yes | Yes | Yes | Hi-Z | Yes |
| XRS Pin | Yes | Yes | No | Hi-Z | - |
| WDR \overline{S} | Yes | Yes | No | Hi-Z | Yes |
| NMIWDR \overline{S} | Yes | Yes | No | Hi-Z | Yes |
| SYSR \overline{S} (Debugger Reset) | Yes | Yes | No | Hi-Z | No |
| SCCRESET | Yes | Yes | No | Hi-Z | No |
| SIMRESET. XRS | Yes | Yes | No | Hi-Z | Yes |
| SIMRESET. CPU1RS | Yes | Yes | No | Hi-Z | No |
| HWBISTR \overline{S} | Yes | No | No | No | No |

The parameter $t_{h(\text{boot-mode})}$ must account for a reset initiated from any of these sources.

See the Resets section of the System Control chapter in the [TMS320F28003x Real-Time Microcontrollers Technical Reference Manual](#).

CAUTION

Some reset sources are internally driven by the device. Some of these sources will drive XRSn low, use this to disable any other devices driving the boot pins. The SCCRESET and debugger reset sources do not drive XRSn; therefore, the pins used for boot mode should not be actively driven by other devices in the system. The boot configuration has a provision for changing the boot pins in OTP.

6.12.2.2 Reset Electrical Data and Timing

6.12.2.2.1 Reset - XRSn - Timing Requirements

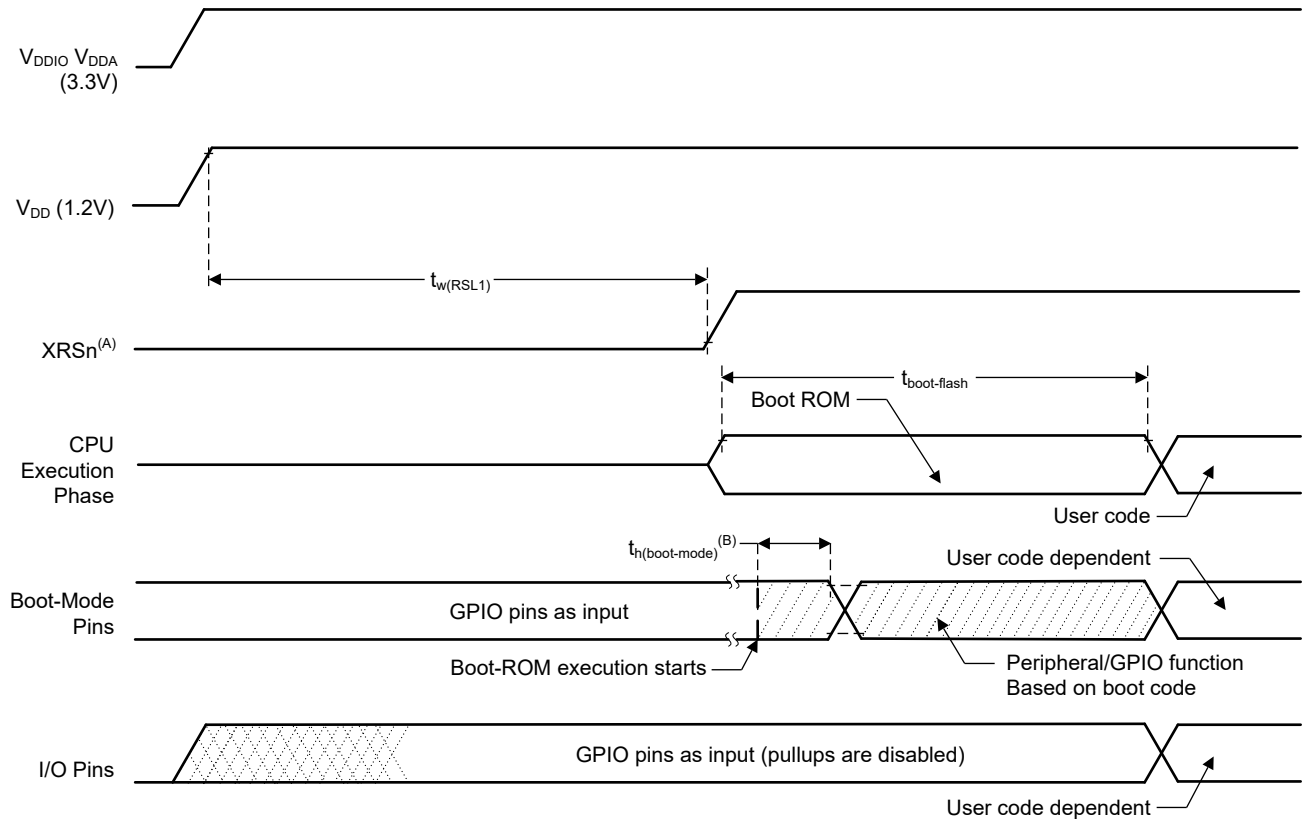
| | | MIN | MAX | UNIT |
|---------------------------|--|-----|-----|---------------|
| $t_{h(\text{boot-mode})}$ | Hold time for boot-mode pins | 1.5 | | ms |
| $t_{w(\text{RSL2})}$ | Pulse duration, XRSn low on warm reset | 3.2 | | μs |

6.12.2.2.2 Reset - XRSn - Switching Characteristics

over recommended operating conditions (unless otherwise noted)

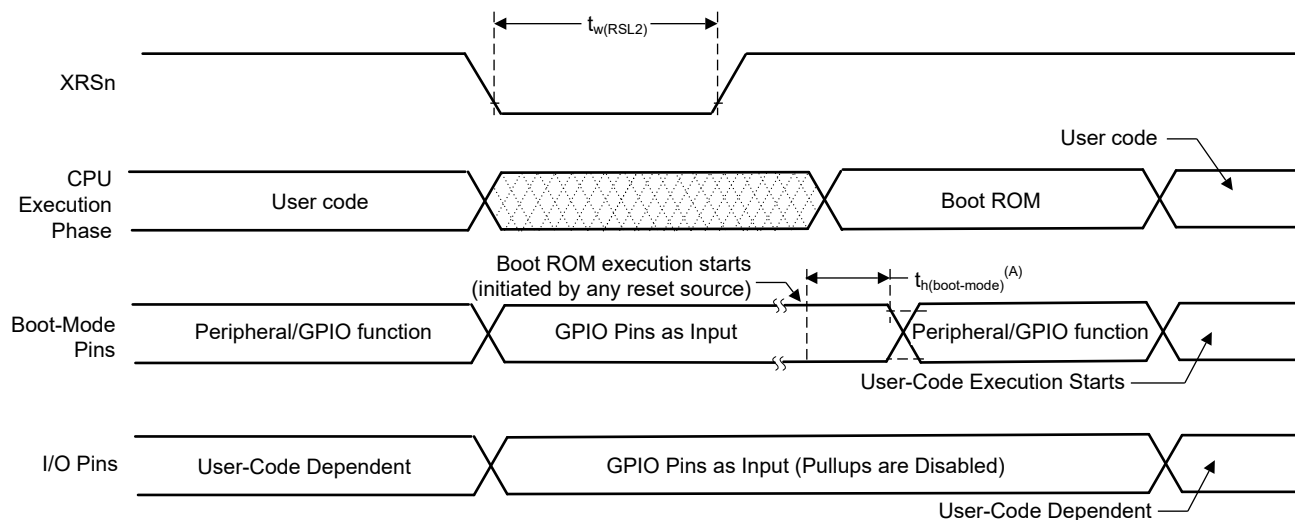
| PARAMETER | | MIN | TYP | MAX | UNIT |
|-------------------------|---|-----|-----------------------------|-----|---------------|
| $t_{w(\text{RSL1})}$ | Pulse duration, XRSn driven low by device after supplies are stable | | 100 | | μs |
| $t_{w(\text{WDRS})}$ | Pulse duration, reset pulse generated by watchdog | | $512t_{c(\text{OSCCLOCK})}$ | | cycles |
| $t_{\text{boot-flash}}$ | Boot-ROM execution time to first instruction fetch in flash | | | 1.2 | ms |

6.12.2.2.3 Reset Timing Diagrams



- A. The XRSn pin can be driven externally by a supervisor or an external pullup resistor, see the Pin Attributes table. On-chip monitors will hold this pin low until the supplies are in a valid range.
- B. After reset from any source (see the Reset Sources section), the boot ROM code samples Boot Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If boot ROM code executes after power-on conditions (in debugger environment), the boot code execution time is based on the current SYSCLK speed. The SYSCLK will be based on user environment and could be with or without PLL enabled.

Figure 6-12. Power-on Reset



- A. After reset from any source (see the Reset Sources section), the Boot ROM code samples BOOT Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If Boot ROM code executes after power-on conditions (in debugger environment), the Boot code execution time is based on the current SYSCLK speed. The SYSCLK will be based on user environment and could be with or without PLL enabled.

Figure 6-13. Warm Reset

6.12.3 Clock Specifications

6.12.3.1 Clock Sources

Table 6-4. Possible Reference Clock Sources

| CLOCK SOURCE | DESCRIPTION |
|------------------------|---|
| INTOSC1 | Internal oscillator 1. Zero-pin overhead 10-MHz internal oscillator. |
| INTOSC2 ⁽¹⁾ | Internal oscillator 2. Zero-pin overhead 10-MHz internal oscillator. |
| X1 (XTAL) | External crystal or resonator connected between the X1 and X2 pins or single-ended clock connected to the X1 pin. |

(1) On reset, internal oscillator 2 (INTOSC2) is the default clock source for the PLL (OSCCLK).

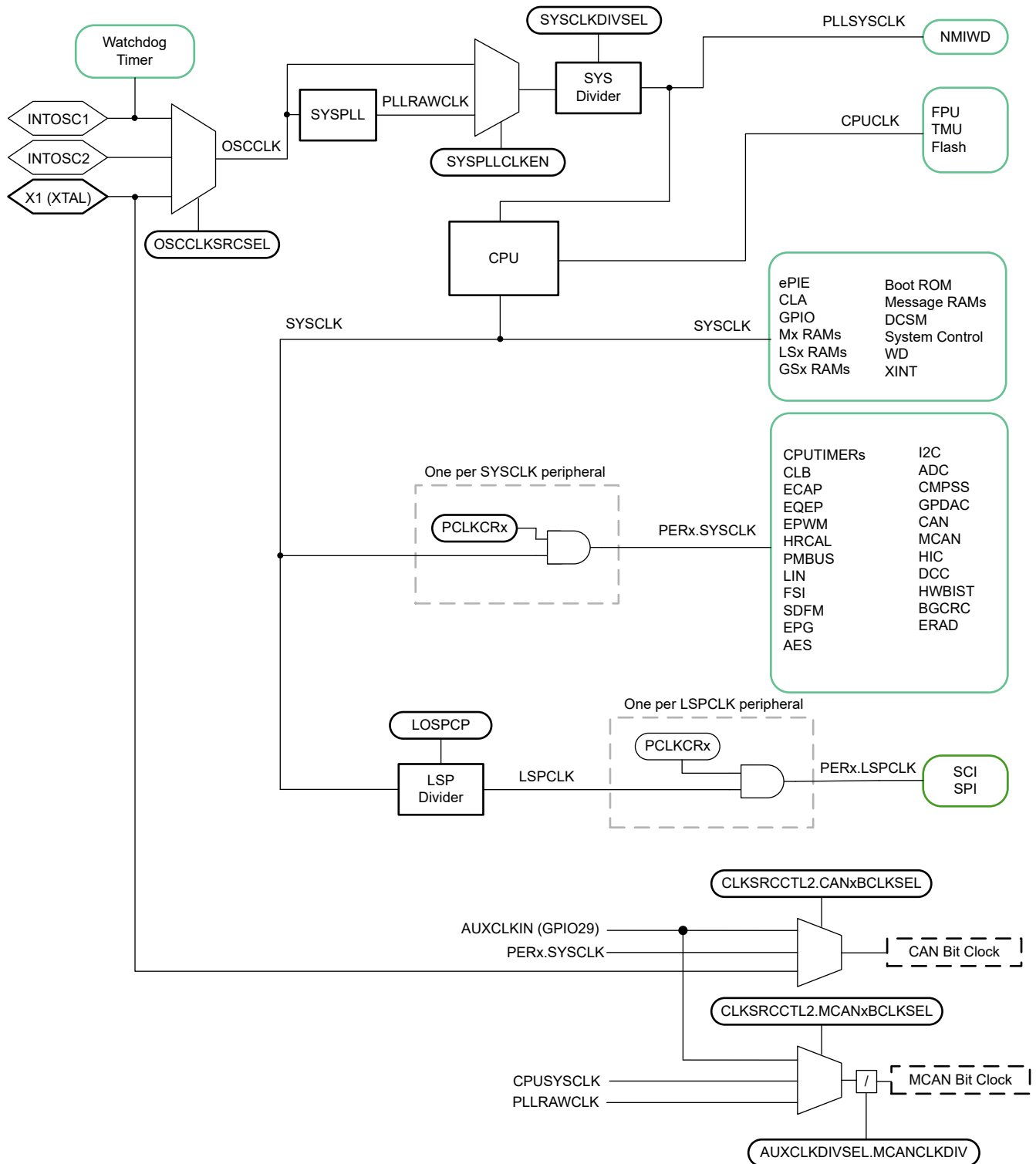


Figure 6-14. Clocking System

SYSPLL

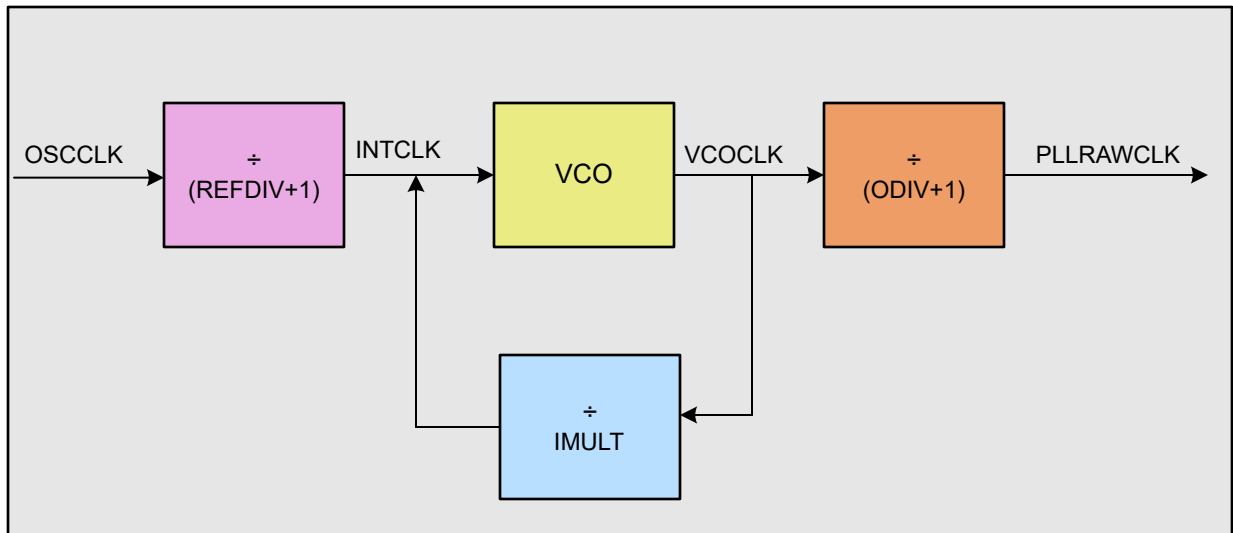


Figure 6-15. System PLL

In the *System PLL* figure,

$$f_{PLLRAWCLK} = \frac{f_{OSCCLK}}{(REFDIV + 1)} \times \frac{IMULT}{(ODIV + 1)} \quad (1)$$

6.12.3.2 Clock Frequencies, Requirements, and Characteristics

This section provides the frequencies and timing requirements of the input clocks, PLL lock times, frequencies of the internal clocks, and the frequency and switching characteristics of the output clock.

6.12.3.2.1 Input Clock Frequency and Timing Requirements, PLL Lock Times

6.12.3.2.1.1 Input Clock Frequency

| | | MIN | MAX | UNIT |
|--------------|--|-----|-----|------|
| $f_{(XTAL)}$ | Frequency, X1/X2, from external crystal or resonator | 10 | 20 | MHz |
| $f_{(X1)}$ | Frequency, X1, from external oscillator | 10 | 25 | MHz |
| $f_{(AUXI)}$ | Frequency, AUXCLKIN, from external oscillator | 10 | 60 | MHz |

6.12.3.2.1.2 XTAL Oscillator Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|-------------|---|-------------|-----|-------------|------|
| X1 V_{IL} | Valid low-level input voltage (Comparator) | -0.3 | | 0.3 * VDDIO | V |
| X1 V_{IH} | Valid high-level input voltage (Comparator) | 0.7 * VDDIO | | VDDIO + 0.3 | V |

6.12.3.2.1.3 X1 Input Level Characteristics When Using an External Clock Source - Not a Crystal

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | MAX | UNIT |
|-------------|---|-------------|-------------|------|
| X1 V_{IL} | Valid low-level input voltage (Buffer) | -0.3 | 0.3 * VDDIO | V |
| X1 V_{IH} | Valid high-level input voltage (Buffer) | 0.7 * VDDIO | VDDIO + 0.3 | V |

6.12.3.2.1.4 X1 Timing Requirements

| | | MIN | MAX | UNIT |
|--------------|--|-----|-----|------|
| $t_{f(X1)}$ | Fall time, X1 | | 6 | ns |
| $t_{r(X1)}$ | Rise time, X1 | | 6 | ns |
| $t_{w(X1L)}$ | Pulse duration, X1 low as a percentage of $t_{c(X1)}$ | 45% | 55% | |
| $t_{w(X1H)}$ | Pulse duration, X1 high as a percentage of $t_{c(X1)}$ | 45% | 55% | |

6.12.3.2.1.5 AUXCLKIN Timing Requirements

| | | MIN | MAX | UNIT |
|---------------|---|-----|-----|------|
| $t_{f(AUXI)}$ | Fall time, AUXCLKIN | | 6 | ns |
| $t_{r(AUXI)}$ | Rise time, AUXCLKIN | | 6 | ns |
| $t_{w(AUXL)}$ | Pulse duration, AUXCLKIN low as a percentage of $t_{c(XCI)}$ | 45% | 55% | |
| $t_{w(AUXH)}$ | Pulse duration, AUXCLKIN high as a percentage of $t_{c(XCI)}$ | 45% | 55% | |

6.12.3.2.1.6 APLL Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | MIN | TYP | MAX | UNIT |
|----------------------------------|-----|-----|--|---------|
| PLL Lock time | | | | |
| SYS PLL Lock Time ⁽¹⁾ | | | $5\mu s + (1024 * (REFDIV + 1) * t_{c(OSCCLK)})$ | μs |

- (1) The PLL lock time here defines the typical time that takes for the PLL to lock once PLL is enabled (SYSPLLCTL1[PLLENA]=1). Additional time to verify the PLL clock using Dual Clock Comparator (DCC) is not accounted here. TI recommends using the latest example software from C2000Ware for initializing the PLLs. For the system PLL, see InitSysPll() or SysCtl_setClock().

6.12.3.2.1.7 XCLKOUT Switching Characteristics - PLL Bypassed or Enabled

over recommended operating conditions (unless otherwise noted)

| PARAMETER ⁽¹⁾ | | MIN | MAX | UNIT |
|--------------------------|------------------------------|----------------------|----------------------|------|
| $t_{f(XCO)}$ | Fall time, XCLKOUT | | 5 | ns |
| $t_{r(XCO)}$ | Rise time, XCLKOUT | | 5 | ns |
| $t_{w(XCOL)}$ | Pulse duration, XCLKOUT low | H - 2 ⁽²⁾ | H + 2 ⁽²⁾ | ns |
| $t_{w(XCOH)}$ | Pulse duration, XCLKOUT high | H - 2 ⁽²⁾ | H + 2 ⁽²⁾ | ns |
| $f_{(XCO)}$ | Frequency, XCLKOUT | | 50 | MHz |

(1) A load of 40 pF is assumed for these parameters.

(2) $H = 0.5t_{c(XCO)}$

6.12.3.2.1.8 Internal Clock Frequencies

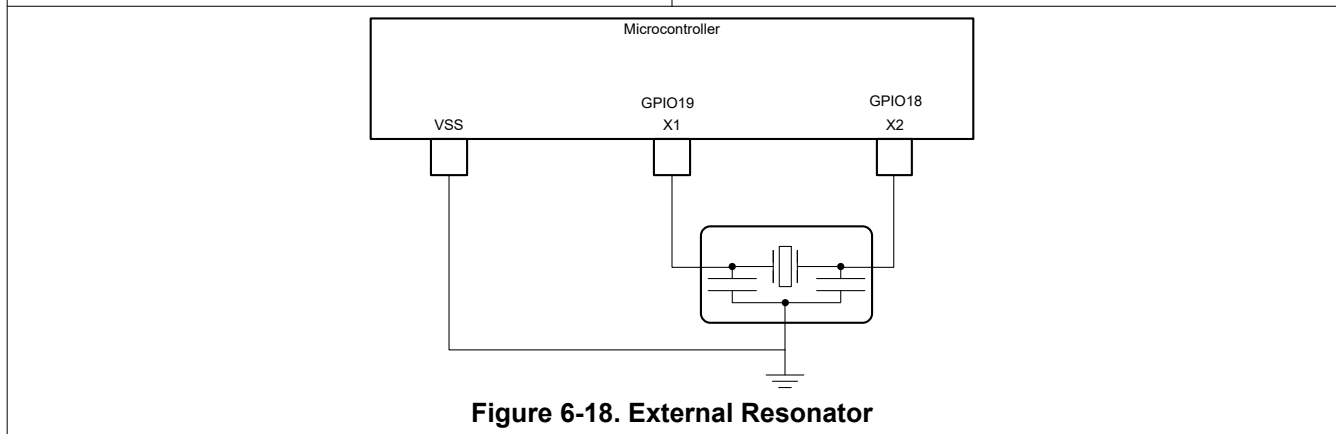
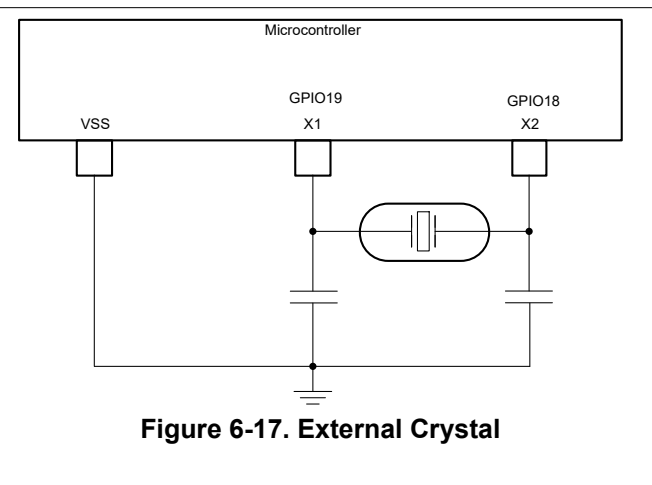
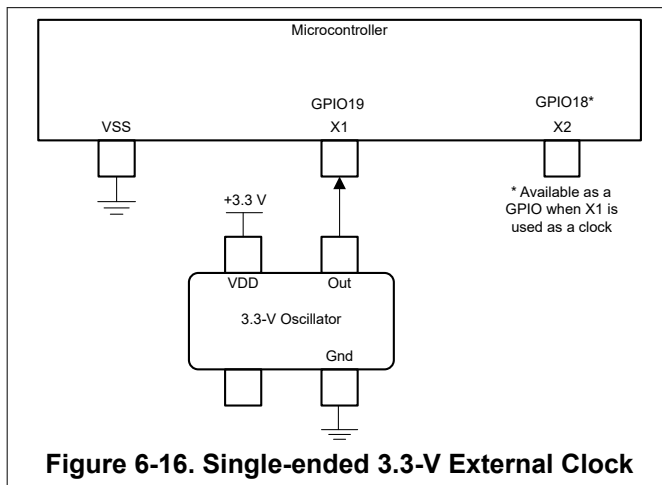
| | | MIN | NOM | MAX | UNIT |
|-------------------|--|------|----------------------|-----|------|
| $f_{(SYSCLK)}$ | Frequency, device (system) clock | 2 | | 120 | MHz |
| $t_{c(SYSCLK)}$ | Period, device (system) clock | 8.33 | | 500 | ns |
| $f_{(INTCLK)}$ | Frequency, system PLL going into VCO (after REFDIV) | 2 | | 20 | MHz |
| $f_{(VCOCLK)}$ | Frequency, system PLL VCO (before ODIV) | 220 | | 600 | MHz |
| $f_{(PLLRAWCLK)}$ | Frequency, system PLL output (before SYSCLK divider) | 6 | | 240 | MHz |
| $f_{(PLL)}$ | Frequency, PLLSYSCLK | 2 | | 120 | MHz |
| $f_{(PLL_LIMP)}$ | Frequency, PLL Limp Frequency ⁽¹⁾ | | 45/(ODIV+1) | | MHz |
| $f_{(LSP)}$ | Frequency, LSPCLK | 2 | | 120 | MHz |
| $t_{c(LSPCLK)}$ | Period, LSPCLK | 8.33 | | 500 | ns |
| $f_{(OSCCLK)}$ | Frequency, OSCCLK (INTOSC1 or INTOSC2 or XTAL or X1) | | See respective clock | | MHz |
| $f_{(EPWM)}$ | Frequency, EPWMCLK | | | 120 | MHz |
| $f_{(HRPWM)}$ | Frequency, HRPWMCLK | 60 | | 120 | MHz |

(1) PLL output frequency when OSCCLK is dead (Loss of OSCCLK causes PLL to Limp).

6.12.3.3 Input Clocks and PLLs

In addition to the internal 0-pin oscillators, three types of external clock sources are supported:

- A single-ended 3.3-V external clock. The clock signal should be connected to X1, as shown in [Figure 6-16](#), with the XTALCR.SE bit set to 1.
- An external crystal. The crystal should be connected across X1 and X2 with its load capacitors connected to VSS as shown in [Figure 6-17](#).
- An external resonator. The resonator should be connected across X1 and X2 with its ground connected to VSS as shown in [Figure 6-18](#).



6.12.3.4 XTAL Oscillator

6.12.3.4.1 Introduction

The crystal oscillator in this device is an embedded electrical oscillator that, when paired with a compatible quartz crystal (or a ceramic resonator), can generate the system clock required by the device.

6.12.3.4.2 Overview

The following sections describe the components of the electrical oscillator and crystal.

6.12.3.4.2.1 Electrical Oscillator

The electrical oscillator in this device is a Pierce oscillator. It is a positive feedback inverter circuit that requires a tuning circuit in order to oscillate. When this oscillator is paired with a compatible crystal, a tank circuit is formed. This tank circuit oscillates at the fundamental frequency of the crystal. On this device, the oscillator is designed to operate in parallel resonance mode due to the shunt capacitor (C0) and required load capacitors (CL). [Figure 6-19](#) illustrates the components of the electrical oscillator and the tank circuit.

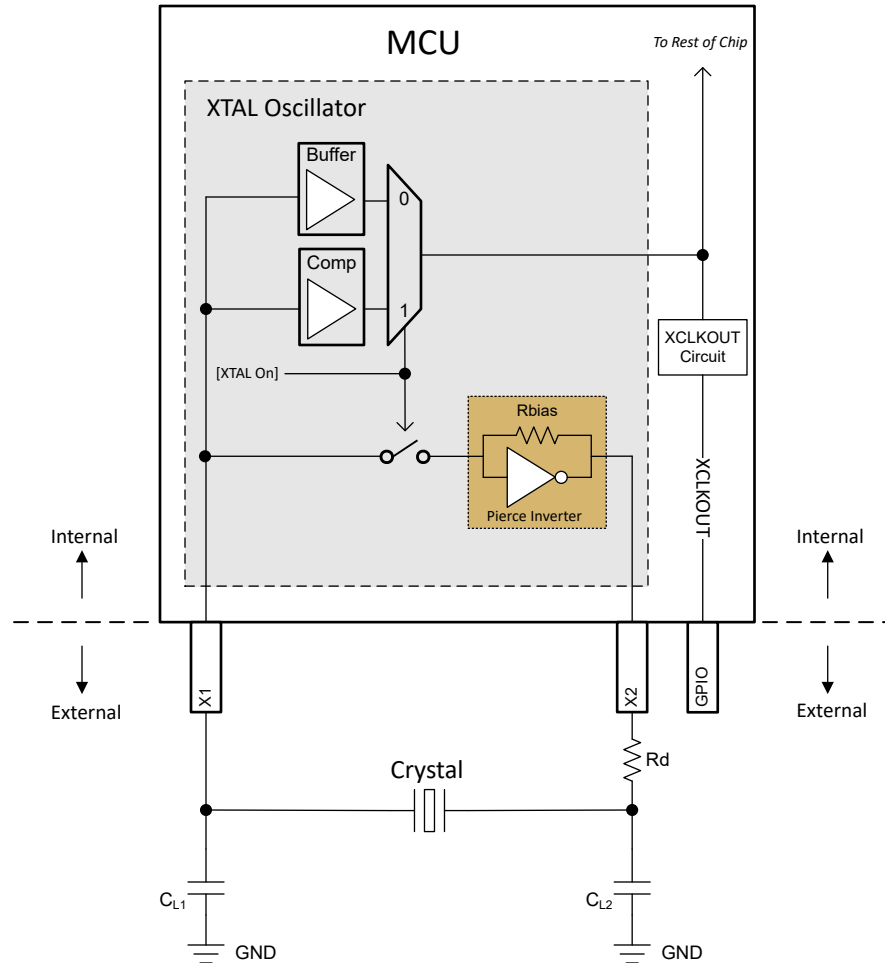


Figure 6-19. Electrical Oscillator Block Diagram

6.12.3.4.2.1.1 Modes of Operation

The electrical oscillator in this device has two modes of operation: crystal mode and single-ended mode.

6.12.3.4.2.1.1.1 Crystal Mode of Operation

In the crystal mode of operation, a quartz crystal with load capacitors has to be connected to X1 and X2.

This mode of operation is engaged when $[XTAL\ On] = 1$, which is achieved by setting $XTALCR.OSCOFF = 0$ and $XTALCR.SE = 0$. There is an internal bias resistor for the feedback loop so an external one should not be used. Adding an external bias resistor will create a parallel resistance with the internal R_{bias} , moving the bias point of operation and possibly leading to clipped waveforms, out-of-specification duty cycle, and reduction in the effective negative resistance.

In this mode of operation, the resultant clock on X1 is passed through a comparator (Comp) to the rest of the chip. The clock on X1 needs to meet the V_{IH} and V_{IL} of the comparator. See the *XTAL Oscillator Characteristics* table for the V_{IH} and V_{IL} requirements of the comparator.

6.12.3.4.2.1.1.2 Single-Ended Mode of Operation

In the single-ended mode of operation, a clock signal is connected to X1 with X2 left unconnected. A quartz crystal should not be used in this mode.

This mode is enabled when $[XTAL\ On] = 0$, which can be achieved by setting $XTALCR.OSCOFF = 1$ and $XTALCR.SE = 1$.

In this mode of operation, the clock on X1 is passed through a buffer (Buffer) to the rest of the chip. See the *X1 Input Level Characteristics When Using an External Clock Source (Not a Crystal)* table for the input requirements of the buffer.

6.12.3.4.2.1.2 XTAL Output on XCLKOUT

The output of the electrical oscillator that is fed to the rest of the chip can be brought out on XCLKOUT for observation by configuring the CLKSRCCTL3.XCLKOUTSEL and XCLKOUTDIVSEL.XCLKOUTDIV registers. See the GPIO Muxed Pins table for a list of GPIOs that XCLKOUT comes out on.

6.12.3.4.2.2 Quartz Crystal

Electrically, a quartz crystal can be represented by an LCR (Inductor-Capacitor-Resistor) circuit. However, unlike an LCR circuit, crystals have very high Q due to the low motional resistance and are also very underdamped. Components of the crystal are shown in [Figure 6-20](#) and explained below.

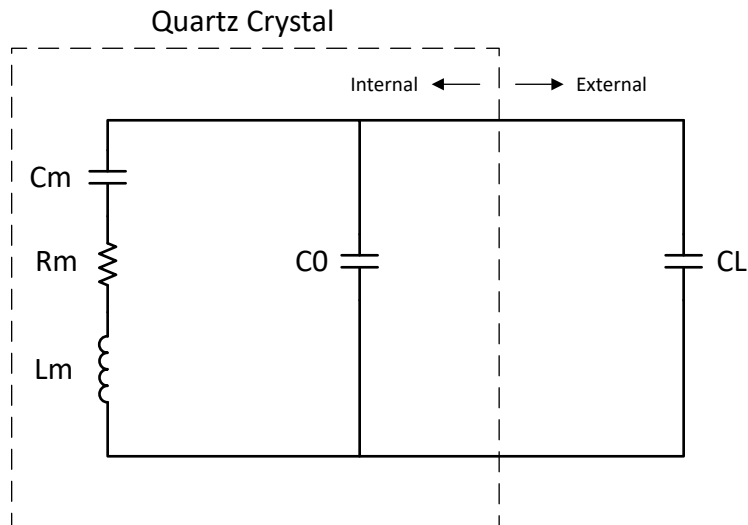


Figure 6-20. Crystal Electrical Representation

C_m (Motional capacitance): Denotes the elasticity of the crystal.

R_m (Motional resistance): Denotes the resistive losses within the crystal. This is not the ESR of the crystal but can be approximated as such depending on the values of the other crystal components.

L_m (Motional inductance): Denotes the vibrating mass of the crystal.

C_0 (Shunt capacitance): The capacitance formed from the two crystal electrodes and stray package capacitance.

CL (Load capacitance): This is the effective capacitance seen by the crystal at its electrodes. It is external to the crystal. The frequency ppm specified in the crystal data sheet is usually tied to the CL parameter.

Note that most crystal manufacturers specify CL as the effective capacitance seen at the crystal pins, while some crystal manufacturers specify CL as the capacitance on just one of the crystal pins. Check with the crystal manufacturer for how the CL is specified in order to use the correct values in calculations.

From [Figure 6-19](#), CL_1 and CL_2 are in series; so, to find the equivalent total capacitance seen by the crystal, the capacitance series formula has to be applied which simply evaluates to $[CL_1]/2$ if $CL_1 = CL_2$.

It is recommended that a stray PCB capacitance be added to this value. 3 pF to 5 pF are reasonable estimates, but the actual value will depend on the PCB in question.

Note that the load capacitance is a requirement of both the electrical oscillator and crystal. The value chosen has to satisfy both the electrical oscillator and the crystal.

The effect of CL on the crystal is frequency-pulling. If the effective load capacitance is lower than the target, the crystal frequency will increase and vice versa. However, the effect of frequency-pulling is usually very minimal and typically results in less than 10-ppm variation from the nominal frequency.

6.12.3.4.2.3 GPIO Modes of Operation

On this device, X1 and X2 can be used as GPIO19 and GPIO18, respectively, depending on the operating mode of the XTAL. Refer to the External Oscillator (XTAL) section of the [TMS320F28003x Real-Time Microcontrollers Technical Reference Manual](#).

6.12.3.4.3 Functional Operation

6.12.3.4.3.1 ESR – Effective Series Resistance

Effective Series Resistance is the resistive load the crystal presents to the electrical oscillator at resonance. The higher the ESR, the lower the Q, and less likely the crystal will start up or maintain oscillation. The relationship between ESR and the crystal components is indicated below.

$$ESR = R_m * \left(1 + \frac{C_0}{CL}\right)^2 \quad (2)$$

Note that ESR is not the same as motional resistance of the crystal, but can be approximated as such if the effective load capacitance is much greater than the shunt capacitance.

6.12.3.4.3.2 Rneg – Negative Resistance

Negative resistance is the impedance presented by the electrical oscillator to the crystal. It is the amount of energy the electrical oscillator must supply to the crystal to overcome the losses incurred during oscillation. Rneg depicts a circuit that provides rather than consume energy and can also be viewed as the overall gain of the circuit.

The generally accepted practice is to have Rneg > 3x ESR to 5x ESR to ensure the crystal starts up under all conditions. Note that it takes slightly more energy to start up the crystal than it does to sustain oscillation; therefore, if it can be ensured that the negative resistance requirement is met at start-up, then oscillation sustenance will not be an issue.

[Figure 6-21](#) and [Figure 6-22](#) show the variation between negative resistance and the crystal components for this device. As can be seen from the graphs, the crystal shunt capacitance (C0) and effective load capacitance (CL) greatly influence the negative resistance of the electrical oscillator. Note that these are typical graphs; so, refer to [Table 6-5](#) for minimum and maximum values for design considerations.

6.12.3.4.3.3 Start-up Time

Start-up time is an important consideration when selecting the components of the crystal circuit. As mentioned in the [Rneg – Negative Resistance](#) section, for reliable start-up across all conditions, it is recommended that the Rneg > 3x ESR to 5x ESR of the crystal.

Crystal ESR and the dampening resistor (Rd) greatly affect the start-up time. The higher the two values, the longer the crystal takes to start up. Longer start-up times are usually a sign that the crystal and components are not a correct match.

Refer to [Crystal Oscillator Specifications](#) for the typical start-up times. Note that the numbers specified here are typical numbers provided for guidance only. Actual start-up time depends heavily on the crystal in question and the external components.

6.12.3.4.3.3.1 X1/X2 Precondition

On this device, the GPIO19/18 alternate functionality on X1/X2 can be used to speed up the start-up time of the crystal if needed. This functionality is achieved by preconditioning the load capacitors CL1 and CL2 to a known state before the XTAL is turned on. See the [TMS320F28003x Real-Time Microcontrollers Technical Reference Manual](#) for details.

6.12.3.4.3.4 DL – Drive Level

Drive level refers to how much power is provided by the electrical oscillator and dissipated by the crystal. The maximum drive level specified in the crystal manufacturer's data sheet is usually the maximum the crystal can dissipate without damage or significant reduction in operating life. On the other hand, the drive level specified by the electrical oscillator is the maximum power it can provide. The actual power provided by the electrical oscillator is not necessarily the maximum power and depends on the crystal and board components.

For cases where the actual drive level from the electrical oscillator exceeds the maximum drive level specification of the crystal, a dampening resistor (R_d) should be installed to limit the current and reduce the power dissipated by the crystal. Note that R_d reduces the circuit gain; and therefore, the actual value to use should be evaluated to make sure all other conditions for start-up and sustained oscillation are met.

6.12.3.4.4 How to Choose a Crystal

Using [Crystal Oscillator Specifications](#) as a reference:

1. Pick a crystal frequency (for example, 20 MHz).
2. Check that the ESR of the crystal $\leq 50 \Omega$ per specifications for 20 MHz.
3. Check that the load capacitance requirement of the crystal manufacturer is within 6 pF and 12 pF per specifications for 20 MHz.
 - As mentioned, CL_1 and CL_2 are in series; so, provided $CL_1 = CL_2$, effective load capacitance $CL = [CL_1]/2$.
 - Adding board parasitics to this results in $CL = [CL_1]/2 + C_{stray}$
4. Check that the maximum drive level of the crystal ≥ 1 mW. If this requirement is not met, a dampening resistor R_d can be used. Refer to [DL – Drive Level](#) on other points to consider when using R_d .

6.12.3.4.5 Testing

It is recommended that the user have the crystal manufacturer completely characterize the crystal with their board to ensure the crystal always starts up and maintains oscillation.

Below is a brief overview of some measurements that can be performed:

Due to how sensitive the crystal circuit is to capacitance, it is recommended that scope probes not be connected to X1 and X2. If scope probes must be used to monitor X1/X2, an active probe with less than 1-pF input capacitance should be used.

Frequency

1. Bring out the XTAL on XCLKOUT.
2. Measure this frequency as the crystal frequency.

Negative Resistance

1. Bring out the XTAL on XCLKOUT.
2. Place a potentiometer in series with the crystal between the load capacitors.
3. Increase the resistance of the potentiometer until the clock on XCLKOUT stops.
4. This resistance plus the crystal's actual ESR is the negative resistance of the electrical oscillator.

Start-Up Time

1. Turn off the XTAL.
2. Bring out the XTAL on XCLKOUT.
3. Turn on the XTAL and measure how long it takes the clock on XCLKOUT to stay within 45% and 55% duty cycle.

6.12.3.4.6 Common Problems and Debug Tips

Crystal Fails to Start Up

- Go through the [How to Choose a Crystal](#) section and make sure there are no violations.

Crystal Takes a Long Time to Start Up

- If a dampening resistor R_d is installed, it is too high.
- If no dampening resistor is installed, either the crystal ESR is too high or the overall circuit gain is too low due to high load capacitance.

6.12.3.4.7 Crystal Oscillator Specifications

6.12.3.4.7.1 Crystal Oscillator Parameters

| | | MIN | MAX | UNIT |
|----------|---------------------------|-----|-----|------|
| CL1, CL2 | Load capacitance | 12 | 24 | pF |
| C0 | Crystal shunt capacitance | | 7 | pF |

6.12.3.4.7.2 Crystal Equivalent Series Resistance (ESR) Requirements

For the [Crystal Equivalent Series Resistance \(ESR\) Requirements](#) table:

- Crystal shunt capacitance (C0) should be less than or equal to 7 pF.
- $ESR = \text{Negative Resistance} / 3$

Table 6-5. Crystal Equivalent Series Resistance (ESR) Requirements

| CRYSTAL FREQUENCY (MHz) | MAXIMUM ESR (Ω) (CL1 = CL2 = 12 pF) | MAXIMUM ESR (Ω) (CL1 = CL2 = 24 pF) |
|-------------------------|---|---|
| 10 | 55 | 110 |
| 12 | 50 | 95 |
| 14 | 50 | 90 |
| 16 | 45 | 75 |
| 18 | 45 | 65 |
| 20 | 45 | 50 |

Negative Resistance vs. 10MHz Crystal

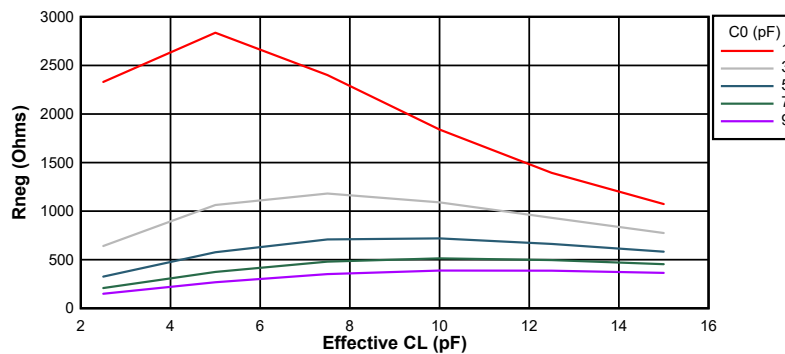


Figure 6-21. Negative Resistance Variation at 10 MHz

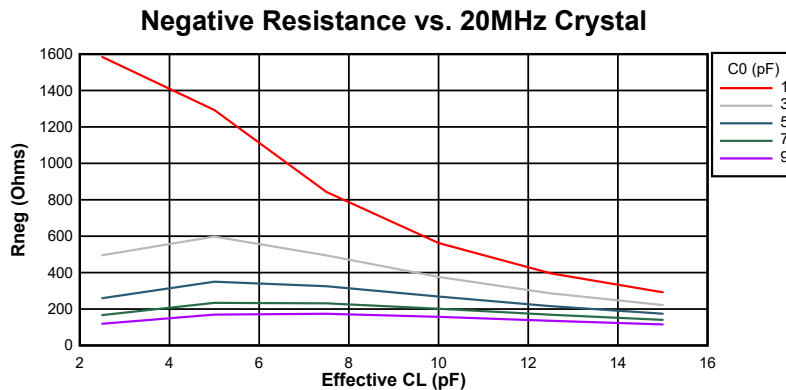


Figure 6-22. Negative Resistance Variation at 20 MHz

6.12.3.4.7.3 Crystal Oscillator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------|------------|---|-----|-----|-----|------|
| Start-up time ⁽¹⁾ | f = 10 MHz | ESR MAX = 110 Ω CL1 = CL2 = 24 pF C0 = 7 pF | | 4 | | ms |
| | f = 20 MHz | ESR MAX = 50 Ω CL1 = CL2 = 24 pF C0 = 7 pF | | 2 | | ms |
| Crystal drive level (DL) | | | | | 1 | mW |

(1) Start-up time is dependent on the crystal and tank circuit components. TI recommends that the crystal vendor characterize the application with the chosen crystal.

6.12.3.5 Internal Oscillators

To reduce production board costs and application development time, all F28003x devices contain two independent internal oscillators, referred to as INTOSC1 and INTOSC2. By default, INTOSC2 is set as the source for the system reference clock (OSCCLK) and INTOSC1 is set as the backup clock source.

Applications requiring tighter **SCI baud rate matching** can use the SCI baud tuning example (baud_tune_via_uart) available in C2000Ware.

6.12.3.5.1 INTOSC Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------|---|-------------------|--------------|-----|-------------|------|
| f _{INTOSC} | Frequency, INTOSC1 and INTOSC2 ⁽¹⁾ | -40°C to 125°C | 9.82 (-1.8%) | 10 | 10.1 (1.0%) | MHz |
| | | -30°C to 90°C | 9.86 (-1.4%) | 10 | 10.1 (1.0%) | |
| | | -10°C to 85°C | 9.9 (-1.0%) | 10 | 10.1 (1.0%) | |
| f _{INTOSC-STABILITY} | Frequency stability at room temperature | 30°C, Nominal VDD | ±0.1 | | | % |
| t _{INTOSC-ST} | Start-up and settling time | | 20 | | | µs |

- (1) INTOSC frequency may shift due to the thermal and mechanical stress of solder reflow. A post-reflow bake can restore the unit to its original data sheet performance.

6.12.4 Flash Parameters

Table 6-6 lists the minimum required Flash wait states with different clock sources and frequencies. Wait state is the value set in register FRDCNTL[RWAIT].

Table 6-6. Minimum Required Flash Wait States with Different Clock Sources and Frequencies

| CPUCLK (MHz) | EXTERNAL OSCILLATOR OR CRYSTAL | | INTOSC1 OR INTOSC2 | |
|--------------------|--------------------------------|-----------------------------------|--------------------|-----------------------------------|
| | NORMAL OPERATION | BANK OR PUMP SLEEP ⁽¹⁾ | NORMAL OPERATION | BANK OR PUMP SLEEP ⁽¹⁾ |
| 116 < CPUCLK ≤ 120 | 5 | 5 | 5 | 6 |
| 100 < CPUCLK ≤ 116 | | | | 5 |
| 97 < CPUCLK ≤ 100 | 4 | 4 | 4 | 5 |
| 80 < CPUCLK ≤ 97 | | | | 4 |
| 77 < CPUCLK ≤ 80 | 3 | 3 | 3 | 4 |
| 60 < CPUCLK ≤ 77 | | | | 3 |
| 58 < CPUCLK ≤ 60 | 2 | 2 | 2 | 3 |
| 40 < CPUCLK ≤ 58 | | | | 2 |
| 38 < CPUCLK ≤ 40 | 1 | 1 | 1 | 2 |
| 20 < CPUCLK ≤ 38 | | | | 1 |
| 19 < CPUCLK ≤ 20 | 0 | 0 | 0 | 1 |
| CPUCLK ≤ 19 | | | | 0 |

(1) Flash SLEEP operations require an extra wait state when using INTOSC as the clock source for the frequency ranges indicated. Any wait state FRDCNTL[RWAIT] change must be made before beginning a SLEEP mode operation. This setting impacts both flash banks.

The F28003x devices have an improved 128-bit prefetch buffer that provides high flash code execution efficiency across wait states. Figure 6-23 and Figure 6-24 illustrate typical efficiency across wait-state settings compared to previous-generation devices with a 64-bit prefetch buffer. Wait-state execution efficiency with a prefetch buffer will depend on how many branches are present in application software. Two examples of linear code and if-then-else code are provided.

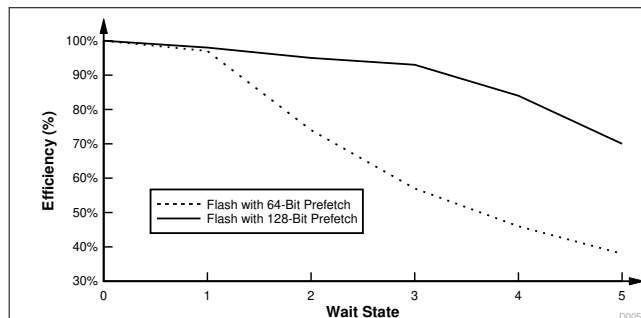


Figure 6-23. Application Code With Heavy 32-Bit Floating-Point Math Instructions

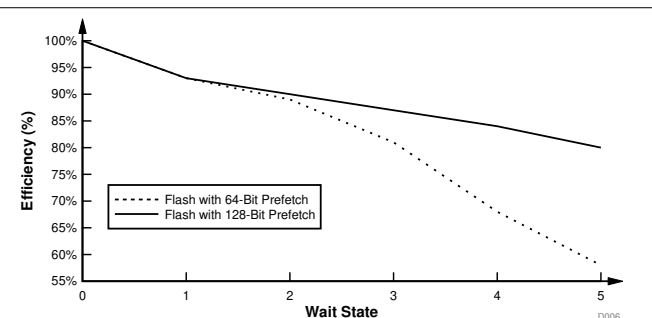


Figure 6-24. Application Code With 16-Bit If-Else Instructions

Section 6.12.4.1 lists the Flash parameters.

Note

The Main Array flash programming must be aligned to 64-bit address boundaries and each 64-bit word may only be programmed once per write/erase cycle.

Note

It is important to provide the correct sector mask for the bank erase command. If the mask is mistakenly chosen to erase an inaccessible sector (belongs to another security zone), the bank erase command will continue attempting to erase the sector endlessly and the FSM will never exit (since erase will not succeed). To avoid such a situation, user must take care to provide the correct mask. However, given that there is a chance of choosing an incorrect mask, TI suggests to initialize the max allowed erase pulses to zero after the max number of pulses are issued by the FSM for the bank erase operation. This will ensure that the FSM will end the bank erase command after trying to erase the inaccessible sector up to the max allowed erase pulses.

The Example_EraseBanks() function in the C2000Ware's flash API usage example depicts the implementation of this sequence (content of the while loop waiting for the FSM to complete the bank erase command). Users must use this code as-is irrespective of whether or not security is used by the application to also ensure that the FSM exits from bank erase operations in case of an erase-failure.

6.12.4.1 Flash Parameters

| PARAMETER | | MIN | TYP | MAX | UNIT |
|--|-----------------------------|--------------|-----|--------|--------|
| Program Time ⁽¹⁾ | 128 data bits + 16 ECC bits | | 150 | 300 | μs |
| | 8KB (Sector) | | 50 | 100 | ms |
| Sector Erase Time ^{(2) (3)} | < 25 cycles | 8KB (Sector) | 15 | 56 | ms |
| | 1k cycles | | 26 | 133 | ms |
| | 2k cycles | | 31 | 226 | ms |
| | 20k cycles | | 123 | 1026 | ms |
| Bank Erase Time ^{(2) (3)} | < 25 cycles | 128KB (Bank) | 21 | 78 | ms |
| | 1k cycles | | 35 | 183 | ms |
| | 2k cycles | | 42 | 310 | ms |
| | 20k cycles | | 169 | 1410 | ms |
| N_{wec} Write/Erase Cycles per Sector | | | | 20000 | cycles |
| N_{wec} Write/Erase Cycles for Entire Flash (Combined for all Sectors) | | | | 100000 | cycles |
| $t_{retention}$ Data retention duration at $T_J = 85^\circ\text{C}$ | | 20 | | | years |

(1) Program time is at the maximum device frequency. Program time includes overhead of the flash state machine but does not include the time to transfer the following into RAM:

- Code that uses flash API to program the flash
- Flash API itself
- Flash data to be programmed

In other words, the time indicated in this table is applicable after all the required code/data is available in the device RAM, ready for programming. The transfer time will significantly vary depending on the speed of the JTAG debug probe used.

Program time calculation is based on programming 144 bits at a time at the specified operating frequency. Program time includes Program verify by the CPU. The program time does not degrade with write/erase (W/E) cycling, but the erase time does.

Erase time includes Erase verify by the CPU and does not involve any data transfer.

(2) Erase time includes Erase verify by the CPU.

(3) The on-chip flash memory is in an erased state when the device is shipped from TI. As such, erasing the flash memory is not required prior to programming, when programming the device for the first time. However, the erase operation is needed on all subsequent programming operations.

6.12.5 RAM and ROM Parameters

All volatile memory (RAM and ROM) on the F28003x device is 0 Wait-state for both reads and writes, meaning the memory operates at the same speed as SYSCLK. [RAM Block Properties](#) summarizes the characteristics of the different RAM instances on the device. [ROM Properties](#) summarizes the aspects of the ROM instances on the device

Table 6-7. RAM Block Properties

| RAM TYPE | SIZE EACH | FETCH TIME (CYCLES) | READ TIME (CYCLES) | WRITE TIME (CYCLES) | SUPPORTED BUS WIDTHS (BITS) | HOST ACCESS LIST | WAIT STATES | BURST ACCESS SUPPORT |
|------------------------|-----------|---------------------|--------------------|---------------------|-----------------------------|------------------|-------------|----------------------|
| M0 | 2KB | 2 | 2 | 1 | 16/32 | C28x | 0 | No |
| M1 | | | | | | C28x/CLA | | |
| LS RAM (LS0–LS7) | 4KB | | | | | C28x/DMA/HIC | | |
| GS RAM (GS0–GS3) | 8KB | | | | | C28x/CLA | | |
| CLA to CPU Message RAM | 256B | | | | | | | |
| CPU to CLA Message RAM | | | | | | | | |
| CLA to DMA Message RAM | | | | | | | | |
| DMA to CLA Message RAM | | | | | | | | |

Table 6-8. ROM Properties

| ROM TYPE | SIZE EACH | FETCH TIME (CYCLES) | READ TIME (CYCLES) | SUPPORTED BUS WIDTHS (BITS) | HOST ACCESS LIST | WAIT STATES | BURST ACCESS SUPPORT |
|-----------------|-----------|---------------------|--------------------|-----------------------------|------------------|-------------|----------------------|
| Boot ROM | 64KB | 2 | 2 | 16/32 | C28x | 0 | No |
| Secure ROM | 48KB | | | | C28x/CLA | | |
| CLA Data ROM | 8KB | | | | CLA | | |
| CLA Program ROM | 96KB | | | | | | |

6.12.6 Emulation/JTAG

The JTAG (IEEE Standard 1149.1-1990 Standard Test Access Port and Boundary Scan Architecture) port has four dedicated pins: TMS, TDI, TDO, and TCK. The cJTAG (IEEE Standard 1149.7-2009 for Reduced-Pin and Enhanced-Functionality Test Access Port and Boundary-Scan Architecture) port is a compact JTAG interface requiring only two pins (TMS and TCK), which allows other device functionality to be muxed to the traditional GPIO35 (TDI) and GPIO37 (TDO) pins.

Typically, no buffers are needed on the JTAG signals when the distance between the MCU target and the JTAG header is smaller than 6 inches (15.24 cm), and no other devices are present on the JTAG chain. Otherwise, each signal should be buffered. Additionally, for most JTAG debug probe operations at 10 MHz, no series resistors are needed on the JTAG signals. However, if high emulation speeds are expected (35 MHz or so), 22-Ω resistors should be placed in series on each JTAG signal.

The PD (Power Detect) pin of the JTAG debug probe header should be connected to the board's 3.3-V supply. Header GND pins should be connected to board ground. TDIS (Cable Disconnect Sense) should also be connected to board ground. The JTAG clock should be looped from the header TCK output pin back to the RTCK input pin of the header (to sense clock continuity by the JTAG debug probe). This MCU does not support the EMU0 and EMU1 signals that are present on 14-pin and 20-pin emulation headers. These signals should always be pulled up at the emulation header through a pair of board pullup resistors ranging from 2.2 kΩ to 4.7 kΩ (depending on the drive strength of the debugger ports). Typically, a 2.2-kΩ value is used.

Header pin $\overline{\text{RESET}}$ is an open-drain output from the JTAG debug probe header that enables board components to be reset through JTAG debug probe commands (available only through the 20-pin header). [Figure 6-25](#) shows how the 14-pin JTAG header connects to the MCU's JTAG port signals. [Figure 6-26](#) shows how to connect to the 20-pin JTAG header. The 20-pin JTAG header pins EMU2, EMU3, and EMU4 are not used and should be grounded.

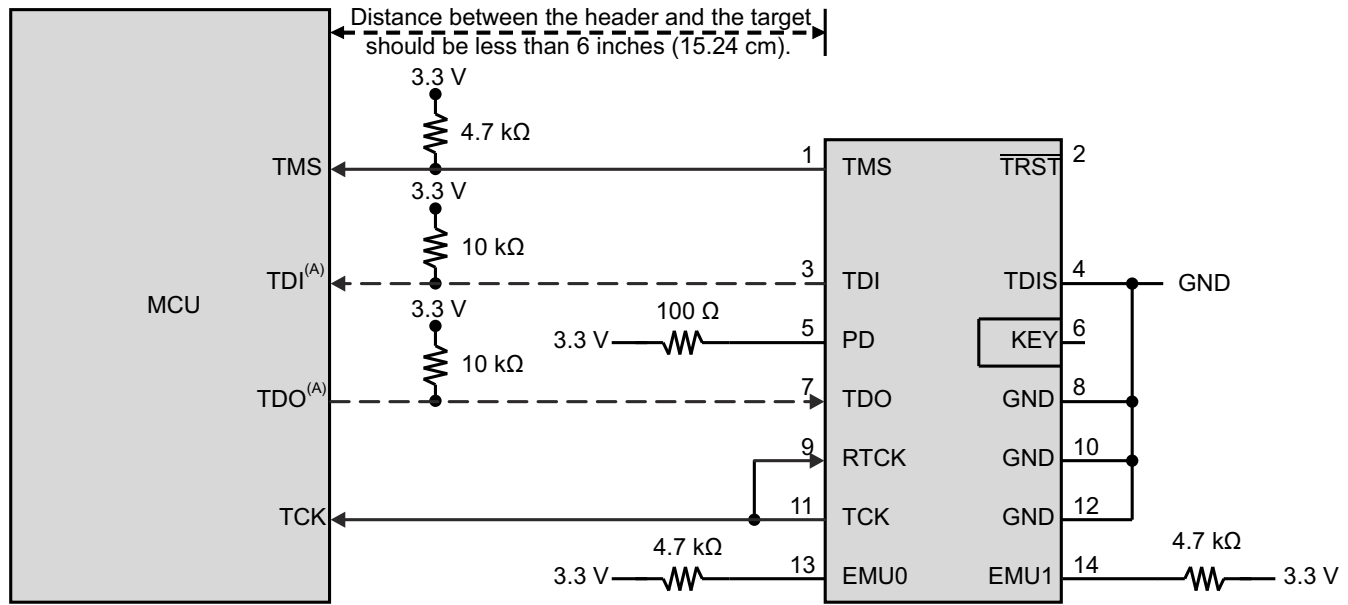
For more information about hardware breakpoints and watchpoints, see [Hardware Breakpoints and Watchpoints in CCS for C2000 devices](#).

For more information about JTAG emulation, see the [XDS Target Connection Guide](#).

Note

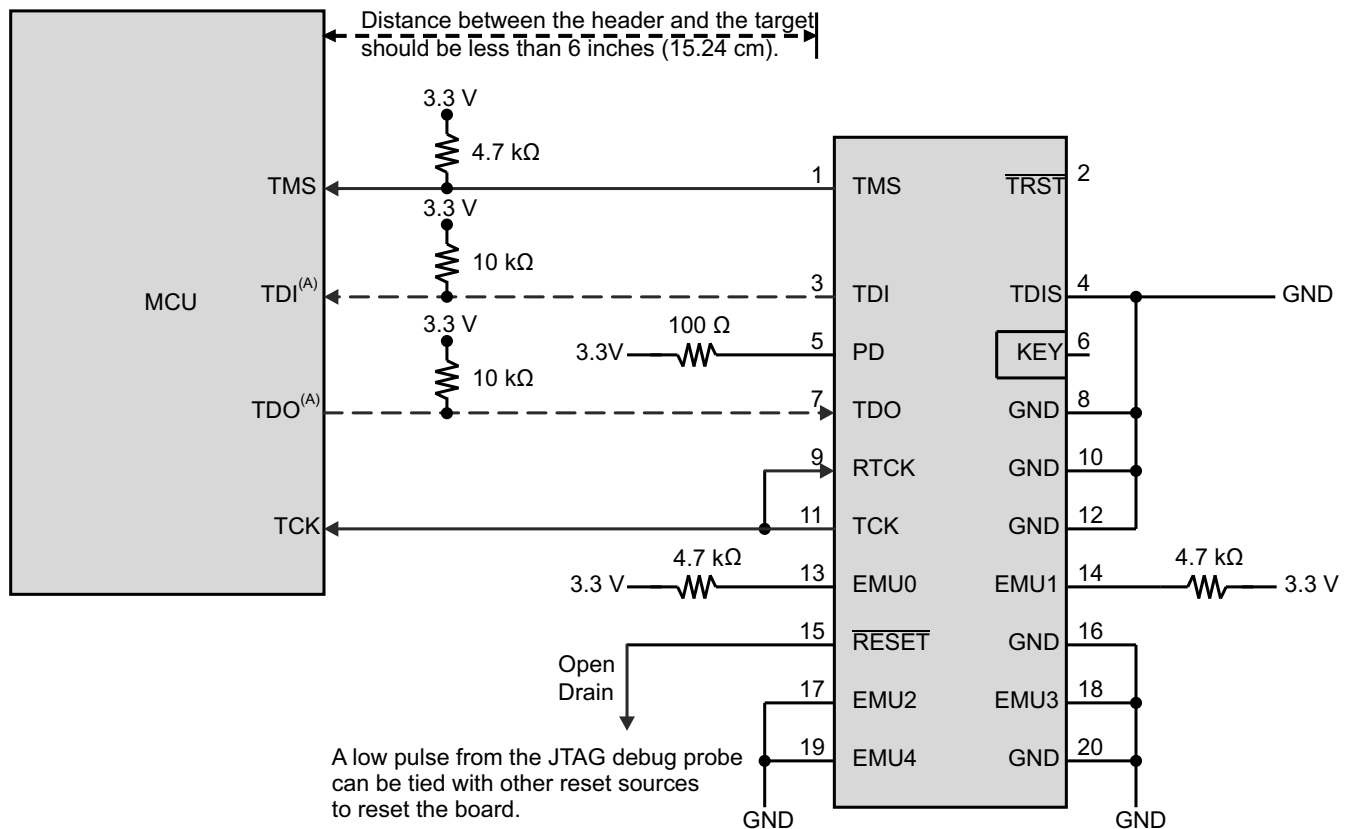
JTAG Test Data Input (TDI) is the default mux selection for the pin. The internal pullup is disabled by default. If this pin is used as JTAG TDI, the internal pullup should be enabled or an external pullup added on the board to avoid a floating input. In the cJTAG option, this pin can be used as GPIO.

JTAG Test Data Output (TDO) is the default mux selection for the pin. The internal pullup is disabled by default. The TDO function will be in a tri-state condition when there is no JTAG activity, leaving this pin floating. The internal pullup should be enabled or an external pullup added on the board to avoid a floating GPIO input. In the cJTAG option, this pin can be used as GPIO.



A. TDI and TDO connections are not required for cJTAG option and these pins can be used as GPIOs instead.

Figure 6-25. Connecting to the 14-Pin JTAG Header



A. TDI and TDO connections are not required for cJTAG option and these pins can be used as GPIOs instead.

Figure 6-26. Connecting to the 20-Pin JTAG Header

6.12.6.1 JTAG Electrical Data and Timing

6.12.6.1.1 JTAG Timing Requirements

| NO. | | | MIN | MAX | UNIT |
|-----|---------------------------|--|-------|-----|------|
| 1 | $t_c(\text{TCK})$ | Cycle time, TCK | 66.66 | | ns |
| 1a | $t_w(\text{TCKH})$ | Pulse duration, TCK high (40% of t_c) | 26.66 | | ns |
| 1b | $t_w(\text{TCKL})$ | Pulse duration, TCK low (40% of t_c) | 26.66 | | ns |
| 3 | $t_{su}(\text{TDI-TCKH})$ | Input setup time, TDI valid to TCK high | 7 | | ns |
| | $t_{su}(\text{TMS-TCKH})$ | Input setup time, TMS valid to TCK high | 7 | | |
| 4 | $t_h(\text{TCKH-TDI})$ | Input hold time, TDI valid from TCK high | 7 | | ns |
| | $t_h(\text{TCKH-TMS})$ | Input hold time, TMS valid from TCK high | 7 | | |

6.12.6.1.2 JTAG Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| NO. | PARAMETER | MIN | MAX | UNIT | |
|-----|------------------------|----------------------------------|-----|------|----|
| 2 | $t_d(\text{TCKL-TDO})$ | Delay time, TCK low to TDO valid | 6 | 20 | ns |

6.12.6.1.3 JTAG Timing Diagram

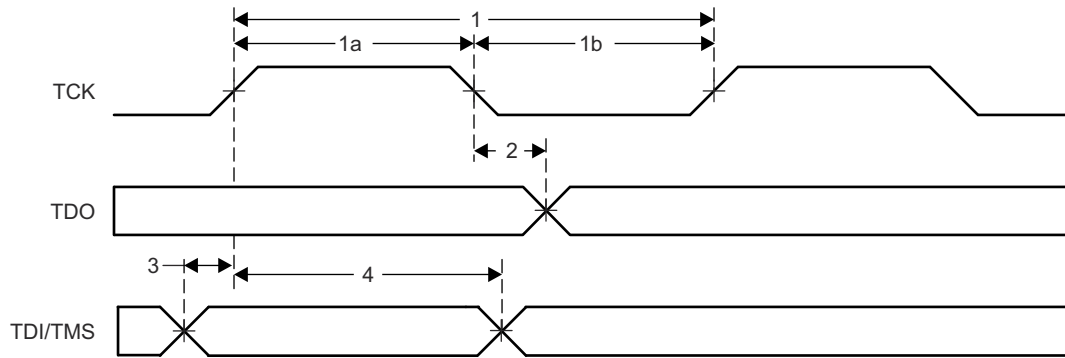


Figure 6-27. JTAG Timing

6.12.6.2 cJTAG Electrical Data and Timing

6.12.6.2.1 cJTAG Timing Requirements

| NO. | | | MIN | MAX | UNIT |
|-----|---------------------------|--|-----|-----|------|
| 1 | $t_c(\text{TCK})$ | Cycle time, TCK | 100 | | ns |
| 1a | $t_w(\text{TCKH})$ | Pulse duration, TCK high (40% of t_c) | 40 | | ns |
| 1b | $t_w(\text{TCKL})$ | Pulse duration, TCK low (40% of t_c) | 40 | | ns |
| 3 | $t_{su}(\text{TMS-TCKH})$ | Input setup time, TMS valid to TCK high | 7 | | ns |
| | $t_{su}(\text{TMS-TCKL})$ | Input setup time, TMS valid to TCK low | 7 | | ns |
| 4 | $t_h(\text{TCKH-TMS})$ | Input hold time, TMS valid from TCK high | 2 | | ns |
| | $t_h(\text{TCKL-TMS})$ | Input hold time, TMS valid from TCK low | 2 | | ns |

6.12.6.2.2 cJTAG Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| NO. | PARAMETER | MIN | MAX | UNIT |
|-----|----------------------------|-----|-----|------|
| 2 | $t_d(\text{TCKL-TMS})$ | 5 | 20 | ns |
| 5 | $t_{dis}(\text{TCKH-TMS})$ | | 20 | ns |

6.12.6.2.3 cJTAG Timing Diagram

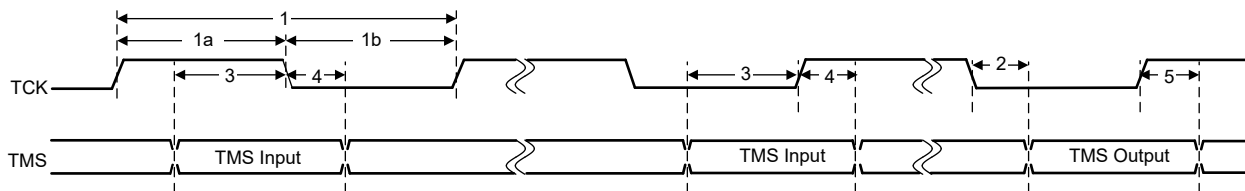


Figure 6-28. cJTAG Timing

6.12.7 GPIO Electrical Data and Timing

The peripheral signals are multiplexed with general-purpose input/output (GPIO) signals. On reset, GPIO pins are configured as inputs. For specific inputs, the user can also select the number of input qualification cycles to filter unwanted noise glitches.

The GPIO module contains an Output X-BAR which allows an assortment of internal signals to be routed to a GPIO in the GPIO mux positions denoted as OUTPUTXBARx. The GPIO module also contains an Input X-BAR which is used to route signals from any GPIO input to different IP blocks such as the ADCs, eCAPs, ePWMs, and external interrupts. For more details, see the X-BAR chapter in the [TMS320F28003x Real-Time Microcontrollers Technical Reference Manual](#).

6.12.7.1 GPIO – Output Timing

6.12.7.1.1 General-Purpose Output Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | MIN | MAX | UNIT |
|--------------|---------------------------------------|-----------|-----|------------------|------|
| $t_{r(GPO)}$ | Rise time, GPIO switching low to high | All GPIOs | | 8 ⁽¹⁾ | ns |
| $t_{f(GPO)}$ | Fall time, GPIO switching high to low | All GPIOs | | 8 ⁽¹⁾ | ns |
| t_{fGPO} | Toggle frequency, GPIO pins | | | 50 | MHz |

(1) Rise time and fall time vary with load. These values assume a 20-pF load.

6.12.7.1.2 General-Purpose Output Timing Diagram

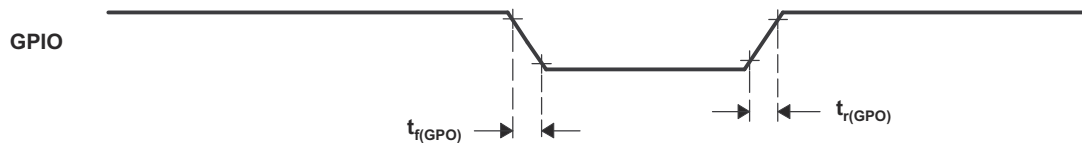


Figure 6-29. General-Purpose Output Timing

6.12.7.2 GPIO – Input Timing

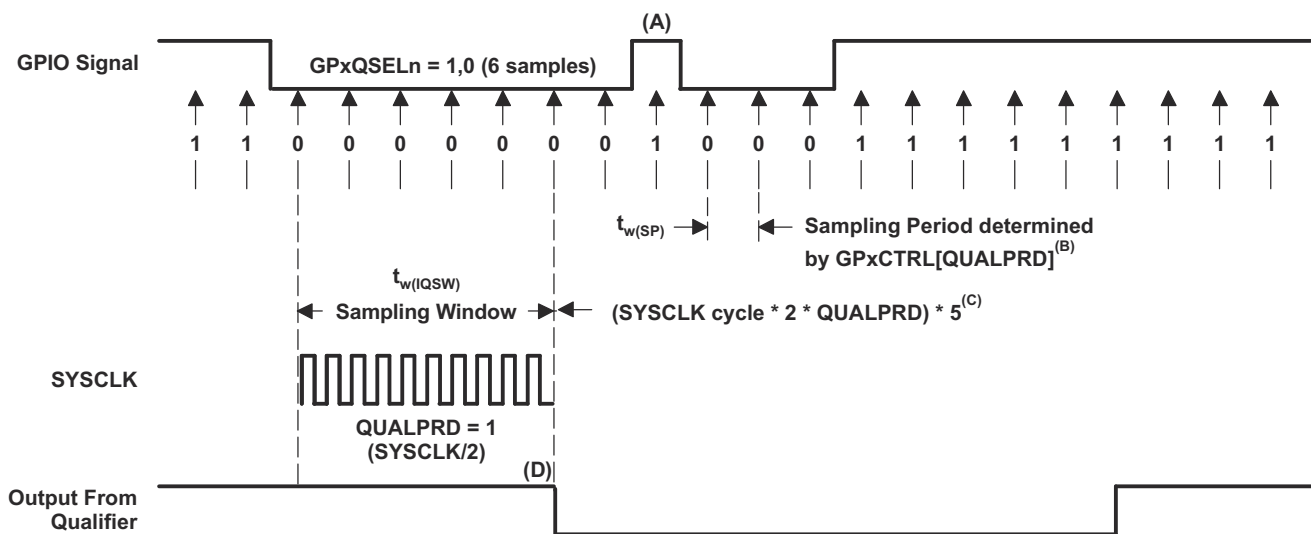
6.12.7.2.1 General-Purpose Input Timing Requirements

| | | | MIN | MAX | UNIT |
|--------------------|---------------------------------|----------------------|---|-----|--------|
| $t_{w(SP)}$ | Sampling period | QUALPRD = 0 | $1t_{c(SYSCCLK)}$ | | cycles |
| | | QUALPRD \neq 0 | $2t_{c(SYSCCLK)} * QUALPRD$ | | cycles |
| $t_{w(IQSW)}$ | Input qualifier sampling window | | $t_{w(SP)} * (n^{(1)} - 1)$ | | cycles |
| $t_{w(GPI)}^{(2)}$ | Pulse duration, GPIO low/high | Synchronous mode | $2t_{c(SYSCCLK)}$ | | cycles |
| | | With input qualifier | $t_{w(IQSW)} + t_{w(SP)} + 1t_{c(SYSCCLK)}$ | | cycles |

(1) "n" represents the number of qualification samples as defined by GPxQSELn register.

(2) For $t_{w(GPI)}$, pulse width is measured from V_{IL} to V_{IL} for an active low signal and V_{IH} to V_{IH} for an active high signal.

6.12.7.2.2 Sampling Mode



- This glitch will be ignored by the input qualifier. The QUALPRD bit field specifies the qualification sampling period. It can vary from 00 to 0xFF. If QUALPRD = 00, then the sampling period is 1 SYSCCLK cycle. For any other value "n", the qualification sampling period is 2n SYSCCLK cycles (that is, at every 2n SYSCCLK cycles, the GPIO pin will be sampled).
- The qualification period selected through the GPxCTRL register applies to groups of eight GPIO pins.
- The qualification block can take either three or six samples. The GPxQSELn Register selects which sample mode is used.
- In the example shown, for the qualifier to detect the change, the input should be stable for 10 SYSCCLK cycles or greater. In other words, the inputs should be stable for $(5 \times QUALPRD \times 2)$ SYSCCLK cycles. This would ensure 5 sampling periods for detection to occur. Because external signals are driven asynchronously, a 13-SYSCCLK-wide pulse ensures reliable recognition.

Figure 6-30. Sampling Mode

6.12.7.3 Sampling Window Width for Input Signals

The following section summarizes the sampling window width for input signals for various input qualifier configurations.

Sampling frequency denotes how often a signal is sampled with respect to SYSCLK.

Sampling frequency = $\text{SYSCLK} / (2 \times \text{QUALPRD})$, if $\text{QUALPRD} \neq 0$

Sampling frequency = SYSCLK , if $\text{QUALPRD} = 0$

Sampling period = $\text{SYSCLK cycle} \times 2 \times \text{QUALPRD}$, if $\text{QUALPRD} \neq 0$

In the previous equations, SYSCLK cycle indicates the time period of SYSCLK.

Sampling period = SYSCLK cycle , if $\text{QUALPRD} = 0$

In a given sampling window, either 3 or 6 samples of the input signal are taken to determine the validity of the signal. This is determined by the value written to GPxQSELn register.

Case 1:

Qualification using 3 samples

Sampling window width = $(\text{SYSCLK cycle} \times 2 \times \text{QUALPRD}) \times 2$, if $\text{QUALPRD} \neq 0$

Sampling window width = $(\text{SYSCLK cycle}) \times 2$, if $\text{QUALPRD} = 0$

Case 2:

Qualification using 6 samples

Sampling window width = $(\text{SYSCLK cycle} \times 2 \times \text{QUALPRD}) \times 5$, if $\text{QUALPRD} \neq 0$

Sampling window width = $(\text{SYSCLK cycle}) \times 5$, if $\text{QUALPRD} = 0$

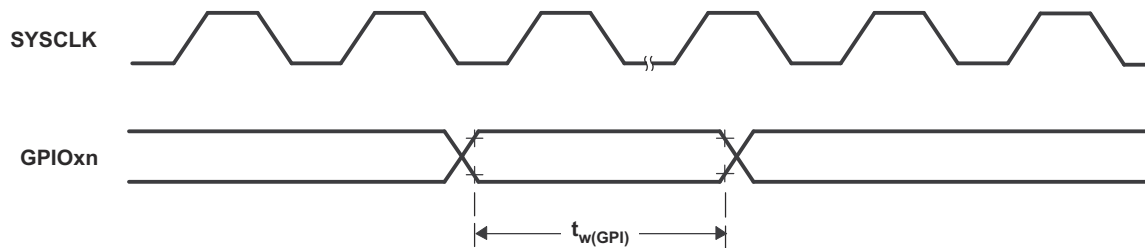


Figure 6-31. General-Purpose Input Timing

6.12.8 Interrupts

The C28x CPU has fourteen peripheral interrupt lines. Two of them (INT13 and INT14) are connected directly to CPU timers 1 and 2, respectively. The remaining twelve are connected to peripheral interrupt signals through the enhanced Peripheral Interrupt Expansion (ePIE) module. The ePIE multiplexes up to sixteen peripheral interrupts into each CPU interrupt line. It also expands the vector table to allow each interrupt to have its own ISR. This allows the CPU to support a large number of peripherals.

An interrupt path is divided into three stages—the peripheral, the ePIE, and the CPU. Each stage has its own enable and flag registers. This system allows the CPU to handle one interrupt while others are pending, implement and prioritize nested interrupts in software, and disable interrupts during certain critical tasks.

Figure 6-32 shows the interrupt architecture for this device.

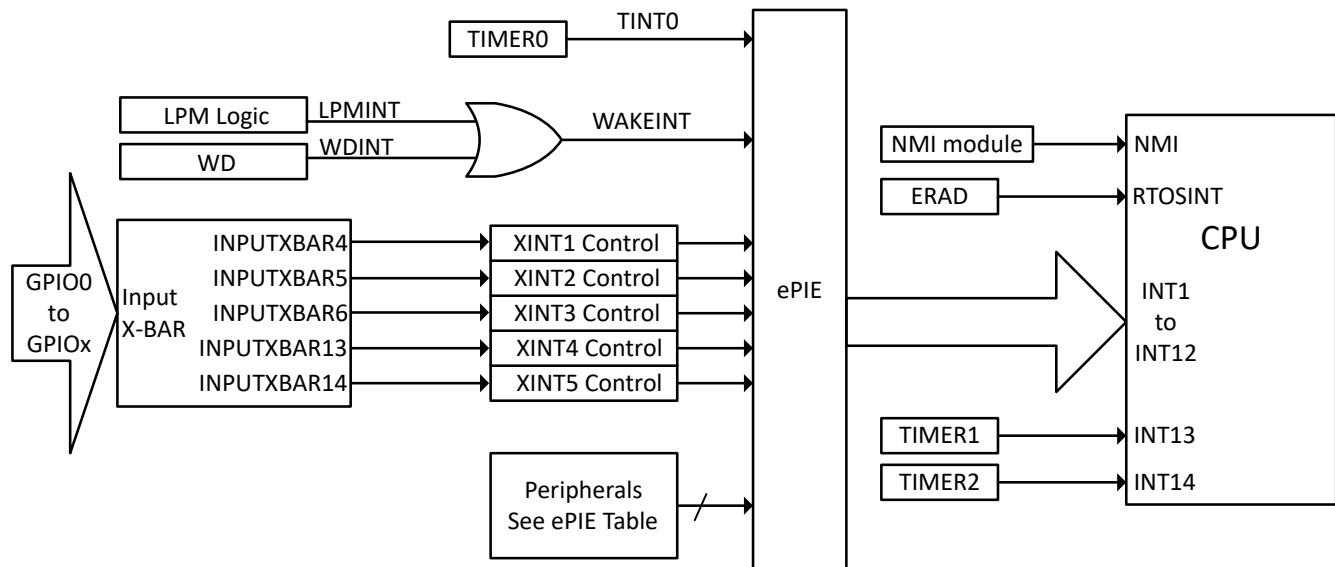


Figure 6-32. Device Interrupt Architecture

6.12.8.1 External Interrupt (XINT) Electrical Data and Timing

For an explanation of the input qualifier parameters, see the General-Purpose Input Timing Requirements table.

6.12.8.1.1 External Interrupt Timing Requirements

| | | | MIN | MAX | UNIT |
|--------------|------------------------------------|----------------|---|-----|--------|
| $t_{w(INT)}$ | Pulse duration, INT input low/high | Synchronous | $2t_{c(SYSCCLK)}$ | | cycles |
| | | With qualifier | $t_{w(IQSW)} + t_{w(SP)} + 1t_{c(SYSCCLK)}$ | | cycles |

6.12.8.1.2 External Interrupt Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | MAX | UNIT |
|--------------|---|----------------------------------|--|--------|
| $t_{d(INT)}$ | Delay time, INT low/high to interrupt-vector fetch ⁽¹⁾ | $t_{w(IQSW)} + 14t_{c(SYSCCLK)}$ | $t_{w(IQSW)} + t_{w(SP)} + 14t_{c(SYSCCLK)}$ | cycles |

(1) This assumes that the ISR is in a single-cycle memory.

6.12.8.1.3 External Interrupt Timing

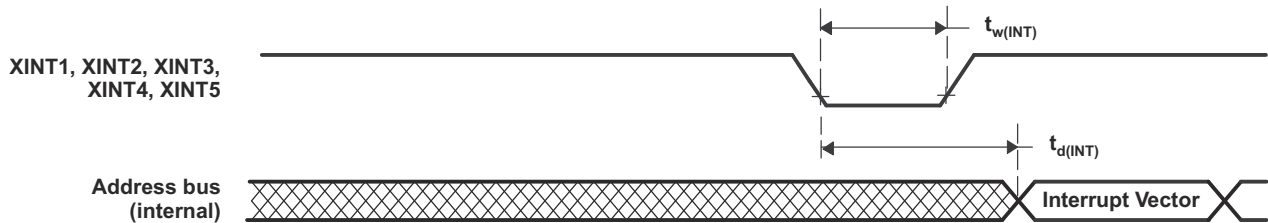


Figure 6-33. External Interrupt Timing

6.12.9 Low-Power Modes

This device has HALT, IDLE and STANDBY as clock-gating low-power modes.

Further details, as well as the entry and exit procedure, for all of the low-power modes can be found in the Low-Power Modes section of the [TMS320F28003x Real-Time Microcontrollers Technical Reference Manual](#).

6.12.9.1 Clock-Gating Low-Power Modes

IDLE and HALT modes on this device are similar to those on other C28x devices. [Table 6-9](#) describes the effect on the system when any of the clock-gating low-power modes are entered.

Table 6-9. Effect of Clock-Gating Low-Power Modes on the Device

| MODULES/ CLOCK DOMAIN | IDLE | STANDBY | HALT |
|---|---------|---------|--|
| SYSCLK | Active | Gated | Gated |
| CPUCLK | Gated | Gated | Gated |
| Clock to modules connected to PERx.SYSCLK | Active | Gated | Gated |
| WDCLK | Active | Active | Gated if CLKSRCCTL1.WDHALTI = 0 |
| PLL | Powered | Powered | Software must power down PLL before entering HALT. |
| INTOSC1 | Powered | Powered | Powered down if CLKSRCCTL1.WDHALTI = 0 |
| INTOSC2 | Powered | Powered | Powered down if CLKSRCCTL1.WDHALTI = 0 |
| Flash ⁽¹⁾ | Powered | Powered | Powered |
| XTAL ⁽²⁾ | Powered | Powered | Powered |

- (1) The Flash module is not powered down by hardware in any LPM. It may be powered down using software if required by the application. For more information, see the Flash and OTP Memory section of the System Control chapter in the [TMS320F28003x Real-Time Microcontrollers Technical Reference Manual](#).
- (2) The XTAL is not powered down by hardware in any LPM. It may be powered down by software setting the XTALCR.OSCOFF bit to 1. This can be done at any time during the application if the XTAL is not required.

6.12.9.2 Low-Power Mode Wake-up Timing

For an explanation of the input qualifier parameters, see the General-Purpose Input Timing Requirements table.

6.12.9.2.1 IDLE Mode Timing Requirements

| | | | MIN | MAX | UNIT |
|---------------|---|-------------------------|--------------------------------|-----|--------|
| $t_{w(WAKE)}$ | Pulse duration, external wake-up signal | Without input qualifier | $2t_{c(SYSCLK)}$ | | cycles |
| | | With input qualifier | $2t_{c(SYSCLK)} + t_{w(IQSW)}$ | | |

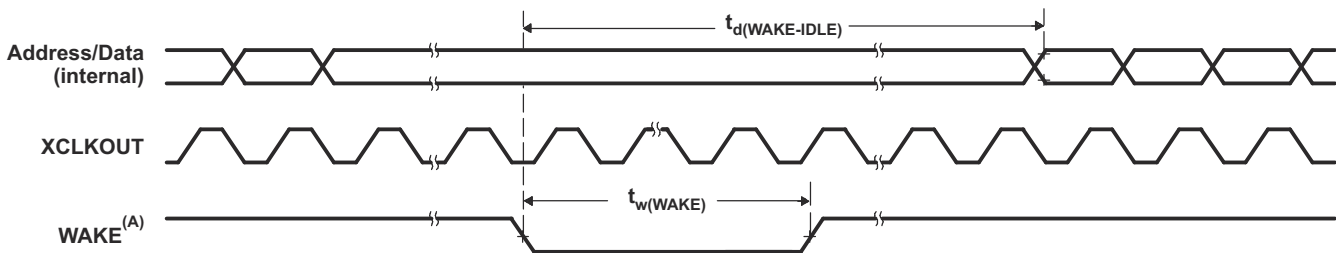
6.12.9.2.2 IDLE Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|--------------------|---|---------------------------|-------------------------|--|--------|
| $t_{d(WAKE-IDLE)}$ | Delay time, external wake signal to program execution resume ⁽¹⁾ | From Flash (active state) | Without input qualifier | $40t_{c(SYSCLK)}$ | cycles |
| | | | With input qualifier | $40t_{c(SYSCLK)} + t_{w(WAKE)}$ | cycles |
| | | From Flash (sleep state) | Without input qualifier | $9316t_{c(SYSCLK)}$ ⁽²⁾ | cycles |
| | | | With input qualifier | $9316t_{c(SYSCLK)}$ ⁽²⁾ + $t_{w(WAKE)}$ | cycles |
| | | From RAM | Without input qualifier | $25t_{c(SYSCLK)}$ | cycles |
| | | | With input qualifier | $25t_{c(SYSCLK)} + t_{w(WAKE)}$ | cycles |

- (1) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. Execution of an ISR (triggered by the wake-up signal) involves additional latency.
- (2) This value is based on the flash power-up time, which is a function of the SYSCLK frequency, flash wait states (RWAIT), and FPAC1[PSLEEP].

6.12.9.2.3 IDLE Entry and Exit Timing Diagram



- A. WAKE can be any enabled interrupt, \overline{WDINT} or XRSn. After the IDLE instruction is executed, a delay of five OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.

Figure 6-34. IDLE Entry and Exit Timing Diagram

6.12.9.2.4 STANDBY Mode Timing Requirements

| | | | MIN | MAX | UNIT |
|-------------------|---|---|-----------------------------------|-----|--------|
| $t_{w(WAKE-INT)}$ | Pulse duration, external wake-up signal | QUALSTDBY = 0 $2t_{c(OSCCLK)}$ | $3t_{c(OSCCLK)}$ | | cycles |
| | | QUALSTDBY > 0 $(2 + QUALSTDBY)t_{c(OSCCLK)}$ ⁽¹⁾ | $(2 + QUALSTDBY) * t_{c(OSCCLK)}$ | | |

(1) QUALSTDBY is a 6-bit field in the LPMCR register.

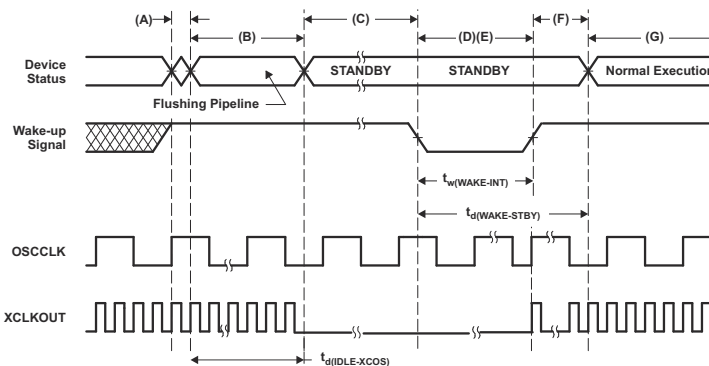
6.12.9.2.5 STANDBY Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|--------------------|--|-----|---|--------|
| $t_{d(IDLE-XCOS)}$ | Delay time, IDLE instruction executed to XCLKOUT stop | | $16t_{c(INTOSC1)}$ | cycles |
| $t_{d(WAKE-STBY)}$ | Wakeup from flash (Flash module in active state) | | $175t_{c(SYSCCLK)} + t_{w(WAKE-INT)}$ | cycles |
| $t_{d(WAKE-STBY)}$ | Delay time, external wake signal to program execution resume ⁽¹⁾ Wakeup from flash (Flash module in sleep state) | | $9316t_{c(SYSCCLK)}$ ⁽²⁾ + $t_{w(WAKE-INT)}$ | cycles |
| $t_{d(WAKE-STBY)}$ | Wakeup from RAM | | $3t_{c(OSC)} + 15t_{c(SYSCCLK)} + t_{w(WAKE-INT)}$ | cycles |

- (1) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. Execution of an ISR (triggered by the wake-up signal) involves additional latency.
(2) This value is based on the flash power-up time, which is a function of the SYSCCLK frequency, flash wait states (RWAIT), and FPAC1[PSLEEP].

6.12.9.2.6 STANDBY Entry and Exit Timing Diagram



- A. IDLE instruction is executed to put the device into STANDBY mode.
B. The LPM block responds to the STANDBY signal, SYSCCLK is held for a maximum 16 INTOSC1 clock cycles before being turned off. This delay enables the CPU pipeline and any other pending operations to flush properly.
C. Clock to the peripherals are turned off. However, the PLL and watchdog are not shut down. The device is now in STANDBY mode. After the IDLE instruction is executed, a delay of five OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.
D. The external wake-up signal is driven active.
E. The wake-up signal fed to a GPIO pin to wake up the device must meet the minimum pulse width requirement. Furthermore, this signal must be free of glitches. If a noisy signal is fed to a GPIO pin, the wake-up behavior of the device will not be deterministic and the device may not exit low-power mode for subsequent wake-up pulses.
F. After a latency period, the STANDBY mode is exited.
G. Normal execution resumes. The device will respond to the interrupt (if enabled).

Figure 6-35. STANDBY Entry and Exit Timing Diagram

6.12.9.2.7 HALT Mode Timing Requirements

| | | MIN | MAX | UNIT |
|---------------------------|---|--|-----|--------|
| $t_{w(\text{WAKE-GPIO})}$ | Pulse duration, GPIO wake-up signal ⁽¹⁾ | $t_{\text{oscst}} + 2t_{c(\text{OSCCLK})}$ | | cycles |
| $t_{w(\text{WAKE-XRS})}$ | Pulse duration, $\overline{\text{XRS}}$ wake-up signal ⁽¹⁾ | $t_{\text{oscst}} + 8t_{c(\text{OSCCLK})}$ | | cycles |

- (1) For applications using X1/X2 for OSCCLK, the user must characterize their specific oscillator start-up time as it is dependent on circuit/layout external to the device. See *Crystal Oscillator (XTAL)* section for more information. For applications using INTOSC1 or INTOSC2 for OSCCLK, see the Internal Oscillators section for t_{oscst} . Oscillator start-up time does not apply to applications using a single-ended crystal on the X1 pin, as it is powered externally to the device.

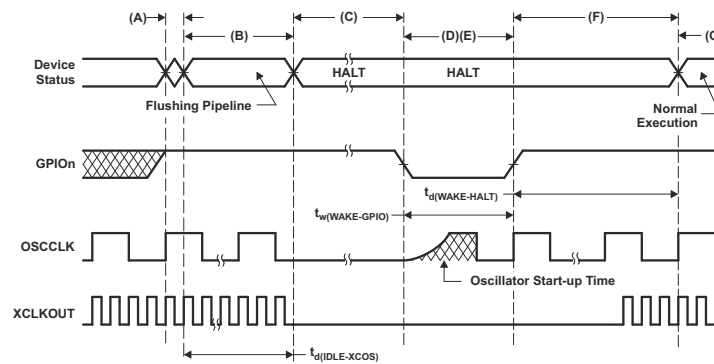
6.12.9.2.8 HALT Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | MAX | UNIT |
|---------------------------|---|-----|--|--------|
| $t_{d(\text{IDLE-XCOS})}$ | Delay time, IDLE instruction executed to XCLKOUT stop | | $16t_{c(\text{INTOSC1})}$ | cycles |
| $t_{d(\text{WAKE-HALT})}$ | Delay time, external wake signal end to CPU1 program execution resume | | | cycles |
| | Wakeup from Flash - Flash module in active state | | $75t_{c(\text{OSCCLK})}$ | |
| | Wakeup from Flash - Flash module in sleep state | | $9316t_{c(\text{SYSCLK})} + 75t_{c(\text{OSCCLK})}$ ⁽¹⁾ | |
| | Wakeup from RAM | | $75t_{c(\text{OSCCLK})}$ | |

- (1) This value is based on the flash power-up time, which is a function of the SYSCLK frequency, flash wait states (RWAIT), and FPAC1[PSLEEP].

6.12.9.2.9 HALT Entry and Exit Timing Diagram



- A. IDLE instruction is executed to put the device into HALT mode.
- B. The LPM block responds to the HALT signal, SYSCLK is held for a maximum 16 INTOSC1 clock cycles before being turned off. This delay enables the CPU pipeline and any other pending operations to flush properly.
- C. Clocks to the peripherals are turned off and the PLL is shut down. If a quartz crystal or ceramic resonator is used as the clock source, the internal oscillator is shut down as well. The device is now in HALT mode and consumes very little power. It is possible to keep the zero-pin internal oscillators (INTOSC1 and INTOSC2) and the watchdog alive in HALT MODE. This is done by writing 1 to CLKSRCCTL1.WDHALTI. After the IDLE instruction is executed, a delay of five OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.
- D. When the GPIOin pin (used to bring the device out of HALT) is driven low, the oscillator is turned on and the oscillator wake-up sequence is initiated. The GPIO pin should be driven high only after the oscillator has stabilized. This enables the provision of a clean clock signal during the PLL lock sequence. Because the falling edge of the GPIO pin asynchronously begins the wake-up procedure, care should be taken to maintain a low noise environment before entering and during HALT mode.
- E. The wake-up signal fed to a GPIO pin to wake up the device must meet the minimum pulse width requirement. Furthermore, this signal must be free of glitches. If a noisy signal is fed to a GPIO pin, the wake-up behavior of the device will not be deterministic and the device may not exit low-power mode for subsequent wake-up pulses.
- F. When CLKIN to the core is enabled, the device will respond to the interrupt (if enabled), after some latency. The HALT mode is now exited.
- G. Normal operation resumes.
- H. The user must relock the PLL upon HALT wakeup to ensure a stable PLL lock.

Figure 6-36. HALT Entry and Exit Timing Diagram

6.13 Analog Peripherals

The analog subsystem module is described in this section.

The analog modules on this device include the ADC, temperature sensor, CMPSS, and buffered DAC.

The analog subsystem has the following features:

- Flexible voltage references
 - The ADCs are referenced to VREFHx and VSSA pins
 - VREFHx pin voltage can be driven in externally or can be generated by an internal bandgap voltage reference
 - The internal voltage reference range can be selected to be 0 V to 3.3 V or 0 V to 2.5 V
 - The buffered DACs are referenced to VREFHx and VSSA
 - Alternately, these DACs can be referenced to the VDAC pin and VSSA
 - The comparator DACs are referenced to VDDA and VSSA
 - Alternately, these DACs can be referenced to the VDAC pin and VSSA
- Flexible pin usage
 - Buffered DAC outputs, comparator subsystem inputs, and digital inputs (AIOs)/outputs (AGPIOs) are multiplexed with ADC inputs
 - Internal connection to V_{REFLO} on all ADCs for offset self-calibration

[Figure 6-37](#) shows the Analog Subsystem Block Diagram for the 100-pin PZ LQFP.

[Figure 6-38](#) shows the Analog Subsystem Block Diagram for the 80-pin PN LQFP.

[Figure 6-39](#) shows the Analog Subsystem Block Diagram for the 64-pin PM LQFP.

[Figure 6-40](#) shows the Analog Subsystem Block Diagram for the 48-pin PT LQFP.

[Figure 6-41](#) shows the analog group connections. [Section 6.13.1](#) lists the analog pins and internal connections. [Section 6.13.2](#) lists descriptions of analog signals.

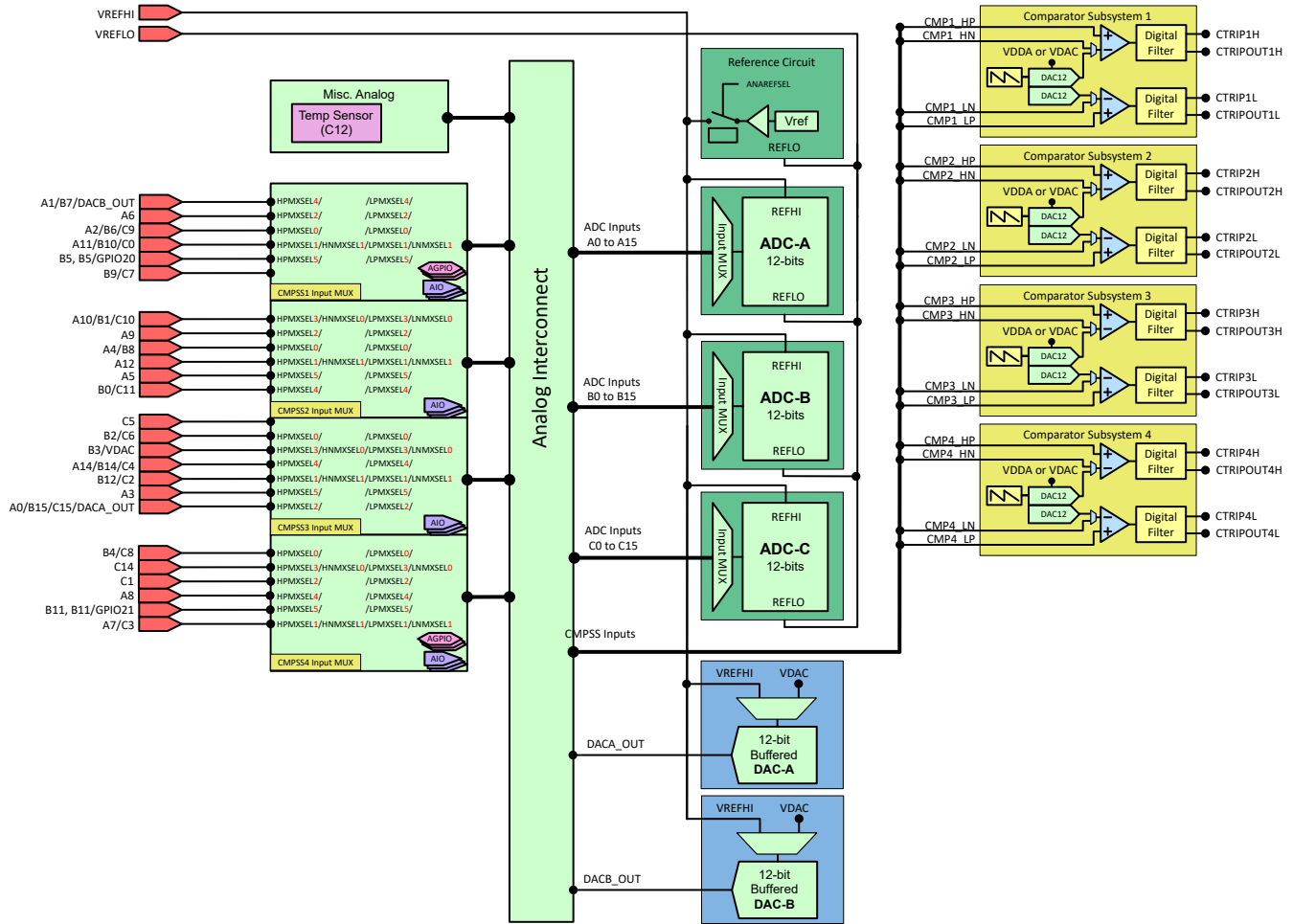


Figure 6-37. Analog Subsystem Block Diagram (100-Pin PZ LQFP)

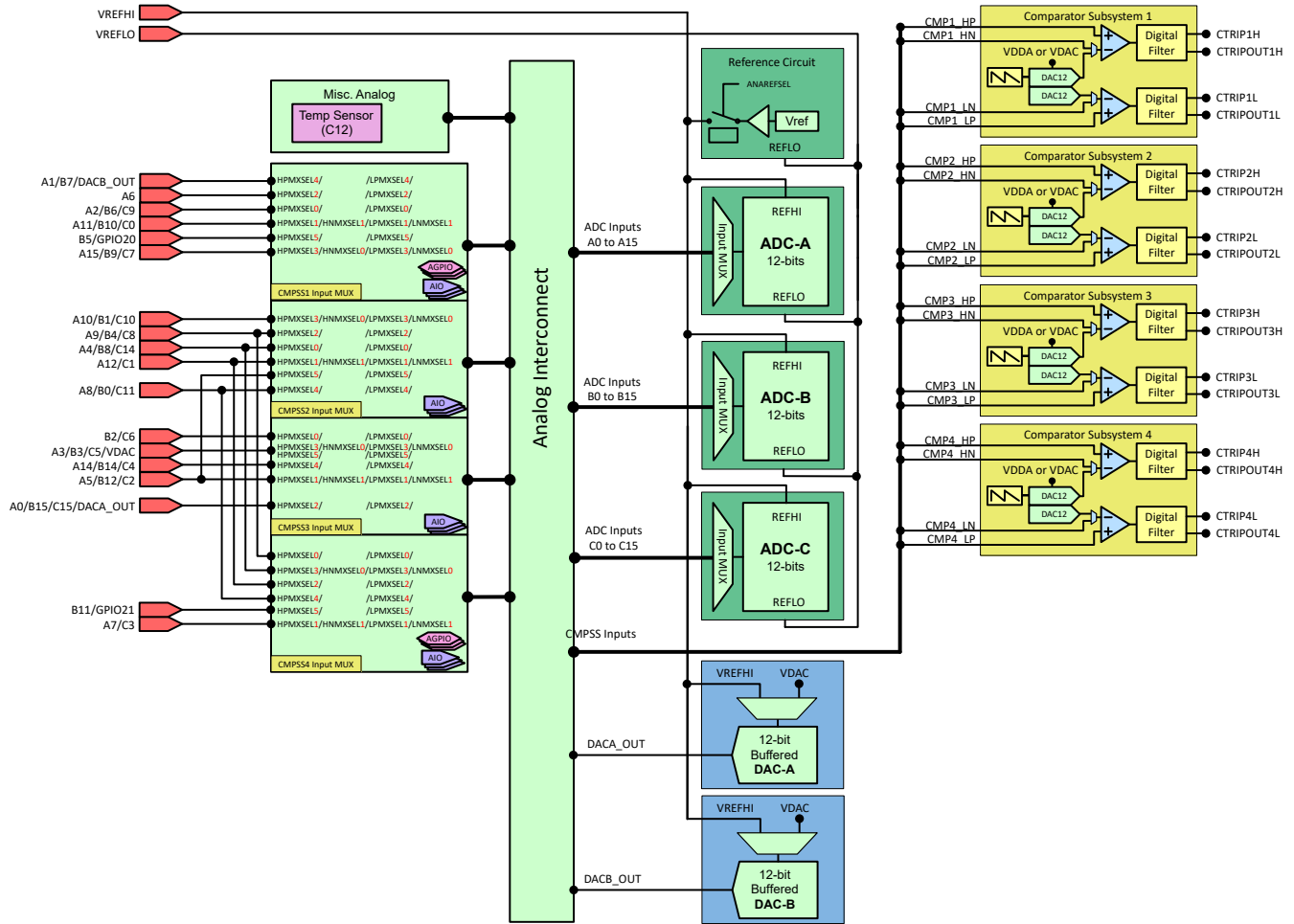


Figure 6-38. Analog Subsystem Block Diagram (80-Pin PN LQFP)

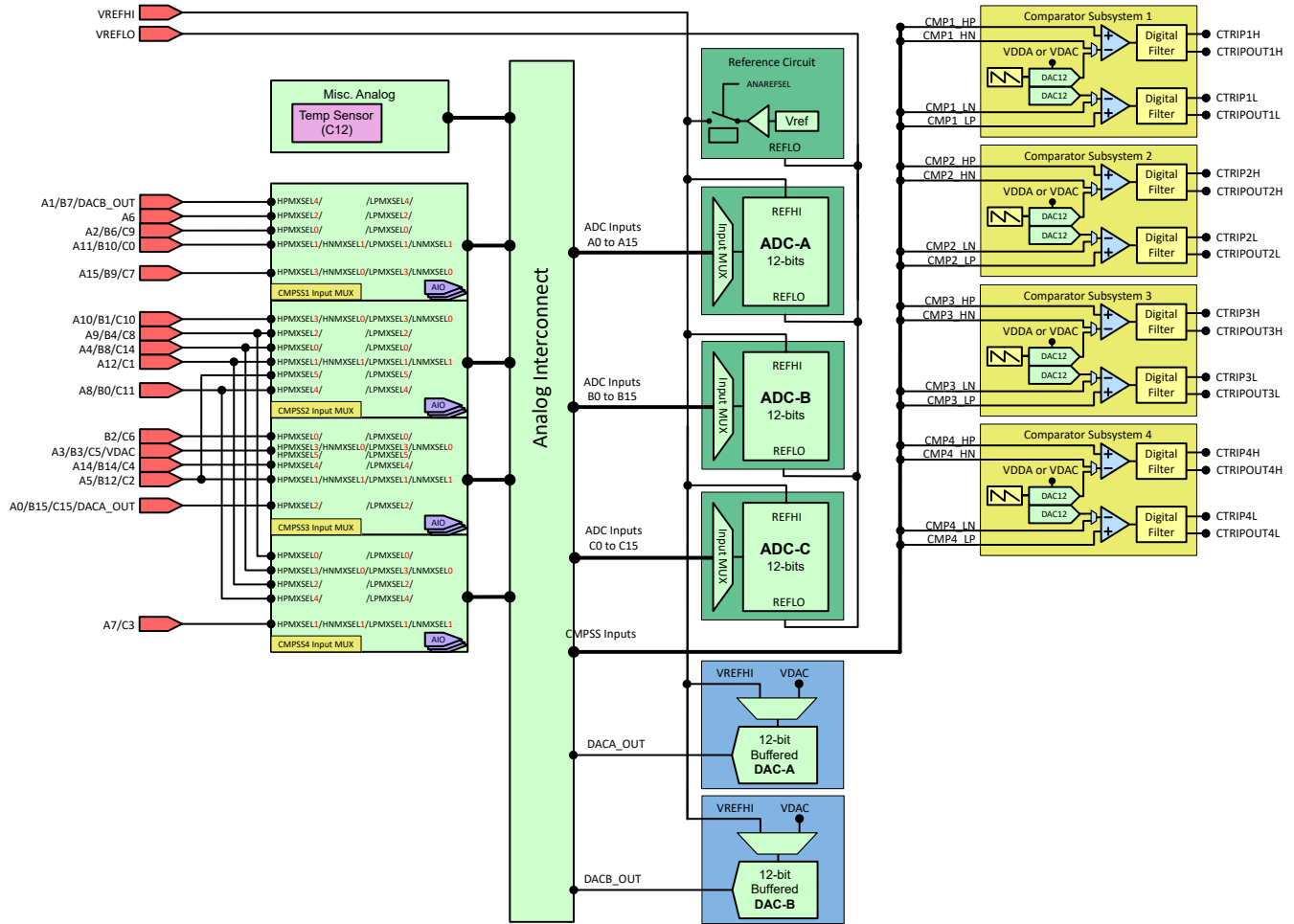


Figure 6-39. Analog Subsystem Block Diagram (64-Pin PM LQFP)

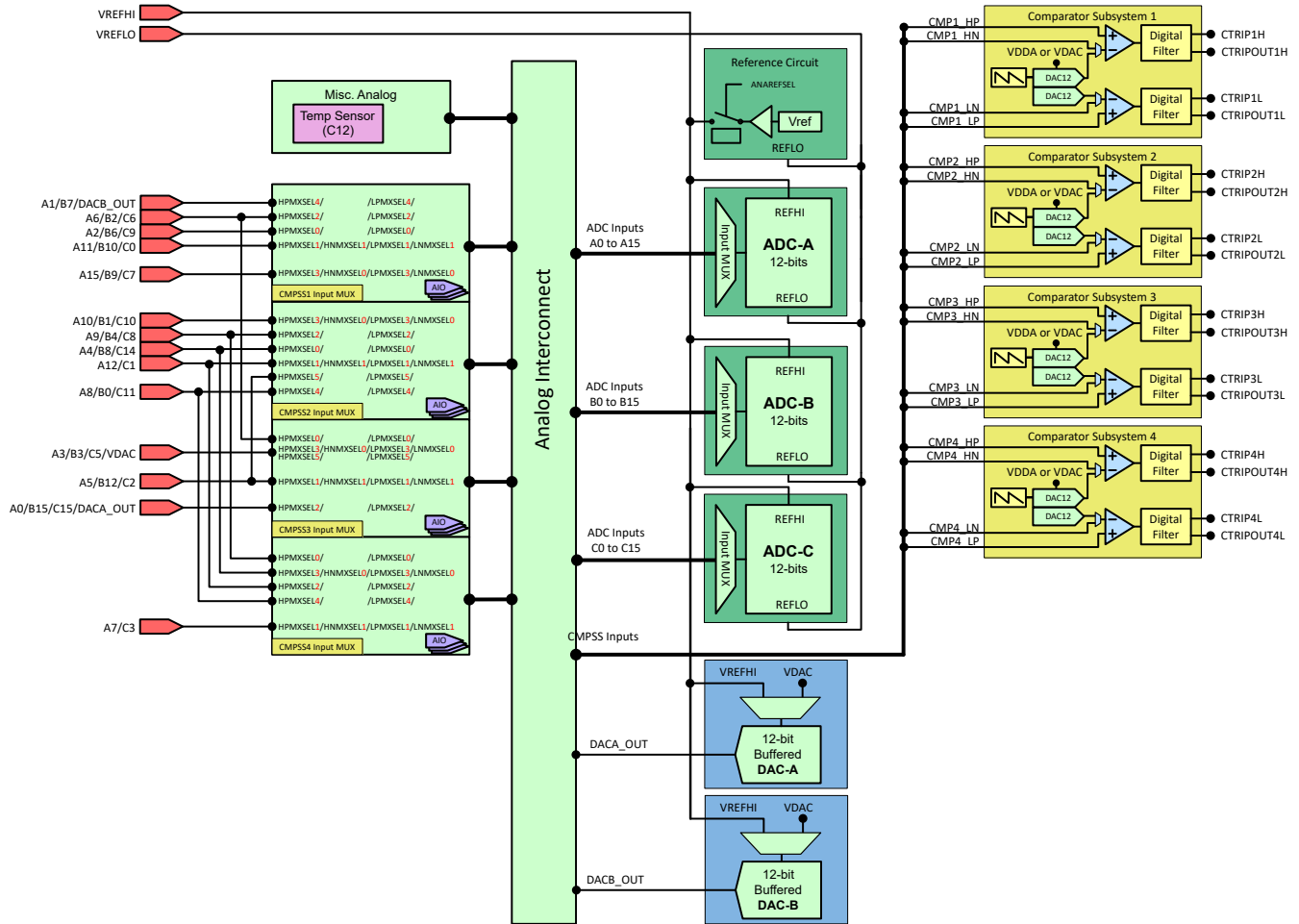
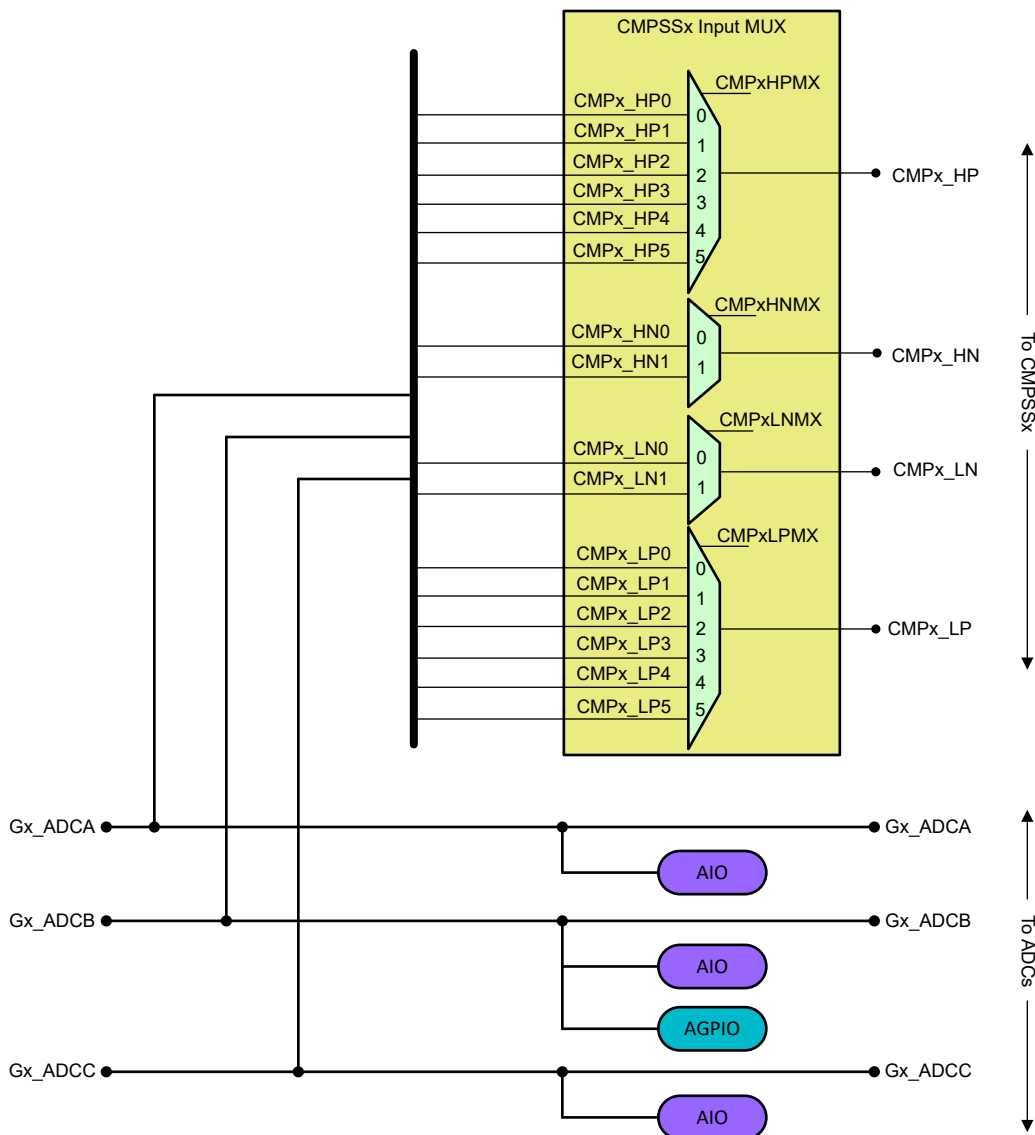


Figure 6-40. Analog Subsystem Block Diagram (48-Pin PT LQFP)



A. AIOs support digital input mode only.

Figure 6-41. Analog Group Connections

6.13.1 Analog Pins and Internal Connections

Table 6-10. Analog Pins and Internal Connections

| Pin Name | Package Pin | | | | ADC | | | Comparator Subsystem (MUX) | | | | AIO Input | |
|----------------------------------|-------------|-------|-------|------------------|-----|-----|-----|----------------------------|------------------|------------------|------------------|------------------|------------------|
| | 100 PZ | 80 PN | 64 PM | 48 PT | A | B | C | High Positive | High Negative | Low Positive | Low Negative | | |
| VREFHI | 24, 25 | 20 | 16 | 12 | | | | | | | | | |
| VREFLO | 26, 27 | 21 | 17 | 13 | A13 | B13 | C13 | | | | | | |
| Analog Group 1 | | | | | | | | CMP1 | | | | | |
| A6 | 14 | 10 | 6 | 4 ⁽¹⁾ | A6 | - | - | CMP1 (HPMXSEL=2) | | CMP1 (LPMXSEL=2) | | AIO228 | |
| A2/B6/C9 | 17 | 13 | 9 | 6 | A2 | B6 | C9 | CMP1 (HPMXSEL=0) | | CMP1 (LPMXSEL=0) | | AIO224 | |
| A15 | - | 14 | 10 | 7 | A15 | - | - | CMP1 (HPMXSEL=3) | CMP1 (HNMXSEL=0) | CMP1 (LPMXSEL=3) | CMP1 (LNMXSEL=0) | AIO233 | |
| B9/C7 | 18 | | | | - | B9 | C7 | | | | | | |
| A11/B10/C0 | 20 | 16 | 12 | 8 | A11 | B10 | C0 | CMP1 (HPMXSEL=1) | CMP1 (HNMXSEL=1) | CMP1 (LPMXSEL=1) | CMP1 (LNMXSEL=1) | AIO237 | |
| A1/B7/DACB_OUT | 22 | 18 | 14 | 10 | A1 | B7 | - | CMP1 (HPMXSEL=4) | | CMP1 (LPMXSEL=4) | | AIO232 | |
| Analog Group 2 | | | | | | | | CMP2 | | | | | |
| A10/B1/C10 | 40 | 29 | 25 | 21 | A10 | B1 | C10 | CMP2 (HPMXSEL=3) | CMP2 (HNMXSEL=0) | CMP2 (LPMXSEL=3) | CMP2 (LNMXSEL=0) | AIO230 | |
| Analog Group 3 | | | | | | | | CMP3 | | | | | |
| B2/C6 | 15 | 11 | 7 | 4 ⁽¹⁾ | - | B2 | C6 | CMP3 (HPMXSEL=0) | | CMP3 (LPMXSEL=0) | | AIO226 | |
| B3/VDAC ⁽²⁾ | 16 | 12 | 8 | 5 | - | B3 | - | CMP3 (HPMXSEL=3) | CMP3 (HNMXSEL=0) | CMP3 (LPMXSEL=3) | CMP3 (LNMXSEL=0) | AIO242 | |
| C5 | 28 | | | | - | - | C5 | | | | | | |
| A3 | - | | | | - | - | - | A3 | - | - | CMP3 (HPMXSEL=5) | | CMP3 (LPMXSEL=5) |
| A14/B14/C4 | 19 | 15 | 11 | - | A14 | B14 | C4 | CMP3 (HPMXSEL=4) | | CMP3 (LPMXSEL=4) | | AIO239 | |
| A0/B15/C15/DACA_OUT | 23 | 19 | 15 | 11 | A0 | B15 | C15 | CMP3 (HPMXSEL=2) | | CMP3 (LPMXSEL=2) | | AIO231 | |
| Analog Group 4 | | | | | | | | CMP4 | | | | | |
| A7/C3 | 31 | 23 | 19 | 15 | A7 | - | C3 | CMP4 (HPMXSEL=1) | CMP4 (HNMXSEL=1) | CMP4 (LPMXSEL=1) | CMP4 (LNMXSEL=1) | AIO245 | |
| Combined Analog Group 2/3 | | | | | | | | CMP2/3 | | | | | |
| A5 | 35 | - | - | - | A5 | - | - | CMP2 (HPMXSEL=5) | | CMP2 (LPMXSEL=5) | | AIO249 | |
| B12/C2 | 21 | 17 | 13 | 9 | - | B12 | C2 | CMP3 (HPMXSEL=1) | CMP3 (HNMXSEL=1) | CMP3 (LPMXSEL=1) | CMP3 (LNMXSEL=1) | AIO244 | |
| Combined Analog Group 2/4 | | | | | | | | CMP2/4 | | | | | |
| A12 | 28 | 22 | 18 | 14 | A12 | - | - | CMP2 (HPMXSEL=1) | CMP2 (HNMXSEL=1) | CMP2 (LPMXSEL=1) | CMP2 (LNMXSEL=1) | AIO238 | |
| C1 | 29 | | | | - | - | C1 | | | CMP4 (HPMXSEL=2) | | CMP4 (LPMXSEL=2) | |

Table 6-10. Analog Pins and Internal Connections (continued)

| Pin Name | Package Pin | | | | ADC | | | Comparator Subsystem (MUX) | | | | AIO Input |
|---------------------------|-------------|-------|-------|-------|-----|-----|-----|----------------------------|---------------|------------------|------------------|------------------|
| | 100 PZ | 80 PN | 64 PM | 48 PT | A | B | C | High Positive | High Negative | Low Positive | Low Negative | |
| A8 | 37 | - | - | - | A8 | - | - | CMP4 (HPMXSEL=4) | | CMP4 (LPMXSEL=4) | | AIO240 |
| | - | 24 | 20 | 16 | | - | - | | | | | AIO241 |
| B0/C11 | - | 24 | 20 | 16 | - | B0 | C11 | CMP2 (HPMXSEL=4) | | CMP2 (LPMXSEL=4) | | AIO253 |
| | 41 | | | | - | | | | | | | - |
| A4/B8 | 36 | 27 | 23 | 19 | A4 | B8 | - | CMP2 (HPMXSEL=0) | | CMP2 (LPMXSEL=0) | | AIO225 |
| C14 | - | | | | - | - | - | - | - | C14 | CMP4 (HPMXSEL=3) | CMP4 (HNMXSEL=0) |
| | 42 | - | - | - | - | - | - | - | - | - | - | AIO227 |
| A9 | 38 | 28 | 24 | 20 | A9 | - | - | CMP2 (HPMXSEL=2) | | CMP2 (LPMXSEL=2) | | AIO227 |
| B4/C8 | 39 | | | | - | B4 | C8 | CMP4 (HPMXSEL=0) | | CMP4 (LPMXSEL=0) | | AIO236 |
| Other Analog | | | | | | | | | | | | |
| B5 | 32 | - | - | - | - | B5 | - | CMP1 (HPMXSEL=5) | | CMP1 (LPMXSEL=5) | | AIO252 |
| B5/GPIO20 ⁽³⁾ | 48 | 33 | - | - | - | | - | | | | | GPIO20 |
| B11 | 30 | - | - | - | - | B11 | - | CMP4 (HPMXSEL=5) | | CMP4 (LPMXSEL=5) | | AIO251 |
| B11/GPIO21 ⁽³⁾ | 49 | 34 | - | - | - | | - | | | | | GPIO21 |
| TempSensor ⁽⁴⁾ | - | - | - | - | - | - | C12 | | | | | |

- (1) A6 and C6 is double bonded as pin # 4.
- (2) Optional external reference voltage for on-chip COMPDACs/GPDACs. There is an internal capacitance to VSSA on this pin whether used for ADC input or COMPDAC/GPDAC reference. If used as a VDAC reference, place at least a 1-μF capacitor on this pin.
- (3) The GPIOs on these analog pins support full digital input and output functionality and are referred to as AGPIOs. By default, the AGPIOs are unconnected; that is, the analog and digital functions are both disabled. For configuration details, see the *Digital Inputs and Outputs on ADC Pins (AGPIOs)* section.
- (4) Internal connection only; does not come to a device pin.

6.13.2 Analog Signal Descriptions

Table 6-11. Analog Signal Descriptions

| Signal Name | Description |
|-------------|---|
| AIOx | Digital input on ADC pin |
| GPIOx | Digital input/output pin with ADC functionality |
| Ax | ADC A Input |
| Bx | ADC B Input |
| Cx | ADC C Input |
| CMPx_DACH | Comparator subsystem high DAC output |
| CMPx_DACL | Comparator subsystem low DAC output |
| CMPx_HNy | Comparator subsystem high comparator negative input |
| CMPx_HPy | Comparator subsystem high comparator positive input |
| CMPx_LNy | Comparator subsystem low comparator negative input |
| CMPx_LPy | Comparator subsystem low comparator positive input |
| DACx_OUT | Buffered DAC Output |
| TempSensor | Internal temperature sensor |
| VDAC | Optional external reference voltage for on-chip COMPDACs. This pin has a higher capacitance compared to the other analog pins. See the <i>Per-Channel Parasitic Capacitance</i> table for details. This capacitance is present whether the pin is being used for ADC input or COMPDAC/GPDAC reference and cannot be disabled. If this pin is being used as a reference for the on-chip COMPDAC/GPDACs, place at least a 1- μ F capacitor on this pin. |

6.13.3 Analog-to-Digital Converter (ADC)

The ADC module described here is a successive approximation (SAR) style ADC with resolution of 12 bits. This section refers to the analog circuits of the converter as the “core,” and includes the channel-select MUX, the sample-and-hold (S/H) circuit, the successive approximation circuits, voltage reference circuits, and other analog support circuits. The digital circuits of the converter are referred to as the “wrapper” and include logic for programmable conversions, result registers, interfaces to analog circuits, interfaces to the peripheral buses, post-processing circuits, and interfaces to other on-chip modules.

Each ADC module consists of a single sample-and-hold (S/H) circuit. The ADC module is designed to be duplicated multiple times on the same chip, allowing simultaneous sampling or independent operation of multiple ADCs. The ADC wrapper is start-of-conversion (SOC)-based (see the SOC Principle of Operation section of the Analog-to-Digital Converter (ADC) chapter in the [TMS320F28003x Real-Time Microcontrollers Technical Reference Manual](#)).

Each ADC has the following features:

- Resolution of 12 bits
- Ratiometric external reference set by VREFHI/VREFLO
- Selectable internal reference of 2.5 V or 3.3 V
- Single-ended signal mode
- Input multiplexer with up to 16 channels
- 16 configurable SOCs
- 16 individually addressable result registers
- Multiple trigger sources
 - Software immediate start
 - All ePWMs: ADCSOC A or B
 - GPIO XINT2
 - CPU Timers 0/1/2
 - ADCINT1/2
- Four flexible PIE interrupts
- Burst-mode triggering option
- Four post-processing blocks, each with:
 - Saturating offset calibration
 - Error from setpoint calculation
 - High, low, and zero-crossing compare, with interrupt and ePWM trip capability
 - Trigger-to-sample delay capture

Note

Not every channel can be pinned out from all ADCs. See the Pin Configuration and Functions section to determine which channels are available.

The block diagram for the ADC core and ADC wrapper are shown in Figure 6-42.

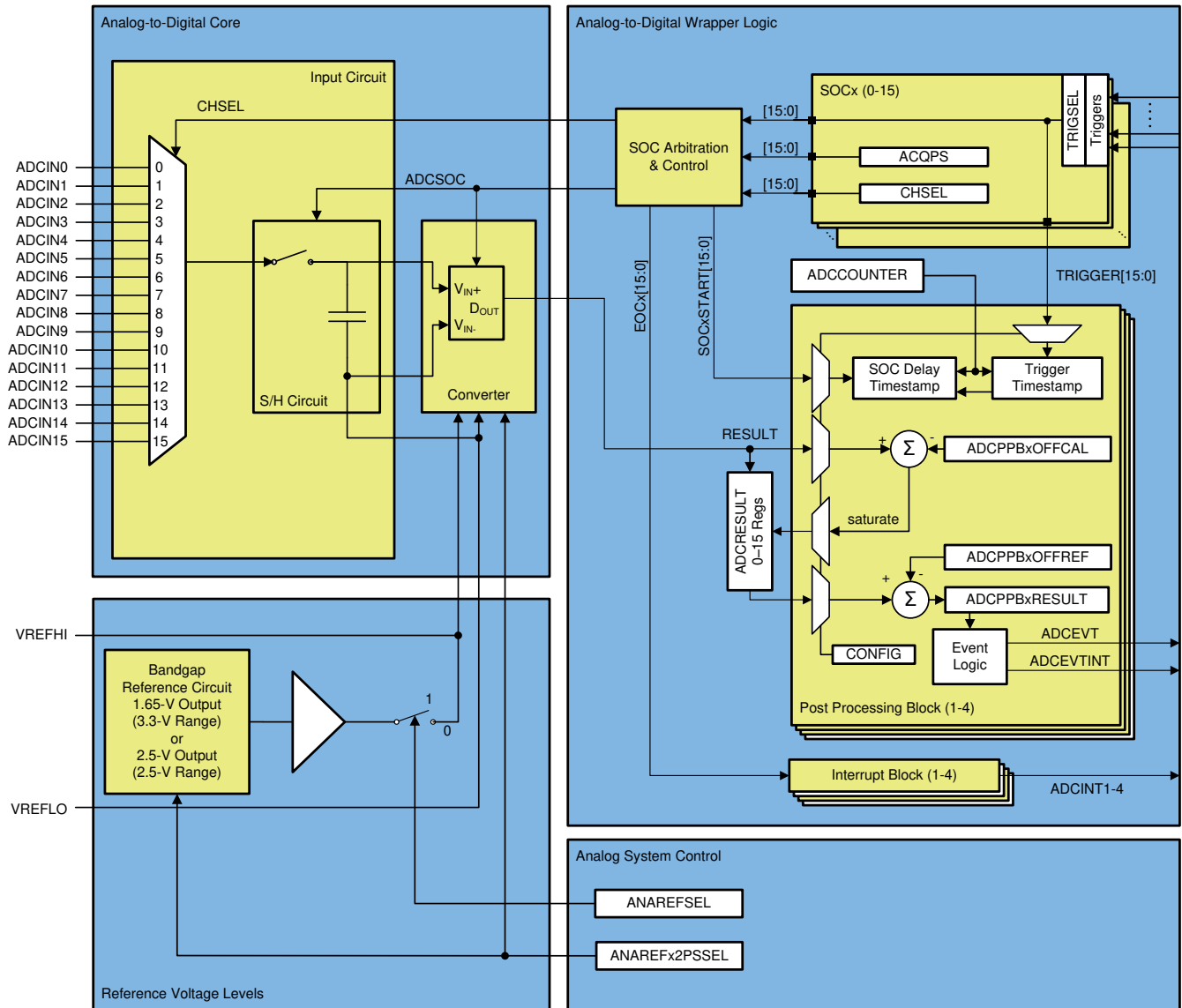


Figure 6-42. ADC Module Block Diagram

6.13.3.1 ADC Configurability

Some ADC configurations are individually controlled by the SOCs, while others are globally controlled per ADC module. Table 6-12 summarizes the basic ADC options and their level of configurability.

Table 6-12. ADC Options and Configuration Levels

| OPTIONS | CONFIGURABILITY |
|-----------------------------|--|
| Clock | Per module ⁽¹⁾ |
| Resolution | Not configurable (12-bit resolution only) |
| Signal mode | Not configurable (single-ended signal mode only) |
| Reference voltage source | Either external or internal for all modules |
| Trigger source | Per SOC ⁽¹⁾ |
| Converted channel | Per SOC |
| Acquisition window duration | Per SOC ⁽¹⁾ |
| EOC location | Per module |
| Burst mode | Per module ⁽¹⁾ |

- (1) Writing these values differently to different ADC modules could cause the ADCs to operate asynchronously. For guidance on when the ADCs are operating synchronously or asynchronously, see the Ensuring Synchronous Operation section of the Analog-to-Digital Converter (ADC) chapter in the *TMS320F28003x Real-Time Microcontrollers Technical Reference Manual*.

6.13.3.1.1 Signal Mode

The ADC supports single-ended signaling. The input voltage to the converter is sampled through a single pin (ADCINx), referenced to VREFLO.

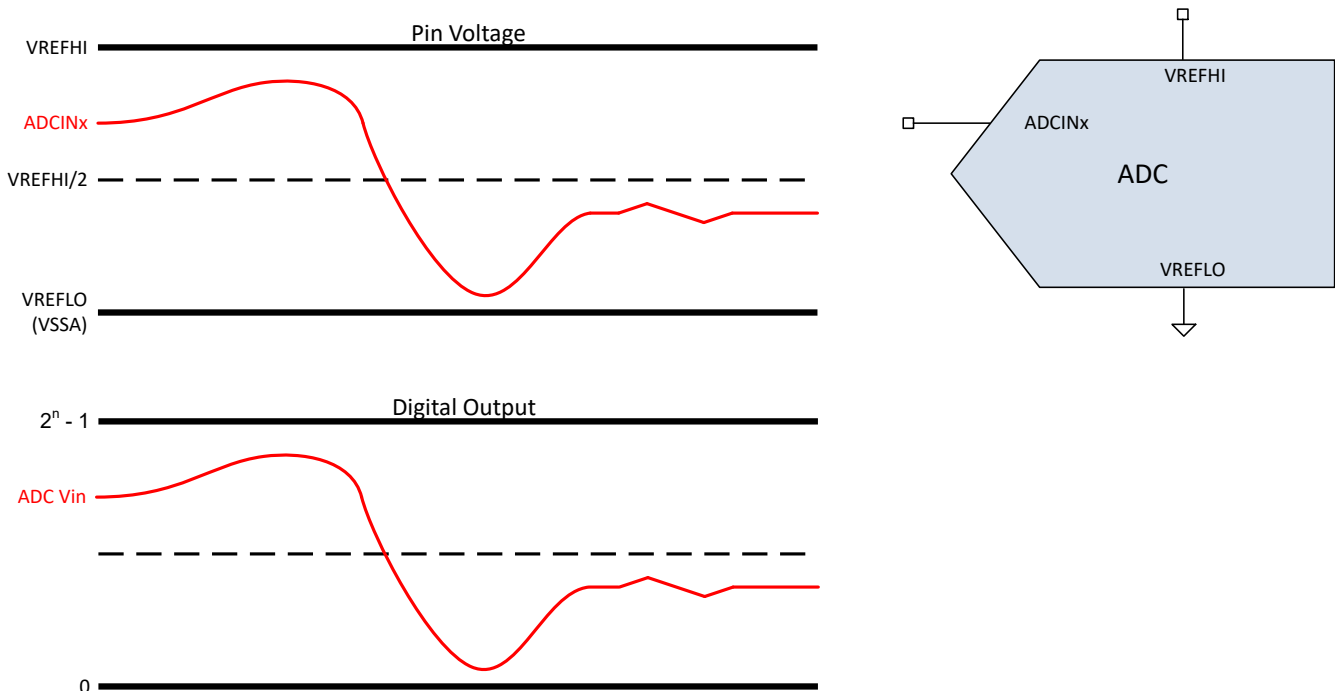


Figure 6-43. Single-ended Signaling Mode

6.13.3.2 ADC Electrical Data and Timing

Note

The ADC inputs should be kept below $V_{DDA} + 0.3$ V. If an ADC input goes above this level, ADC disturbances to other channels may occur by two mechanisms:

- ADC input overvoltage will overdrive the CMPSS mux, disturbing all other channels which share a common CMPSS mux. This disturbance will be continuous regardless of if the overvoltage input is sampled by the ADC
- When the ADC samples the overvoltage ADC input, V_{REFHI} will be pulled up to a higher level. This will disturb subsequent ADC conversions on any channel until the V_{REF} stabilizes

Note

The V_{REFHI} pin must be kept below $V_{DDA} + 0.3$ V to ensure proper functional operation. If the V_{REFHI} pin exceeds this level, a blocking circuit may activate, and the internal value of V_{REFHI} may float to 0 V internally, giving improper ADC conversion.

6.13.3.2.1 ADC Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|-----------|-------------|-------------|------|
| ADCCLK (derived from PERx.SYSCLK) | | 5 | | 60 | MHz |
| Sample rate | 120-MHz SYSCLK | | | 4 | MSPS |
| | 120-MHz SYSCLK (AGPIO Pin) | | | 3.75 | MSPS |
| Sample window duration (set by ACQPS and PERx.SYSCLK) ⁽¹⁾ | With 50 Ω or less R_s | 75 | | | ns |
| | With 50 Ω or less R_s (AGPIO Pin) | 90 | | | ns |
| V_{REFHI} | External Reference | 2.4 | 2.5 or 3.0 | V_{DDA} | V |
| V_{REFHI} ⁽²⁾ | Internal Reference = 3.3V Range | | 1.65 | | V |
| | Internal Reference = 2.5V Range | | 2.5 | | V |
| V_{REFLO} | | V_{SSA} | | V_{SSA} | V |
| $V_{REFHI} - V_{REFLO}$ | | 2.4 | | V_{DDA} | V |
| Conversion range | Internal Reference = 3.3 V Range | 0 | | 3.3 | V |
| | Internal Reference = 2.5 V Range | 0 | | 2.5 | V |
| | External Reference | | V_{REFLO} | V_{REFHI} | V |

(1) The sample window must also be at least as long as 1 ADCCLK cycle for correct ADC operation.

(2) In internal reference mode, the reference voltage is driven out of the V_{REFHI} pin by the device. The user should not drive a voltage into the pin in this mode.

6.13.3.2.2 ADC Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|------|---------------|------|---------|
| General | | | | | |
| ADCCLK Conversion Cycles | 120-MHz SYSCLK | 10.1 | | 11 | ADCCLKs |
| Power Up Time | External Reference mode | | | 500 | μs |
| | Internal Reference mode | | | 5000 | μs |
| | Internal Reference mode, when switching between 2.5-V range and 3.3-V range. | | | 5000 | μs |
| VREFHI input current ⁽¹⁾ | | | 130 | | μA |
| Internal Reference Capacitor Value ⁽²⁾ | | 2.2 | | | μF |
| External Reference Capacitor Value ⁽²⁾ | | 2.2 | | | μF |
| DC Characteristics | | | | | |
| Gain Error | Internal reference | -45 | | 45 | LSB |
| | External reference | -5 | ±3 | 5 | |
| Offset Error | | -5 | ±2 | 5 | LSB |
| Channel-to-Channel Gain Error ⁽⁴⁾ | | | 2 | | LSB |
| Channel-to-Channel Offset Error ⁽⁴⁾ | | | 2 | | LSB |
| ADC-to-ADC Gain Error ⁽⁵⁾ | Identical VREFHI and VREFLO for all ADCs | | 4 | | LSB |
| ADC-to-ADC Offset Error ⁽⁵⁾ | Identical VREFHI and VREFLO for all ADCs | | 2 | | LSB |
| DNL Error | | >-1 | ±0.5 | 1 | LSB |
| INL Error | | -2 | ±1.0 | 2 | LSB |
| ADC-to-ADC Isolation | VREFHI = 2.5 V, synchronous ADCs | -1 | | 1 | LSBs |
| AC Characteristics | | | | | |
| SNR ⁽³⁾ | External VREFHI/Internal VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1 | | 70.5 | | dB |
| | Internal VREFHI = 1.65 V (0 to 3.3 V range), fin = 100 kHz, SYSCLK from X1 | | 68.2 | | |
| | External/Internal VREFHI, fin = 100 kHz, SYSCLK from INTOSC | | 60.1 | | dB |
| THD ⁽³⁾ | External VREFHI/Internal VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1 | | -85.0 | | dB |
| | Internal VREFHI = 1.65 V (0 to 3.3 V range), fin = 100 kHz, SYSCLK from X1 | | -82.3 | | dB |
| SFDR ⁽³⁾ | External/Internal VREFHI, fin = 100 kHz | | 79.2 | | dB |
| SINAD ⁽³⁾ | External VREFHI/Internal VREFHI = 2.5V, fin = 100 kHz, SYSCLK from X1 | | 70.4 | | dB |
| | Internal VREFHI = 1.65 V (0 to 3.3 V range), fin = 100 kHz, SYSCLK from X1 | | 68.0 | | |
| | External/Internal VREFHI, fin = 100 kHz, SYSCLK from INTOSC | | 60.0 | | dB |
| ENOB ⁽³⁾ | External VREFHI/Internal VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, single and synchronous ADCs | | 11.4 | | bits |
| | Internal VREFHI = 1.65 V (0 to 3.3 V range), fin = 100 kHz, SYSCLK from X1, single and synchronous ADCs | | 11.0 | | |
| | Any VREF mode, fin = 100 kHz, SYSCLK from X1, asynchronous ADCs | | Not Supported | | |

6.13.3.2.2 ADC Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|---|-----|-----|-----|------|
| PSRR | VDD = 1.2-V DC + 100mV DC up to Sine at 1 kHz | | 60 | | dB |
| | VDD = 1.2-V DC + 100 mV DC up to Sine at 300 kHz | | 57 | | |
| | VDDA = 3.3-V DC + 200 mV DC up to Sine at 1 kHz | | 60 | | |
| | VDDA = 3.3-V DC + 200 mV Sine at 900 kHz | | 57 | | |

- (1) Load current on VREFHI increases when ADC input is greater than VDDA. This causes inaccurate conversions.
- (2) A ceramic capacitor with package size of 0805 or smaller is preferred. Up to ±20% tolerance is acceptable.
- (3) IO activity is minimized on pins adjacent to ADC input and VREFHI pins as part of best practices to reduce capacitive coupling and crosstalk.
- (4) Variation across all channels belonging to the same ADC module.
- (5) Worst case variation compared to other ADC modules.

6.13.3.2.3 ADC Input Model

The ADC input characteristics are given by [Table 6-13](#) and [Figure 6-44](#).

Table 6-13. Input Model Parameters

| | DESCRIPTION | REFERENCE MODE | VALUE |
|-----------------|-----------------------------|--|--|
| C _p | Parasitic input capacitance | All | See Table 6-14 to Table 6-17 |
| R _{on} | Sampling switch resistance | External Reference, 2.5-V Internal Reference | 500 Ω |
| | | 3.3-V Internal Reference | 860 Ω |
| C _h | Sampling capacitor | External Reference, 2.5-V Internal Reference | 12.5 pF |
| | | 3.3-V Internal Reference | 7.5 pF |
| R _s | Nominal source impedance | All | 50 Ω |

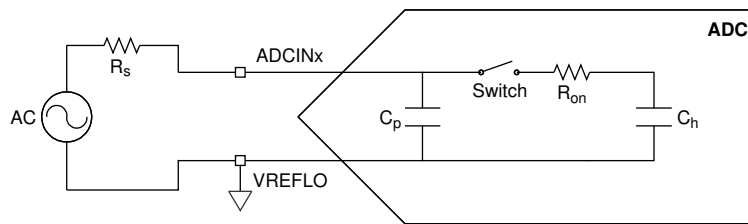


Figure 6-44. Input Model

This input model should be used with actual signal source impedance to determine the acquisition window duration. For more information, see the Choosing an Acquisition Window Duration section of the Analog-to-Digital Converter (ADC) chapter in the [TMS320F28003x Real-Time Microcontrollers Technical Reference Manual](#). For recommendations on improving ADC input circuits, see the [ADC Input Circuit Evaluation for C2000 MCUs](#) Application Report.

Table 6-14. Per-Channel Parasitic Capacitance for 100-Pin PZ LQFP

| ADC CHANNEL | C _p (pF) | |
|---------------------|---------------------|--------------------|
| | COMPARATOR DISABLED | COMPARATOR ENABLED |
| A0/B15/C15/DACA_OUT | 9.1 | 11.6 |
| A1/B7/DACB_OUT | 7.4 | 9.9 |
| A2/B6/C9 | 4.1 | 6.6 |
| A3 | 3.3 | 5.8 |

**Table 6-14. Per-Channel Parasitic Capacitance for 100-Pin PZ LQFP
(continued)**

| ADC CHANNEL | C _p (pF) | |
|-------------|---------------------|--------------------|
| | COMPARATOR DISABLED | COMPARATOR ENABLED |
| A4/B8 | 3.8 | 6.3 |
| A5 | 3.5 | 6 |
| A6 | 3.2 | 5.7 |
| A7/C3 | 3.8 | 6.3 |
| A8 | 4.1 | 6.6 |
| A9 | 3.1 | 5.6 |
| A10/B1/C10 | 4.7 | 7.2 |
| A11/B11/C0 | 4 | 6.5 |
| A12 | 3.4 | 5.9 |
| A14/B14/C4 | 3.8 | 6.3 |
| B0/C11 | 4.1 | 6.6 |
| B2/C6 | 3.9 | 6.4 |
| B3/VDAC | 75 | 77.5 |
| B4/C8 | 3.8 | 6.3 |
| B5 | 3.5 | 6 |
| B9/C7 | 3.3 | 5.8 |
| B11 | 3 | 5.5 |
| B12/C2 | 3.6 | 6.1 |
| C1 | 3 | 5.5 |
| C5 | 3.6 | 6.1 |
| C14 | 4.2 | 6.7 |
| AGPIO_B5 | 3.2 | 5.7 |
| AGPIO_B11 | 3.1 | 5.6 |

Table 6-15. Per-Channel Parasitic Capacitance for 80-Pin PN LQFP

| ADC CHANNEL | C _p (pF) | |
|---------------------|---------------------|--------------------|
| | COMPARATOR DISABLED | COMPARATOR ENABLED |
| A0/B15/C15/DACA_OUT | 9.1 | 11.6 |
| A1/B7/DACB_OUT | 7.4 | 9.9 |
| A2/B6/C9 | 4.1 | 6.6 |
| A3/B3/C5/VDAC | 81.9 | 89.4 |
| A4/B8/C14 | 8 | 13 |
| A5/B12/C2 | 7.1 | 12.1 |
| A6 | 3.2 | 5.7 |
| A7/C3 | 3.8 | 6.3 |
| A8/B0/C11 | 8.2 | 13.2 |
| A9/B4/C8 | 6.9 | 11.9 |
| A10/B1/C10 | 4.7 | 7.2 |
| A11/B11/C0 | 4 | 6.5 |
| A12/C1 | 6.4 | 11.4 |
| A14/B14/C4 | 3.8 | 6.3 |
| A15/B9/C7 | 7.1 | 12.1 |
| B2/C6 | 3.9 | 6.4 |
| AGPIO_B5 | 3.2 | 5.7 |

Table 6-15. Per-Channel Parasitic Capacitance for 80-Pin PN LQFP (continued)

| ADC CHANNEL | C _p (pF) | |
|-------------|---------------------|--------------------|
| | COMPARATOR DISABLED | COMPARATOR ENABLED |
| AGPIO_B11 | 3.1 | 5.6 |

Table 6-16. Per-Channel Parasitic Capacitance for 64-Pin PM LQFP

| ADC CHANNEL | C _p (pF) | |
|---------------------|---------------------|--------------------|
| | COMPARATOR DISABLED | COMPARATOR ENABLED |
| A0/B15/C15/DACA_OUT | 9.1 | 11.6 |
| A1/B7/DACB_OUT | 7.4 | 9.9 |
| A2/B6/C9 | 4.1 | 6.6 |
| A3/B3/C5/VDAC | 81.9 | 89.4 |
| A4/B8/C14 | 8 | 13 |
| A5/B12/C2 | 7.1 | 12.1 |
| A6 | 3.2 | 5.7 |
| A7/C3 | 3.8 | 6.3 |
| A8/B0/C11 | 8.2 | 13.2 |
| A9/B4/C8 | 6.9 | 11.9 |
| A10/B1/C10 | 4.7 | 7.2 |
| A11/B11/C0 | 4 | 6.5 |
| A12/C1 | 6.4 | 11.4 |
| A14/B14/C4 | 3.8 | 6.3 |
| A15/B9/C7 | 7.1 | 12.1 |
| B2/C6 | 3.9 | 6.4 |

Table 6-17. Per-Channel Parasitic Capacitance for 48-Pin PT LQFP

| ADC CHANNEL | C _p (pF) | |
|---------------------|---------------------|--------------------|
| | COMPARATOR DISABLED | COMPARATOR ENABLED |
| A0/B15/C15/DACA_OUT | 9.1 | 11.6 |
| A1/B7/DACB_OUT | 7.4 | 9.9 |
| A2/B6/C9 | 4.1 | 6.6 |
| A3/B3/C5/VDAC | 81.9 | 89.4 |
| A4/B8/C14 | 8 | 13 |
| A5/B12/C2 | 7.1 | 12.1 |
| A6/B2/C6 | 7.1 | 12.1 |
| A7/C3 | 3.8 | 6.3 |
| A8/B0/C11 | 8.2 | 13.2 |
| A9/B4/C8 | 6.9 | 11.9 |
| A10/B1/C10 | 4.7 | 7.2 |
| A11/B11/C0 | 4 | 6.5 |
| A12/C1 | 6.4 | 11.4 |
| A15/B9/C7 | 7.1 | 12.1 |

6.13.3.2.4 ADC Timing Diagrams

Figure 6-45 shows the ADC conversion timings for two SOC's given the following assumptions:

- SOC0 and SOC1 are configured to use the same trigger.
- No other SOC's are converting or pending when the trigger occurs.
- The round-robin pointer is in a state that causes SOC0 to convert first.
- ADCINTSEL is configured to set an ADCINT flag upon end of conversion for SOC0 (whether this flag propagates through to the CPU to cause an interrupt is determined by the configurations in the PIE module).

Table 6-18 lists the descriptions of the ADC timing parameters. Table 6-19 lists the ADC timings.

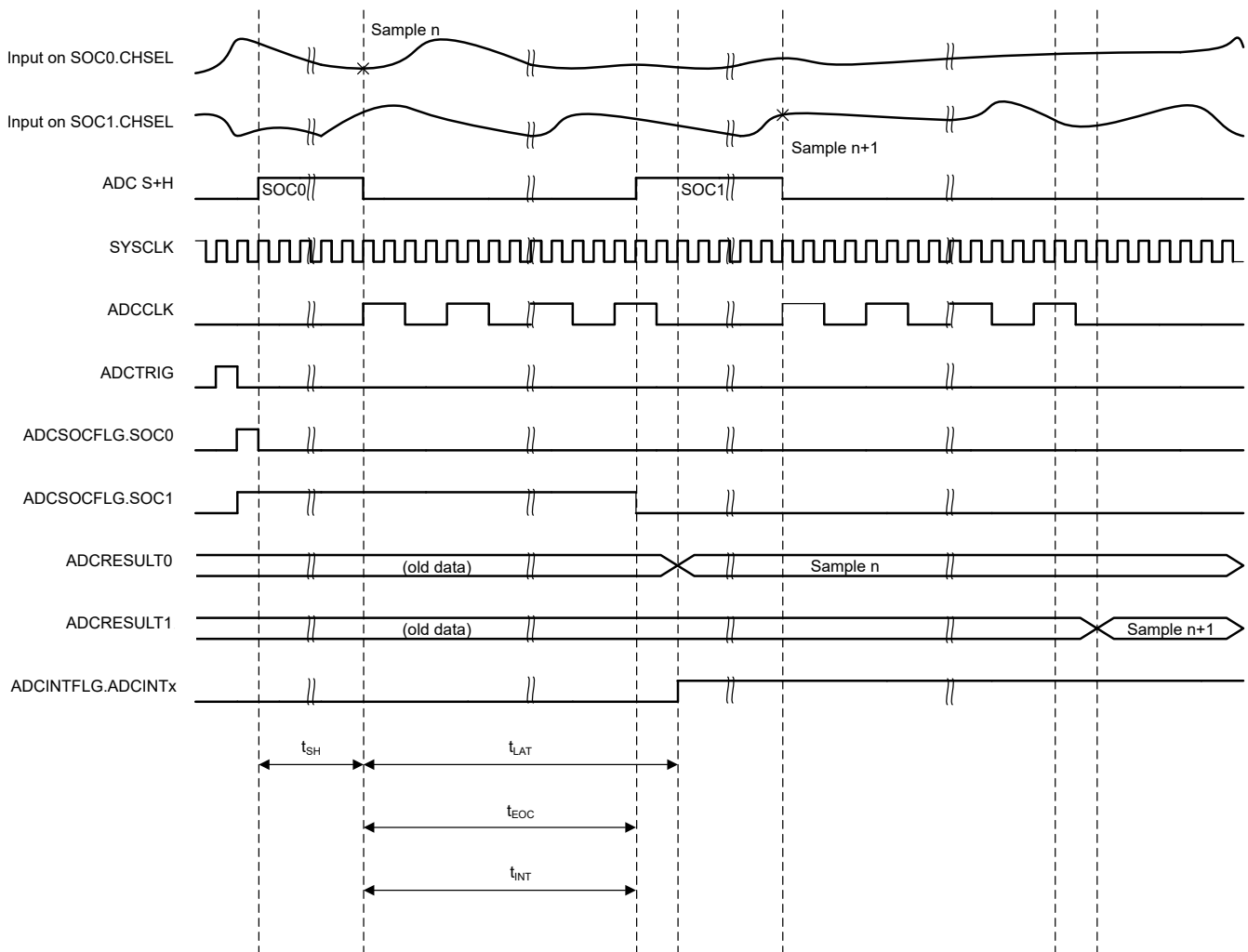


Figure 6-45. ADC Timings

Table 6-18. ADC Timing Parameter Descriptions

| PARAMETER | DESCRIPTION |
|-----------|---|
| t_{SH} | The duration of the S+H window. At the end of this window, the value on the S+H capacitor becomes the voltage to be converted into a digital value. The duration is given by (ACQPS + 1) SYSCLK cycles. ACQPS can be configured individually for each SOC, so t_{SH} is not necessarily the same for different SOCs. Note: The value on the S+H capacitor is captured approximately 5 ns before the end of the S+H window regardless of device clock settings. |
| t_{LAT} | The time from the end of the S+H window until the ADC results latch in the ADCRESULTx register. If the ADCRESULTx register is read before this time, the previous conversion results are returned. |
| t_{EOC} | The time from the end of the S+H window until the S+H window for the next ADC conversion can begin. The subsequent sample can start before the conversion results are latched. |
| t_{INT} | The time from the end of the S+H window until an ADCINT flag is set (if configured). If the INTPULSEPOS bit in the ADCCTL1 register is set, t_{INT} coincides with the end of conversion (EOC) signal. If the INTPULSEPOS bit is 0, t_{INT} coincides with the end of the S+H window. If t_{INT} triggers a read of the ADC result register (directly through DMA or indirectly by triggering an ISR that reads the result), care must be taken to make sure the read occurs after the results latch (otherwise, the previous results are read). If the INTPULSEPOS bit is 0, and the OFFSET field in the ADCINTCYCLE register is not 0, then there is a delay of OFFSET SYSCLK cycles before the ADCINT flag is set. This delay can be used to enter the ISR or trigger the DMA exactly when the sample is ready. |

Table 6-19. ADC Timings

| ADCCLK PRESCALE | | SYSCLK CYCLES | | | | ADCCLK CYCLES |
|--------------------|---------------------|---------------|-----------------|------------------------|-----------------|---------------|
| ADCCTL2 [PRESCALE] | RATIO ADCCLK:SYSCLK | t_{EOC} | $t_{LAT}^{(1)}$ | $t_{INT(EARLY)}^{(2)}$ | $t_{INT(LATE)}$ | t_{EOC} |
| 0 | 1 | 11 | 13 | 1 | 11 | 11 |
| 2 | 2 | 21 | 23 | 1 | 21 | 10.5 |
| 4 | 3 | 31 | 34 | 1 | 31 | 10.3 |
| 6 | 4 | 41 | 44 | 1 | 41 | 10.3 |
| 8 | 5 | 51 | 55 | 1 | 51 | 10.2 |
| 10 | 6 | 61 | 65 | 1 | 61 | 10.2 |
| 12 | 7 | 71 | 76 | 1 | 71 | 10.1 |
| 14 | 8 | 81 | 86 | 1 | 81 | 10.1 |

- (1) Refer to the "ADC: DMA Read of Stale Result" advisory in the [TMS320F28003x Real-Time MCUs Silicon Errata](#).
(2) By default, t_{INT} occurs one SYSCLK cycle after the S+H window if INTPULSEPOS is 0. This can be changed by writing to the OFFSET field in the ADCINTCYCLE register.

6.13.4 Temperature Sensor

6.13.4.1 Temperature Sensor Electrical Data and Timing

The temperature sensor can be used to measure the device junction temperature. The temperature sensor is sampled through an internal connection to the ADC and translated into a temperature through TI-provided software. When sampling the temperature sensor, the ADC must meet the acquisition time in the Temperature Sensor Characteristics table.

6.13.4.1.1 Temperature Sensor Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------|--|--------------------|-----|-----|-----|------|
| T_{acc} | Temperature Accuracy | External reference | | ±15 | | °C |
| $t_{startup}$ | Start-up time (TSNSCTL[ENABLE] to sampling temperature sensor) | | | 500 | | µs |
| t_{acq} | ADC acquisition time | | 450 | | | ns |

6.13.5 Comparator Subsystem (CMPSS)

The Comparator Subsystem (CMPSS) consists of analog comparators and supporting circuits that are useful for power applications such as peak current mode control, switched-mode power supply, power factor correction, voltage trip monitoring, and so forth.

The comparator subsystem is built around a number of modules. Each subsystem contains two comparators, two reference 12-bit DACs, and two digital filters. The subsystem also includes one ramp generator. Comparators are denoted "H" or "L" within each module where "H" and "L" represent high and low, respectively. Each comparator generates a digital output which indicates whether the voltage on the positive input is greater than the voltage on the negative input. The positive input of the comparator is driven from an external pin (see the *Analog Subsystem* chapter of the [TMS320F28003x Real-Time Microcontrollers Technical Reference Manual](#) for mux options available to the CMPSS). The negative input can be driven by an external pin or by the programmable reference 12-bit DAC. Each comparator output passes through a programmable digital filter that can remove spurious trip signals. An unfiltered output is also available if filtering is not required. A ramp generator circuit is optionally available to control the reference 12-bit DAC value for the high comparator in the subsystem.

Each CMPSS includes:

- Two analog comparators
- Two programmable reference 12-bit DACs
- One ramp generator
- Two digital filters, 65536 max filter clock prescale
- Ability to synchronize submodules with EPWMSYNCPER
- Ability to extend clear signal with EPWMBLANK
- Ability to synchronize output with SYSCLK
- Ability to latch output
- Ability to invert output
- Option to use hysteresis on the input
- Option for negative input of comparator to be driven by an external signal or by the reference DAC
- Option to choose between VDDA or VDACC to be the DAC reference voltage

6.13.5.1 CMPSS Connectivity Diagram

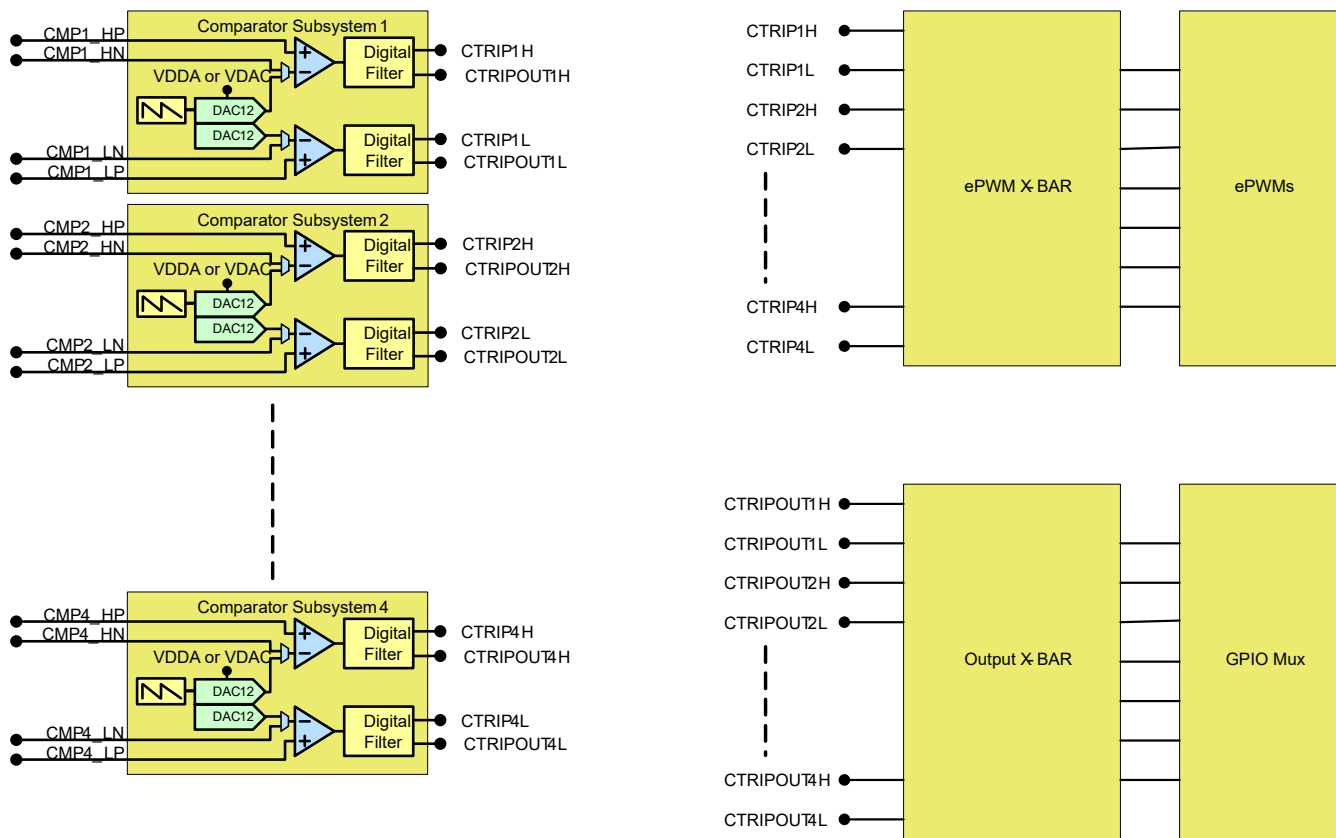


Figure 6-46. CMPSS Connectivity

6.13.5.2 Block Diagram

The block diagram for the CMPSS is shown in Figure 6-47.

- CTRIPx(x= "H" or "L") signals are connected to the ePWM X-BAR for ePWM trip response. See the *Enhanced Pulse Width Modulator (ePWM)* chapter of the [TMS320F28003x Real-Time Microcontrollers Technical Reference Manual](#) for more details on the ePWM X-BAR mux configuration.
- CTRIPxOUTx(x= "H" or "L") signals are connected to the Output X-BAR for external signaling. See the *General-Purpose Input/Output (GPIO)* chapter of the [TMS320F28003x Real-Time Microcontrollers Technical Reference Manual](#) for more details on the Output X-BAR mux configuration.

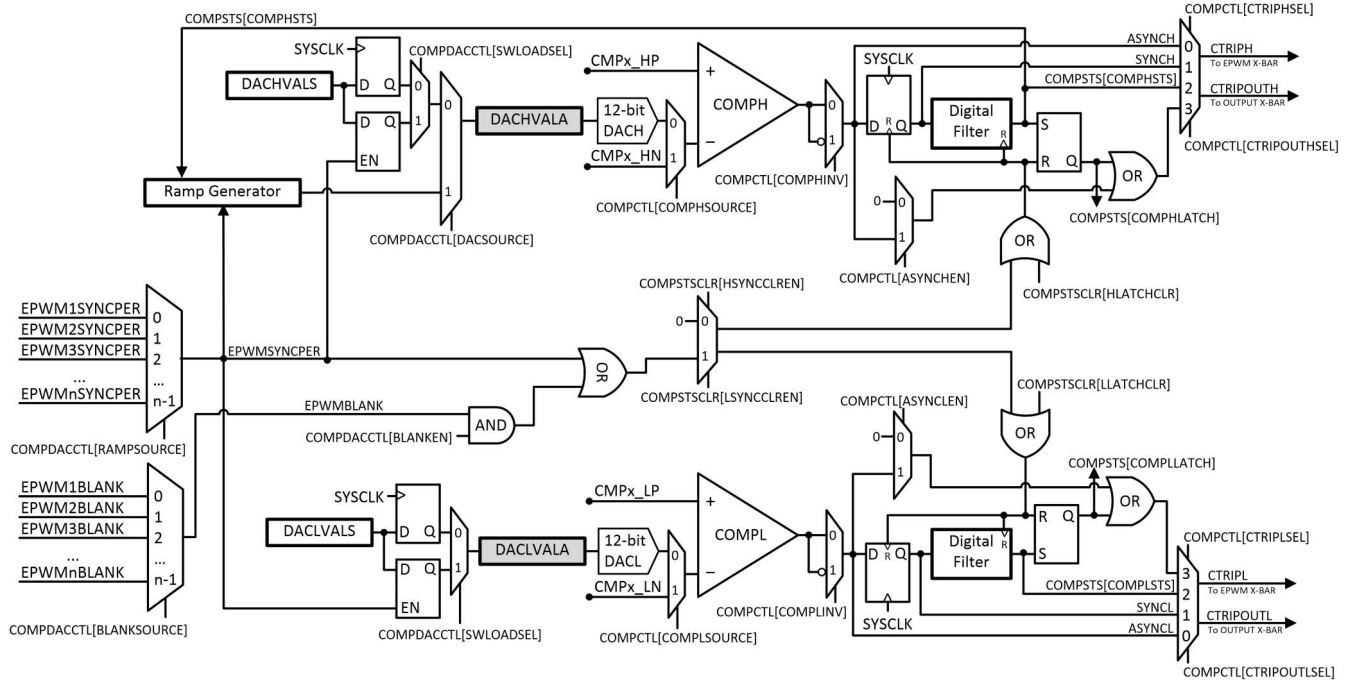


Figure 6-47. CMPSS Module Block Diagram

Each reference 12-bit DAC can be configured to drive a reference voltage into the negative input of the respective comparator. The reference 12-bit DAC output is internal only and cannot be observed externally. The reference 12-bit DAC is illustrated in Figure 6-48.

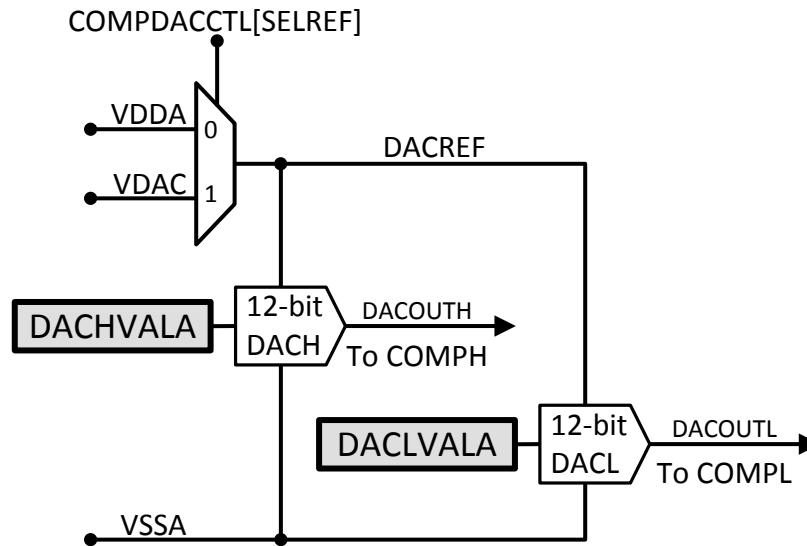


Figure 6-48. Reference DAC Block Diagram

6.13.5.3 CMPSS Electrical Data and Timing

6.13.5.3.1 Comparator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|------------------------------|--|-----|-----|------|------|
| TPU | Power-up time | | | | 500 | µs |
| Comparator input (CMPINxx) range | | | 0 | | VDDA | V |
| Input referred offset error | | Low common mode, inverting input set to 50mV | -20 | | 20 | mV |
| Hysteresis ⁽¹⁾ | 1x | | 4 | 12 | 20 | LSB |
| | 2x | | 17 | 24 | 33 | |
| | 3x | | 25 | 36 | 50 | |
| | 4x | | 30 | 48 | 67 | |
| Response time (delay from CMPINx input pin change to GPIO output pin through either ePWM X-BAR or Output X-BAR) | | Step response | | 21 | 60 | ns |
| | | Ramp response (1.65V/µs) | | 26 | | |
| | | Ramp response (8.25mV/µs) | | 30 | | ns |
| PSRR | Power Supply Rejection Ratio | Up to 250 kHz | | 46 | | dB |
| CMRR | Common Mode Rejection Ratio | | 40 | | | dB |

- (1) The CMPSS DAC is used as the reference to determine how much hysteresis to apply. Therefore, hysteresis will scale with the CMPSS DAC reference voltage. Hysteresis is available for all comparator input source configurations.

CMPSS Comparator Input Referred Offset and Hysteresis

Note

The CMPSS inputs must be kept below $VDDA + 0.3$ V to ensure proper functional operation. If a CMPSS input exceeds this level, an internal blocking circuit isolates the internal comparator from the external pin until the external pin voltage returns below $VDDA + 0.3$ V. During this time, the internal comparator input is floating and can decay below $VDDA$ within approximately 0.5 µs. After this time, the comparator could begin to output an incorrect result depending on the value of the other comparator input.

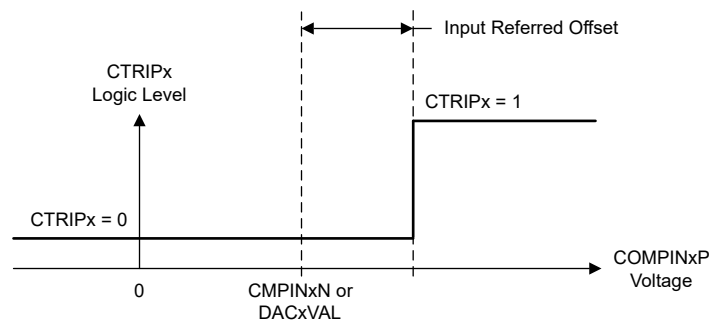


Figure 6-49. CMPSS Comparator Input Referred Offset

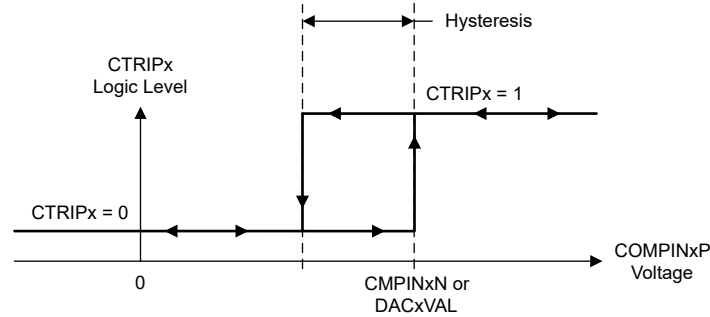


Figure 6-50. CMPSS Comparator Hysteresis

6.13.5.3.2 CMPSS DAC Static Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|------|------------|---------------------|----------|
| CMPSS DAC output range | Internal reference | 0 | | VDDA | V |
| | External reference | 0 | | VDAC ⁽⁴⁾ | |
| Static offset error ⁽¹⁾ | | -25 | | 25 | mV |
| Static gain error ⁽¹⁾ | | -2 | | 2 | % of FSR |
| Static DNL | Endpoint corrected | >-1 | | 4 | LSB |
| Static INL | Endpoint corrected | -16 | | 16 | LSB |
| Settling time | Settling to 1LSB after full-scale output change | | | 1 | μs |
| Resolution | | | 12 | | bits |
| CMPSS DAC output disturbance ⁽²⁾ | Error induced by comparator trip or CMPSS DAC code change within the same CMPSS module | -100 | | 100 | LSB |
| CMPSS DAC disturbance time ⁽²⁾ | | | | 200 | ns |
| VDAC reference voltage | When VDAC is reference | 2.4 | 2.5 or 3.0 | VDDA | V |
| VDAC load ⁽³⁾ | When VDAC is reference | 6 | 8 | 10 | kΩ |

- (1) Includes comparator input referred errors.
- (2) Disturbance error may be present on the CMPSS DAC output for a certain amount of time after a comparator trip.
- (3) Per active CMPSS module.
- (4) The maximum output voltage is VDDA when VDAC > VDDA.

6.13.5.3.3 CMPSS Illustrative Graphs

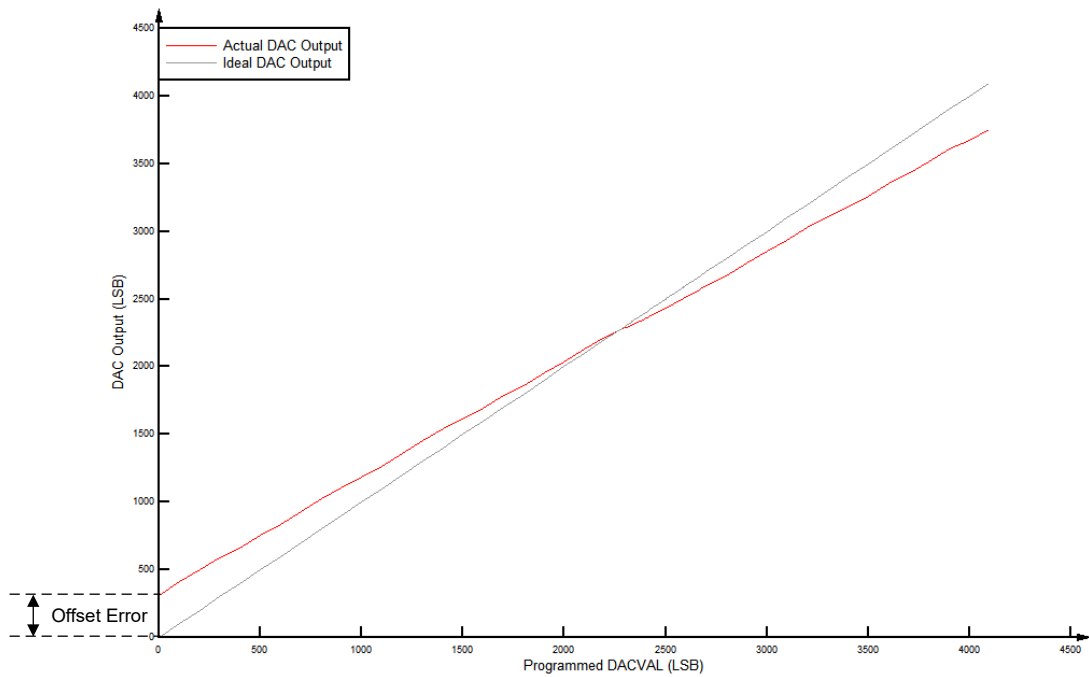


Figure 6-51. CMPSS DAC Static Offset

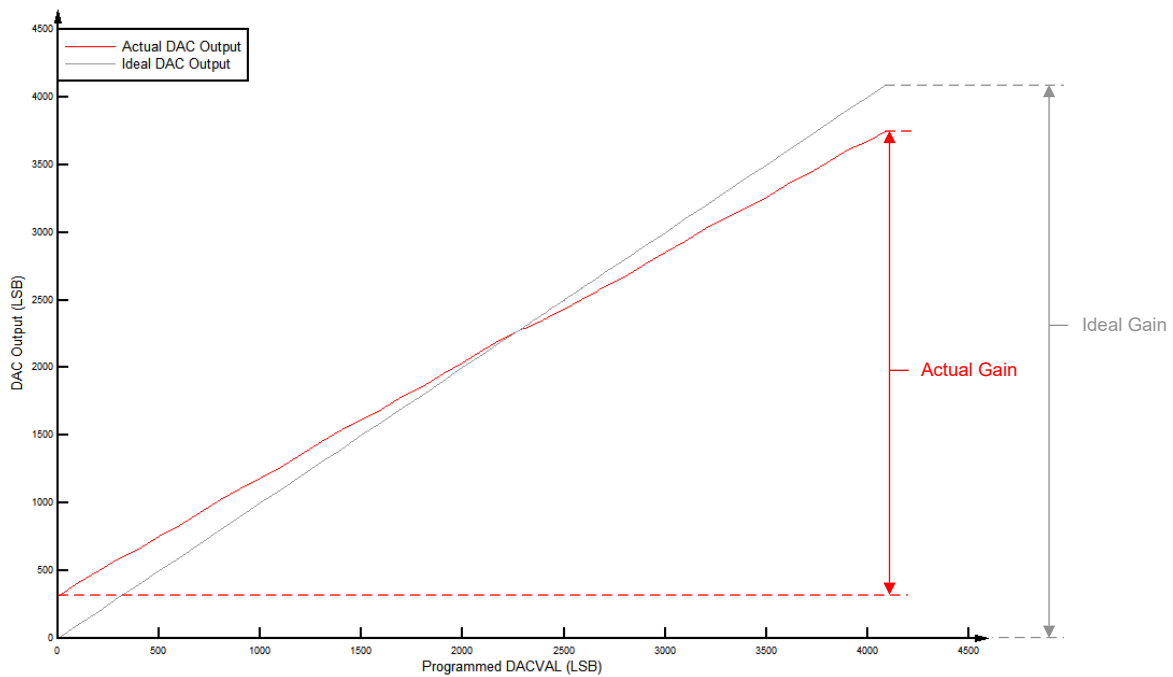


Figure 6-52. CMPSS DAC Static Gain

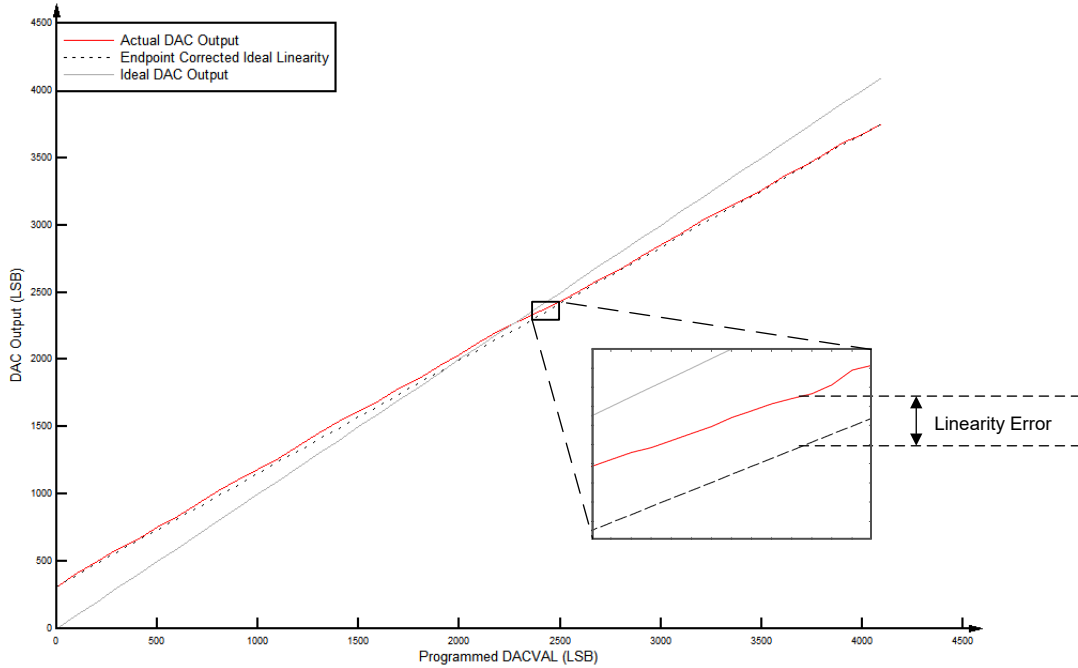


Figure 6-53. CMPSS DAC Static Linearity

6.13.5.3.4 CMPSS DAC Dynamic Error

When using the ramp generator to control the internal DAC, the step size can vary based on the application need. Since the step size of the DAC is less than a full scale transition, the settling time is improved from the electrical specification listed in the *CMPSS DAC Static Electrical Characteristics* table. The equation below and [Figure 6-54](#) can give guidance on the expected voltage error from ideal based on different RAMPxDECVALA values.

$$DYNAMICERROR = (m \times RAMPxDECVALA) + b \tag{3}$$

Table 6-20. DAC Max Dynamic Error Terms

| EQUATION PARAMETER | MIN (LSB) | MAX (LSB) |
|--------------------|-----------|-----------|
| m | 0.10 | 0.18 |
| b | 3.7 | 5.6 |

Note

Above error terms are based on the max SYSCLK of the target device. If operating below the max SYSCLK then the "m" error term should be scaled accordingly.

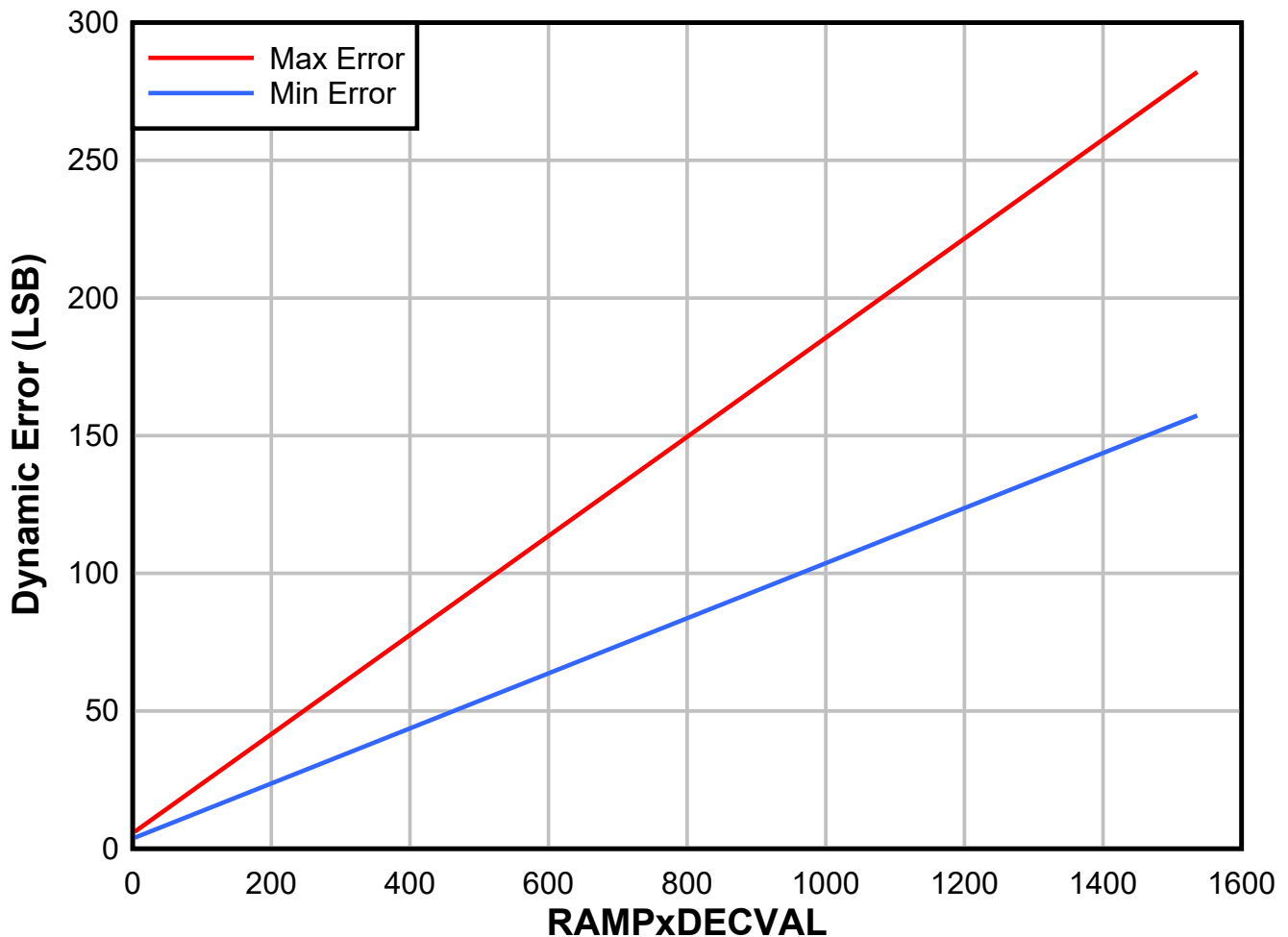


Figure 6-54. CMPSS DAC Dynamic Error

6.13.6 Buffered Digital-to-Analog Converter (DAC)

The buffered DAC module consists of an internal 12-bit DAC and an analog output buffer that can drive an external load. For driving even higher loads than typical, a trade-off can be made between load size and output voltage swing. For the load conditions of the buffered DAC, see the Buffered DAC Electrical Data and Timing section. The buffered DAC is a general-purpose DAC that can be used to generate a DC voltage or AC waveforms such as sine waves, square waves, triangle waves and so forth. Software writes to the DAC value register can take effect immediately or can be synchronized with EPWMSYNCO events.

Each buffered DAC has the following features:

- 12-bit resolution
- Selectable reference voltage source
- x1 and x2 gain modes when using internal VREFHI
- Ability to synchronize with EPWMSYNCPER

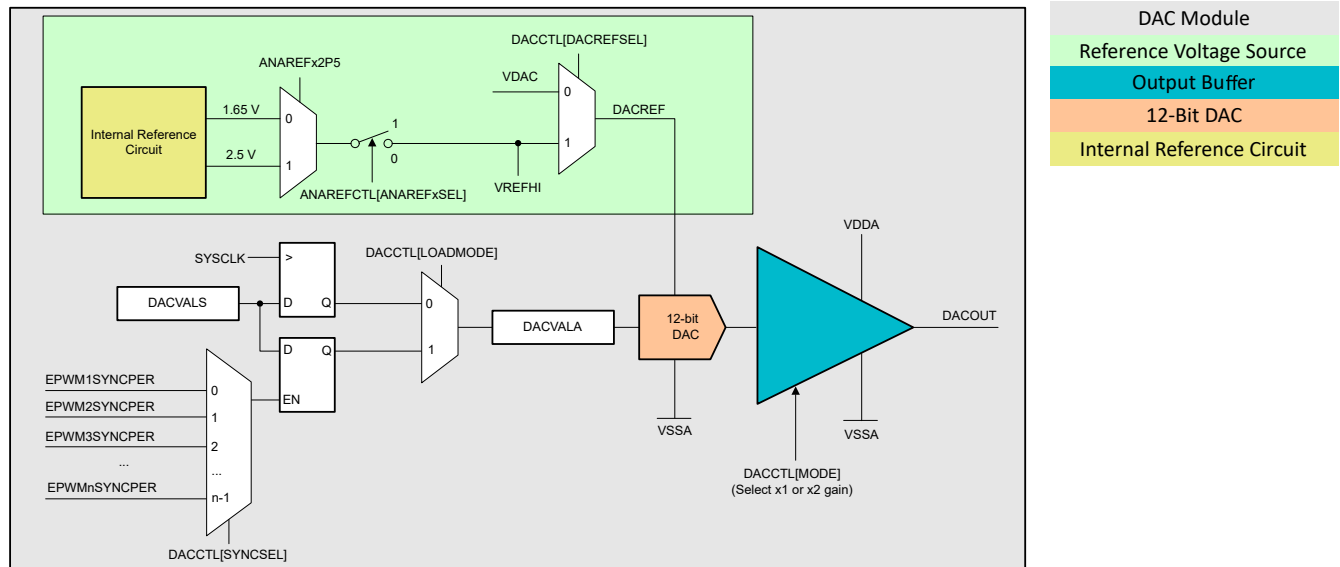


Figure 6-55. DAC Module Block Diagram

6.13.6.1 Buffered DAC Electrical Data and Timing

6.13.6.1.1 Buffered DAC Operating Conditions

over recommended operating conditions (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------------|---|-----------------------|-----|------------|------------|------|
| R _L | Resistive Load ⁽²⁾ | | 5 | | | kΩ |
| C _L | Capacitive Load | | | | 100 | pF |
| V _{OUT} | Valid Output Voltage Range ⁽³⁾ | R _L = 5 kΩ | 0.3 | | VDDA – 0.3 | V |
| | | R _L = 1 kΩ | 0.6 | | VDDA – 0.6 | V |
| Reference Voltage ⁽⁴⁾ | | VDAC or VREFHI | 2.4 | 2.5 or 3.0 | VDDA | V |

- (1) Typical values are measured with VREFHI = 3.3 V and VREFLO = 0 V, unless otherwise noted. Minimum and maximum values are tested or characterized with VREFHI = 2.5 V and VREFLO = 0 V.
- (2) DAC can drive a minimum resistive load of 1 kΩ, but the output range will be limited.
- (3) This is the linear output range of the DAC. The DAC can generate voltages outside this range, but the output voltage will not be linear due to the buffer.
- (4) For best PSRR performance, VDAC or VREFHI should be less than VDDA.

6.13.6.1.2 Buffered DAC Electrical Characteristics

over recommended operating conditions (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|------|-------|------|-----------|
| General | | | | | | |
| Resolution | | | | 12 | | bits |
| Load Regulation | | | –1 | | 1 | mV/V |
| Glitch Energy | | | | 1.5 | | V-ns |
| Voltage Output Settling Time Full-Scale | | Settling to 2 LSBs after 0.3V-to-3V transition | | | 2 | μs |
| Voltage Output Settling Time 1/4 th Full-Scale | | Settling to 2 LSBs after 0.3V-to-0.75V transition | | | 1.6 | μs |
| Voltage Output Slew Rate | | Slew rate from 0.3V-to-3V transition | 2.8 | | 4.5 | V/μs |
| Load Transient Settling Time | | 5-kΩ Load | | | 328 | ns |
| | | 1-kΩ Load | | | 557 | ns |
| Reference Input Resistance ⁽²⁾ | | VDAC or VREFHI | 160 | 200 | 240 | kΩ |
| TPU | Power Up Time | External Reference mode | | | 500 | μs |
| | | Internal Reference mode | | | 5000 | μs |
| DC Characteristics | | | | | | |
| Offset | Offset Error | Midpoint | –10 | | 10 | mV |
| Gain | Gain Error ⁽³⁾ | | –2.5 | | 2.5 | % of FSR |
| DNL | Differential Non Linearity ⁽⁴⁾ | Endpoint corrected | –1 | ±0.4 | 1 | LSB |
| INL | Integral Non Linearity | Endpoint corrected | –5 | ±2 | 5 | LSB |
| AC Characteristics | | | | | | |
| Output Noise | | Integrated noise from 100 Hz to 100 kHz | | 600 | | μVrms |
| | | Noise density at 10 kHz | | 800 | | nVrms/√Hz |
| SNR | Signal to Noise Ratio | 1 kHz, 200 KSPS | | 64 | | dB |
| THD | Total Harmonic Distortion | 1 kHz, 200 KSPS | | –64.2 | | dB |
| SFDR | Spurious Free Dynamic Range | 1 kHz, 200 KSPS | | 66 | | dB |
| SINAD | Signal to Noise and Distortion Ratio | 1 kHz, 200 KSPS | | 61.7 | | dB |

6.13.6.1.2 Buffered DAC Electrical Characteristics (continued)

 over recommended operating conditions (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|---|-----------------|-----|-----|-----|------|
| PSRR | Power Supply Rejection Ratio ⁽⁵⁾ | DC | | 70 | | dB |
| | | 100 kHz | | 30 | | dB |

- (1) Typical values are measured with VREFHI = 3.3 V and VREFLO = 0 V, unless otherwise noted. Minimum and maximum values are tested or characterized with VREFHI = 2.5 V and VREFLO = 0 V.
- (2) Per active Buffered DAC module.
- (3) Gain error is calculated for linear output range.
- (4) The DAC output is monotonic.
- (5) VREFHI = 3.2 V, VDDA = 3.3 V DC + 100 mV Sine.

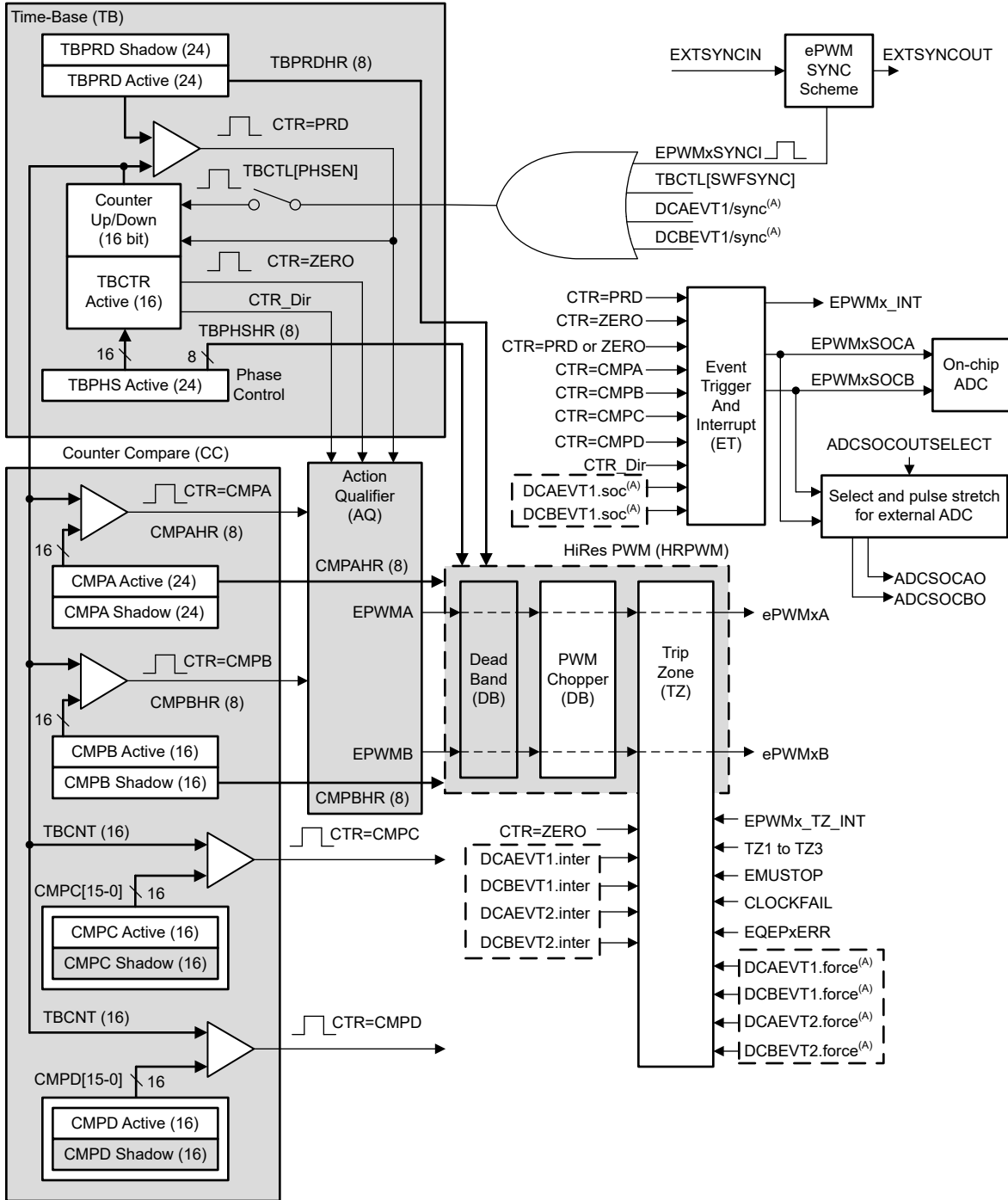
6.14 Control Peripherals

6.14.1 Enhanced Pulse Width Modulator (ePWM)

The ePWM peripheral is a key element in controlling many of the power electronic systems found in both commercial and industrial equipment. The ePWM type-4 module is able to generate complex pulse width waveforms with minimal CPU overhead by building the peripheral up from smaller modules with separate resources that can operate together to form a system. Some of the highlights of the ePWM type-4 module include complex waveform generation, dead-band generation, a flexible synchronization scheme, advanced trip-zone functionality, and global register reload capabilities.

The ePWM and eCAP synchronization scheme on the device provides flexibility in partitioning the ePWM and eCAP modules and allows localized synchronization within the modules.

[Figure 6-56](#) shows the ePWM module. [Figure 6-57](#) shows the ePWM trip input connectivity.



A. These events are generated by the ePWM digital compare (DC) submodule based on the levels of the TRIPIN inputs.

Figure 6-56. ePWM Submodules and Critical Internal Signal Interconnects

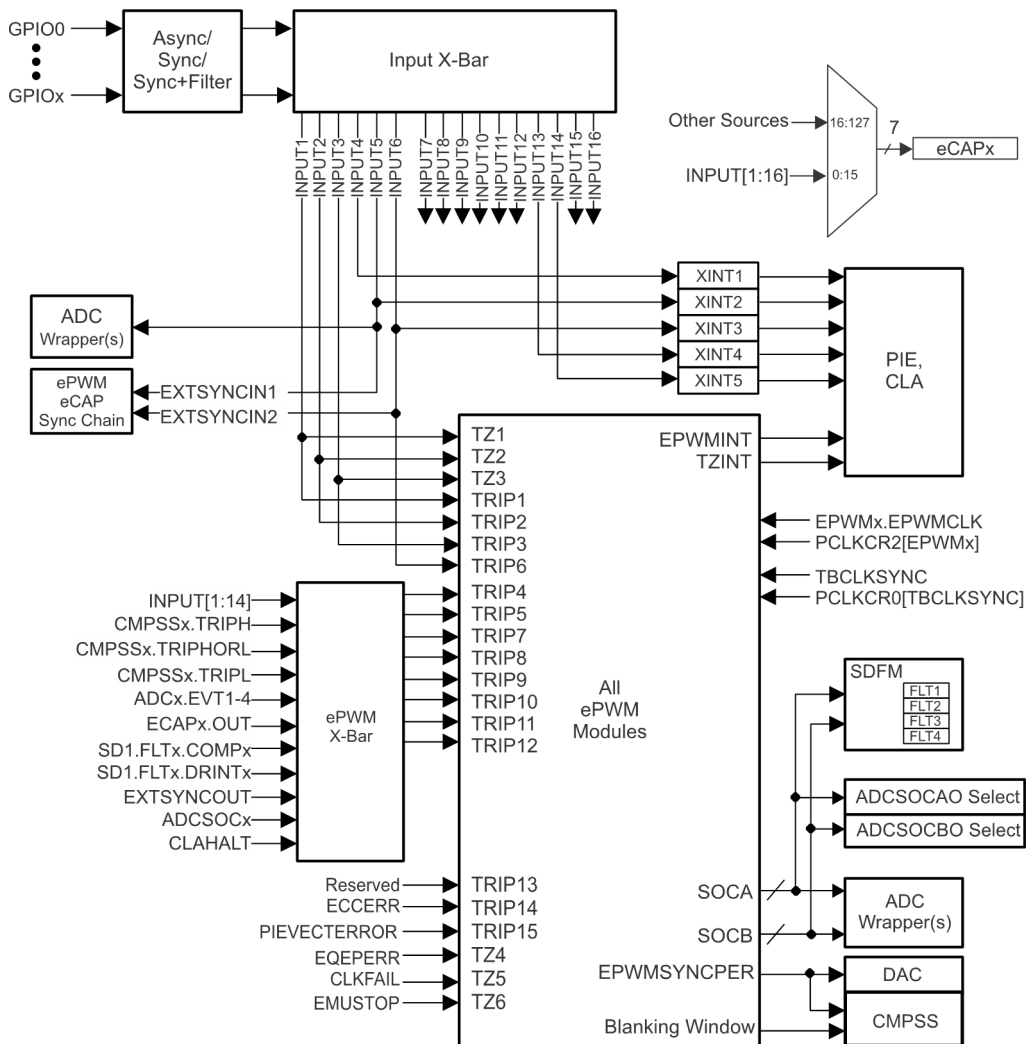


Figure 6-57. ePWM Trip Input Connectivity

6.14.1.1 ePWM Electrical Data and Timing

For an explanation of the input qualifier parameters, see the General-Purpose Input Timing Requirements table.

6.14.1.1.1 ePWM Timing Requirements

| | | | MIN | MAX | UNIT |
|-----------------|------------------------|----------------------|---------------------------------|-----|--------|
| $t_{w(SYNCIN)}$ | Sync input pulse width | Asynchronous | $2t_{c(EPWMCLK)}$ | | cycles |
| | | Synchronous | $2t_{c(EPWMCLK)}$ | | |
| | | With input qualifier | $1t_{c(EPWMCLK)} + t_{w(IQSW)}$ | | |

6.14.1.1.2 ePWM Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER ⁽¹⁾ | | MIN | MAX | UNIT |
|--------------------------|--|-------------------|-----|--------|
| $t_{w(PWM)}$ | Pulse duration, PWMx output high/low | 20 | | ns |
| $t_{w(SYNCOUT)}$ | Sync output pulse width | $8t_{c(SYSCCLK)}$ | | cycles |
| $t_{d(TZ-PWM)}$ | Delay time, trip input active to PWM forced high | | 25 | ns |
| | Delay time, trip input active to PWM forced low | | | |
| | Delay time, trip input active to PWM Hi-Z | | | |

(1) 20-pF load on pin.

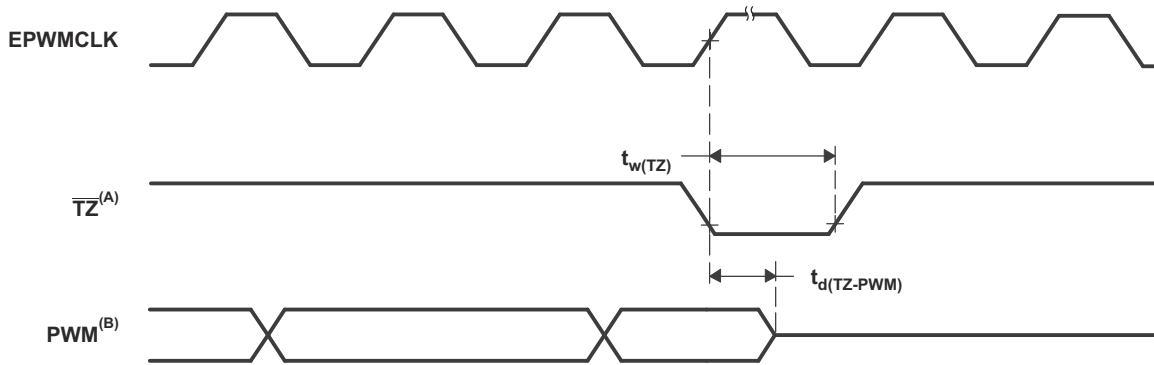
6.14.1.1.3 Trip-Zone Input Timing

For an explanation of the input qualifier parameters, see the General-Purpose Input Timing Requirements table.

6.14.1.1.3.1 Trip-Zone Input Timing Requirements

| | | | MIN | MAX | UNIT |
|-------------|--|----------------------|---------------------------------|-----|--------|
| $t_{w(TZ)}$ | Pulse duration, \overline{TZx} input low | Asynchronous | $1t_{c(EPWMCLK)}$ | | cycles |
| | | Synchronous | $2t_{c(EPWMCLK)}$ | | cycles |
| | | With input qualifier | $1t_{c(EPWMCLK)} + t_{w(IQSW)}$ | | cycles |

6.14.1.1.3.2 PWM Hi-Z Characteristics Timing Diagram



A. TZ: TZ1, TZ2, TZ3, TRIP1–TRIP12

B. PWM refers to all the PWM pins in the device. The state of the PWM pins after TZ is taken high depends on the PWM recovery software.

Figure 6-58. PWM Hi-Z Characteristics

6.14.2 High-Resolution Pulse Width Modulator (HRPWM)

The HRPWM combines multiple delay lines in a single module and a simplified calibration system by using a dedicated calibration delay line. For each ePWM module, there are two HR outputs:

- HR Duty and Deadband control on Channel A
- HR Duty and Deadband control on Channel B

The HRPWM module offers PWM resolution (time granularity) that is significantly better than what can be achieved using conventionally derived digital PWM methods. The key points for the HRPWM module are:

- Significantly extends the time resolution capabilities of conventionally derived digital PWM
- This capability can be used in both single edge (duty cycle and phase-shift control) as well as dual edge control for frequency/period modulation.
- Finer time granularity control or edge positioning is controlled through extensions to the Compare A, B, phase, period and deadband registers of the ePWM module.

6.14.2.1 HRPWM Electrical Data and Timing

6.14.2.1.1 High-Resolution PWM Characteristics

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|-----|-----|-----|------|
| Micro Edge Positioning (MEP) step size ⁽¹⁾ | | 150 | 310 | ps |

- (1) The MEP step size will be largest at high temperature and minimum voltage on V_{DD} . MEP step size will increase with higher temperature and lower voltage and decrease with lower temperature and higher voltage. Applications that use the HRPWM feature should use MEP Scale Factor Optimizer (SFO) estimation software functions. See the TI software libraries for details of using SFO functions in end applications. SFO functions help to estimate the number of MEP steps per SYSCLK period dynamically while the HRPWM is in operation.

6.14.3 External ADC Start-of-Conversion Electrical Data and Timing

6.14.3.1 External ADC Start-of-Conversion Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | MIN | MAX | UNIT |
|--|------------------------|-----|--------|
| $t_{w(ADCSOCL)}$ Pulse duration, $\overline{ADCSOCxO}$ low | $32t_c(\text{SYSCLK})$ | | cycles |

6.14.3.2 $\overline{ADCSOCAO}$ or $\overline{ADCSOCBO}$ Timing Diagram

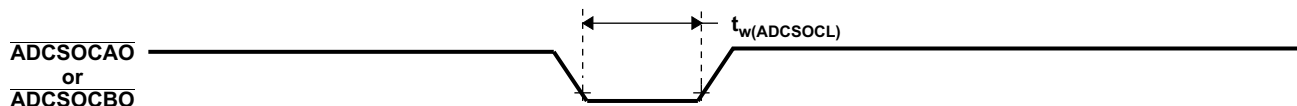


Figure 6-59. $\overline{ADCSOCAO}$ or $\overline{ADCSOCBO}$ Timing

6.14.4 Enhanced Capture (eCAP)

The features of the eCAP module include:

- Speed measurements of rotating machinery (for example, toothed sprockets sensed by way of Hall sensors)
- Elapsed time measurements between position sensor pulses
- Period and duty cycle measurements of pulse train signals
- Decoding current or voltage amplitude derived from duty cycle encoded current/voltage sensors

The eCAP module features described in this chapter include:

- 4-event time-stamp registers (each 32 bits)
- Edge polarity selection for up to four sequenced time-stamp capture events
- Interrupt on either of the four events
- Single-shot capture of up to four event time-stamps
- Continuous mode capture of time stamps in a four-deep circular buffer
- Absolute time-stamp capture
- Difference (Delta) mode time-stamp capture
- When not used in capture mode, the eCAP module can be configured as a single-channel PWM output

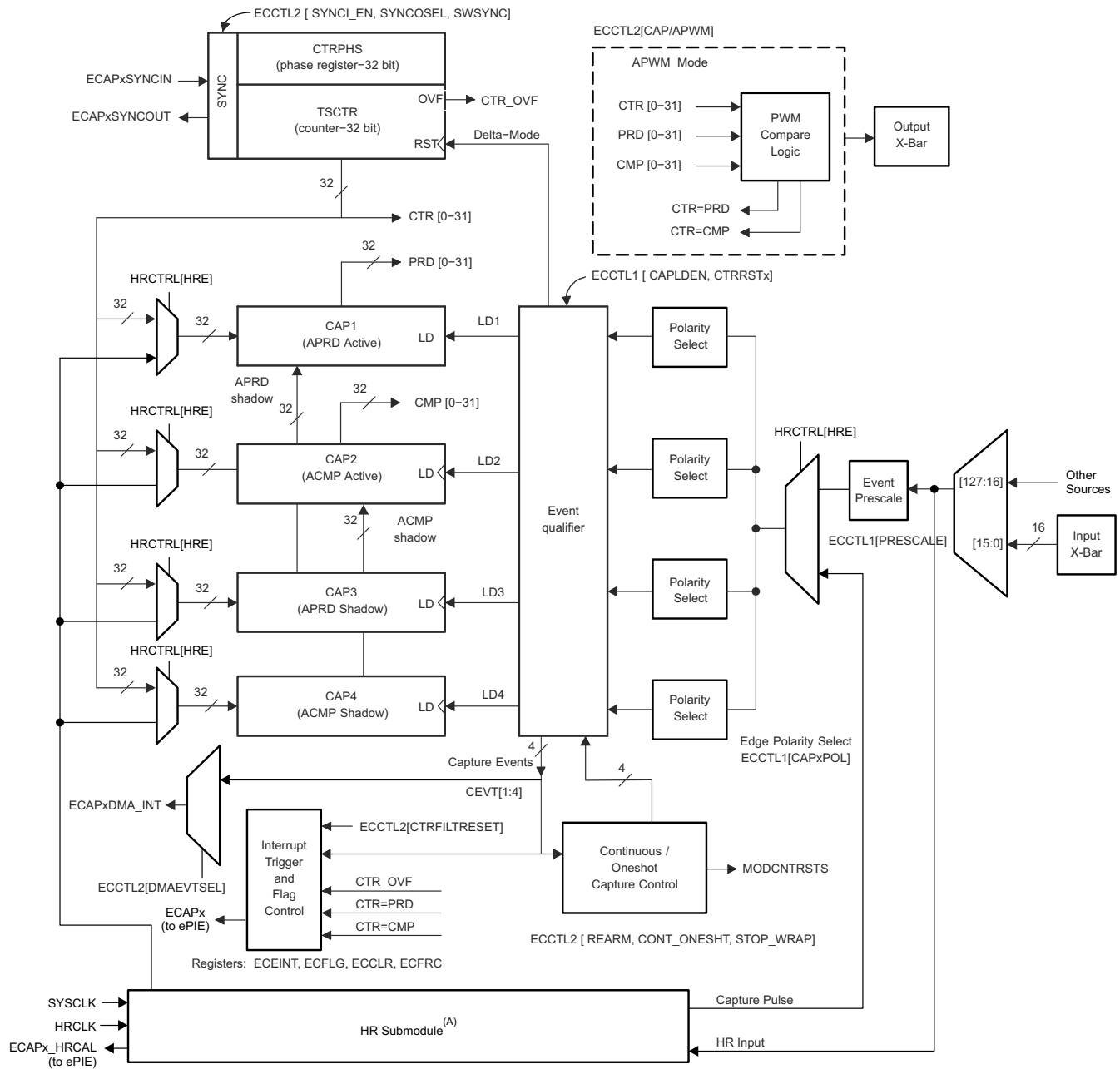
The capture functionality of the Type 1 eCAP is enhanced from the Type 0 eCAP with the following added features:

- Event filter reset bit
 - Writing a 1 to ECCTL2[CTRFILTRESET] clears the event filter, the modulo counter, and any pending interrupts flags. Resetting the bit is useful for initialization and debug.
- Modulo counter status bits
 - The modulo counter (ECCTL2 [MODCNRSTS]) indicates which capture register is loaded next. In the Type 0 eCAP, to know the current state of the modulo counter was not possible
- DMA trigger source
 - eCAPxDMA was added as a DMA trigger. CEVT[1-4] can be configured as the source for eCAPxDMA.
- Input multiplexer
 - ECCTL0 [INPUTSEL] selects one of 128 input signals, which are detailed in the Configuring Device Pins for the eCAP section of the Enhanced Capture (eCAP) chapter in the [TMS320F28003x Real-Time Microcontrollers Technical Reference Manual](#).
- EALLOW protection
 - EALLOW protection was added to critical registers. To maintain software compatibility with Type-0, configure DEV_CFG_REGS.ECAPTYPE to make these registers unprotected.

The capture functionality of the Type 2 eCAP is enhanced from the Type 1 eCAP with the following added features:

- Added ECAPxSYNCINSEL register
 - ECAPxSYNCINSEL register is added for each eCAP to select an external SYNCIN. Every eCAP can have a separate SYNCIN signal.

6.14.4.1 eCAP and HRCAP Block Diagram



A. The HRCAP submodule is not available on all eCAP modules; in this case, the high-resolution muxes and hardware are not implemented.

Figure 6-60. eCAP and HRCAP Block Diagram

6.14.4.2 eCAP Synchronization

The eCAP modules can be synchronized with each other by selecting a common SYNCIN source. SYNCIN source for eCAP can be either software sync-in or external sync-in. The external sync-in signal can come from EPWM, eCAP, or X-Bar. The SYNC signal is defined by the selection in the ECAPxSYNCINSEL[SEL] bit for ECAPx as shown in Figure 6-61.

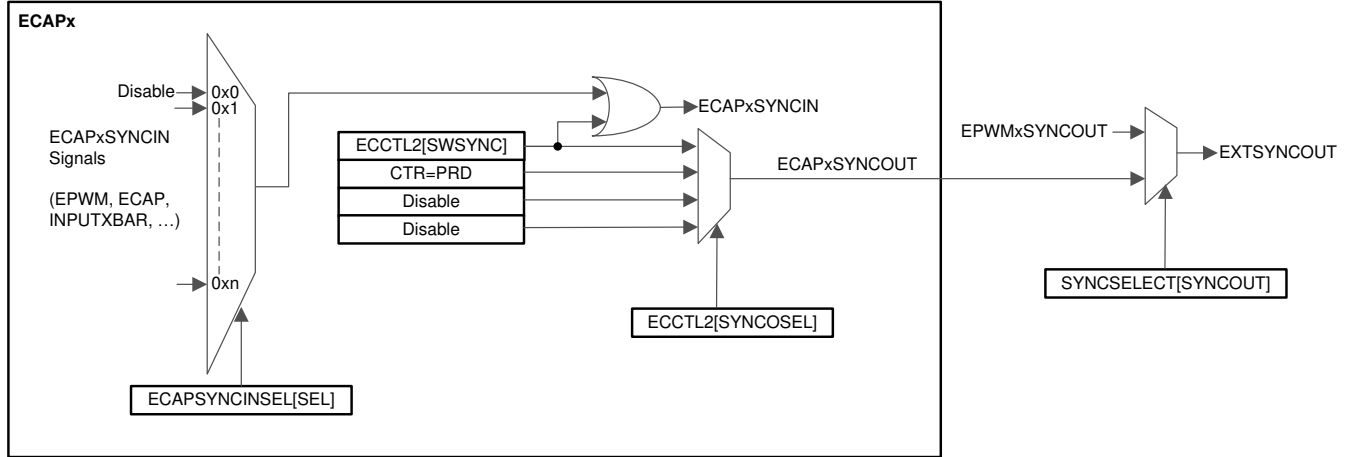


Figure 6-61. eCAP Synchronization Scheme

6.14.4.3 eCAP Electrical Data and Timing

6.14.4.3.1 eCAP Timing Requirements

| | | | MIN | NOM | MAX | UNIT |
|--------------|---------------------------|----------------------|--------------------------------|-----|-----|------|
| $t_{w(CAP)}$ | Capture input pulse width | Asynchronous | $2t_{c(SYSCLK)}$ | | | ns |
| | | Synchronous | $2t_{c(SYSCLK)}$ | | | |
| | | With input qualifier | $1t_{c(SYSCLK)} + t_{w_IQSW}$ | | | |

6.14.4.3.2 eCAP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---------------|---------------------------------------|-----|-----|-----|------|
| $t_{w(APWM)}$ | Pulse duration, APWMx output high/low | 20 | | | ns |

6.14.5 High-Resolution Capture (HRCAP)

The eCAP3 module can be configured as high-resolution capture (HRCAP) submodules. The HRCAP submodule measures the difference, in time, between pulses asynchronously to the system clock. This submodule is new to the eCAP Type 1 module, and features many enhancements over the Type 0 HRCAP module.

Applications for the HRCAP include:

- Capacitive touch applications
- High-resolution period and duty-cycle measurements of pulse train cycles
- Instantaneous speed measurements
- Instantaneous frequency measurements
- Voltage measurements across an isolation boundary
- Distance/sonar measurement and scanning
- Flow measurements

The HRCAP submodule includes the following features:

- Pulse-width capture in either non-high-resolution or high-resolution modes
- Absolute mode pulse-width capture
- Continuous or "one-shot" capture
- Capture on either falling or rising edge
- Continuous mode capture of pulse widths in 4-deep buffer
- Hardware calibration logic for precision high-resolution capture
- All of the resources in this list are available on any pin using the Input X-BAR.

The HRCAP submodule includes one high-resolution capture channel in addition to a calibration block. The calibration block allows the HRCAP submodule to be continually recalibrated, at a set interval, with no "down time". Because the HRCAP submodule now uses the same hardware as its respective eCAP, if the HRCAP is used, the corresponding eCAP will be unavailable.

Each high-resolution-capable channel has the following independent key resources.

- All hardware of the respective eCAP
- High-resolution calibration logic
- Dedicated calibration interrupt

6.14.5.1 eCAP and HRCAP Block Diagram

For the HRCAP Block Diagram, see the eCAP and HRCAP Block Diagram in the *Enhanced Capture (eCAP)* section.

6.14.5.2 HRCAP Electrical Data and Timing

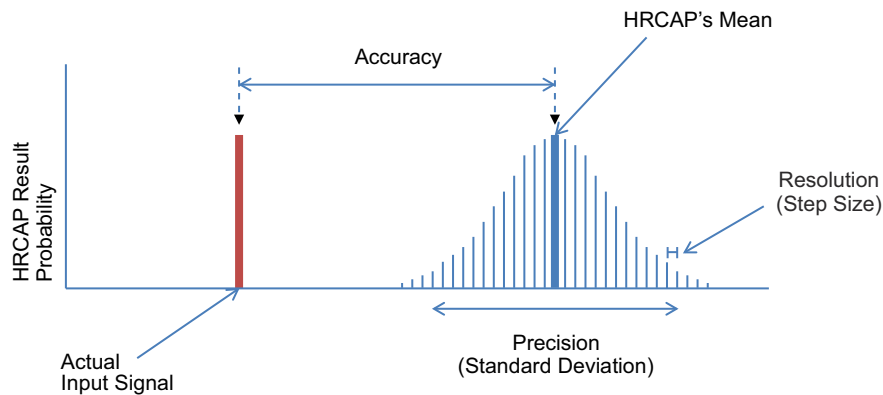
6.14.5.2.1 HRCAP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------------|---|-----|---|------|------|
| Input pulse width | | 110 | | | ns |
| Accuracy ^{(1) (2) (3) (4)} | Measurement length $\leq 5 \mu\text{s}$ | | ± 390 | 540 | ps |
| | Measurement length $> 5 \mu\text{s}$ | | ± 450 | 1450 | ps |
| Standard deviation | | | See HRCAP Standard Deviation Characteristics figure | | |
| Resolution | | | 300 | | ps |

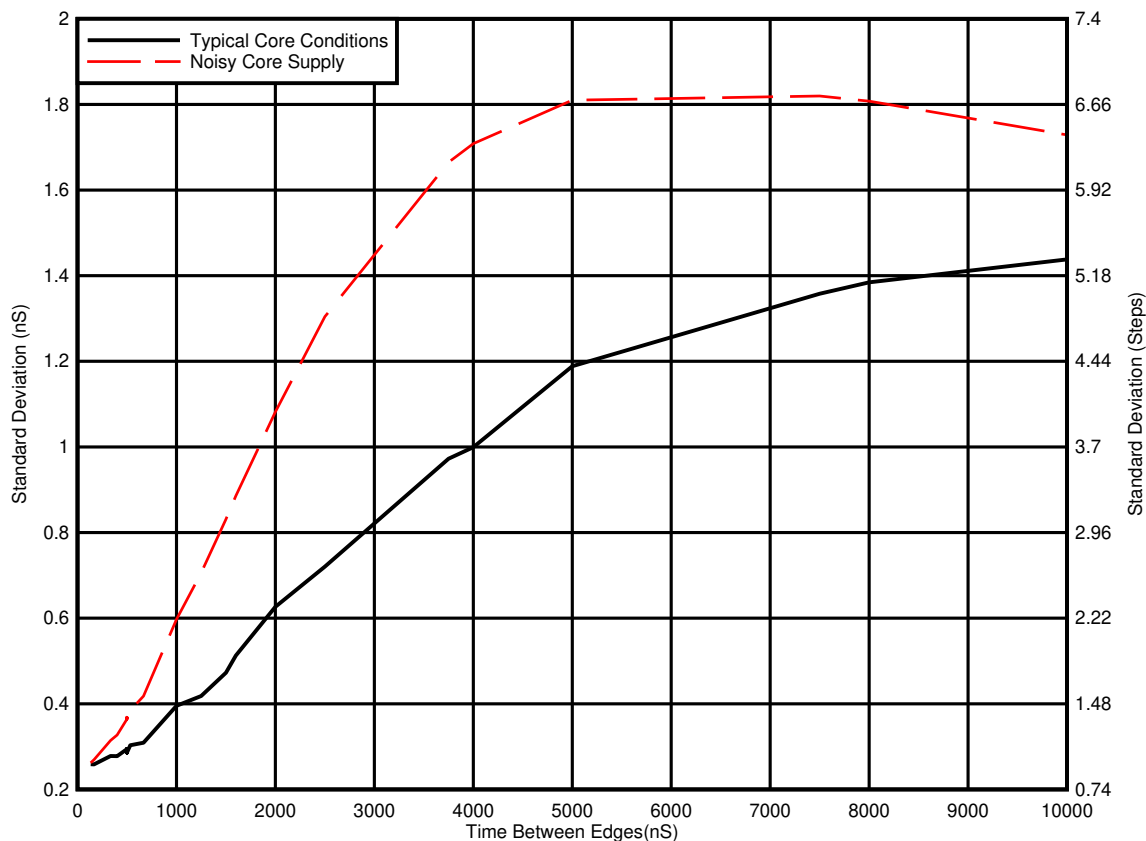
- (1) Value obtained using an oscillator of 100 PPM, oscillator accuracy directly affects the HRCAP accuracy.
- (2) Measurement is completed using rising-rising or falling-falling edges
- (3) Opposite polarity edges will have an additional inaccuracy due to the difference between V_{IH} and V_{IL} . This effect is dependent on the signal's slew rate.
- (4) Accuracy only applies to time-converted measurements.

6.14.5.2.2 HRCAP Figure and Graph



- A. The HRCAP has some variation in performance, this results in a probability distribution which is described using the following terms:
- Accuracy: The time difference between the input signal and the mean of the HRCAP's distribution.
 - Precision: The width of the HRCAP's distribution, this is given as a standard deviation.
 - Resolution: The minimum measurable increment.

Figure 6-62. HRCAP Accuracy Precision and Resolution



- A. Typical core conditions: All peripheral clocks are enabled.
- B. Noisy core supply: All core clocks are enabled and disabled with a regular period during the measurement.
- C. Fluctuations in current and voltage on the 1.2-V rail cause the standard deviation of the HRCAP to rise. Care should be taken to ensure that the 1.2-V supply is clean, and that noisy internal events, such as enabling and disabling clock trees, have been minimized while using the HRCAP.

Figure 6-63. HRCAP Standard Deviation Characteristics

6.14.6 Enhanced Quadrature Encoder Pulse (eQEP)

The eQEP module on this device is Type-2. The eQEP interfaces directly with linear or rotary incremental encoders to obtain position, direction, and speed information from rotating machines used in high-performance motion and position control systems.

The eQEP peripheral contains the following major functional units (see [Figure 6-64](#)):

- Programmable input qualification for each pin (part of the GPIO MUX)
- Quadrature decoder unit (QDU)
- Position counter and control unit for position measurement (PCCU)
- Quadrature edge-capture unit for low-speed measurement (QCAP)
- Unit time base for speed/frequency measurement (UTIME)
- Watchdog timer for detecting stalls (QWDOG)
- Quadrature Mode Adapter (QMA)

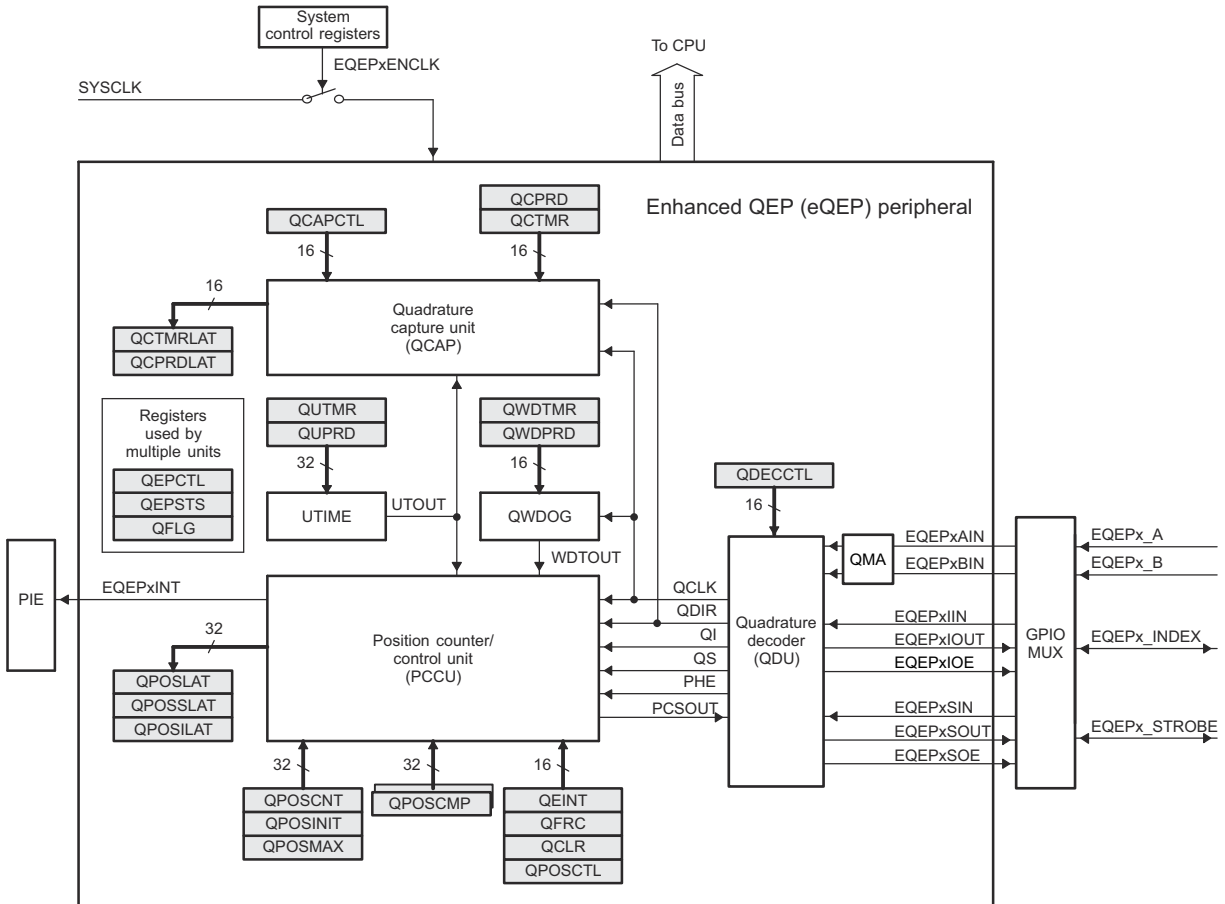


Figure 6-64. eQEP Block Diagram

6.14.6.1 eQEP Electrical Data and Timing

For an explanation of the input qualifier parameters, see the General-Purpose Input Timing Requirements table.

6.14.6.1.1 eQEP Timing Requirements

| | | | MIN | MAX | UNIT |
|-----------------|---------------------------|----------------------------------|-----------------------------------|-----|--------|
| $t_{w(QEPP)}$ | QEP input period | Synchronous ⁽¹⁾ | $2t_{c(SYSCLK)}$ | | cycles |
| | | Synchronous with input qualifier | $2[1t_{c(SYSCLK)} + t_{w(IQSW)}]$ | | |
| $t_{w(INDEXH)}$ | QEP Index Input High time | Synchronous ⁽¹⁾ | $2t_{c(SYSCLK)}$ | | cycles |
| | | Synchronous with input qualifier | $2t_{c(SYSCLK)} + t_{w(IQSW)}$ | | |
| $t_{w(INDEXL)}$ | QEP Index Input Low time | Synchronous ⁽¹⁾ | $2t_{c(SYSCLK)}$ | | cycles |
| | | Synchronous with input qualifier | $2t_{c(SYSCLK)} + t_{w(IQSW)}$ | | |
| $t_{w(STROBH)}$ | QEP Strobe High time | Synchronous ⁽¹⁾ | $2t_{c(SYSCLK)}$ | | cycles |
| | | Synchronous with input qualifier | $2t_{c(SYSCLK)} + t_{w(IQSW)}$ | | |
| $t_{w(STROBL)}$ | QEP Strobe Input Low time | Synchronous ⁽¹⁾ | $2t_{c(SYSCLK)}$ | | cycles |
| | | Synchronous with input qualifier | $2t_{c(SYSCLK)} + t_{w(IQSW)}$ | | |

(1) The GPIO GPxQSELn Asynchronous mode should not be used for eQEP module input pins.

6.14.6.1.2 eQEP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | MAX | UNIT |
|------------------------|--|-----|------------------|--------|
| $t_{d(CNTR)_{xin}}$ | Delay time, external clock to counter increment | | $5t_{c(SYSCLK)}$ | cycles |
| $t_{d(PCS-OUT)_{QEP}}$ | Delay time, QEP input edge to position compare sync output | | $7t_{c(SYSCLK)}$ | cycles |

6.14.7 Sigma-Delta Filter Module (SDFM)

SDFM features include:

- Eight external pins per SDFM module
 - Four sigma-delta data input pins per SDFM module (SD-Dx, where x = 1 to 4)
 - Four sigma-delta clock input pins per SDFM module (SD-Cx, where x = 1 to 4)
- Different configurable modulator clock modes supported:
 - Mode 0: Modulator clock rate equals the modulator data rate.
- Four independent, configurable secondary filter (comparator) units per SDFM module:
 - Four different filter type selection (Sinc1/Sinc2/SincFast/Sinc3) options available
 - Ability to detect over-value condition, under-value condition, and Threshold-crossing conditions
 1. Two independent Higher Threshold comparators (used to detect over-value condition)
 2. Two independent Lower Threshold comparators (used to detect under-value condition)
 3. One independent Threshold-Crossing comparator (used to measure duty cycle/frequency with eCAP)
 - OSR value for comparator filter unit (COSR) programmable from 1 to 32
- Four independent configurable primary filter (data filter) units per SDFM module:
 - Four different filter type selection (Sinc1/Sinc2/SincFast/Sinc3) options available
 - OSR value for data filter unit (DOSR) programmable from 1 to 256
 - Ability to enable or disable (or both) individual filter module
 - Ability to synchronize all four independent filters of an SDFM module by using the Main Filter Enable (MFE) bit or by using PWM signals
- Data filter output can be represented in either 16 bits or 32 bits.
- Data filter unit has a programmable mode FIFO to reduce interrupt overhead. The FIFO has the following features:
 - The primary filter (data filter) has a 16-deep x 32-bit FIFO.
 - The FIFO can interrupt the CPU after programmable number of data-ready events.
 - FIFO Wait-for-Sync feature: Ability to ignore data-ready events until the PWM synchronization signal (SDSYNC) is received. Once the SDSYNC event is received, the FIFO is populated on every data-ready event.
 - Data filter output can be represented in either 16 bits or 32 bits.
- PWMx.SOCA/SOCB can be configured to serve as SDSYNC source on a per-data-filter-channel basis.
- PWMs can be used to generate a modulator clock for sigma-delta modulators.
- Configurable Input Qualification available for both SD-Cx and SD-Dx
- Ability to use one filter channel clock (SD-C1) to provide clock to other filter clock channels.
- Configurable digital filter available on comparator filter events to blank out comparator events caused by spurious noise

Figure 6-65 shows the SDFM module block diagram.

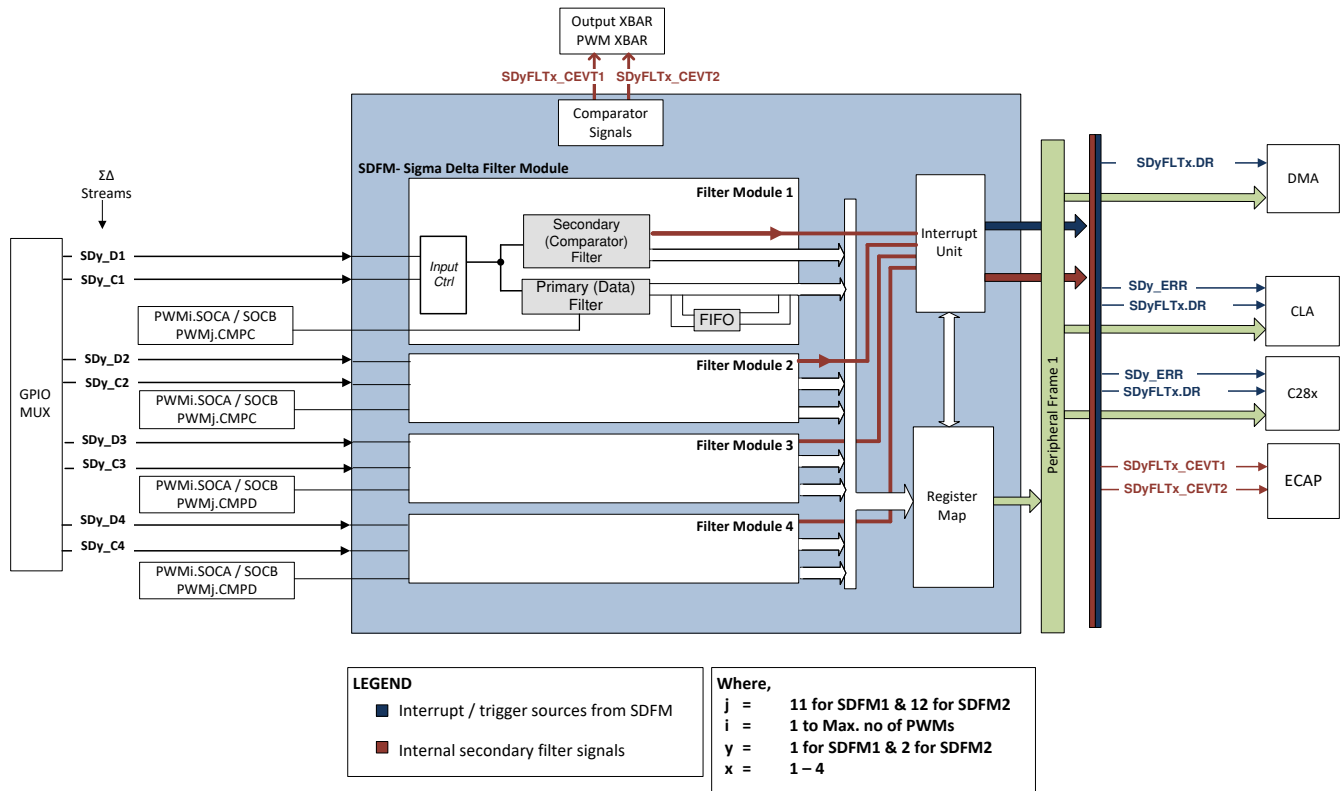


Figure 6-65. Sigma Delta Filter Module (SDFM) Block Diagram

6.14.7.1 SDFM Electrical Data and Timing

WARNING

Special precautions should be taken on both SD-Cx and SD-Dx signals to ensure a clean and noise-free signal that meets SDFM timing requirements. Precautions such as series termination resistors for ringing noise due to any impedance mismatch of clock driver and spacing of traces from other noisy signals are recommended.

Note

The SDFM SD-Cx and SD-Dx signals, when synchronized to PLLRAWCLK, provide protection against SDFM module corruption due to occasional random noise glitches that may result in a false comparator trip and filter output. However, the signals do not provide protection against persistent violations of the above timing requirements. Timing violations will result in data corruption proportional to the number of bits which violate the requirements.

6.14.7.1.1 SDFM Timing Requirements When Using Asynchronous GPIO - ASYNC - Option

| | | MIN | MAX | UNIT |
|-----------------------|--|----------------------------|-----------------------|------|
| Mode 0 | | | | |
| $t_{c(SDC)M0}$ | Cycle time, SDx_Cy | $4 * t_{c(PLLRAWCLK)}$ | $256 * SYSCLK$ period | ns |
| $t_{w(SDDL)M0}$ | Pulse duration, SDx_Dy (high / Low) | $2 * t_{c(PLLRAWCLK)}$ | | ns |
| $t_{su(SDDV-SDCH)M0}$ | Setup time, SDx_Dy valid before SDx_Cy goes high | $1 * t_{c(PLLRAWCLK)} + 3$ | | ns |
| $t_{h(SDCH-SDD)M0}$ | Hold time, SDx_Dy wait after SDx_Cy goes high | $1 * t_{c(PLLRAWCLK)} + 3$ | | ns |

6.15 Communications Peripherals

6.15.1 Controller Area Network (CAN)

Note

The CAN module uses the IP known as *DCAN*. This document uses the names *CAN* and *DCAN* interchangeably to reference this peripheral.

The CAN module implements the following features:

- Complies with ISO11898-1 (Bosch® CAN protocol specification 2.0 A and B)
- Bit rates up to 1 Mbps
- Multiple clock sources
- 32 message objects (mailboxes), each with the following properties:
 - Configurable as receive or transmit
 - Configurable with standard (11-bit) or extended (29-bit) identifier
 - Supports programmable identifier receive mask
 - Supports data and remote frames
 - Holds 0 to 8 bytes of data
 - Parity-checked configuration and data RAM
- Individual identifier mask for each message object
- Programmable FIFO mode for message objects
- Programmable loopback modes for self-test operation
- Suspend mode for debug support
- Software module reset
- Automatic bus on after bus-off state by a programmable 32-bit timer
- Two interrupt lines
- DMA support

Note

For a CAN bit clock of 100 MHz, the smallest bit rate possible is 3.90625Kbps.

Note

The accuracy of the on-chip zero-pin oscillator is in the INTOSC Characteristics table. Depending on parameters such as the CAN bit timing settings, bit rate, bus length, and propagation delay, the accuracy of this oscillator may not meet the requirements of the CAN protocol. In this situation, an external clock source must be used.

Figure 6-66 shows the CAN block diagram.

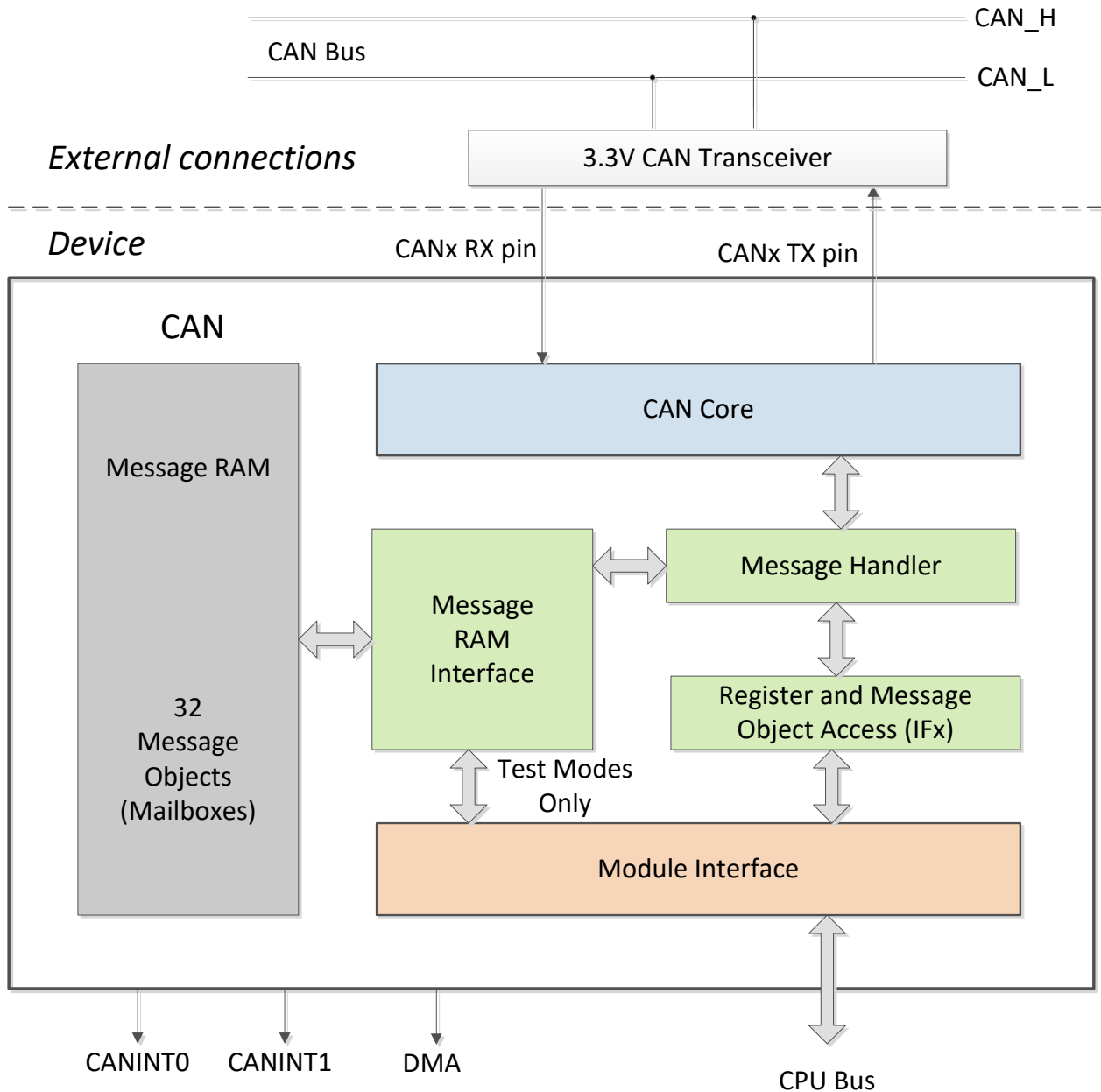


Figure 6-66. CAN Block Diagram

6.15.2 Modular Controller Area Network (MCAN)

The Controller Area Network (CAN) is a serial communications protocol that efficiently supports distributed real-time control with a high level of reliability. CAN has high immunity to electrical interference and the ability to detect various type of errors. In CAN, many short messages are broadcast to the entire network, which provides data consistency in every node of the system.

The MCAN module supports both classic CAN and CAN FD (CAN with flexible data-rate) protocols. The CAN FD feature allows higher throughput and increased payload per data frame. Classic CAN and CAN FD devices may coexist on the same network without any conflict provided that partial network transceivers, which can detect and ignore CAN FD without generating bus errors, are used by the classic CAN devices. The MCAN module is compliant to ISO 11898-1:2015.

Note

The availability of the CAN FD feature is dependent on the device's part number. Refer to the device data sheet for more information.

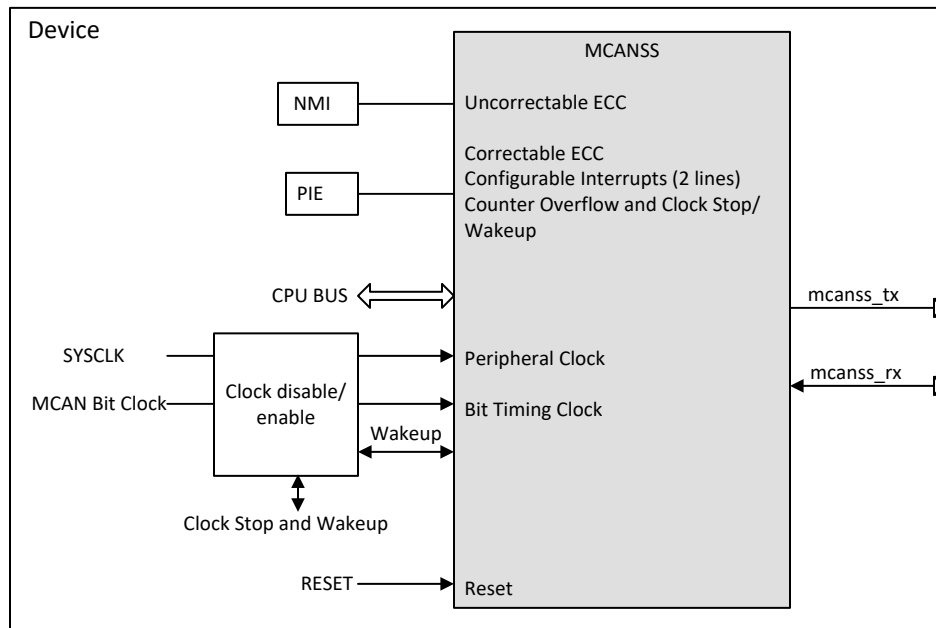


Figure 6-67. MCAN Module Overview

The MCAN module implements the following features:

- Conforms with CAN Protocol 2.0 A, B and ISO 11898-1:2015
- Full CAN FD support (up to 64 data bytes)
- AUTOSAR and SAE J1939 support
- Flexible Message RAM allocation (maximum configuration below is for a device with 4352 32-bit word message RAM)
 - Up to 32 dedicated transmit buffers
 - Configurable transmit FIFO, up to 32 elements
 - Configurable transmit queue, up to 32 elements
 - Configurable transmit Event FIFO, up to 32 elements
 - Up to 64 dedicated receive buffers
 - Two configurable receive FIFOs, up to 64 elements each
 - Up to 128 filter elements
- Loop-back mode for self-test
- Maskable interrupt (two configurable interrupt lines, correctable ECC, counter overflow and clock stop/wakeup)
- Non-maskable interrupt (uncorrectable ECC)
- Two clock domains (CAN clock/host clock)
- ECC check for Message RAM
- Clock stop and wake-up support
- Timestamp counter

Non-supported features:

- Host bus firewall
- Clock calibration
- Debug over CAN

6.15.3 Inter-Integrated Circuit (I2C)

The I2C module has the following features:

- Compliance with the NXP Semiconductors I²C-bus specification (version 2.1):
 - Support for 8-bit format transfers
 - 7-bit and 10-bit addressing modes
 - General call
 - START byte mode
 - Support for multiple master-transmitters and slave-receivers
 - Support for multiple slave-transmitters and master-receivers
 - Combined master transmit/receive and receive/transmit mode
 - Data transfer rate from 10Kbps up to 400Kbps (Fast-mode)
- Supports voltage thresholds compatible to:
 - SMBus 2.0 and below
 - PMBus 1.2 and below
- One 16-byte receive FIFO and one 16-byte transmit FIFO
- Supports two ePIE interrupts
 - I2Cx interrupt – Any of the below conditions can be configured to generate an I2Cx interrupt:
 - Transmit Ready
 - Receive Ready
 - Register-Access Ready
 - No-Acknowledgment
 - Arbitration-Lost
 - Stop Condition Detected
 - Addressed-as-Slave
 - I2Cx_FIFO interrupts:
 - Transmit FIFO interrupt
 - Receive FIFO interrupt
- Module enable and disable capability
- Free data format mode

Figure 6-68 shows how the I2C peripheral module interfaces within the device.

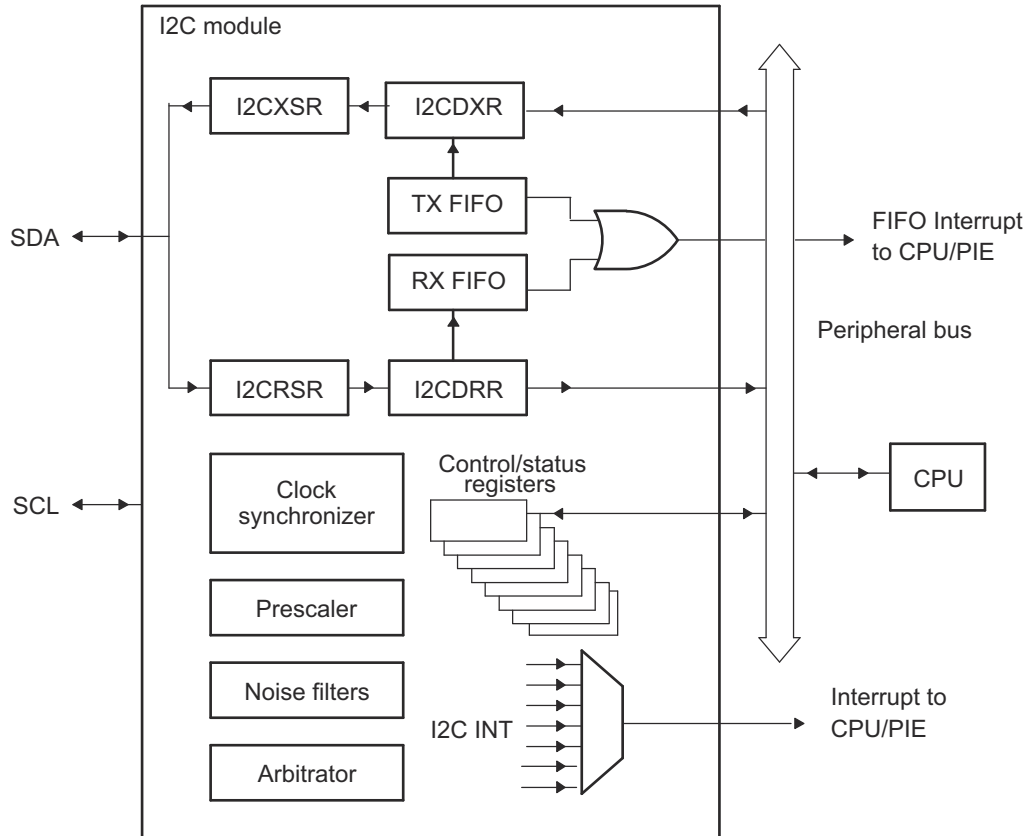


Figure 6-68. I2C Peripheral Module Interfaces

6.15.3.1 I2C Electrical Data and Timing

Note

To meet all of the I2C protocol timing specifications, the I2C module clock must be configured in the range from 7 MHz to 12 MHz.

A pullup resistor must be chosen to meet the I2C standard timings. In most circumstances, 2.2 kΩ of total bus resistance to VDDIO is sufficient. For evaluating pullup resistor values for a particular design, see the [I2C Bus Pullup Resistor Calculation](#) Application Report.

6.15.3.1.1 I2C Timing Requirements

| NO. | | | MIN | MAX | UNIT |
|----------------------|-------------------------------|--|--------------------|---------------------|------|
| Standard mode | | | | | |
| T0 | f_{mod} | I2C module frequency | 7 | 12 | MHz |
| T1 | $t_{\text{h(SDA-SCL)START}}$ | Hold time, START condition, SCL fall delay after SDA fall | 4.0 | | μs |
| T2 | $t_{\text{su(SCL-SDA)START}}$ | Setup time, Repeated START, SCL rise before SDA fall delay | 4.0 | | μs |
| T3 | $t_{\text{h(SCL-DAT)}}$ | Hold time, data after SCL fall | 0 | | μs |
| T4 | $t_{\text{su(DAT-SCL)}}$ | Setup time, data before SCL rise | 250 ⁽²⁾ | | ns |
| T5 | $t_{\text{r(SDA)}}$ | Rise time, SDA | | 1000 ⁽¹⁾ | ns |
| T6 | $t_{\text{r(SCL)}}$ | Rise time, SCL | | 1000 ⁽¹⁾ | ns |
| T7 | $t_{\text{f(SDA)}}$ | Fall time, SDA | | 300 | ns |
| T8 | $t_{\text{f(SCL)}}$ | Fall time, SCL | | 300 | ns |
| T9 | $t_{\text{su(SCL-SDA)STOP}}$ | Setup time, STOP condition, SCL rise before SDA rise delay | 4.0 | | μs |
| T10 | $t_{\text{w(SP)}}$ | Pulse duration of spikes that will be suppressed by filter | 0 | 50 | ns |
| T11 | C_{b} | capacitance load on each bus line | | 400 | pF |
| Fast mode | | | | | |
| T0 | f_{mod} | I2C module frequency | 7 | 12 | MHz |
| T1 | $t_{\text{h(SDA-SCL)START}}$ | Hold time, START condition, SCL fall delay after SDA fall | 0.6 | | μs |
| T2 | $t_{\text{su(SCL-SDA)START}}$ | Setup time, Repeated START, SCL rise before SDA fall delay | 0.6 | | μs |
| T3 | $t_{\text{h(SCL-DAT)}}$ | Hold time, data after SCL fall | 0 | | μs |
| T4 | $t_{\text{su(DAT-SCL)}}$ | Setup time, data before SCL rise | 100 | | ns |
| T5 | $t_{\text{r(SDA)}}$ | Rise time, SDA | 20 | 300 | ns |
| T6 | $t_{\text{r(SCL)}}$ | Rise time, SCL | 20 | 300 | ns |
| T7 | $t_{\text{f(SDA)}}$ | Fall time, SDA | 11.4 | 300 | ns |
| T8 | $t_{\text{f(SCL)}}$ | Fall time, SCL | 11.4 | 300 | ns |
| T9 | $t_{\text{su(SCL-SDA)STOP}}$ | Setup time, STOP condition, SCL rise before SDA rise delay | 0.6 | | μs |
| T10 | $t_{\text{w(SP)}}$ | Pulse duration of spikes that will be suppressed by filter | 0 | 50 | ns |
| T11 | C_{b} | capacitance load on each bus line | | 400 | pF |

- (1) In order to minimize the rise time, TI recommends using a strong pullup on both the SDA and SCL bus lines on the order of 2.2-kΩ net pullup resistance. It is also recommended that the value of the pullup resistance used on both SCL and SDA pins be matched.
- (2) The C2000 I2C is a Fast-mode device. There is a limitation when using the I2C as a target transmitter with a standard mode host. For more information, see the [TMS320F28003x Real-Time MCUs Silicon Errata](#).

6.15.3.1.2 I2C Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| NO. | PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT | |
|----------------------|------------------|---|-----------------------------------|------|---------|---------|
| Standard mode | | | | | | |
| S1 | f_{SCL} | SCL clock frequency | 0 | 100 | kHz | |
| S2 | T_{SCL} | SCL clock period | 10 | | μs | |
| S3 | $t_{w(SCLL)}$ | Pulse duration, SCL clock low | 4.7 | | μs | |
| S4 | $t_{w(SCLH)}$ | Pulse duration, SCL clock high | 4.0 | | μs | |
| S5 | t_{BUF} | Bus free time between STOP and START conditions | 4.7 | | μs | |
| S6 | $t_{v(SCL-DAT)}$ | Valid time, data after SCL fall | | 3.45 | μs | |
| S7 | $t_{v(SCL-ACK)}$ | Valid time, Acknowledge after SCL fall | | 3.45 | μs | |
| S8 | I_I | Input current on pins | $0.1 V_{bus} < V_i < 0.9 V_{bus}$ | -10 | 10 | μA |
| Fast mode | | | | | | |
| S1 | f_{SCL} | SCL clock frequency | 0 | 400 | kHz | |
| S2 | T_{SCL} | SCL clock period | 2.5 | | μs | |
| S3 | $t_{w(SCLL)}$ | Pulse duration, SCL clock low | 1.3 | | μs | |
| S4 | $t_{w(SCLH)}$ | Pulse duration, SCL clock high | 0.6 | | μs | |
| S5 | t_{BUF} | Bus free time between STOP and START conditions | 1.3 | | μs | |
| S6 | $t_{v(SCL-DAT)}$ | Valid time, data after SCL fall | | 0.9 | μs | |
| S7 | $t_{v(SCL-ACK)}$ | Valid time, Acknowledge after SCL fall | | 0.9 | μs | |
| S8 | I_I | Input current on pins | $0.1 V_{bus} < V_i < 0.9 V_{bus}$ | -10 | 10 | μA |

6.15.3.1.3 I2C Timing Diagram

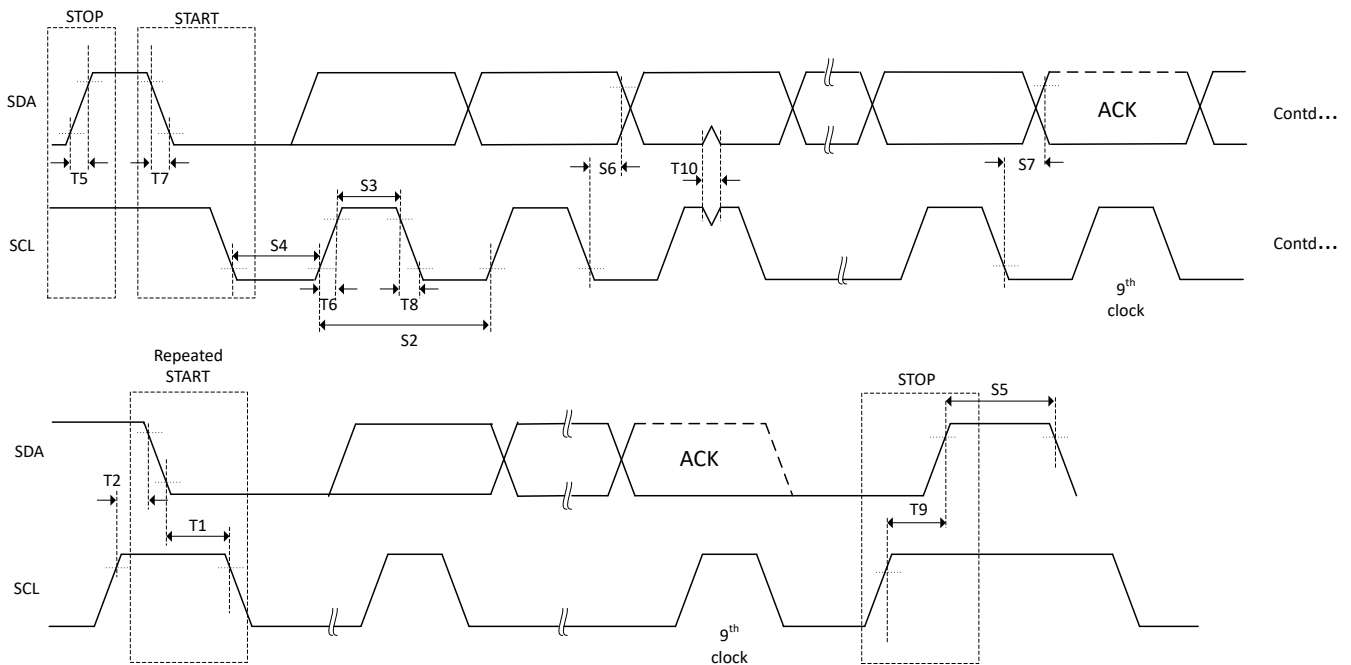


Figure 6-69. I2C Timing Diagram

6.15.4 Power Management Bus (PMBus) Interface

The PMBus module has the following features:

- Compliance with the SMI Forum PMBus Specification (Part I v1.0 and Part II v1.1)
- Supports voltage thresholds compatible to:
 - PMBus 1.2 and below
 - SMBus 2.0 and below
- Support for master and slave modes
- Support for I2C mode
- Support for two speeds:
 - Standard Mode: Up to 100 kHz
 - Fast Mode: 400 kHz
- Packet error checking
- CONTROL and ALERT signals
- Clock high and low time-outs
- Four-byte transmit and receive buffers
- One maskable interrupt, which can be generated by several conditions:
 - Receive data ready
 - Transmit buffer empty
 - Slave address received
 - End of message
 - ALERT input asserted
 - Clock low time-out
 - Clock high time-out
 - Bus free

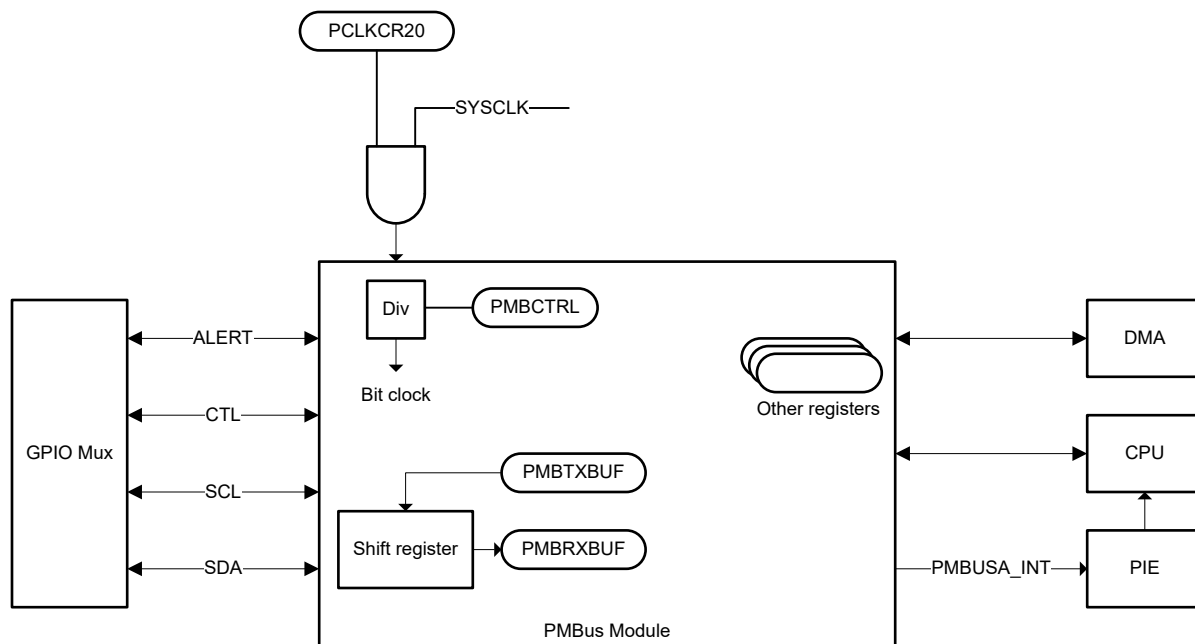


Figure 6-70. PMBus Block Diagram

6.15.4.1 PMBus Electrical Data and Timing

6.15.4.1.1 PMBus Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|---|--|-----|-------|-----|------|
| V _{IL} | Valid low-level input voltage | | | | 0.8 | V |
| V _{IH} | Valid high-level input voltage | | 2.1 | VDDIO | | V |
| V _{OL} | Low-level output voltage | At I _{pullup} = 4 mA | | | 0.4 | V |
| I _{OL} | Low-level output current | V _{OL} ≤ 0.4 V | 4 | | | mA |
| t _{SP} | Pulse width of spikes that must be suppressed by the input filter | | 0 | | 50 | ns |
| I _i | Input leakage current on each pin | 0.1 V _{bus} < V _i < 0.9 V _{bus} | -10 | | 10 | μA |
| C _i | Capacitance on each pin | | | | 10 | pF |

6.15.4.1.2 PMBus Fast Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|---|--------------------|----------------|-----|-----|------|
| f _{FSM_CLK} | FSM_CLK clock frequency | | SYSCLK K/32 | | 10 | MHz |
| f _{SCL} | SCL clock frequency | | 10 | | 400 | kHz |
| t _{BUF} | Bus free time between STOP and START conditions | | 1.3 | | | μs |
| t _{HD;STA} | START condition hold time -- SDA fall to SCL fall delay | | 0.6 | | | μs |
| t _{SU;STA} | Repeated START setup time -- SCL rise to SDA fall delay | | 0.6 | | | μs |
| t _{SU;STO} | STOP condition setup time -- SCL rise to SDA rise delay | | 0.6 | | | μs |
| t _{HD;DAT} | Data hold time after SCL fall | | 300 | | | ns |
| t _{SU;DAT} | Data setup time before SCL rise | | 100 | | | ns |
| t _{Timeout} | Clock low time-out | | 25 | | 35 | ms |
| t _{LOW} | Low period of the SCL clock | | 1.3 | | | μs |
| t _{HIGH} | High period of the SCL clock | | 0.6 | | 50 | μs |
| t _{LOW;SEXT} | Cumulative clock low extend time (slave device) | From START to STOP | | | 25 | ms |
| t _{LOW;MEXT} | Cumulative clock low extend time (master device) | Within each byte | | | 10 | ms |
| t _r | Rise time of SDA and SCL | 5% to 95% | 20 | | 300 | ns |
| t _f | Fall time of SDA and SCL | 95% to 5% | 20 | | 300 | ns |

6.15.4.1.3 PMBus Standard Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|---|--------------------|---------------|-----|------|------|
| f _{FSM_CLK} | FSM_CLK clock frequency | | SYSCL K/32 | | 10 | MHz |
| f _{SCL} | SCL clock frequency | | 10 | | 100 | kHz |
| t _{BUF} | Bus free time between STOP and START conditions | | 4.7 | | | μs |
| t _{HD;STA} | START condition hold time -- SDA fall to SCL fall delay | | 4 | | | μs |
| t _{SU;STA} | Repeated START setup time -- SCL rise to SDA fall delay | | 4.7 | | | μs |
| t _{SU;STO} | STOP condition setup time -- SCL rise to SDA rise delay | | 4 | | | μs |
| t _{HD;DAT} | Data hold time after SCL fall | | 300 | | | ns |
| t _{SU;DAT} | Data setup time before SCL rise | | 250 | | | ns |
| t _{Timeout} | Clock low time-out | | 25 | | 35 | ms |
| t _{LOW} | Low period of the SCL clock | | 4.7 | | | μs |
| t _{HIGH} | High period of the SCL clock | | 4 | | 50 | μs |
| t _{LOW;SEXT} | Cumulative clock low extend time (slave device) | From START to STOP | | | 25 | ms |
| t _{LOW;MEXT} | Cumulative clock low extend time (master device) | Within each byte | | | 10 | ms |
| t _r | Rise time of SDA and SCL | | | | 1000 | ns |
| t _f | Fall time of SDA and SCL | | | | 300 | ns |

6.15.5 Serial Communications Interface (SCI)

The SCI is a 2-wire asynchronous serial port, commonly known as a UART. The SCI module supports digital communications between the CPU and other asynchronous peripherals that use the standard non-return-to-zero (NRZ) format

The SCI receiver and transmitter each have a 16-level-deep FIFO for reducing servicing overhead, and each has its own separate enable and interrupt bits. Both can be operated independently for half-duplex communication, or simultaneously for full-duplex communication. To specify data integrity, the SCI checks received data for break detection, parity, overrun, and framing errors. The bit rate is programmable to different speeds through a 16-bit baud-select register.

Features of the SCI module include:

- Two external pins:
 - SCITXD: SCI transmit-output pin
 - SCIRXD: SCI receive-input pin
 - Baud rate programmable to 64K different rates
- Data-word format
 - 1 start bit
 - Data-word length programmable from 1 to 8 bits
 - Optional even/odd/no parity bit
 - 1 or 2 stop bits
- Four error-detection flags: parity, overrun, framing, and break detection
- Two wake-up multiprocessor modes: idle-line and address bit
- Half- or full-duplex operation
- Double-buffered receive and transmit functions
- Transmitter and receiver operations can be accomplished through interrupt-driven or polled algorithms with status flags.
 - Transmitter: TXRDY flag (transmitter-buffer register is ready to receive another character) and TX EMPTY flag (transmitter-shift register is empty)
 - Receiver: RXRDY flag (receiver-buffer register is ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR flag (monitoring four interrupt conditions)
- Separate enable bits for transmitter and receiver interrupts (except BRKDT)
- NRZ format
- Auto baud-detect hardware logic
- 16-level transmit and receive FIFO

Note

All registers in this module are 8-bit registers. When a register is accessed, the register data is in the lower byte (bits 7–0), and the upper byte (bits 15–8) is read as zeros. Writing to the upper byte has no effect.

Figure 6-71 shows the SCI block diagram.

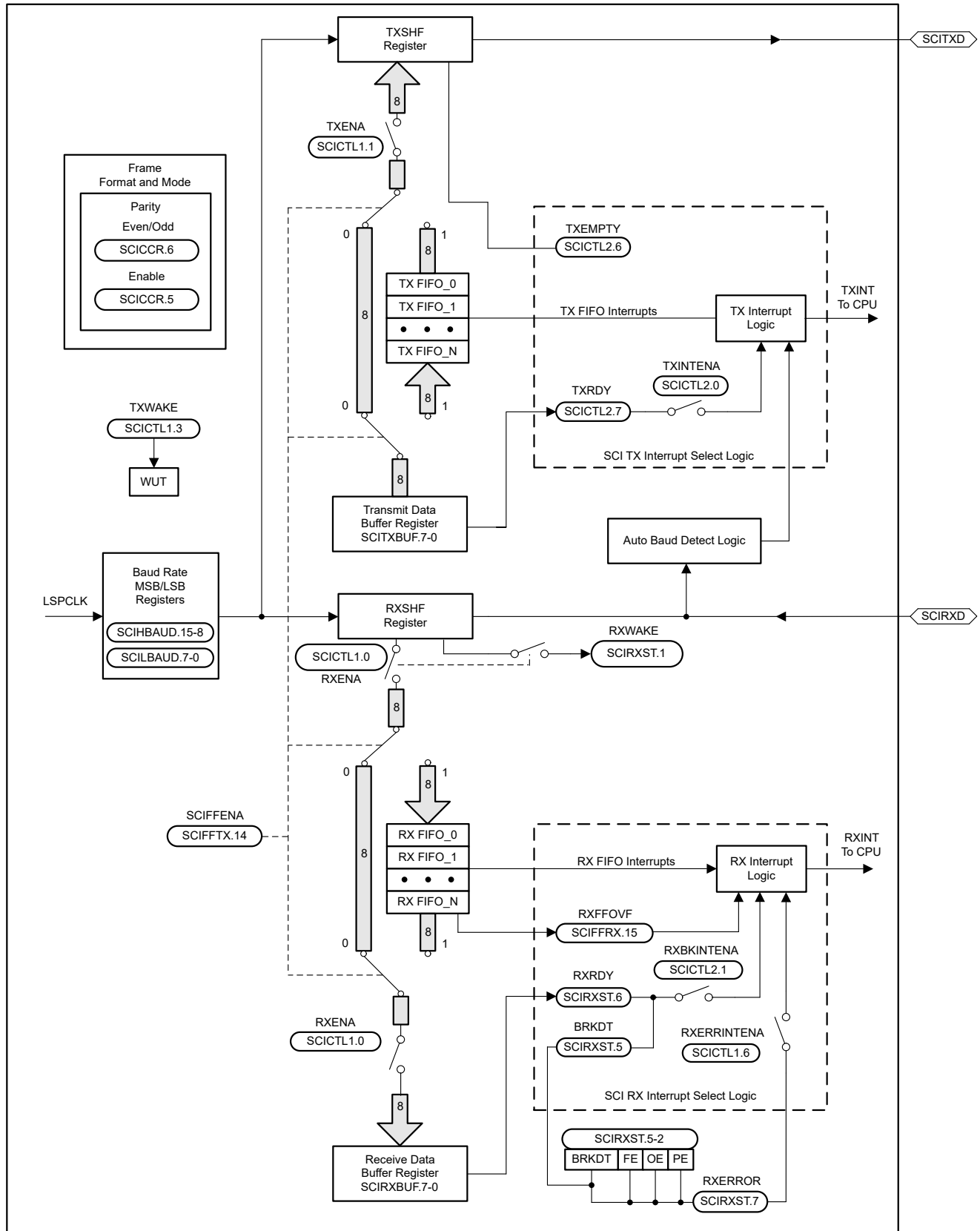


Figure 6-71. SCI Block Diagram

6.15.6 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) is a high-speed synchronous serial input and output (I/O) port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI is normally used for communications between the MCU controller and external peripherals or another controller. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and analog-to-digital converters (ADCs). Multidevice communications are supported by the master or slave operation of the SPI. The port supports a 16-level, receive and transmit FIFO for reducing CPU servicing overhead.

The SPI module features include:

- SPISOMI: SPI slave-output/master-input pin
- SPISIMO: SPI slave-input/master-output pin
- SPISTE: SPI slave transmit-enable pin
- SPICLK: SPI serial-clock pin
- Two operational modes: Master and Slave
- Baud rate: 125 different programmable rates. The maximum baud rate that can be employed is limited by the maximum speed of the I/O buffers used on the SPI pins.
- Data word length: 1 to 16 data bits
- Four clocking schemes (controlled by clock polarity and clock phase bits) include:
 - Falling edge without phase delay: SPICLK active-high. SPI transmits data on the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
 - Falling edge with phase delay: SPICLK active-high. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
 - Rising edge without phase delay: SPICLK inactive-low. SPI transmits data on the rising edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
 - Rising edge with phase delay: SPICLK inactive-low. SPI transmits data one half-cycle ahead of the rising edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
- Simultaneous receive and transmit operation (transmit function can be disabled in software)
- Transmitter and receiver operations are accomplished through either interrupt-driven or polled algorithm
- 16-level transmit/receive FIFO
- DMA support
- High-speed mode
- Delayed transmit control
- 3-wire SPI mode
- SPISTE inversion for digital audio interface receive mode on devices with two SPI modules

Figure 6-72 shows the SPI CPU interfaces.

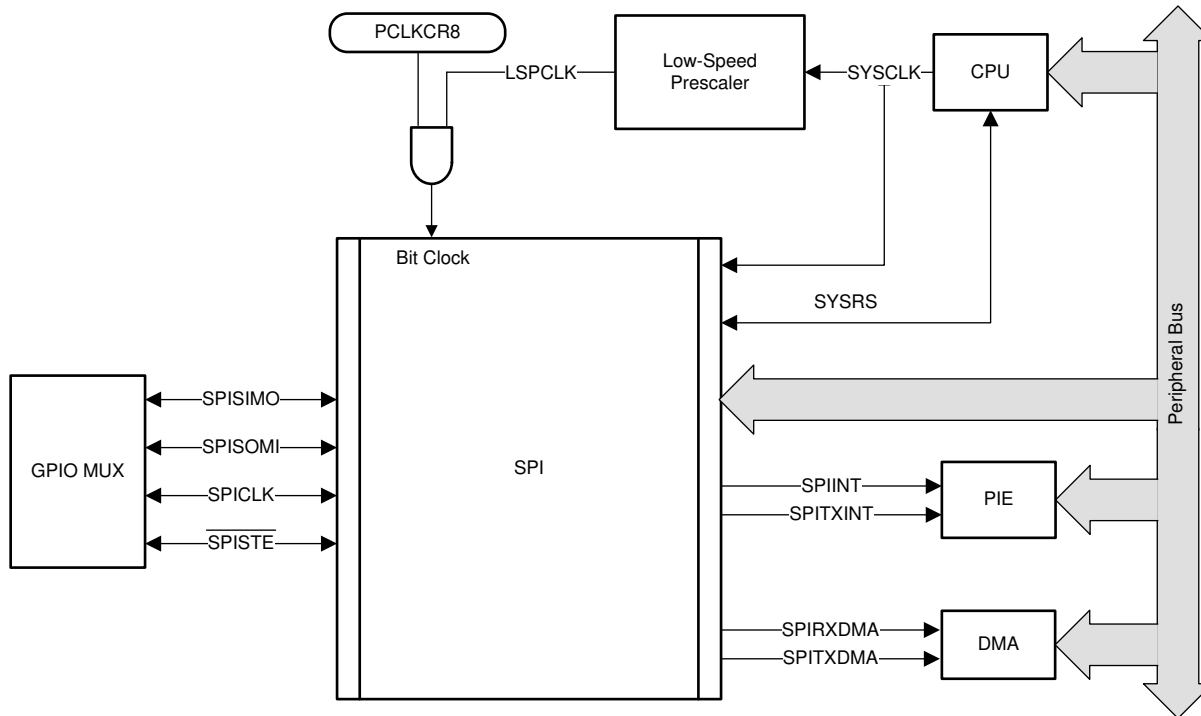


Figure 6-72. SPI CPU Interface

6.15.6.1 SPI Master Mode Timings

The following section contains the SPI Master Mode Timings. For more information about the SPI in High-Speed mode, see the Serial Peripheral Interface (SPI) chapter of the [TMS320F28003x Real-Time Microcontrollers Technical Reference Manual](#).

Note

All timing parameters for SPI High-Speed Mode assume a load capacitance of 5 pF on SPICLK, SPISIMO, and SPISOMI.

6.15.6.1.1 SPI Master Mode Timing Requirements

| NO. | | | (BRR + 1) ⁽¹⁾ | MIN | MAX | UNIT |
|------------------------|-----------------|---|--------------------------|-----|-----|------|
| High-Speed Mode | | | | | | |
| 8 | $t_{su(SOMI)M}$ | Setup time, SPISOMI valid before SPICLK | Even, Odd | 1 | | ns |
| 9 | $t_{h(SOMI)M}$ | Hold time, SPISOMI valid after SPICLK | Even, Odd | 6.5 | | ns |
| Normal Mode | | | | | | |
| 8 | $t_{su(SOMI)M}$ | Setup time, SPISOMI valid before SPICLK | Even, Odd | 15 | | ns |
| 9 | $t_{h(SOMI)M}$ | Hold time, SPISOMI valid after SPICLK | Even, Odd | 0 | | ns |

- (1) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.

6.15.6.1.2 SPI Master Mode Switching Characteristics - Clock Phase 0

over recommended operating conditions (unless otherwise noted)

| NO. | PARAMETER ⁽¹⁾ (2) | (BRR + 1) ⁽³⁾ | MIN | MAX | UNIT |
|------------------------|------------------------------|--|-----------|---|---------|
| General | | | | | |
| 1 | $t_{c(SPC)M}$ | Cycle time, SPICLK | Even | $4t_{c(LSPCLK)}$ $128t_{c(LSPCLK)}$ | ns |
| | | | Odd | $5t_{c(LSPCLK)}$ $127t_{c(LSPCLK)}$ | |
| 2 | $t_{w(SPC1)M}$ | Pulse duration, SPICLK, first pulse | Even | $0.5t_{c(SPC)M} - 1$ $0.5t_{c(SPC)M} + 1$ | ns |
| | | | Odd | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$ $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 1$ | |
| 3 | $t_{w(SPC2)M}$ | Pulse duration, SPICLK, second pulse | Even | $0.5t_{c(SPC)M} - 1$ $0.5t_{c(SPC)M} + 1$ | ns |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$ $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 1$ | |
| 23 | $t_{d(SPC)M}$ | Delay time, \overline{SPISTE} active to SPICLK | Even | $1.5t_{c(SPC)M} - 3t_{c(SYSCLK)} - 3$ $1.5t_{c(SPC)M} - 3t_{c(SYSCLK)} + 3$ | ns |
| | | | Odd | $1.5t_{c(SPC)M} - 4t_{c(SYSCLK)} - 3$ $1.5t_{c(SPC)M} - 4t_{c(SYSCLK)} + 3$ | |
| 24 | $t_{v(STE)M}$ | Valid time, SPICLK to \overline{SPISTE} inactive | Even | $0.5t_{c(SPC)M} - 3$ $0.5t_{c(SPC)M} + 3$ | ns |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$ $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 3$ | |
| High-Speed Mode | | | | | |
| 4 | $t_{d(SIMO)M}$ | Delay time, SPICLK to SPISIMO valid | Even, Odd | | 1 ns |
| 5 | $t_{v(SIMO)M}$ | Valid time, SPISIMO valid after SPICLK | Even | $0.5t_{c(SPC)M} - 3$ | ns |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$ | |
| Normal Mode | | | | | |
| 4 | $t_{d(SIMO)M}$ | Delay time, SPICLK to SPISIMO valid | Even, Odd | | 2 ns |
| 5 | $t_{v(SIMO)M}$ | Valid time, SPISIMO valid after SPICLK | Even | $0.5t_{c(SPC)M} - 3$ | ns |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$ | |

(1) 10-pF load on pin for High-Speed Mode.

(2) 20-pF load on pin for Normal Mode.

(3) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.

6.15.6.1.3 SPI Master Mode Switching Characteristics - Clock Phase 1

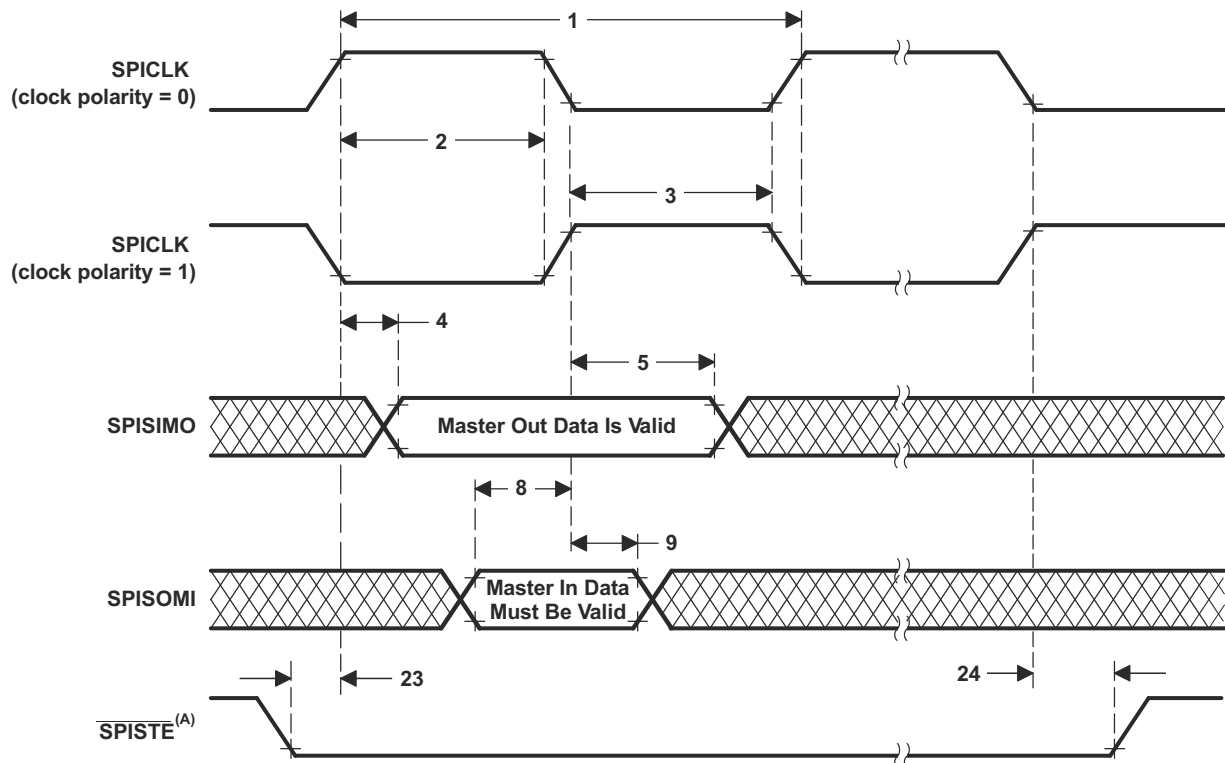
over recommended operating conditions (unless otherwise noted)

| NO. | PARAMETER ^{(1) (2)} | (BRR + 1) | MIN | MAX | UNIT | |
|------------------------|------------------------------|---|-----------|---|---|----|
| General | | | | | | |
| 1 | $t_{c(SPC)M}$ | Cycle time, SPICLK | Even | $4t_{c(LSPCLK)}$ | $128t_{c(LSPCLK)}$ | ns |
| | | | Odd | $5t_{c(LSPCLK)}$ | $127t_{c(LSPCLK)}$ | |
| 2 | $t_{w(SPCH)M}$ | Pulse duration, SPICLK, first pulse | Even | $0.5t_{c(SPC)M} - 1$ | $0.5t_{c(SPC)M} + 1$ | ns |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$ | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 1$ | |
| 3 | $t_{w(SPC2)M}$ | Pulse duration, SPICLK, second pulse | Even | $0.5t_{c(SPC)M} - 1$ | $0.5t_{c(SPC)M} + 1$ | ns |
| | | | Odd | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$ | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 1$ | |
| 23 | $t_{d(SPC)M}$ | Delay time, \overline{SPISTE} valid to SPICLK | Even, Odd | $2t_{c(SPC)M} - 3t_{c(SYSCCLK)} - 3$ | $2t_{c(SPC)M} - 3t_{c(SYSCCLK)} + 3$ | ns |
| 24 | $t_{d(STE)M}$ | Delay time, SPICLK to \overline{SPISTE} invalid | Even | -3 | 3 | ns |
| | | | Odd | -3 | 3 | |
| High-Speed Mode | | | | | | |
| 4 | $t_{d(SIMO)M}$ | Delay time, SPISIMO valid to SPICLK | Even | $0.5t_{c(SPC)M} - 2$ | | ns |
| | | | Odd | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 2$ | | |
| 5 | $t_{v(SIMO)M}$ | Valid time, SPISIMO valid after SPICLK | Even | $0.5t_{c(SPC)M} - 3$ | | ns |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$ | | |
| Normal Mode | | | | | | |
| 4 | $t_{d(SIMO)M}$ | Delay time, SPISIMO valid to SPICLK | Even | $0.5t_{c(SPC)M} - 2$ | | ns |
| | | | Odd | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 2$ | | |
| 5 | $t_{v(SIMO)M}$ | Valid time, SPISIMO valid after SPICLK | Even | $0.5t_{c(SPC)M} - 3$ | | ns |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$ | | |

(1) 10-pF load on pin for High-Speed Mode.

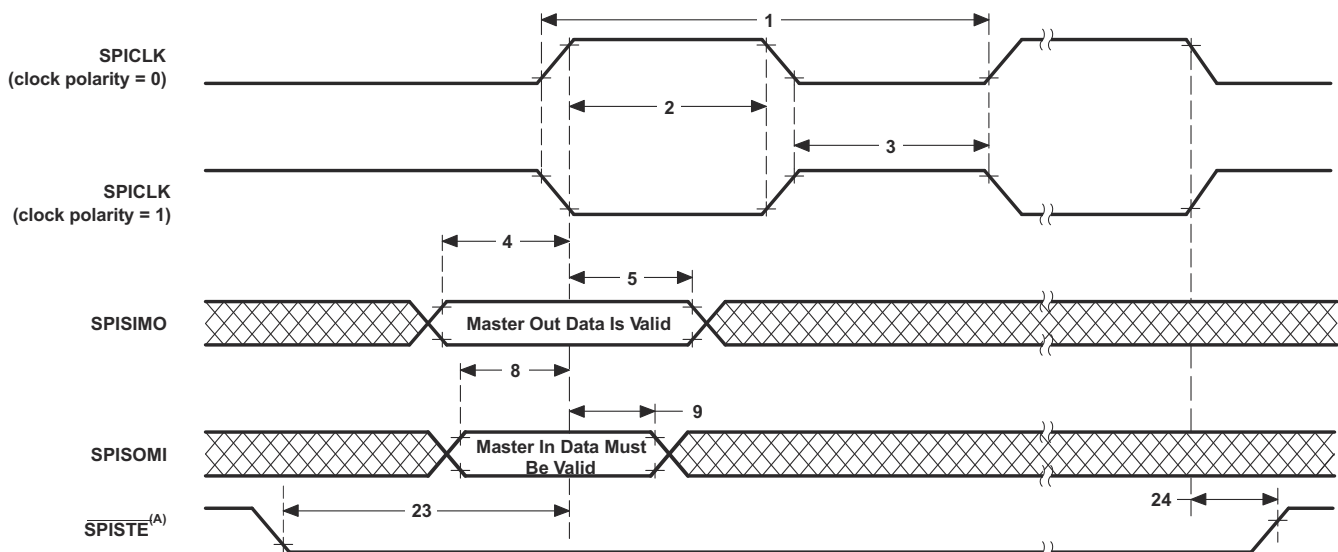
(2) 20-pF load on pin for Normal Mode.

6.15.6.1.4 SPI Master Mode Timing Diagrams



- A. On the trailing end of the word, $\overline{\text{SPISTE}}$ will go inactive except between back-to-back transmit words in both FIFO and non-FIFO modes.

Figure 6-73. SPI Master Mode External Timing (Clock Phase = 0)



- A. On the trailing end of the word, $\overline{\text{SPISTE}}$ will go inactive except between back-to-back transmit words in both FIFO and non-FIFO modes.

Figure 6-74. SPI Master Mode External Timing (Clock Phase = 1)

6.15.6.2 SPI Slave Mode Timings

The following section contains the SPI Slave Mode Timings. For more information about the SPI in High-Speed mode, see the Serial Peripheral Interface (SPI) chapter of the [TMS320F28003x Real-Time Microcontrollers Technical Reference Manual](#).

6.15.6.2.1 SPI Slave Mode Timing Requirements

| NO. | | | MIN | MAX | UNIT |
|-----|-----------------|--|-----------------------|-----|------|
| 12 | $t_{c(SPC)}S$ | Cycle time, SPICLK | $4t_{c(SYSCLK)}$ | | ns |
| 13 | $t_{w(SPC1)}S$ | Pulse duration, SPICLK, first pulse | $2t_{c(SYSCLK)} - 1$ | | ns |
| 14 | $t_{w(SPC2)}S$ | Pulse duration, SPICLK, second pulse | $2t_{c(SYSCLK)} - 1$ | | ns |
| 19 | $t_{su(SIMO)}S$ | Setup time, SPISIMO valid before SPICLK | $1.5t_{c(SYSCLK)}$ | | ns |
| 20 | $t_{h(SIMO)}S$ | Hold time, SPISIMO valid after SPICLK | $1.5t_{c(SYSCLK)}$ | | ns |
| 25 | $t_{su(STE)}S$ | Setup time, SPISTE valid before SPICLK (Clock Phase = 0) | $2t_{c(SYSCLK)} + 15$ | | ns |
| | | Setup time, SPISTE valid before SPICLK (Clock Phase = 1) | $2t_{c(SYSCLK)} + 15$ | | ns |
| 26 | $t_{h(STE)}S$ | Hold time, SPISTE invalid after SPICLK | $1.5t_{c(SYSCLK)}$ | | ns |

6.15.6.2.2 SPI Slave Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| NO. | PARAMETER ⁽¹⁾ | | MIN | MAX | UNIT |
|-----|--------------------------|--|-----|-----|------|
| 15 | $t_{d(SOMI)}S$ | Delay time, SPICLK to SPISOMI valid | | 12 | ns |
| 16 | $t_{v(SOMI)}S$ | Valid time, SPISOMI valid after SPICLK | 0 | | ns |

(1) 20-pF load on pin.

6.15.6.2.3 SPI Slave Mode Timing Diagrams

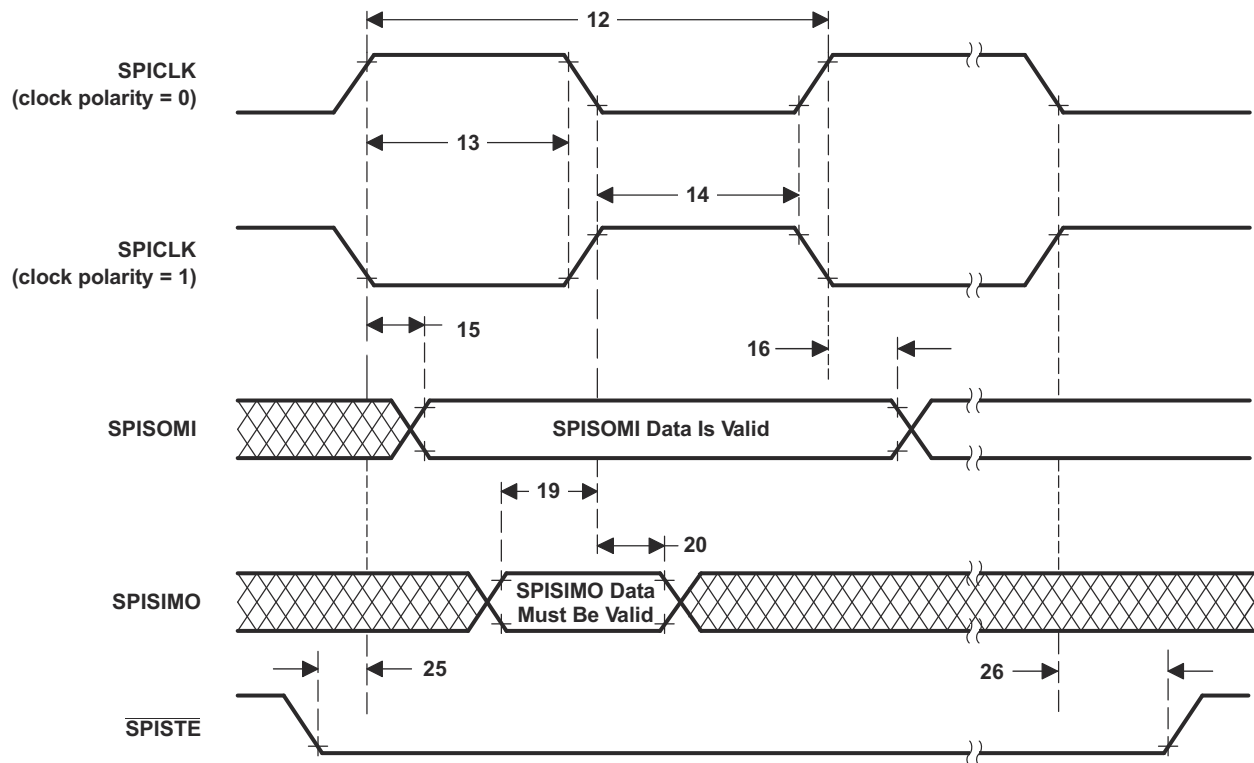


Figure 6-75. SPI Slave Mode External Timing (Clock Phase = 0)

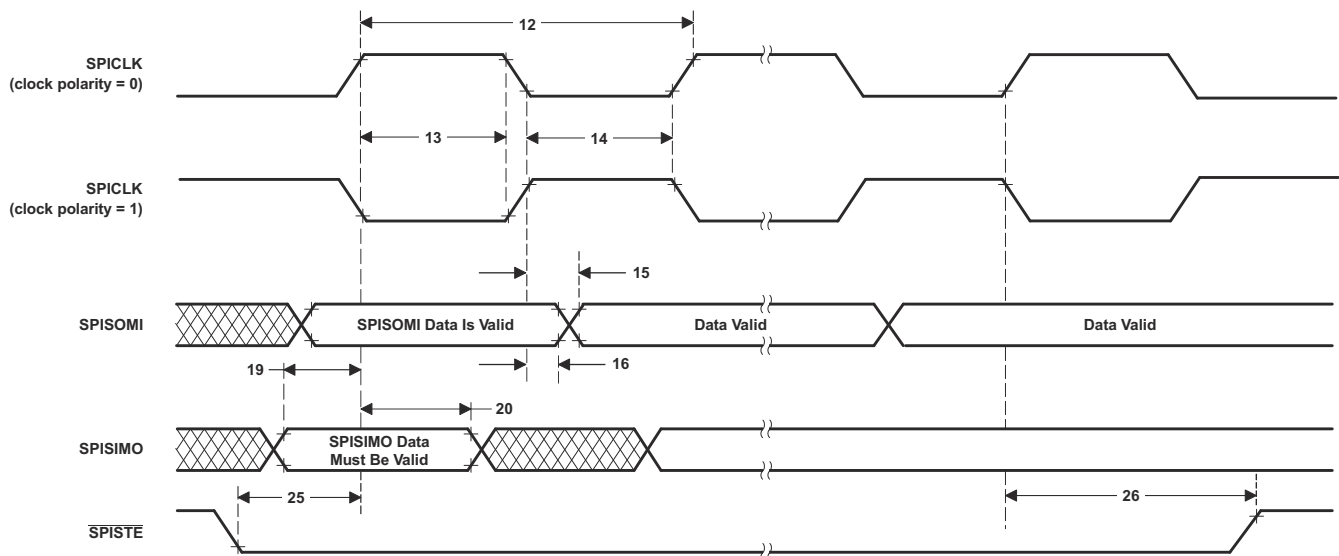


Figure 6-76. SPI Slave Mode External Timing (Clock Phase = 1)

6.15.7 Local Interconnect Network (LIN)

This device contains one Local Interconnect Network (LIN) module. The LIN module adheres to the LIN 2.1 standard as defined by the *LIN Specification Package Revision 2.1*. The LIN is a low-cost serial interface designed for applications where the CAN protocol may be too expensive to implement, such as small subnetworks for cabin comfort functions like interior lighting or window control in an automotive application.

The LIN standard is based on the SCI (UART) serial data link format. The communication concept is single-master and multiple-slave with a message identification for multicast transmission between any network nodes.

The LIN module can be programmed to work either as an SCI or as a LIN as the core of the module is an SCI. The hardware features of the SCI are augmented to achieve LIN compatibility. The SCI module is a universal asynchronous receiver-transmitter (UART) that implements the standard non-return-to-zero format.

Though the registers are common for LIN and SCI, the register descriptions have notes to identify the register/bit usage in different modes. Because of this, code written for this module cannot be directly ported to the stand-alone SCI module and vice versa.

The LIN module has the following features:

- Compatibility with LIN 1.3, 2.0 and 2.1 protocols
- Configurable baud rate up to 20 kbps (as per LIN 2.1 protocol)
- Two external pins: LINRX and LINTX
- Multibuffered receive and transmit units
- Identification masks for message filtering
- Automatic master header generation
 - Programmable synchronization break field
 - Synchronization field
 - Identifier field
- Slave automatic synchronization
 - Synchronization break detection
 - Optional baud rate update
 - Synchronization validation
- 2³¹ programmable transmission rates with 7 fractional bits
- Wakeup on LINRX dominant level from transceiver
- Automatic wake-up support
 - Wakeup signal generation
 - Expiration times on wakeup signals
- Automatic bus idle detection
- Error detection
 - Bit error
 - Bus error
 - No-response error
 - Checksum error
 - Synchronization field error
 - Parity error
- Capability to use direct memory access (DMA) for transmit and receive data
- Two interrupt lines with priority encoding for:
 - Receive
 - Transmit
 - ID, error, and status
- Support for LIN 2.0 checksum
- Enhanced synchronizer finite state machine (FSM) support for frame processing
- Enhanced handling of extended frames
- Enhanced baud rate generator
- Update wakeup/go to sleep

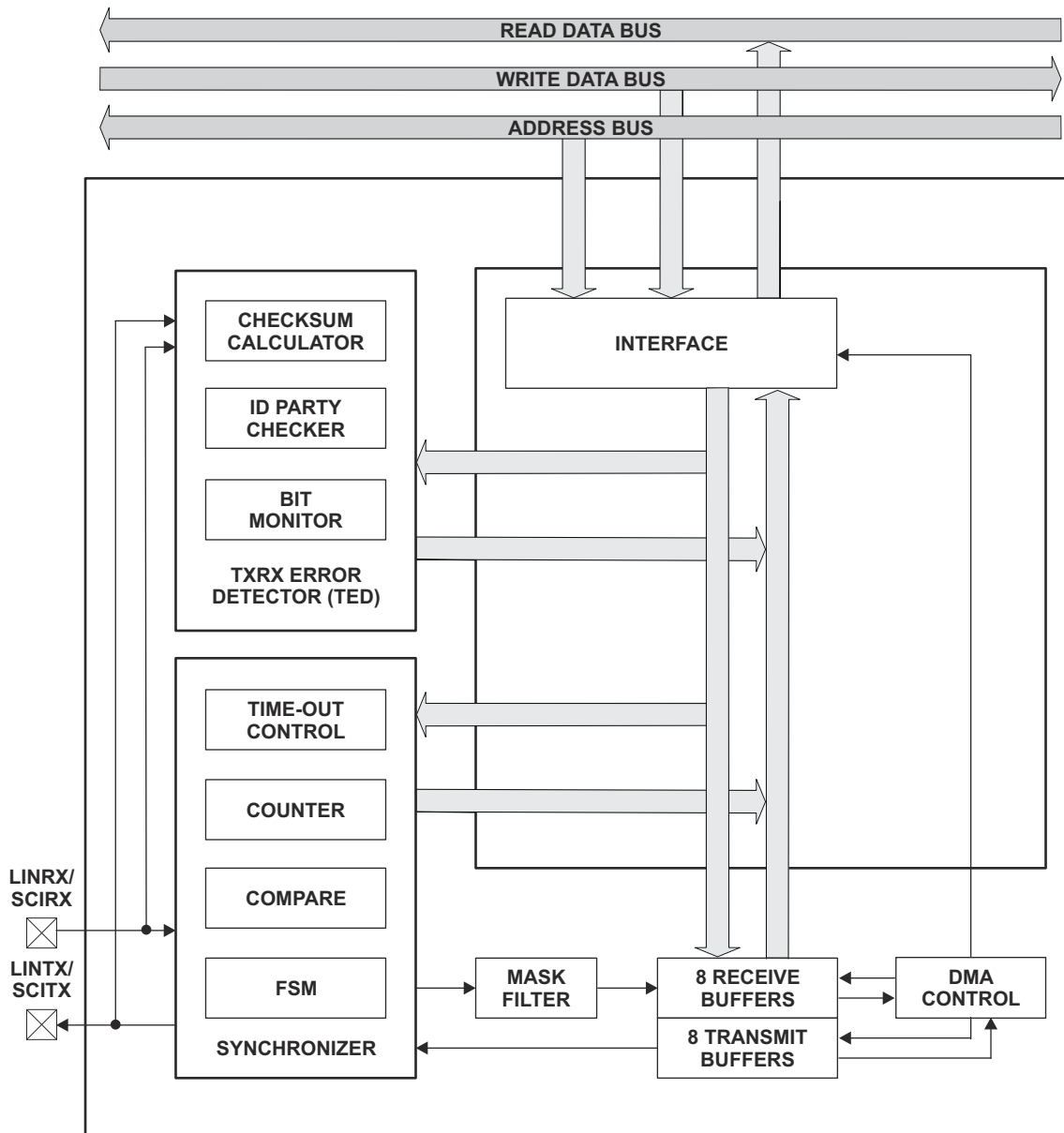


Figure 6-77. LIN Block Diagram

6.15.8 Fast Serial Interface (FSI)

The Fast Serial Interface (FSI) module is a serial communication peripheral capable of reliable and robust high-speed communications. The FSI is designed to ensure data robustness across many system conditions such as chip-to-chip as well as board-to-board across an isolation barrier. Payload integrity checks such as CRC, start- and end-of-frame patterns, and user-defined tags, are encoded before transmit and then verified after receipt without additional CPU interaction. Line breaks can be detected using periodic transmissions, all managed and monitored by hardware. The FSI is also tightly integrated with other control peripherals on the device. To ensure that the latest sensor data or control parameters are available, frames can be transmitted on every control loop period. An integrated skew-compensation block has been added on the receiver to handle skew that may occur between the clock and data signals due to a variety of factors, including trace-length mismatch and skews induced by an isolation chip. With embedded data robustness checks, data-link integrity checks, skew compensation, and integration with control peripherals, the FSI can enable high-speed, robust communication in any system. These and many other features of the FSI follow.

The FSI module includes the following features:

- Independent transmitter and receiver cores
- Source-synchronous transmission
- Dual data rate (DDR)
- One or two data lines
- Programmable data length
- Skew adjustment block to compensate for board and system delay mismatches
- Frame error detection
- Programmable frame tagging for message filtering
- Hardware ping to detect line breaks during communication (ping watchdog)
- Two interrupts per FSI core
- Externally triggered frame generation
- Hardware- or software-calculated CRC
- Embedded ECC computation module
- Register write protection
- DMA support
- SPI compatibility mode (limited features available)

Operating the FSI at maximum speed (60 MHz) at dual data rate (120Mbps) may require the integrated skew compensation block to be configured according to the specific operating conditions on a case-by-case basis. The [Fast Serial Interface \(FSI\) Skew Compensation](#) Application Report provides example software on how to configure and set up the integrated skew compensation block on the Fast Serial Interface.

The FSI consists of independent transmitter (FSITX) and receiver (FSIRX) cores. The FSITX and FSIRX cores are configured and operated independently. The features available on the FSITX and FSIRX are described in the [FSI Transmitter](#) section and the [FSI Receiver](#) section, respectively.

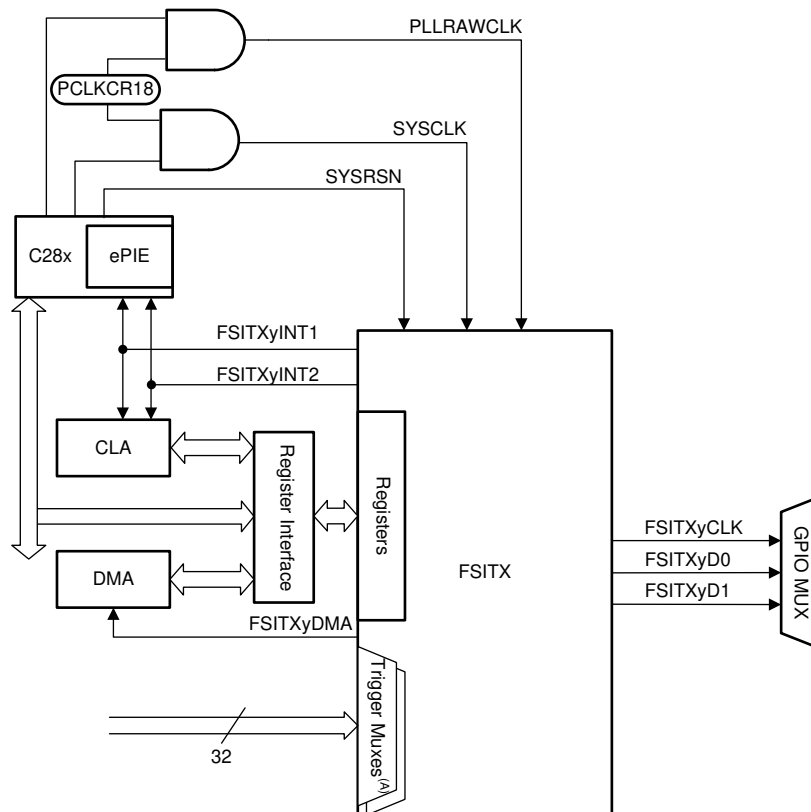
6.15.8.1 FSI Transmitter

The FSI transmitter module handles the framing of data, CRC generation, signal generation of TXCLK, TXD0, and TXD1, as well as interrupt generation. The operation of the transmitter core is controlled and configured through programmable control registers. The transmitter control registers let the CPU program, control, and monitor the operation of the FSI transmitter. The transmit data buffer is accessible by the CPU and the DMA.

The transmitter has the following features:

- Automated ping frame generation
- Externally triggered ping frames
- Software-configurable frame lengths
- 16-word data buffer
- Data buffer underrun and overrun detection
- Hardware-generated CRC on data bits
- Software ECC calculation on select data
- DMA support

Figure 6-78 shows the FSITX CPU interface. Figure 6-79 shows the high-level block diagram of the FSITX. Not all data paths and internal connections are shown. This diagram provides a high-level overview of the internal modules present in the FSITX.



- A. The signals connected to the trigger muxes are described in the External Frame Trigger Mux section of the Fast Serial Interface (FSI) chapter in the [TMS320F28003x Real-Time Microcontrollers Technical Reference Manual](#).

Figure 6-78. FSITX CPU Interface

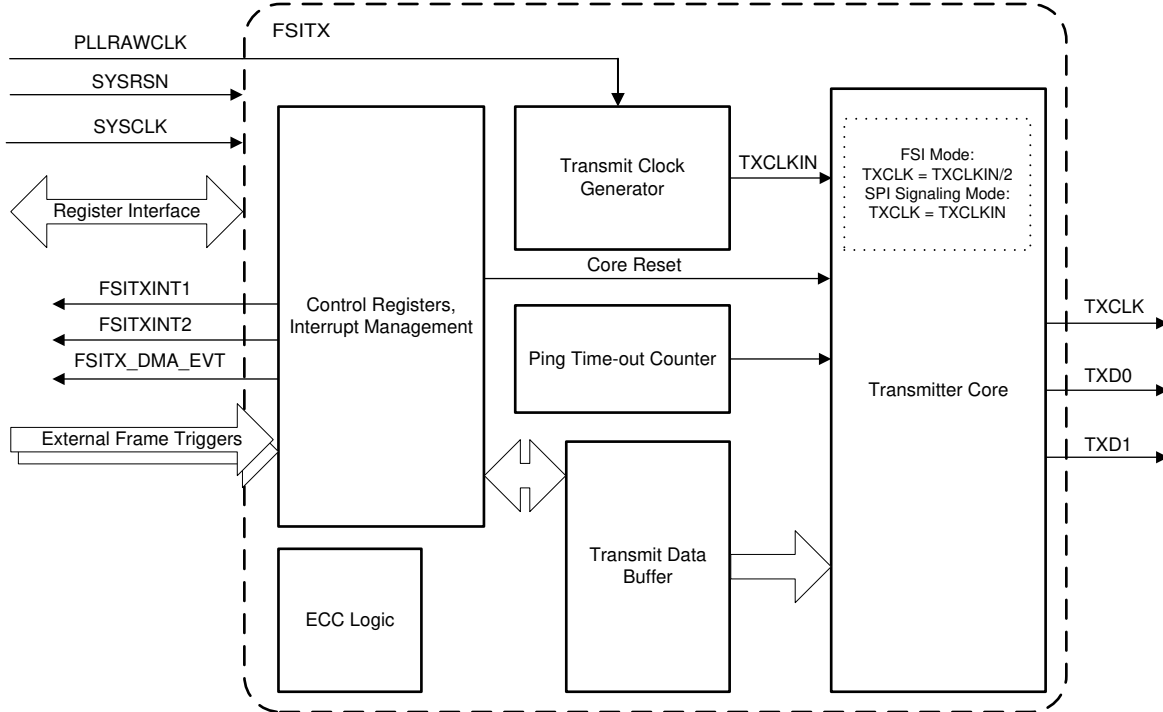


Figure 6-79. FSITX Block Diagram

6.15.8.1.1 FSITX Electrical Data and Timing

6.15.8.1.1.1 FSITX Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

| NO. | PARAMETER ⁽¹⁾ | | MIN | MAX | UNIT |
|------|--|--|-------------------------------|-------------------------------|------|
| 1 | $t_c(\text{TXCLK})$ | Cycle time, TXCLK | 16.67 | | ns |
| 2 | $t_w(\text{TXCLK})$ | Pulse width, TXCLK low or TXCLK high | $(0.5t_c(\text{TXCLK})) - 1$ | $(0.5t_c(\text{TXCLK})) + 1$ | ns |
| 3 | $t_d(\text{TXCLK-TXD})$ | Delay time, TXCLK rising or falling to TXD valid | $(0.25t_c(\text{TXCLK})) - 2$ | $(0.25t_c(\text{TXCLK})) + 2$ | ns |
| 4 | $t_d(\text{TXCLK})$ | TXCLK delay compensation at TX_DLYLINE_CTRL[TXCLK_DLY]=31 | 9.95 | 30 | ns |
| 5 | $t_d(\text{TXD0})$ | TXD0 delay compensation at TX_DLYLINE_CTRL[TXD0_DLY]=31 | 9.95 | 30 | ns |
| 6 | $t_d(\text{TXD1})$ | TXD1 delay compensation at TX_DLYLINE_CTRL[TXD1_DLY]=31 | 9.95 | 30 | ns |
| 7 | $t_d(\text{DELAY_ELEMENT})$ | Incremental delay of each delay line element for TXCLK, TXD0, and TXD1 | 0.3 | 1 | ns |
| TDM1 | $t_{\text{skew}}(\text{TDM_CLK-TDM_Dx})$ | Delay skew introduced between TXCLK-TDM_CLK delay and TXDx-TDM_Dx delays | -2.5 | 2.5 | ns |

(1) 10-pF load on pin.

6.15.8.1.1.2 FSITX Timings

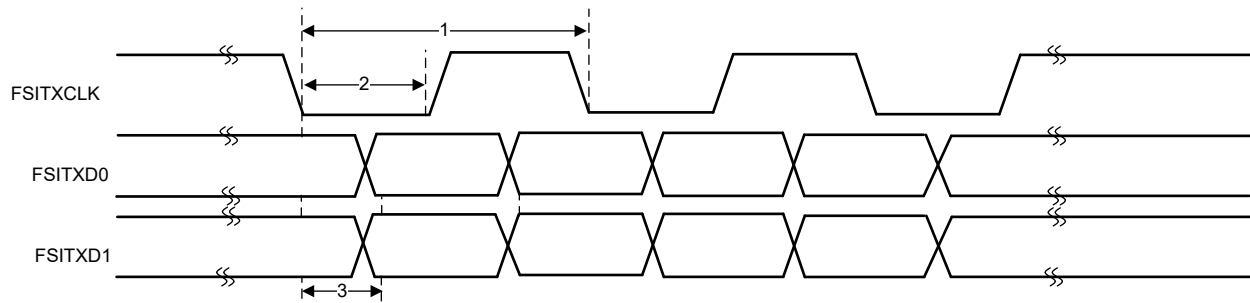


Figure 6-80. FSITX Timings

6.15.8.2 FSI Receiver

The receiver module interfaces to the FSI clock (RXCLK), and data lines (RXD0 and RXD1) after they pass through an optional programmable delay line. The receiver core handles the data framing, CRC computation, and frame-related error checking. The receiver bit clock and state machine are run by the RXCLK input, which is asynchronous to the device system clock.

The receiver control registers let the CPU program, control, and monitor the operation of the FSIRX. The receive data buffer is accessible by the CPU, HIC, and the DMA.

The receiver core has the following features:

- 16-word data buffer
- Multiple supported frame types
- Ping frame watchdog
- Frame watchdog
- CRC calculation and comparison in hardware
- ECC detection
- Programmable delay line control on incoming signals
- DMA support
- SPI compatibility mode

Figure 6-81 shows the FSIRX CPU interface. Figure 6-82 provides a high-level overview of the internal modules present in the FSIRX. Not all data paths and internal connections are shown.

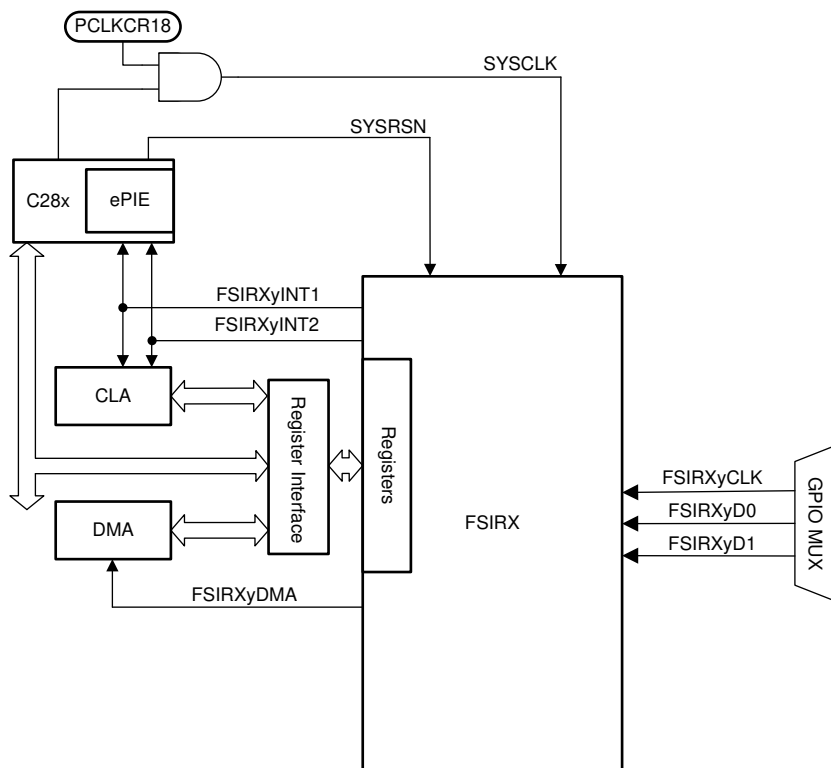


Figure 6-81. FSIRX CPU Interface

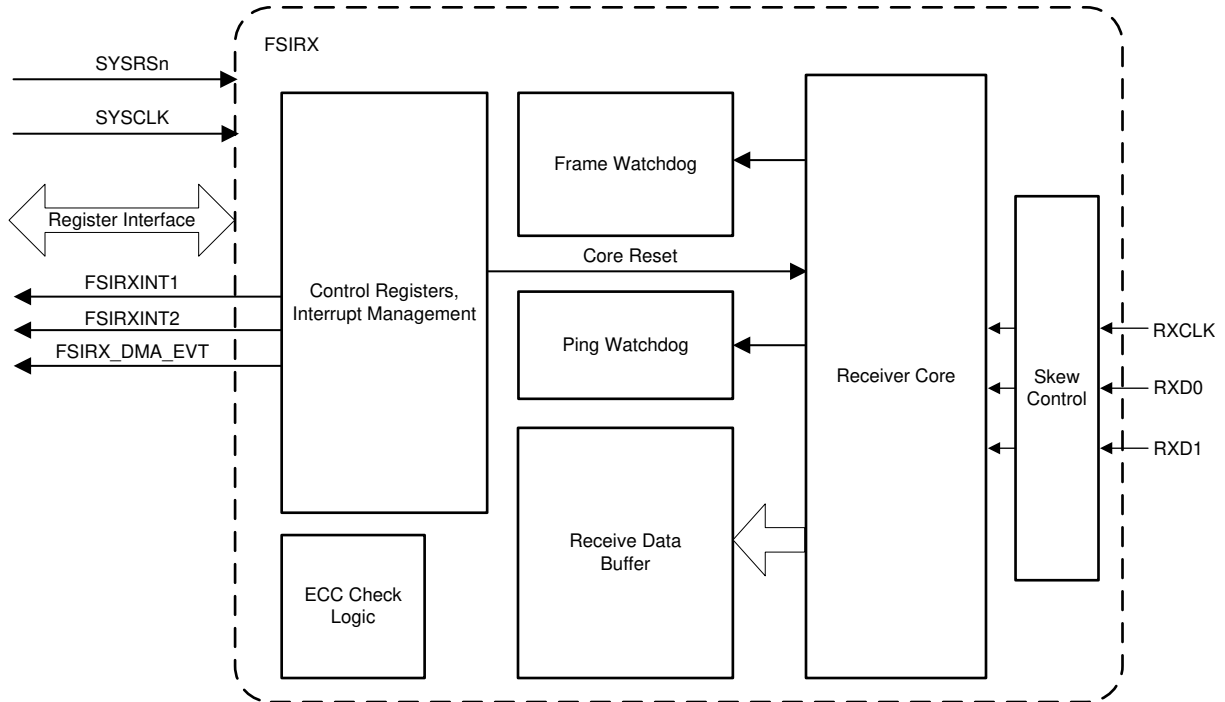


Figure 6-82. FSIRX Block Diagram

6.15.8.2.1 FSIRX Electrical Data and Timing

6.15.8.2.1.1 FSIRX Timing Requirements

| NO. | | | MIN | MAX | UNIT |
|-----|---------------------|--|--------------------|--------------------|------|
| 1 | $t_{c(RXCLK)}$ | Cycle time, RXCLK | 16.67 | | ns |
| 2 | $t_{w(RXCLK)}$ | Pulse width, RXCLK low or RXCLK high. | $0.35t_{c(RXCLK)}$ | $0.65t_{c(RXCLK)}$ | ns |
| 3 | $t_{su(RXCLK-RXD)}$ | Setup time with respect to RXCLK, applies to both edges of the clock | 1.7 | | ns |
| 4 | $t_{h(RXCLK-RXD)}$ | Hold time with respect to RXCLK, applies to both edges of the clock | 2 | | ns |

6.15.8.2.1.2 FSIRX Switching Characteristics

| NO. | PARAMETER ⁽¹⁾ | | MIN | MAX | UNIT |
|------|------------------------------|--|-----|-----|------|
| 1 | $t_{d(RXCLK)}$ | RXCLK delay compensation at RX_DLYLINE_CTRL[RXCLK_DLY]=31 | 10 | 30 | ns |
| 2 | $t_{d(RXD0)}$ | RXD0 delay compensation at RX_DLYLINE_CTRL[RXD0_DLY]=31 | 10 | 30 | ns |
| 3 | $t_{d(RXD1)}$ | RXD1 delay compensation at RX_DLYLINE_CTRL[RXD1_DLY]=31 | 10 | 30 | ns |
| 4 | $t_{d(DELAY_ELEMENT)}$ | Incremental delay of each delay line element for RXCLK, RXD0, and RXD1 | 0.3 | 1 | ns |
| TDM1 | $t_{skew(TDM_CLK-TDM_Dx)}$ | Delay skew introduced between RXCLK-TDM_CLK delay and RXDx-TDM_Dx delays | -3 | 3 | ns |

(1) 10-pF load on pin.

6.15.8.2.1.3 FSIRX Timings

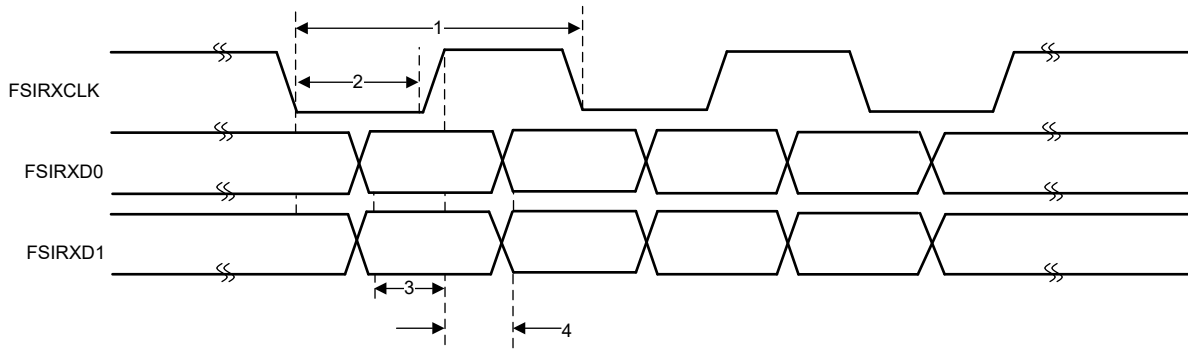


Figure 6-83. FSIRX Timings

6.15.8.3 FSI SPI Compatibility Mode

The FSI supports a SPI compatibility mode to enable communication with programmable SPI devices. In this mode, the FSI transmits its data in the same manner as a SPI in a single clock configuration mode. While the FSI is able to physically interface with a SPI in this mode, the external device must be able to encode and decode an FSI frame to communicate successfully. This is because the FSI transmits all SPI frame phases with the exception of the preamble and postamble. The FSI provides the same data validation and frame checking as if it was in standard FSI mode, allowing for more robust communication without consuming CPU cycles. The external SPI is required to send all relevant information and can access standard FSI features such as the ping frame watchdog on the FSIRX, frame tagging, or custom CRC values. The list of features of SPI compatibility mode follows:

- Data will transmit on rising edge and receive on falling edge of the clock.
- Only 16-bit word size is supported.
- TXD1 will be driven like an active-low chip-select signal. The signal will be low for the duration of the full frame transmission.
- No receiver chip-select input is required. RXD1 is not used. Data is shifted into the receiver on every active clock edge.
- No preamble or postamble clocks will be transmitted. All signals return to the idle state after the frame phase is finished.
- It is not possible to transmit in the SPI slave configuration because the FSI TXCLK cannot take an external clock source.

6.15.8.3.1 FSITX SPI Signaling Mode Electrical Data and Timing

Special timings are not required for the FSIRX in SPI signaling mode. FSIRX timings listed in the FSIRX Timing Requirements table are applicable in SPI compatibility mode. Setup and Hold times are only valid on the falling edge of FSIRXCLK because this is the active edge in SPI signaling mode.

6.15.8.3.1.1 FSITX SPI Signaling Mode Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

| NO. | PARAMETER ⁽¹⁾ | | MIN | MAX | UNIT |
|-----|--------------------------|---|-------------------------|-------------------------|------|
| 1 | $t_{c(TXCLK)}$ | Cycle time, TXCLK | 16.67 | | ns |
| 2 | $t_{w(TXCLK)}$ | Pulse width, TXCLK low or TXCLK high | $(0.5t_{c(TXCLK)}) - 1$ | $(0.5t_{c(TXCLK)}) + 1$ | ns |
| 3 | $t_{d(TXCLKH-TXD0)}$ | Delay time, TXD0 valid after TXCLK high | | 3 | ns |
| 4 | $t_{d(TXD1-TXCLK)}$ | Delay time, TXCLK high after TXD1 low | $t_{w(TXCLK)} - 3$ | | ns |
| 5 | $t_{d(TXCLK-TXD1)}$ | Delay time, TXD1 high after TXCLK low | $t_{w(TXCLK)}$ | | ns |

(1) 10-pF load on pin

6.15.8.3.1.2 FSITX SPI Signaling Mode Timings

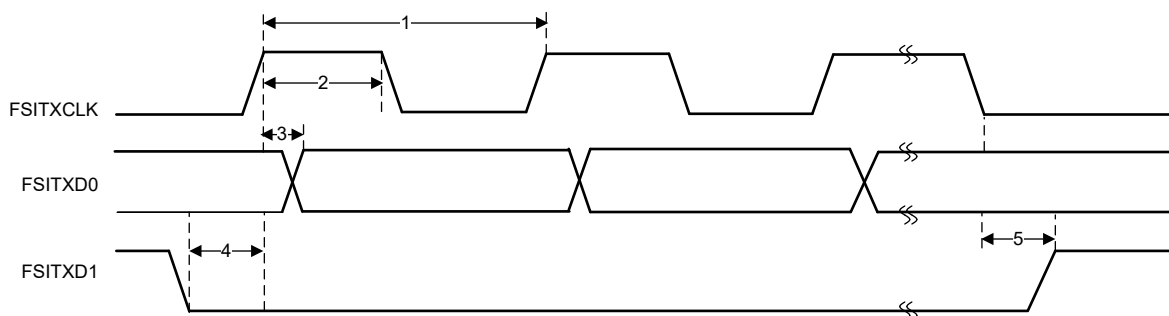


Figure 6-84. FSITX SPI Signaling Mode Timings

6.15.9 Host Interface Controller (HIC)

The HIC module allows an external host controller (master) to directly access resources of the device (slave) by emulating the ASRAM protocol. It has two modes of operation: direct access and mailbox access. In direct access mode, device resources is written to and read from directly by the external host. In mailbox access mode, external host and device write to and read from a buffer and notify each other when the buffer write/read is complete. For security reasons, the HIC has to be enabled by the device before the external host can access it.

Features of the HIC include:

- Configurable I/O data lines of 8 bits and 16 bits
- Direct and mailbox access modes
- 8 address lines and 8 configurable base addresses for a total of 2048 possible addressable regions
- Two 64-byte buffers for external host and device when using mailbox access mode
- Interrupt generation on buffer full/empty
- High throughput
- Trigger HIC activity from other peripherals
- Error indicators to the system or interface
- Commit feature that blocks writes to configuration registers

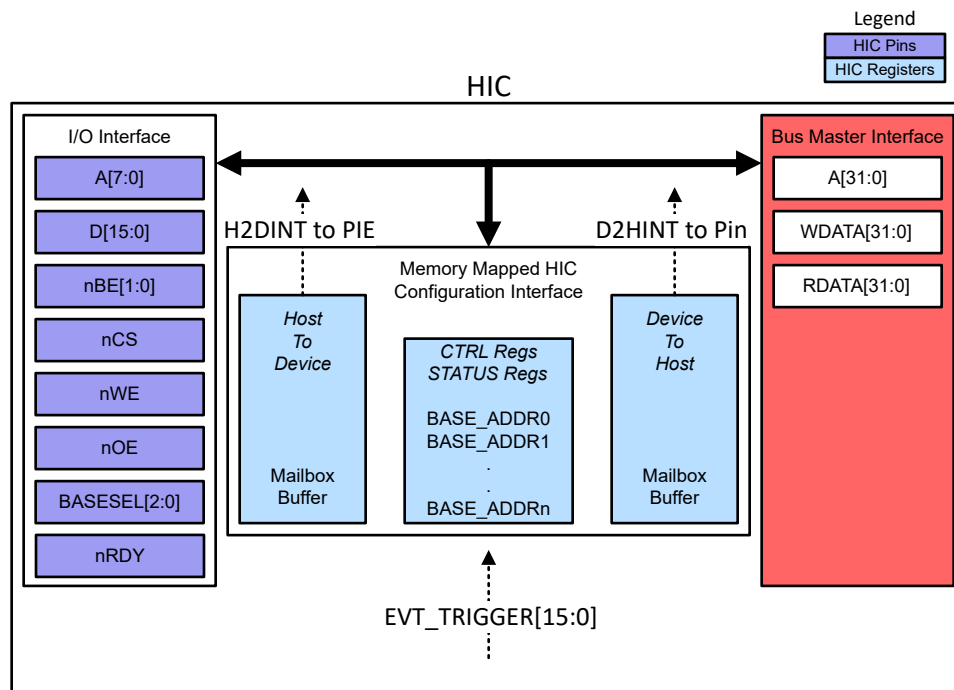


Figure 6-85. HIC Block Diagram

6.15.9.1 HIC Electrical Data and Timing

6.15.9.1.1 HIC Timing Requirements

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|--------------------|-----|------|
| Read/Write Parameters with nOE and nWE pins - Dual Read/Write pins | | | | |
| $t_{su}(ABBV-OEV)$ | Setup time, A/BASESEL/nBE before nOE active | 0 | | ns |
| $t_{su}(ABBV-WEV)$ | Setup time, A/BASESEL/nBE before nWE active | 0 | | ns |
| $t_{su}(CSV-OEV)$ | Setup time, nCS active before nOE active | $0.5t_{c(SYSCLK)}$ | | ns |
| $t_{su}(CSV-WEV)$ | Setup time, nCS active before nWE active | $0.5t_{c(SYSCLK)}$ | | ns |
| $t_h(ABBV-OEIV)$ | Hold time, A/BASESEL/nBE/nCS after nOE inactive | 6 | | ns |
| $t_h(ABBV-WEIV)$ | Hold time, A/BASESEL/nBE/nCS after nWE inactive | 6 | | ns |
| $t_w(OEV)$ | Active pulse width of nOE (Read) ⁽¹⁾ | $4t_{c(SYSCLK)}$ | | ns |
| $t_w(WEV)$ | Active pulse width of nWE (Write) | $4t_{c(SYSCLK)}$ | | ns |
| $t_w(CSIV)$ | Inactive pulse width of nCS ⁽²⁾ | $3t_{c(SYSCLK)}$ | | ns |
| $t_w(OEIV)$ | Inactive Read pulse width of nOE ⁽²⁾ | $3t_{c(SYSCLK)}$ | | ns |
| $t_w(WEIV)$ | Inactive Write pulse width of nWE ⁽²⁾ | $3t_{c(SYSCLK)}$ | | ns |
| $t_{su}(DV-WEV)$ | Setup time, D before nWE active | 0 | | ns |
| $t_h(DV-WEIV)$ | Hold time, D after nWE inactive | 6 | | ns |
| Read/Write Parameters with RnW pin - Single Read/Write pin | | | | |
| $t_{su}(ABBV-CSV)$ | Setup time, A/BASESEL/nBE before nCS active | 0 | | ns |
| $t_{su}(RNWV-CSV)$ | Setup time, RnW before nCS active | $0.5t_{c(SYSCLK)}$ | | ns |
| $t_h(ABBV-CSIV)$ | Hold time, A/BASESEL/nBE/RnW after nCS inactive | 5 | | ns |
| $t_w(CSV_RD)$ | Active pulse width of nCS for read operation ⁽¹⁾ | $4t_{c(SYSCLK)}$ | | ns |
| $t_w(CSV_WR)$ | Active pulse width of nCS for write operation | $4t_{c(SYSCLK)}$ | | ns |
| $t_w(CSIV)$ | Inactive pulse width of nCS ⁽²⁾ | $3t_{c(SYSCLK)}$ | | ns |
| $t_w(RNWIV)$ | Inactive pulse width of RnW ⁽²⁾ | $3t_{c(SYSCLK)}$ | | ns |
| $t_{su}(DV-CSV)$ | Setup time, D before nCS active | 0 | | ns |
| $t_h(DV-CSIV)$ | Hold time, D after nCS inactive | 5 | | ns |

(1) For accesses to the device region, additional 2 SYSCLK cycles are required.

(2) For accesses to the device region with nRDY pin, additional SYSCLK cycle is required.

6.15.9.1.2 HIC Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER ⁽¹⁾ | | MIN | MAX | UNIT |
|--|---|------------------|-----------------------|------|
| Read/Write Parameters with nOE and nWE pins | | | | |
| $t_d(OEV-DV)$ | Output data delay time : nOE to D output valid ⁽²⁾ | $3t_{c(SYSCLK)}$ | $4t_{c(SYSCLK)} + 15$ | ns |
| $t_d(OEIV-DIV)$ | Output data hold time : nOE invalid to D output invalid (tri-state) | $1t_{c(SYSCLK)}$ | $2t_{c(SYSCLK)} + 15$ | ns |
| $t_d(OEV-RDYV)$ | Read Ready delay time : nOE to nRDY output valid | 0 | 12 | ns |
| $t_d(WEV-RDYV)$ | Write Ready delay time : nWE to nRDY output valid | 0 | 12 | ns |
| $t_d(RDYV-DV)$ | Ready to Data delay time : nRDY output valid to D output valid | -3 | 3 | ns |
| $t_w(RDYACT)$ | Active pulse width of nRDY output | $2t_{c(SYSCLK)}$ | | ns |
| Read/Write Parameters with RnW pin | | | | |
| $t_d(CSV-DV)$ | Output delay time : nCS active to D output valid ⁽²⁾ | $3t_{c(SYSCLK)}$ | $4t_{c(SYSCLK)} + 14$ | ns |
| $t_d(CSIV-DIV)$ | Output hold time : nCS inactive to D output invalid (tri-state) | $1t_{c(SYSCLK)}$ | $2t_{c(SYSCLK)} + 14$ | ns |
| $t_d(CSV-RDYV)$ | Output delay time : nCS to nRDY output valid | 0 | 12 | ns |
| $t_d(RDYV-DV)$ | Ready to Data delay time : nRDY output valid to D output valid | -3 | 3 | ns |

6.15.9.1.2 HIC Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER ⁽¹⁾ | | MIN | MAX | UNIT |
|--------------------------|-----------------------------------|-----------------------|-----|------|
| $t_{w(RDYACT)}$ | Active pulse width of nRDY output | $2t_c(\text{SYSCLK})$ | | ns |

- (1) 10-pF load on pin.
- (2) Applicable to mailbox accesses only. Direct memory map (Device) accesses are qualified with nRDY pin.

6.15.9.1.3 HIC Timing Diagrams

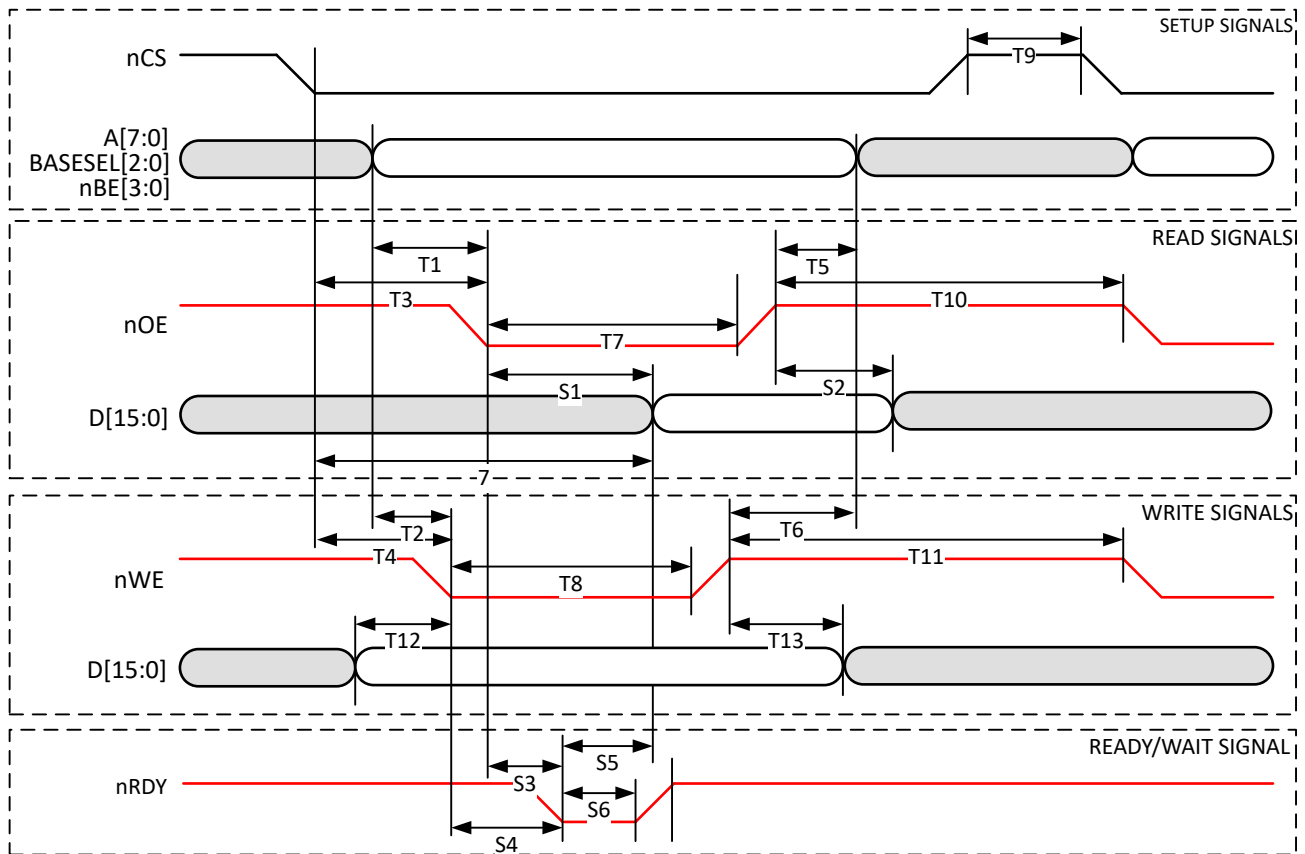


Figure 6-86. Read/Write Operation With nOE and nWE Pins

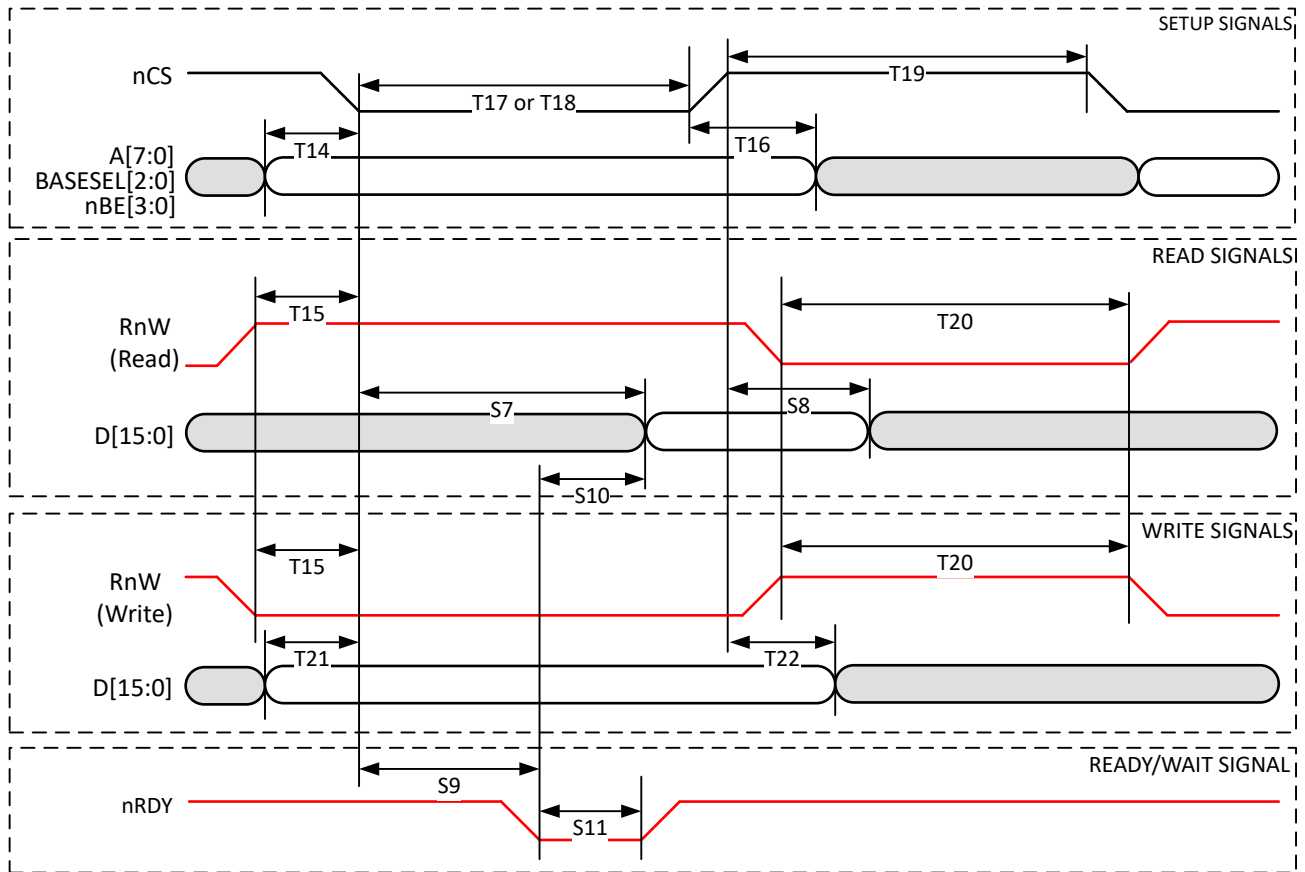


Figure 6-87. Read/Write Operation With RnW Pin

7 Detailed Description

7.1 Overview

C2000™ 32-bit Real-Time microcontrollers are optimized for processing, sensing, and actuation to improve closed-loop performance in **real-time control applications** such as **industrial motor drives; solar inverters and digital power; electrical vehicles and transportation; motor control; and sensing and signal processing.**

The TMS320F28003x (F28003x) is a powerful 32-bit floating-point microcontroller unit (MCU) that lets designers incorporate crucial control peripherals, differentiated analog, and nonvolatile memory on a single device.

The real-time control subsystem is based on TI's 32-bit C28x CPU, which provides 120 MHz of signal processing performance. The C28x CPU is further boosted by the FPU, new TMU extended instruction set, which enables fast execution of algorithms with trigonometric operations commonly found in transforms and torque loop calculations; and the VCRC extended instruction set, which reduces the latency for complex math operations commonly found in encoded applications.

The CLA allows significant offloading of common tasks from the main C28x CPU. The CLA is an independent 32-bit floating-point math accelerator that executes in parallel with the CPU. Additionally, the CLA has its own dedicated memory resources and it can directly access the key peripherals that are required in a typical control system. Support of a subset of ANSI C is standard, as are key features like hardware breakpoints and hardware task-switching.

The F28003x supports up to 384KB (192KW) of flash memory divided into three 128KB (64KW) banks, which enable programming and execution in parallel. Up to 69KB (34.5KW) of on-chip SRAM is also available to supplement the flash memory.

The Live Firmware Update hardware enhancements on F28003x allow fast context switching from the old firmware to the new firmware to minimize application downtime when updating the device firmware.

High-performance analog blocks are integrated on the F28003x real-time MCU to further enable system consolidation. Three separate 12-bit ADCs provide precise and efficient management of multiple analog signals, which ultimately boosts system throughput. Four analog comparator modules provide continuous monitoring of input voltage levels for trip conditions.

The TMS320C2000™ devices contain industry-leading control peripherals with frequency-independent ePWM/HRPWM and eCAP allow for a best-in-class level of control to the system.

Connectivity is supported through various industry-standard communication ports (such as SPI, SCI, I2C, PMBus, LIN, CAN and CAN FD) and offers multiple muxing options for optimal signal placement in a variety of applications. New to the C2000™ platform is Host Interface Controller (HIC), a high throughput interface that allows an external host to access resources of the TMS320F28003x. Additionally, in an industry first, the FSI enables high-speed, robust communication to complement the rich set of peripherals that are embedded in the device.

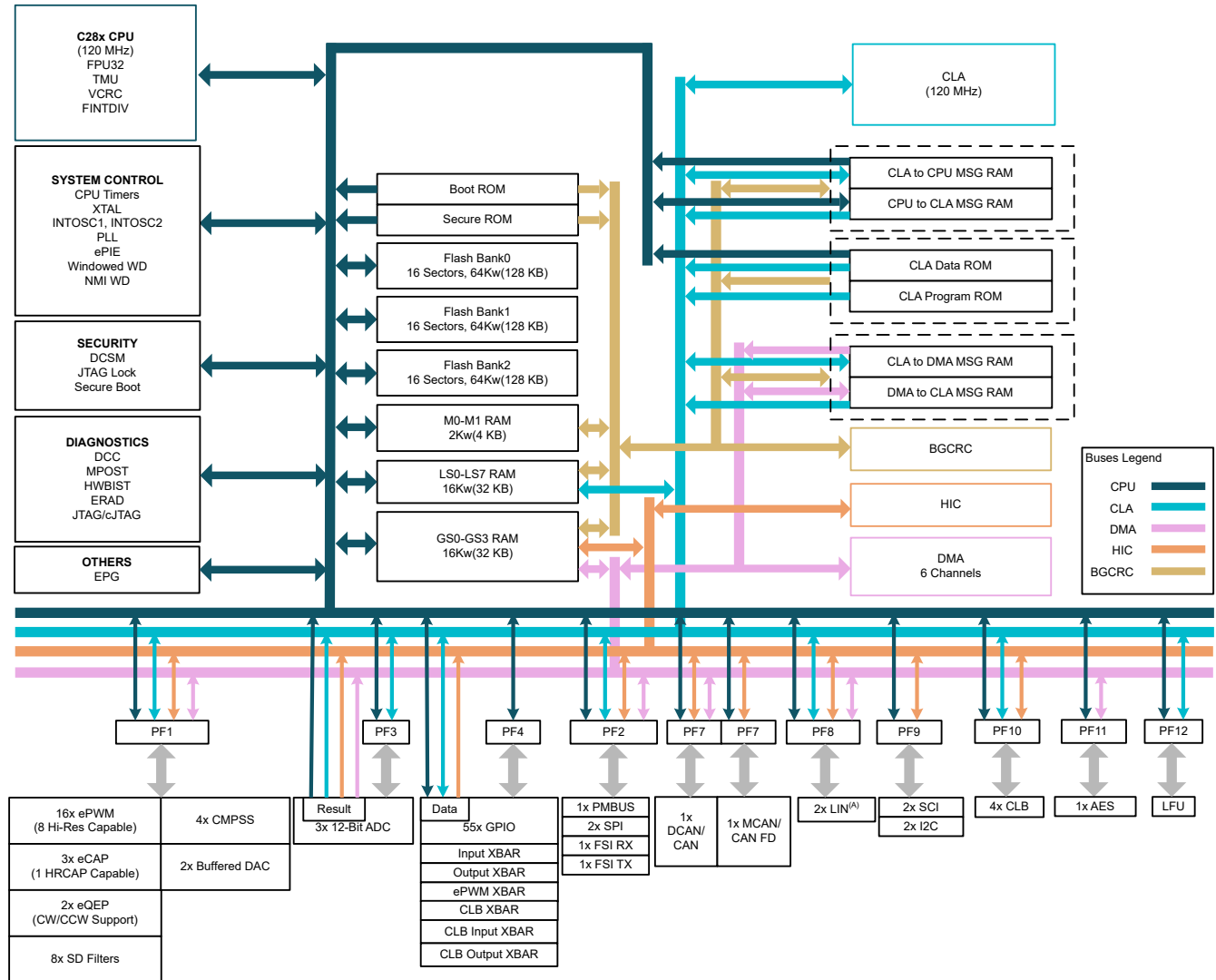
A specially enabled device variant, TMS320F28003xC, allows access to the Configurable Logic Block (CLB) for additional interfacing features. See [Table 4-1](#) for more information.

The Embedded Real-Time Analysis and Diagnostic (ERAD) module enhances the debug and system analysis capabilities of the device by providing additional hardware breakpoints and counters for profiling.

To learn more about the C2000 real-time MCUs, visit the [C2000™ real-time control MCUs](#) page.

7.2 Functional Block Diagram

Figure 7-1 shows the CPU system and associated peripherals.



A. The LIN module can also work as an SCI.

Figure 7-1. Functional Block Diagram

7.3 Memory

7.3.1 Memory Map

The Memory Map table describes the memory map. See the Memory Controller Module section of the System Control chapter in the *TMS320F28003x Real-Time Microcontrollers Technical Reference Manual*.

Table 7-1. Memory Map

| MEMORY | SIZE | START ADDRESS | END ADDRESS | HIC ACCESS | DMA ACCESS | CLA ACCESS | ECC/PARITY | ACCESS PROTECTION | SECURITY |
|---|-----------|---------------|-------------|------------|------------|------------|------------|-------------------|------------------|
| M0 RAM | 1K x 16 | 0x0000 0000 | 0x0000 03FF | - | - | - | ECC | Yes | - |
| M1 RAM | 1K x 16 | 0x0000 0400 | 0x0000 07FF | - | - | - | ECC | Yes | - |
| PieVectTable | 512 x 16 | 0x0000 0D00 | 0x0000 0EFF | - | - | - | - | - | - |
| PieVectTable Swap | 512 x 16 | 0x0100 0900 | 0x0100 0AFF | - | - | - | - | - | - |
| LS0 RAM | 2K x 16 | 0x0000 8000 | 0x0000 87FF | - | - | Yes | ECC | Yes | Yes |
| LS1 RAM | 2K x 16 | 0x0000 8800 | 0x0000 8FFF | - | - | Yes | ECC | Yes | Yes |
| LS2 RAM | 2K x 16 | 0x0000 9000 | 0x0000 97FF | - | - | Yes | ECC | Yes | Yes |
| LS3 RAM | 2K x 16 | 0x0000 9800 | 0x0000 9FFF | - | - | Yes | ECC | Yes | Yes |
| LS4 RAM | 2K x 16 | 0x0000 A000 | 0x0000 A7FF | - | - | Yes | ECC | Yes | Yes |
| LS5 RAM | 2K x 16 | 0x0000 A800 | 0x0000 AFFF | - | - | Yes | ECC | Yes | Yes |
| LS6 RAM | 2K x 16 | 0x0000 B000 | 0x0000 B7FF | - | - | Yes | ECC | Yes | Yes |
| LS7 RAM | 2K x 16 | 0x0000 B800 | 0x0000 BFFF | - | - | Yes | ECC | Yes | Yes |
| GS0 RAM | 4K x 16 | 0x0000 C000 | 0x0000 CFFF | Yes | Yes | - | ECC | Yes | - |
| GS1 RAM | 4K x 16 | 0x0000 D000 | 0x0000 DFFF | Yes | Yes | - | ECC | Yes | - |
| GS2 RAM | 4K x 16 | 0x0000 E000 | 0x0000 EFFF | Yes | Yes | - | ECC | Yes | - |
| GS3 RAM | 4K x 16 | 0x0000 F000 | 0x0000 FFFF | Yes | Yes | - | ECC | Yes | - |
| CAN A Message RAM | 2K x 16 | 0x0004 9000 | 0x0004 97FF | Yes | Yes | - | Parity | - | - |
| MCAN Message RAM | 8K x 16 | 0x0005 8000 | 0x0005 9FFF | Yes | - | - | Parity | - | - |
| CLA to CPU Message RAM | 128 x 16 | 0x0000 1480 | 0x0000 14FF | - | - | Yes | ECC | - | - |
| CPU to CLA Message RAM | 128 x 16 | 0x0000 1500 | 0x0000 157F | - | - | Yes | ECC | - | - |
| CLA to DMA Message RAM | 128 x 16 | 0x0000 1680 | 0x0000 16FF | - | Yes | Yes | ECC | - | - |
| DMA to CLA Message RAM | 128 x 16 | 0x0000 1700 | 0x0000 177F | - | Yes | Yes | ECC | - | - |
| TI OTP ¹ | 3K x 16 | 0x0007 0000 | 0x0007 0BFF | - | - | - | ECC | - | Yes ² |
| User OTP | 3K x 16 | 0x0007 8000 | 0x0007 8BFF | - | - | - | ECC | - | Yes ² |
| Flash | 192K x 16 | 0x0008 0000 | 0x000A FFFF | - | - | - | ECC | - | Yes |
| Secure ROM | 24K x 16 | 0x003F 2000 | 0x003F 7FFF | - | - | - | Parity | - | Yes |
| Boot ROM | 32K x 16 | 0x003F 8000 | 0x003F FFFF | - | - | - | Parity | - | - |
| Pie Vector Fetch Error (part of Boot ROM) | 1 x 16 | 0x003F FFBE | 0x003F FFBF | - | - | - | Parity | - | - |
| Default Vectors (part of Boot ROM) | 64 x 16 | 0x003F FFC0 | 0x003F FFFF | - | - | - | Parity | - | - |

(1) TI OTP is for TI internal use only.

(2) Only a subset is secure.

7.3.1.1 Dedicated RAM (Mx RAM)

The CPU subsystem has two dedicated ECC-capable RAM blocks: M0 and M1. These memories are small nonsecure blocks that are tightly coupled with the CPU (that is, only the CPU has access to them).

7.3.1.2 Local Shared RAM (LSx RAM)

Local shared RAMs (LSx RAMs) are accessible to the CPU, CLA, and BGCR. All LSx RAM blocks have ECC. These memories are secure and have CPU access protection (CPU write/CPU fetch).

7.3.1.3 Global Shared RAM (GSx RAM)

Global shared RAMs (GSx RAMs) are accessible from the CPU, HIC, BGCRC and DMA. The CPU, HIC, and DMA have full read and write access to these memories. All GSx RAM blocks have ECC. The GSx RAMs have access protection (CPU write/CPU fetch/DMA write/HIC write).

7.3.1.4 Message RAM

There are two types of message RAMs on this device that can be used to share between CPU, CLA and DMA. CLA-CPU message RAM shares data between the CLA and CPU while the CLA-DMA message RAM shares data between the CLA and DMA.

7.3.2 Control Law Accelerator (CLA) Memory Map

Table 7-2 shows the CLA data ROM memory map. For information about the CLA program ROM, see the CLA Program ROM (CLAPROMCRC) chapter in the [TMS320F28003x Real-Time Microcontrollers Technical Reference Manual](#).

Table 7-2. CLA Data ROM Memory Map

| MEMORY | START ADDRESS | END ADDRESS | LENGTH |
|-------------------|---------------|-------------|--------|
| FFT Tables (Load) | 0x0100 1070 | 0x0100 186F | 0x0800 |
| Data (Load) | 0x0100 1870 | 0x0100 1FF9 | 0x078A |
| Version (Load) | 0x0100 1FFA | 0x0100 1FFF | 0x0006 |
| FFT Tables (Run) | 0x0000 F070 | 0x0000 F86F | 0x0800 |
| Data (Run) | 0x0000 F870 | 0x0000 FFF9 | 0x078A |
| Version (Run) | 0x0000 FFFA | 0x0000 FFFF | 0x0006 |

7.3.3 Flash Memory Map

On the F28003x devices, three flash banks (384KB [192KW]) are available. Code to program the flash should be executed out of RAM, there should not be any kind of access to the flash bank when an erase or program operation is in progress. The Addresses of Flash Sectors table lists the addresses of flash sectors available for each part number.

7.3.3.1 Addresses of Flash Sectors

Table 7-3. Addresses of Flash Sectors

| PART NUMBER | SECTOR | ADDRESS | | | ECC ADDRESS | | |
|--|-----------------------------------|-----------|-------------|-------------|-------------|-------------|-------------|
| | | SIZE | START | END | SIZE | START | END |
| OTP Sectors | | | | | | | |
| All F28003x | TI OTP Bank 0 (Unsecure) | 1008 x 16 | 0x0007 0000 | 0x0007 03EF | 126 x 16 | 0x0107 0000 | 0x0107 007D |
| | TI OTP Bank 0 (Secure) | 16 x 16 | 0x0007 03F0 | 0x0007 03FF | 2 x 16 | 0x0107 007E | 0x0107 007F |
| | TI OTP Bank 1 | 1K x 16 | 0x0007 0400 | 0x0007 07FF | 128 x 16 | 0x0107 0080 | 0x0107 00FF |
| F280039, F280038 | TI OTP Bank 2 | 1K x 16 | 0x0007 0800 | 0x0007 0BFF | 128 x 16 | 0x0107 0100 | 0x0107 017F |
| All F28003x | User configurable DCSM OTP Bank 0 | 1K x 16 | 0x0007 8000 | 0x0007 83FF | 128 x 16 | 0x0107 1000 | 0x0107 107F |
| | User configurable OTP Bank 1 | 1K x 16 | 0x0007 8400 | 0x0007 87FF | 128 x 16 | 0x0107 1080 | 0x0107 10FF |
| F280039, F280038 | User configurable OTP Bank 2 | 1K x 16 | 0x0007 8800 | 0x0007 8BFF | 128 x 16 | 0x0107 1100 | 0x0107 117F |
| Bank 0 Sectors | | | | | | | |
| F280039, F280038, F280037, F280036 | Sector 0 | 4K x 16 | 0x0008 0000 | 0x0008 0FFF | 512 x 16 | 0x0108 0000 | 0x0108 01FF |
| | Sector 1 | 4K x 16 | 0x0008 1000 | 0x0008 1FFF | 512 x 16 | 0x0108 0200 | 0x0108 03FF |
| | Sector 2 | 4K x 16 | 0x0008 2000 | 0x0008 2FFF | 512 x 16 | 0x0108 0400 | 0x0108 05FF |
| | Sector 3 | 4K x 16 | 0x0008 3000 | 0x0008 3FFF | 512 x 16 | 0x0108 0600 | 0x0108 07FF |
| | Sector 4 | 4K x 16 | 0x0008 4000 | 0x0008 4FFF | 512 x 16 | 0x0108 0800 | 0x0108 09FF |
| | Sector 5 | 4K x 16 | 0x0008 5000 | 0x0008 5FFF | 512 x 16 | 0x0108 0A00 | 0x0108 0BFF |
| | Sector 6 | 4K x 16 | 0x0008 6000 | 0x0008 6FFF | 512 x 16 | 0x0108 0C00 | 0x0108 0DFF |
| | Sector 7 | 4K x 16 | 0x0008 7000 | 0x0008 7FFF | 512 x 16 | 0x0108 0E00 | 0x0108 0FFF |
| F280039, F280038, F280037, F280036, F280034, F280033 | Sector 8 | 4K x 16 | 0x0008 8000 | 0x0008 8FFF | 512 x 16 | 0x0108 1000 | 0x0108 11FF |
| | Sector 9 | 4K x 16 | 0x0008 9000 | 0x0008 9FFF | 512 x 16 | 0x0108 1200 | 0x0108 13FF |
| | Sector 10 | 4K x 16 | 0x0008 A000 | 0x0008 AFFF | 512 x 16 | 0x0108 1400 | 0x0108 15FF |
| | Sector 11 | 4K x 16 | 0x0008 B000 | 0x0008 BFFF | 512 x 16 | 0x0108 1600 | 0x0108 17FF |
| | Sector 12 | 4K x 16 | 0x0008 C000 | 0x0008 CFFF | 512 x 16 | 0x0108 1800 | 0x0108 19FF |
| | Sector 13 | 4K x 16 | 0x0008 D000 | 0x0008 DFFF | 512 x 16 | 0x0108 1A00 | 0x0108 1BFF |
| | Sector 14 | 4K x 16 | 0x0008 E000 | 0x0008 EFFF | 512 x 16 | 0x0108 1C00 | 0x0108 1DFF |
| | Sector 15 | 4K x 16 | 0x0008 F000 | 0x0008 FFFF | 512 x 16 | 0x0108 1E00 | 0x0108 1FFF |

Table 7-3. Addresses of Flash Sectors (continued)

| PART NUMBER | SECTOR | ADDRESS | | | ECC ADDRESS | | |
|---|-----------|---------|-------------|-------------|-------------|-------------|-------------|
| | | SIZE | START | END | SIZE | START | END |
| Bank 1 Sectors | | | | | | | |
| F280039, F280038, F280037, F280036, F280034, F280033 | Sector 0 | 4K x 16 | 0x0009 0000 | 0x0009 0FFF | 512 x 16 | 0x0108 2000 | 0x0108 21FF |
| | Sector 1 | 4K x 16 | 0x0009 1000 | 0x0009 1FFF | 512 x 16 | 0x0108 2200 | 0x0108 23FF |
| | Sector 2 | 4K x 16 | 0x0009 2000 | 0x0009 2FFF | 512 x 16 | 0x0108 2400 | 0x0108 25FF |
| | Sector 3 | 4K x 16 | 0x0009 3000 | 0x0009 3FFF | 512 x 16 | 0x0108 2600 | 0x0108 27FF |
| | Sector 4 | 4K x 16 | 0x0009 4000 | 0x0009 4FFF | 512 x 16 | 0x0108 2800 | 0x0108 29FF |
| | Sector 5 | 4K x 16 | 0x0009 5000 | 0x0009 5FFF | 512 x 16 | 0x0108 2A00 | 0x0108 2BFF |
| | Sector 6 | 4K x 16 | 0x0009 6000 | 0x0009 6FFF | 512 x 16 | 0x0108 2C00 | 0x0108 2DFF |
| | Sector 7 | 4K x 16 | 0x0009 7000 | 0x0009 7FFF | 512 x 16 | 0x0108 2E00 | 0x0108 2FFF |
| F280039, F280038, F280037, F280036 | Sector 8 | 4K x 16 | 0x0009 8000 | 0x0009 8FFF | 512 x 16 | 0x0108 3000 | 0x0108 31FF |
| | Sector 9 | 4K x 16 | 0x0009 9000 | 0x0009 9FFF | 512 x 16 | 0x0108 3200 | 0x0108 33FF |
| | Sector 10 | 4K x 16 | 0x0009 A000 | 0x0009 AFFF | 512 x 16 | 0x0108 3400 | 0x0108 35FF |
| | Sector 11 | 4K x 16 | 0x0009 B000 | 0x0009 BFFF | 512 x 16 | 0x0108 3600 | 0x0108 37FF |
| | Sector 12 | 4K x 16 | 0x0009 C000 | 0x0009 CFFF | 512 x 16 | 0x0108 3800 | 0x0108 39FF |
| | Sector 13 | 4K x 16 | 0x0009 D000 | 0x0009 DFFF | 512 x 16 | 0x0108 3A00 | 0x0108 3BFF |
| | Sector 14 | 4K x 16 | 0x0009 E000 | 0x0009 EFFF | 512 x 16 | 0x0108 3C00 | 0x0108 3DFF |
| | Sector 15 | 4K x 16 | 0x0009 F000 | 0x0009 FFFF | 512 x 16 | 0x0108 3E00 | 0x0108 3FFF |
| Bank 2 Sectors | | | | | | | |
| F280039, F280038 | Sector 0 | 4K x 16 | 0x000A 0000 | 0x000A 0FFF | 512 x 16 | 0x0108 4000 | 0x0108 41FF |
| | Sector 1 | 4K x 16 | 0x000A 1000 | 0x000A 1FFF | 512 x 16 | 0x0108 4200 | 0x0108 43FF |
| | Sector 2 | 4K x 16 | 0x000A 2000 | 0x000A 2FFF | 512 x 16 | 0x0108 4400 | 0x0108 45FF |
| | Sector 3 | 4K x 16 | 0x000A 3000 | 0x000A 3FFF | 512 x 16 | 0x0108 4600 | 0x0108 47FF |
| | Sector 4 | 4K x 16 | 0x000A 4000 | 0x000A 4FFF | 512 x 16 | 0x0108 4800 | 0x0108 49FF |
| | Sector 5 | 4K x 16 | 0x000A 5000 | 0x000A 5FFF | 512 x 16 | 0x0108 4A00 | 0x0108 4BFF |
| | Sector 6 | 4K x 16 | 0x000A 6000 | 0x000A 6FFF | 512 x 16 | 0x0108 4C00 | 0x0108 4DFF |
| | Sector 7 | 4K x 16 | 0x000A 7000 | 0x000A 7FFF | 512 x 16 | 0x0108 4E00 | 0x0108 4FFF |
| | Sector 8 | 4K x 16 | 0x000A 8000 | 0x000A 8FFF | 512 x 16 | 0x0108 5000 | 0x0108 51FF |
| | Sector 9 | 4K x 16 | 0x000A 9000 | 0x000A 9FFF | 512 x 16 | 0x0108 5200 | 0x0108 53FF |
| | Sector 10 | 4K x 16 | 0x000A A000 | 0x000A AFFF | 512 x 16 | 0x0108 5400 | 0x0108 55FF |
| | Sector 11 | 4K x 16 | 0x000A B000 | 0x000A BFFF | 512 x 16 | 0x0108 5600 | 0x0108 57FF |
| | Sector 12 | 4K x 16 | 0x000A C000 | 0x000A CFFF | 512 x 16 | 0x0108 5800 | 0x0108 59FF |
| | Sector 13 | 4K x 16 | 0x000A D000 | 0x000A DFFF | 512 x 16 | 0x0108 5A00 | 0x0108 5BFF |
| | Sector 14 | 4K x 16 | 0x000A E000 | 0x000A EFFF | 512 x 16 | 0x0108 5C00 | 0x0108 5DFF |
| | Sector 15 | 4K x 16 | 0x000A F000 | 0x000A FFFF | 512 x 16 | 0x0108 5E00 | 0x0108 5FFF |

7.3.4 Peripheral Registers Memory Map

The Peripheral Registers Memory Map (C28) table lists the peripheral registers.

Table 7-4. Peripheral Registers Memory Map

| Structure | DriverLib Name | Base Address | CPU1 | DMA | HIC | CLA | Pipeline Protected |
|---------------------------------|-------------------|--------------|------|-----|-----|-----|--------------------|
| Peripheral Frame 0 (PF0) | | | | | | | |
| ADC_RESULT_REGS | ADCARESLT_BASE | 0x0000_0B00 | YES | YES | YES | YES | - |
| ADC_RESULT_REGS | ADCBRESULT_BASE | 0x0000_0B20 | YES | YES | YES | YES | - |
| ADC_RESULT_REGS | ADCCRESULT_BASE | 0x0000_0B40 | YES | YES | YES | YES | - |
| CPUTIMER_REGS | CPUTIMER0_BASE | 0x0000_0C00 | YES | - | - | - | - |
| CLA_ONLY_REGS | CLA1_ONLY_BASE | 0x0000_0C00 | - | - | - | YES | - |
| CPUTIMER_REGS | CPUTIMER1_BASE | 0x0000_0C08 | YES | - | - | - | - |
| CPUTIMER_REGS | CPUTIMER2_BASE | 0x0000_0C10 | YES | - | - | - | - |
| CLA_SOFTINT_REGS | CLA1_SOFTINT_BASE | 0x0000_0CE0 | - | - | - | YES | - |
| PIE_CTRL_REGS | PIECTRL_BASE | 0x0000_0CE0 | YES | - | - | - | - |
| PIE_VECT_TABLE | PIEVECTABLE_BASE | 0x0000_0D00 | YES | - | - | - | - |
| DMA_REGS | DMA_BASE | 0x0000_1000 | YES | - | - | - | - |
| DMA_CH_REGS | DMA_CH1_BASE | 0x0000_1020 | YES | - | - | - | - |
| DMA_CH_REGS | DMA_CH2_BASE | 0x0000_1040 | YES | - | - | - | - |
| DMA_CH_REGS | DMA_CH3_BASE | 0x0000_1060 | YES | - | - | - | - |
| DMA_CH_REGS | DMA_CH4_BASE | 0x0000_1080 | YES | - | - | - | - |
| DMA_CH_REGS | DMA_CH5_BASE | 0x0000_10A0 | YES | - | - | - | - |
| DMA_CH_REGS | DMA_CH6_BASE | 0x0000_10C0 | YES | - | - | - | - |
| CLA_REGS | CLA1_BASE | 0x0000_1400 | YES | - | - | - | - |
| UID_REGS | UID_BASE | 0x0007_0200 | YES | - | - | - | - |
| DSCM_Z1_OTP | DSCM_Z1OTP_BASE | 0x0007_8000 | YES | - | - | - | - |
| DSCM_Z2_OTP | DSCM_Z2OTP_BASE | 0x0007_8200 | YES | - | - | - | - |
| Peripheral Frame 1 (PF1) | | | | | | | |
| EPWM_REGS | EPWM1_BASE | 0x0000_4000 | YES | YES | YES | YES | YES |
| EPWM_REGS | EPWM2_BASE | 0x0000_4100 | YES | YES | YES | YES | YES |
| EPWM_REGS | EPWM3_BASE | 0x0000_4200 | YES | YES | YES | YES | YES |
| EPWM_REGS | EPWM4_BASE | 0x0000_4300 | YES | YES | YES | YES | YES |
| EPWM_REGS | EPWM5_BASE | 0x0000_4400 | YES | YES | YES | YES | YES |
| EPWM_REGS | EPWM6_BASE | 0x0000_4500 | YES | YES | YES | YES | YES |
| EPWM_REGS | EPWM7_BASE | 0x0000_4600 | YES | YES | YES | YES | YES |
| EPWM_REGS | EPWM8_BASE | 0x0000_4700 | YES | YES | YES | YES | YES |
| EQEP_REGS | EQEP1_BASE | 0x0000_5100 | YES | YES | YES | YES | YES |
| EQEP_REGS | EQEP2_BASE | 0x0000_5140 | YES | YES | YES | YES | YES |
| ECAP_REGS | ECAP1_BASE | 0x0000_5200 | YES | YES | YES | YES | YES |
| ECAP_REGS | ECAP2_BASE | 0x0000_5240 | YES | YES | YES | YES | YES |
| ECAP_REGS | ECAP3_BASE | 0x0000_5280 | YES | YES | YES | YES | YES |
| HRCAP_REGS | HRCAP3_BASE | 0x0000_52A0 | YES | YES | YES | YES | YES |
| DAC_REGS | DACA_BASE | 0x0000_5C00 | YES | YES | YES | YES | YES |
| DAC_REGS | DACB_BASE | 0x0000_5C10 | YES | YES | YES | YES | YES |
| CMPSS_REGS | CMPSS1_BASE | 0x0000_5C80 | YES | YES | YES | YES | YES |
| CMPSS_REGS | CMPSS2_BASE | 0x0000_5CA0 | YES | YES | YES | YES | YES |
| CMPSS_REGS | CMPSS3_BASE | 0x0000_5CC0 | YES | YES | YES | YES | YES |
| CMPSS_REGS | CMPSS4_BASE | 0x0000_5CE0 | YES | YES | YES | YES | YES |
| SDFM_REGS | SDFM1_BASE | 0x0000_5E00 | YES | YES | YES | YES | YES |
| SDFM_REGS | SDFM2_BASE | 0x0000_5E80 | YES | YES | YES | YES | YES |

Table 7-4. Peripheral Registers Memory Map (continued)

| Structure | DriverLib Name | Base Address | CPU1 | DMA | HIC | CLA | Pipeline Protected |
|---------------------------------|--------------------|--------------|------|-----|-----|-----|--------------------|
| Peripheral Frame 2 (PF2) | | | | | | | |
| SPI_REGS | SPIA_BASE | 0x0000_6100 | YES | YES | YES | YES | YES |
| SPI_REGS | SPIB_BASE | 0x0000_6110 | YES | YES | YES | YES | YES |
| BGCRC_REGS | BGCRC_CPU_BASE | 0x0000_6340 | YES | - | - | - | YES |
| BGCRC_REGS | BGCRC_CLA1_BASE | 0x0000_6380 | YES | - | - | YES | YES |
| PMBUS_REGS | PMBUSA_BASE | 0x0000_6400 | YES | YES | YES | YES | YES |
| HIC_CFG_REGS | HIC_BASE | 0x0000_6500 | YES | YES | - | - | YES |
| FSI_TX_REGS | FSITXA_BASE | 0x0000_6600 | YES | YES | YES | YES | YES |
| FSI_RX_REGS | FSIRXA_BASE | 0x0000_6680 | YES | YES | YES | YES | YES |
| Peripheral Frame 3 (PF3) | | | | | | | |
| ADC_REGS | ADCA_BASE | 0x0000_7400 | YES | - | - | YES | YES |
| ADC_REGS | ADCB_BASE | 0x0000_7480 | YES | - | - | YES | YES |
| ADC_REGS | ADCC_BASE | 0x0000_7500 | YES | - | - | YES | YES |
| Peripheral Frame 4 (PF4) | | | | | | | |
| INPUT_XBAR_REGS | INPUTXBAR_BASE | 0x0000_7900 | YES | - | - | - | YES |
| XBAR_REGS | XBAR_BASE | 0x0000_7920 | YES | - | - | - | YES |
| SYNC_SOC_REGS | SYNCSOC_BASE | 0x0000_7940 | YES | - | - | - | YES |
| INPUT_XBAR_REGS | CLBINPUTXBAR_BASE | 0x0000_7960 | YES | - | - | - | YES |
| DMA_CLA_SRC_SEL_REGS | DMACLASRCSEL_BASE | 0x0000_7980 | YES | - | - | - | YES |
| EPWM_XBAR_REGS | EPWMXBAR_BASE | 0x0000_7A00 | YES | - | - | - | YES |
| CLB_XBAR_REGS | CLBXBAR_BASE | 0x0000_7A40 | YES | - | - | - | YES |
| OUTPUT_XBAR_REGS | OUTPUTXBAR_BASE | 0x0000_7A80 | YES | - | - | - | YES |
| OUTPUT_XBAR_REGS | CLBOUTPUTXBAR_BASE | 0x0000_7BC0 | YES | - | - | - | YES |
| GPIO_CTRL_REGS | GPIOCTRL_BASE | 0x0000_7C00 | YES | - | - | - | YES |
| GPIO_DATA_REGS | GPIODATA_BASE | 0x0000_7F00 | YES | - | - | YES | YES |
| GPIO_DATA_READ_REGS | GPIODATAREAD_BASE | 0x0000_7F80 | YES | - | YES | YES | YES |
| CLK_CFG_REGS | CLKCFG_BASE | 0x0005_D200 | YES | - | - | - | YES |
| CPU_SYS_REGS | CPUSYS_BASE | 0x0005_D300 | YES | - | - | - | YES |
| SYS_STATUS_REGS | SYSSTAT_BASE | 0x0005_D400 | YES | - | - | - | YES |
| PERIPH_AC_REGS | PERIPHAC_BASE | 0x0005_D500 | YES | - | - | - | YES |
| ANALOG_SUBSYS_REGS | ANALOGSUBSYS_BASE | 0x0005_D700 | YES | - | - | - | YES |
| Peripheral Frame 5 (PF5) | | | | | | | |
| DEV_CFG_REGS | DEVCFG_BASE | 0x0005_D000 | YES | - | - | - | YES |
| ERAD_GLOBAL_REGS | ERAD_GLOBAL_BASE | 0x0005_E800 | YES | - | - | - | YES |
| ERAD_HWBP_REGS | ERAD_HWBP1_BASE | 0x0005_E900 | YES | - | - | - | YES |
| ERAD_HWBP_REGS | ERAD_HWBP2_BASE | 0x0005_E908 | YES | - | - | - | YES |
| ERAD_HWBP_REGS | ERAD_HWBP3_BASE | 0x0005_E910 | YES | - | - | - | YES |
| ERAD_HWBP_REGS | ERAD_HWBP4_BASE | 0x0005_E918 | YES | - | - | - | YES |
| ERAD_HWBP_REGS | ERAD_HWBP5_BASE | 0x0005_E920 | YES | - | - | - | YES |
| ERAD_HWBP_REGS | ERAD_HWBP6_BASE | 0x0005_E928 | YES | - | - | - | YES |
| ERAD_HWBP_REGS | ERAD_HWBP7_BASE | 0x0005_E930 | YES | - | - | - | YES |
| ERAD_HWBP_REGS | ERAD_HWBP8_BASE | 0x0005_E938 | YES | - | - | - | YES |
| ERAD_COUNTER_REGS | ERAD_COUNTER1_BASE | 0x0005_E980 | YES | - | - | - | YES |
| ERAD_COUNTER_REGS | ERAD_COUNTER2_BASE | 0x0005_E990 | YES | - | - | - | YES |

Table 7-4. Peripheral Registers Memory Map (continued)

| Structure | DriverLib Name | Base Address | CPU1 | DMA | HIC | CLA | Pipeline Protected |
|-----------------------------------|-----------------------|--------------|------|-----|-----|-----|--------------------|
| ERAD_COUNTER_REGS | ERAD_COUNTER3_BASE | 0x0005_E9A0 | YES | - | - | - | YES |
| ERAD_COUNTER_REGS | ERAD_COUNTER4_BASE | 0x0005_E9B0 | YES | - | - | - | YES |
| ERAD_CRC_GLOBAL_REGS | ERAD_CRC_GLOBAL_BASE | 0x0005_EA00 | YES | - | - | - | YES |
| ERAD_CRC_REGS | ERAD_CRC1_BASE | 0x0005_EA10 | YES | - | - | - | YES |
| ERAD_CRC_REGS | ERAD_CRC2_BASE | 0x0005_EA20 | YES | - | - | - | YES |
| ERAD_CRC_REGS | ERAD_CRC3_BASE | 0x0005_EA30 | YES | - | - | - | YES |
| ERAD_CRC_REGS | ERAD_CRC4_BASE | 0x0005_EA40 | YES | - | - | - | YES |
| ERAD_CRC_REGS | ERAD_CRC5_BASE | 0x0005_EA50 | YES | - | - | - | YES |
| ERAD_CRC_REGS | ERAD_CRC6_BASE | 0x0005_EA60 | YES | - | - | - | YES |
| ERAD_CRC_REGS | ERAD_CRC7_BASE | 0x0005_EA70 | YES | - | - | - | YES |
| ERAD_CRC_REGS | ERAD_CRC8_BASE | 0x0005_EA80 | YES | - | - | - | YES |
| EPG_REGS | EPG1_BASE | 0x0005_EC00 | YES | - | - | - | YES |
| EPG_MUX_REGS | EPG1MUX_BASE | 0x0005_ECD0 | YES | - | - | - | YES |
| DCSM_Z1_REGS | DCSM_Z1_BASE | 0x0005_F000 | YES | - | - | - | YES |
| DCSM_Z2_REGS | DCSM_Z2_BASE | 0x0005_F080 | YES | - | - | - | YES |
| DCSM_COMMON_REGS | DCSMCOMMON_BASE | 0x0005_F0C0 | YES | - | - | - | YES |
| MEM_CFG_REGS | MEMCFG_BASE | 0x0005_F400 | YES | - | - | - | YES |
| ACCESS_PROTECTION_REGS | ACCESSPROTECTION_BASE | 0x0005_F500 | YES | - | - | - | YES |
| MEMORY_ERROR_REGS | MEMORYERROR_BASE | 0x0005_F540 | YES | - | - | - | YES |
| TEST_ERROR_REGS | TESTERROR_BASE | 0x0005_F590 | YES | - | - | - | YES |
| FLASH_CTRL_REGS | FLASH0CTRL_BASE | 0x0005_F800 | YES | - | - | - | YES |
| FLASH_ECC_REGS | FLASH0ECC_BASE | 0x0005_FB00 | YES | - | - | - | YES |
| Peripheral Frame 7 (PF7) | | | | | | | |
| CAN_REGS | CANA_BASE | 0x0004_8000 | YES | YES | YES | - | YES |
| MCANSS_REGS | MCANASS_BASE | 0x0005_C400 | YES | - | YES | - | YES |
| MCAN_REGS | MCANA_BASE | 0x0005_C600 | YES | - | YES | - | YES |
| MCAN_ERROR_REGS | MCANA_ERROR_BASE | 0x0005_C800 | YES | - | YES | - | YES |
| HWBIST_REGS | HWBIST_BASE | 0x0005_E000 | YES | - | - | - | YES |
| PBIST_REGS | MPOST_BASE | 0x0005_E200 | YES | - | - | - | YES |
| DCC_REGS | DCC0_BASE | 0x0005_E700 | YES | - | - | - | YES |
| DCC_REGS | DCC1_BASE | 0x0005_E740 | YES | - | - | - | YES |
| Peripheral Frame 8 (PF8) | | | | | | | |
| LIN_REGS | LINA_BASE | 0x0000_6A00 | YES | YES | YES | YES | YES |
| LIN_REGS | LINB_BASE | 0x0000_6B00 | YES | YES | YES | YES | YES |
| Peripheral Frame 9 (PF9) | | | | | | | |
| WD_REGS | WD_BASE | 0x0000_7000 | YES | - | - | - | YES |
| NMI_INTERRUPT_REGS | NMI_BASE | 0x0000_7060 | YES | - | - | - | YES |
| XINT_REGS | XINT_BASE | 0x0000_7070 | YES | - | - | - | YES |
| SCI_REGS | SCIA_BASE | 0x0000_7200 | YES | - | YES | - | YES |
| SCI_REGS | SCIB_BASE | 0x0000_7210 | YES | - | YES | - | YES |
| I2C_REGS | I2CA_BASE | 0x0000_7300 | YES | - | YES | - | YES |
| I2C_REGS | I2CB_BASE | 0x0000_7340 | YES | - | YES | - | YES |
| Peripheral Frame 10 (PF10) | | | | | | | |
| CLB_LOGIC_CONFIG_REGS | CLB1_LOGICCFG_BASE | 0x0000_3000 | YES | - | YES | YES | - |

Table 7-4. Peripheral Registers Memory Map (continued)

| Structure | DriverLib Name | Base Address | CPU1 | DMA | HIC | CLA | Pipeline Protected |
|-----------------------------------|---------------------|--------------|------|-----|-----|-----|--------------------|
| CLB_LOGIC_CONTROL_REGS | CLB1_LOGICCTRL_BASE | 0x0000_3100 | YES | - | YES | YES | - |
| CLB_DATA_EXCHANGE_REGS | CLB1_DATAEXCH_BASE | 0x0000_3180 | YES | - | YES | YES | - |
| CLB_LOGIC_CONFIG_REGS | CLB2_LOGICCFG_BASE | 0x0000_3400 | YES | - | YES | YES | - |
| CLB_LOGIC_CONTROL_REGS | CLB2_LOGICCTRL_BASE | 0x0000_3500 | YES | - | YES | YES | - |
| CLB_DATA_EXCHANGE_REGS | CLB2_DATAEXCH_BASE | 0x0000_3580 | YES | - | YES | YES | - |
| CLB_LOGIC_CONFIG_REGS | CLB3_LOGICCFG_BASE | 0x0000_3800 | YES | - | YES | YES | - |
| CLB_LOGIC_CONTROL_REGS | CLB3_LOGICCTRL_BASE | 0x0000_3900 | YES | - | YES | YES | - |
| CLB_DATA_EXCHANGE_REGS | CLB3_DATAEXCH_BASE | 0x0000_3980 | YES | - | YES | YES | - |
| CLB_LOGIC_CONFIG_REGS | CLB4_LOGICCFG_BASE | 0x0000_3C00 | YES | - | YES | YES | - |
| CLB_LOGIC_CONTROL_REGS | CLB4_LOGICCTRL_BASE | 0x0000_3D00 | YES | - | YES | YES | - |
| CLB_DATA_EXCHANGE_REGS | CLB4_DATAEXCH_BASE | 0x0000_3D80 | YES | - | YES | YES | - |
| Peripheral Frame 11 (PF11) | | | | | | | |
| AES_REGS | AESA_BASE | 0x0004_2000 | YES | YES | - | - | - |
| AES_SS_REGS | AESA_SS_BASE | 0x0004_2C00 | YES | YES | - | - | - |
| Peripheral Frame 12 (PF12) | | | | | | | |
| LFU_REGS | LFU_BASE | 0x0000_7FE0 | YES | - | - | YES | YES |

7.4 Identification

Table 7-5 lists the Device Identification Registers. Additional information on these device identification registers can be found in the [TMS320F28003x Real-Time Microcontrollers Technical Reference Manual](#). See the register descriptions of PARTIDH and PARTIDL for identification of production status (TMX or TMS) and other device information.

Table 7-5. Device Identification Registers

| NAME | ADDRESS | SIZE (x16) | DESCRIPTION |
|--------------------------------------|-------------|------------|---|
| PARTIDH | 0x0005 D00A | 2 | Device part identification number |
| | | | TMS320F280039C 0x05FF 0500 |
| | | | TMS320F280039 0x05FF 0500 |
| | | | TMS320F280038C 0x05FE 0500 |
| | | | TMS320F280038 0x05FE 0500 |
| | | | TMS320F280037C 0x05FD 0500 |
| | | | TMS320F280037 0x05FD 0500 |
| | | | TMS320F280036C 0x05FC 0500 |
| | | | TMS320F280036 0x05FC 0500 |
| | | | TMS320F280034 0x05FA 0500 |
| TMS320F280033 0x05F9 0500 | | | |
| REVID | 0x0005 D00C | 2 | Silicon revision number Revision 0 0x0000 0000 |
| UID_UNIQUE | 0x0007 020C | 2 | Unique identification number. This number is different on each individual device with the same PARTIDH. This unique number can be used as a serial number in the application. This number is present only on TMS devices. |

7.5 Bus Architecture – Peripheral Connectivity

The Peripheral Connectivity table lists a broad view of the peripheral and configuration register accessibility from each bus master.

Table 7-6. Peripheral Connectivity

| PERIPHERAL | DMA | HIC | BGCRC | CLA | C28 |
|------------------------------------|-----|-----|-------|-----|-----|
| SYSTEM PERIPHERALS | | | | | |
| CPU Timers | | | | | Y |
| ERAD | | | | | Y |
| GPIO Data | | Y | | Y | Y |
| GPIO Pin Mapping and Configuration | | | | | Y |
| XBAR Configuration | | | | | Y |
| System Configuration | | | | | Y |
| AES | Y | | | | Y |
| EPG | | | | | Y |
| LFU | | | | Y | Y |
| DCC | | | | | Y |
| MEMORY | | | | | |
| M0/M1 | | | Y | | Y |
| LSx | | | Y | Y | Y |
| GSx | Y | Y | Y | | Y |
| ROM | | | Y | | Y |
| FLASH | | | | | Y |
| CONTROL PERIPHERALS | | | | | |
| ePWM/HRPWM | Y | Y | | Y | Y |
| eCAP/HRCAP | Y | Y | | Y | Y |
| eQEP ¹ | Y | Y | | Y | Y |
| CLB | | Y | | Y | Y |
| SDFM | Y | Y | | Y | Y |
| ANALOG PERIPHERALS | | | | | |
| CMPSS ¹ | Y | Y | | Y | Y |
| DAC ¹ | Y | Y | | Y | Y |
| ADC Configuration | | | | Y | Y |
| ADC Results ¹ | Y | Y | | Y | Y |
| COMMUNICATION PERIPHERALS | | | | | |
| DCAN | Y | Y | | | Y |
| MCAN | | Y | | | Y |
| FSITX/FSIRX | Y | Y | | Y | Y |
| I2C | | Y | | | Y |
| LIN | Y | Y | | Y | Y |
| PMBus | Y | Y | | Y | Y |
| SCI | | Y | | | Y |
| SPI | Y | Y | | Y | Y |

(1) These modules are accessible from DMA but cannot trigger a DMA transfer.

7.6 C28x Processor

The CPU is a 32-bit fixed-point processor. This device draws from the best features of digital signal processing; reduced instruction set computing (RISC); and microcontroller architectures, firmware, and tool sets.

The CPU features include a modified Harvard architecture and circular addressing. The RISC features are single-cycle instruction execution, register-to-register operations, and modified Harvard architecture. The microcontroller features include ease of use through an intuitive instruction set, byte packing and unpacking, and bit manipulation. The modified Harvard architecture of the CPU enables instruction and data fetches to be performed in parallel. The CPU can read instructions and data while it writes data simultaneously to maintain the single-cycle instruction operation across the pipeline. The CPU does this over six separate address/data buses.

For more information on CPU architecture and instruction set, see the [TMS320C28x CPU and Instruction Set Reference Guide](#).

7.6.1 Floating-Point Unit (FPU)

The C28x plus floating-point (C28x+FPU) processor extends the capabilities of the C28x fixed-point CPU by adding registers and instructions to support IEEE single-precision floating-point operations.

Devices with the C28x+FPU include the standard C28x register set plus an additional set of floating-point unit registers. The additional floating-point unit registers are the following:

- Eight floating-point result registers, RnH (where n = 0–7)
- Floating-point Status Register (STF)
- Repeat Block Register (RB)

All of the floating-point registers, except the RB, are shadowed. This shadowing can be used in high-priority interrupts for fast context save and restore of the floating-point registers.

For more information on the C28x Floating Point Unit (FPU), see the [TMS320C28x Extended Instruction Sets Technical Reference Manual](#).

7.6.2 Fast Integer Division Unit

The Fast Integer Division (FINTDIV) unit of the C28x CPU uniquely supports three types of integer division (Truncated, Modulus, Euclidean) of varying data type sizes (16/16, 32/16, 32/32, 64/32, 64/64) in unsigned or signed formats.

- Truncated integer division is naturally supported by C language (/, % operators).
- Modulus and Euclidean divisions are variants that are more efficient for control algorithms and are supported by C intrinsics.

All three types of integer division produce both a quotient and remainder component, are interruptible, and execute in a minimum number of deterministic cycles (10 cycles for a 32/32 division). In addition, the Fast Division capabilities of the C28x CPU uniquely support fast execution of floating-point 32-bit (in 5 cycles) and 64-bit (in 20 cycles) division.

For more information about fast integer division, see the [Fast Integer Division – A Differentiated Offering From C2000™ Product Family Application Report](#).

7.6.3 Trigonometric Math Unit (TMU)

The trigonometric math unit (TMU) extends the capabilities of a C28x+FPU by adding instructions and leveraging existing FPU instructions to speed up the execution of common trigonometric and arithmetic operations listed in [Table 7-7](#).

Table 7-7. TMU Supported Instructions

| Instructions | C Equivalent Operation | Pipeline Cycles |
|-------------------|------------------------|-----------------|
| MPY2PIF32 RaH,RbH | $a = b * 2\pi$ | 2/3 |
| DIV2PIF32 RaH,RbH | $a = b / 2\pi$ | 2/3 |

Table 7-7. TMU Supported Instructions (continued)

| Instructions | C Equivalent Operation | Pipeline Cycles |
|-------------------------|--|-----------------|
| DIVF32 RaH,RbH,RcH | $a = b/c$ | 5 |
| SQRTF32 RaH,RbH | $a = \text{sqrt}(b)$ | 5 |
| SINPUF32 RaH,RbH | $a = \sin(b*2\pi)$ | 4 |
| COSPUF32 RaH,RbH | $a = \cos(b*2\pi)$ | 4 |
| ATANPUF32 RaH,RbH | $a = \text{atan}(b)/2\pi$ | 4 |
| QUADF32 RaH,RbH,RcH,RdH | Operation to assist in calculating ATANPU2 | 5 |

Exponent instruction IEXP2F32 and logarithmic instruction LOG2F32 have been added to support computation of floating-point power function for the nonlinear proportional integral derivative control (NLPID) component of the C2000 Digital Control Library. These two added instructions reduce the power function calculations from a typical of 300 cycles using library emulation to less than 10 cycles.

No changes have been made to existing instructions, pipeline or memory bus architecture. All TMU instructions use the existing FPU register set (R0H to R7H) to carry out their operations.

For more information, see the [TMS320C28x Extended Instruction Sets Technical Reference Manual](#).

7.6.4 VCRC Unit

Cyclic redundancy check (CRC) algorithms provide a straightforward method for verifying data integrity over large data blocks, communication packets, or code sections. The C28x+VCRC can perform 8-bit, 16-bit, 24-bit, and 32-bit CRCs. For example, the VCRC can compute the CRC for a block length of 10 bytes in 10 cycles. A CRC result register contains the current CRC, which is updated whenever a CRC instruction is executed.

The following are the CRC polynomials used by the CRC calculation logic of the VCRC:

- CRC8 polynomial = 0x07
- CRC16 polynomial 1 = 0x8005
- CRC16 polynomial 2 = 0x1021
- CRC24 polynomial = 0x5d6dcb
- CRC32 polynomial 1 = 0x04c11db7
- CRC32 polynomial 2 = 0x1edc6f41

This module can calculate CRCs for a byte of data in a single cycle. The CRC calculation for CRC8, CRC16, CRC24, and CRC32 is done byte-wise (instead of computing on a complete 16-bit or 32-bit data read by the C28x core) to match the byte-wise computation requirement mandated by various standards.

The VCRC Unit also allows the user to provide the size (1b-32b) and value of any polynomial to fit custom CRC requirements. The CRC execution time increases to three cycles when using a custom polynomial.

For more information on the Cyclic Redundancy Check (VCRC) instruction sets, see the [TMS320C28x Extended Instruction Sets Technical Reference Manual](#).

7.7 Control Law Accelerator (CLA)

The CLA Type-2 is an independent, fully programmable, 32-bit floating-point math processor that brings concurrent control-loop execution to the C28x family. The low interrupt-latency of the CLA allows it to read ADC samples "just-in-time." This significantly reduces the ADC sample to output delay to enable faster system response and higher MHz control loops. By using the CLA to service time-critical control loops, the main CPU is free to perform other system tasks such as communications and diagnostics.

The control law accelerator extends the capabilities of the C28x CPU by adding parallel processing. Time-critical control loops serviced by the CLA can achieve low ADC sample to output delay. Thus, the CLA enables faster system response and higher frequency control loops. Using the CLA for time-critical tasks frees up the main CPU to perform other system and communication functions concurrently.

The following is a list of major features of the CLA:

- C compilers are available for CLA software development
- Clocked at the same rate as the main CPU (SYSCLKOUT).
- An independent architecture allowing CLA algorithm execution independent of the main C28x CPU.
 - Complete bus architecture:
 - Program Address Bus (PAB) and Program Data Bus (PDB)
 - Data Read Address Bus (DRAB), Data Read Data Bus (DRDB), Data Write Address Bus (DWAB), and Data Write Data Bus (DWDB)
 - Independent 8-stage pipeline.
 - 16-bit program counter (MPC)
 - Four 32-bit result registers (MR0 to MR3)
 - Two 16-bit auxiliary registers (MAR0, MAR1)
 - Status register (MSTF)
- Instruction set includes:
 - IEEE single-precision (32-bit) floating-point math operations
 - Floating-point math with parallel load or store
 - Floating-point multiply with parallel add or subtract
 - 1/X and 1/sqrt(X) estimations
 - Data type conversions
 - Conditional branch and call
 - Data load/store operations
- The CLA program code can consist of up to eight tasks or interrupt service routines, or seven tasks and a main background task.
 - The start address of each task is specified by the MVECT registers.
 - No limit on task size as long as the tasks fit within the configurable CLA program memory space.
 - One task is serviced at a time until its completion. There is no nesting of tasks.
 - Upon task completion a task-specific interrupt is flagged within the PIE.
 - When a task finishes the next highest-priority pending task is automatically started.
 - The Type-2 CLA can have a main task that runs continuously in the background, while other high-priority events trigger a foreground task.
- Task trigger mechanisms:
 - C28x CPU through the IACK instruction
 - Task1 to Task8: up to 256 possible trigger sources from peripherals connected to the shared bus on which the CLA assumes secondary ownership.
 - Task8 can be set to be the background task, while Tasks 1 to 7 take peripheral triggers.
- Memory and Shared Peripherals:
 - Two dedicated message RAMs for communication between the CLA and the main CPU.
 - The C28x CPU can map CLA program and data memory to the main CPU space or CLA space.

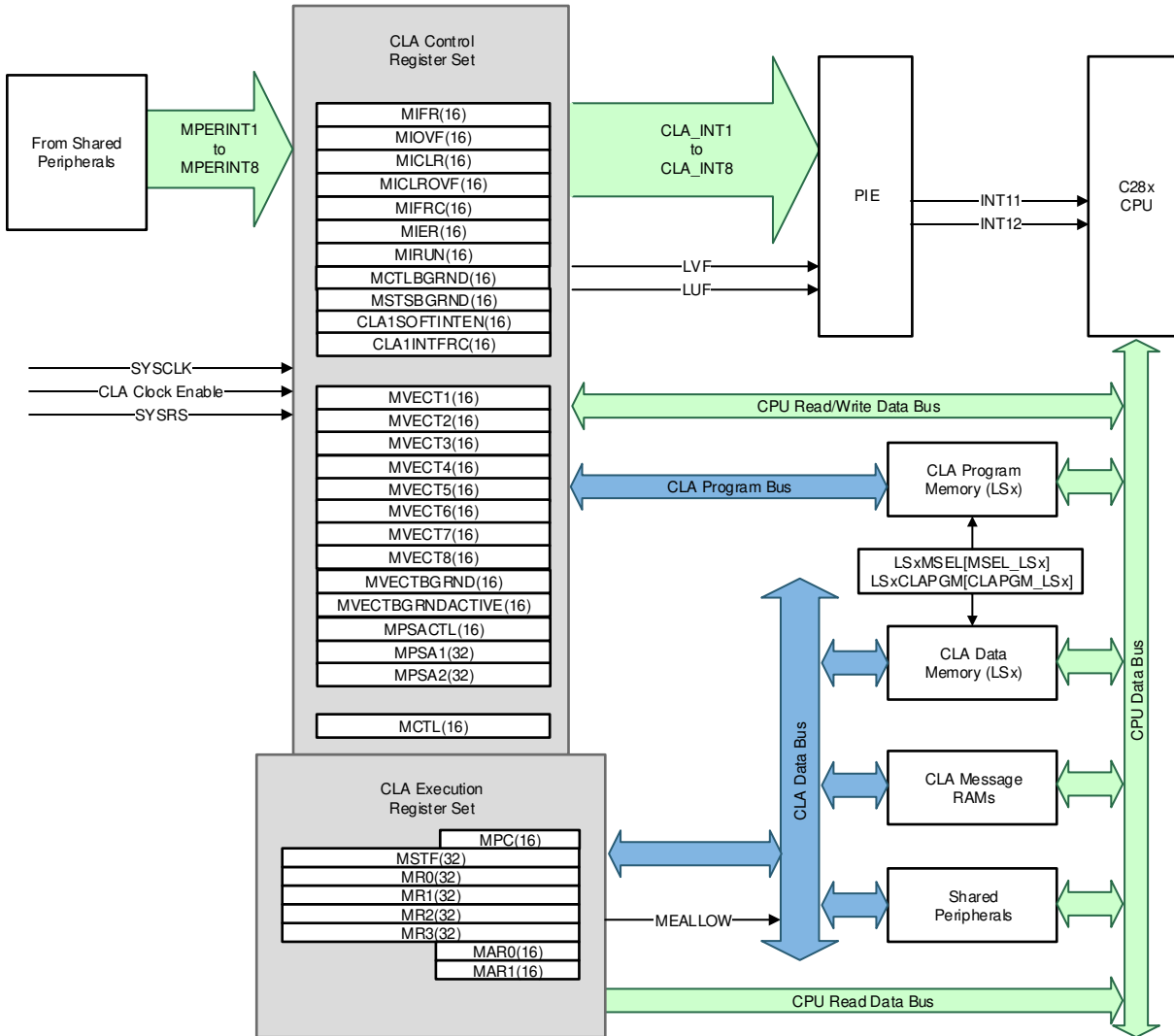


Figure 7-2. CLA Block Diagram

7.8 Embedded Real-Time Analysis and Diagnostic (ERAD)

The ERAD module enhances the debug and system-analysis capabilities of the device. The debug and system-analysis enhancements provided by the ERAD module is done outside of the CPU. The ERAD module consists of the Enhanced Bus Comparator units and the System Event Counter units. The Enhanced Bus Comparator units are used to generate hardware breakpoints, hardware watch points, and other output events. The System Event Counter units are used to analyze and profile the system. The ERAD module is accessible by the debugger and by the application software, which significantly increases the debug capabilities of many real-time systems, especially in situations where debuggers are not connected. In the TMS320F28003x devices, the ERAD module contains eight Enhanced Bus Comparator units (which increases the number of Hardware breakpoints from two to ten) and four Benchmark System Event Counter units.

7.9 Background CRC-32 (BGCRC)

The Background CRC (BGCRC) module computes a CRC-32 on a configurable block of memory. It accomplishes this by fetching the specified block of memory during idle cycles (when the CPU, HIC, CLA or DMA is not accessing the memory block). The calculated CRC-32 value is compared against a golden CRC-32 value to indicate a pass or fail. In essence, the BGCRC helps identify memory faults and corruption.

The BGCRC module has the following features:

- One cycle CRC-32 computation on 32 bits of data
- No CPU bandwidth impact for zero wait state memory
- Minimal CPU bandwidth impact for non-zero wait state memory
- Dual operation modes (CRC-32 mode and scrub mode)
- Watchdog timer to time CRC-32 completion
- Ability to pause and resume CRC-32 computation

7.10 Direct Memory Access (DMA)

The DMA module provides a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Additionally, the DMA has the capability to orthogonally rearrange the data as it is transferred as well as “ping-pong” data between buffers. These features are useful for structuring data into blocks for optimal CPU processing. Figure 7-3 shows a device-level block diagram of the DMA.

DMA features include:

- Six channels with independent PIE interrupts
- Peripheral interrupt trigger sources
 - ADC interrupts and EVT signals
 - External Interrupts
 - ePWM SOC signals
 - CPU timers
 - eCAP
 - SPI transmit and receive
 - CAN transmit and receive
 - LIN transmit and receive
- Data sources and destinations:
 - GSx RAM
 - ADC result registers
 - Control peripheral registers (ePWM, eQEP, eCAP)
 - SPI, LIN, CAN, and PMBus registers
- Word Size: 16-bit or 32-bit (SPI limited to 16-bit)
- Throughput: Four cycles per word without arbitration

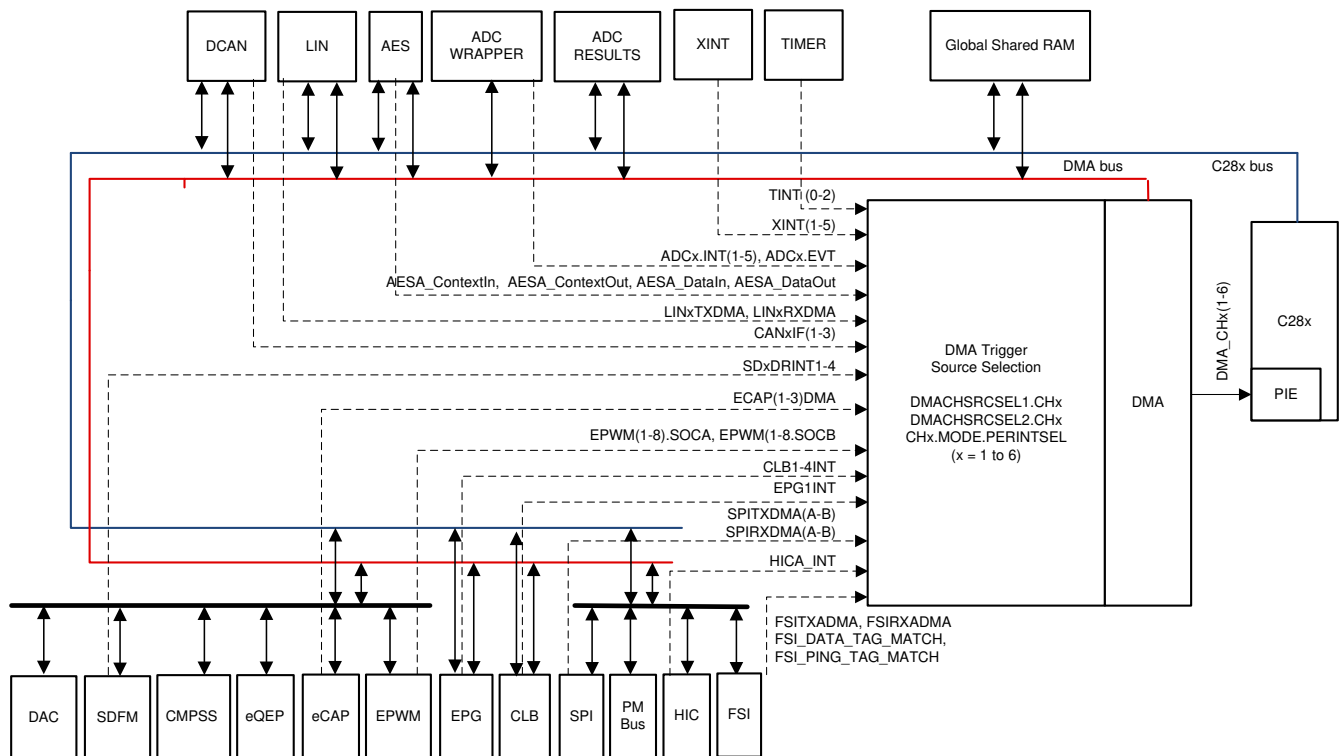


Figure 7-3. DMA Block Diagram

7.11 Device Boot Modes

This section explains the default boot modes, as well as all the available boot modes supported on this device. The boot ROM uses the boot mode select, general-purpose input/output (GPIO) pins to determine the boot mode configuration.

Table 7-8 shows the boot mode options available for selection by the default boot mode select pins. Users have the option to program the device to customize the boot modes selectable in the boot-up table as well as the boot mode select pin GPIOs used.

All the peripheral boot modes that are supported use the first instance of the peripheral module (SCIA, SPIA, I2CA, CANA, and so forth). Whenever these boot modes are referred to in this chapter, such as SCI boot, it is actually referring to the first module instance, which means the SCI boot on the SCIA port. The same applies to the other peripheral boots.

See Section 6.12.2.2.2 and the Power-on Reset figure for $t_{boot-flash}$, the boot ROM execution time to first instruction fetch in flash.

Table 7-8. Device Default Boot Modes

| BOOT MODE | GPIO24 (DEFAULT BOOT MODE SELECT PIN 1) | GPIO32 (DEFAULT BOOT MODE SELECT PIN 0) |
|--------------------------------|--|--|
| Parallel IO | 0 | 0 |
| SCI / Wait Boot ⁽¹⁾ | 0 | 1 |
| CAN | 1 | 0 |
| Flash | 1 | 1 |

- (1) SCI boot mode can be used as a wait boot mode as long as SCI continues to wait for an 'A' or 'a' during the SCI autobaud lock process.

7.11.1 Device Boot Configurations

This section details what boot configurations are available and how to configure them. This device supports from 0 boot mode select pins up to 3 boot mode select pins as well as from 1 configured boot mode up to 8 configured boot modes.

To change and configure the device from the default settings to custom settings for your application, use the following process:

1. Determine all the various ways you want application to be able to boot. (For example: Primary boot option of Flash boot for your main application, secondary boot option of CAN boot for firmware updates, tertiary boot option of SCI boot for debugging, etc)
2. Based on the number of boot modes needed, determine how many boot mode select pins (BMSPs) are required to select between your selected boot modes. (For example: 2 BMSPs are required to select between 3 boot mode options)
3. Assign the required BMSPs to a physical GPIO pin. (For example, BMSP0 to GPIO10, BMSP1 to GPIO51, and BMSP2 left as default which is disabled). Refer to [Section 7.11.1.1](#) for all the details on performing these configurations.
4. Assign the determined boot mode definitions to indexes in your custom boot table that correlate to the decoded value of the BMSPs. For example, BOOTDEF0=Boot to Flash, BOOTDEF1=CAN Boot, BOOTDEF2=SCI Boot; all other BOOTDEFx are left as default/nothing). Refer to [Section 7.11.1.2](#) for all the details on setting up and configuring the custom boot mode table.

Additionally, the Boot Mode Example Use Cases section of the [TMS320F28003x Real-Time Microcontrollers Technical Reference Manual](#) provides some example use cases on how to configure the BMSPs and custom boot tables.

Note

The CAN boot mode turns on the XTAL. Be sure an XTAL is installed in the application before using CAN boot mode.

7.11.1.1 Configuring Boot Mode Pins

This section explains how the boot mode select pins can be customized by the user, by programming the BOOTPIN-CONFIG location (refer to [Table 7-9](#)) in the user-configurable dual-zone security module (DCSM) OTP. The location in the DCSM OTP is Z1-OTP-BOOTPIN-CONFIG or Z2-OTP-BOOTPIN-CONFIG. When debugging, EMU-BOOTPIN-CONFIG is the emulation equivalent of Z1-OTP-BOOTPIN-CONFIG/Z2-OTP-BOOTPIN-CONFIG, and can be programmed to experiment with different boot modes without writing to OTP. The device can be programmed to use 0, 1, 2, or 3 boot mode select pins as needed.

Note

When using Z2-OTP-BOOTPIN-CONFIG, the configurations programmed in this location will take priority over the configurations in Z1-OTP-BOOTPIN-CONFIG. It is recommended to use Z1-OTP-BOOTPIN-CONFIG first and then if OTP configurations need to be altered, switch to using Z2-OTP-BOOTPIN-CONFIG.

Table 7-9. BOOTPIN-CONFIG Bit Fields

| BIT | NAME | DESCRIPTION |
|-------|--------------------------------|--|
| 31:24 | Key | Write 0x5A to these 8-bits to indicate the bits in this register are valid |
| 23:16 | Boot Mode Select Pin 2 (BMSP2) | Refer to BMSP0 description except for BMSP2 |
| 15:8 | Boot Mode Select Pin 1 (BMSP1) | Refer to BMSP0 description except for BMSP1 |
| 7:0 | Boot Mode Select Pin 0 (BMSP0) | Set to the GPIO pin to be used during boot (up to 255): - 0x0 = GPIO0 - 0x01 = GPIO1 - and so on Writing 0xFF disables BMSP0 and this pin is no longer used to select the boot mode. |

The following GPIOs cannot be used as a BMSP. If selected for a particular BMSP, the boot ROM automatically selects the factory default GPIO (the factory default for BMSP2 is 0xFF, which disables the BMSP).

- GPIO 20 and GPIO 21
- GPIO 36 and GPIO 38
- GPIO 62 to GPIO 223

Table 7-10. Standalone Boot Mode Select Pin Decoding

| BOOTPIN_CONFIG KEY | BMSP0 | BMSP1 | BMSP2 | REALIZED BOOT MODE |
|--------------------|--------------|--------------|--|--|
| != 0x5A | Don't Care | Don't Care | Don't Care | Boot as defined by the factory default BMSPs |
| = 0x5A | 0xFF | 0xFF | 0xFF | Boot as defined in the boot table for boot mode 0 (All BMSPs disabled) |
| | Valid GPIO | 0xFF | 0xFF | Boot as defined by the value of BMSP0 (BMSP1 and BMSP2 disabled) |
| | 0xFF | Valid GPIO | 0xFF | Boot as defined by the value of BMSP1 (BMSP0 and BMSP2 disabled) |
| | 0xFF | 0xFF | Valid GPIO | Boot as defined by the value of BMSP2 (BMSP0 and BMSP1 disabled) |
| | Valid GPIO | Valid GPIO | 0xFF | Boot as defined by the values of BMSP0 and BMSP1 (BMSP2 disabled) |
| | Valid GPIO | 0xFF | Valid GPIO | Boot as defined by the values of BMSP0 and BMSP2 (BMSP1 disabled) |
| | 0xFF | Valid GPIO | Valid GPIO | Boot as defined by the values of BMSP1 and BMSP2 (BMSP0 disabled) |
| | Valid GPIO | Valid GPIO | Valid GPIO | Boot as defined by the values of BMSP0, BMSP1, and BMSP2 |
| | Invalid GPIO | Valid GPIO | Valid GPIO | BMSP0 is reset to the factory default BMSP0 GPIO Boot as defined by the values of BMSP0, BMSP1, and BMSP2 |
| | Valid GPIO | Invalid GPIO | Valid GPIO | BMSP1 is reset to the factory default BMSP1 GPIO Boot as defined by the values of BMSP0, BMSP1, and BMSP2 |
| Valid GPIO | Valid GPIO | Invalid GPIO | BMSP2 is reset to the factory default state, which is disabled Boot as defined by the values of BMSP0 and BMSP1 | |

Note

When decoding the boot mode, BMSP0 is the least-significant-bit and BMSP2 is the most-significant-bit of the boot table index value. It is recommended when disabling BMSPs to start with disabling BMSP2. For example, in an instance when only using BMSP2 (BMSP1 and BMSP0 are disabled), then only the boot table indexes of 0 and 4 will be selectable. In the instance when using only BMSP0, then the selectable boot table indexes are 0 and 1.

7.11.1.2 Configuring Boot Mode Table Options

This section explains how to configure the boot definition table, BOOTDEF, for the device and the associated boot options. The 64-bit location is located in user-configurable DCSM OTP in the Z1-OTP-BOOTDEF-LOW and Z1-OTP-BOOTDEF-HIGH locations. When debugging, EMU-BOOTDEF-LOW and EMU-BOOTDEF-HIGH are the emulation equivalents of Z1-OTP-BOOTDEF-LOW and Z1-OTP-BOOTDEF-HIGH, and can be programmed to experiment with different boot mode options without writing to OTP. The range of customization to the boot definition table depends on how many boot mode select pins (BMSP) are being used. For example, 0 BMSPs equals to 1 table entry, 1 BMSP equals to 2 table entries, 2 BMSPs equals to 4 table entries, and 3 BMSPs equals to 8 table entries. Refer to the [TMS320F28003x Real-Time Microcontrollers Technical Reference Manual](#) for examples on how to set up the BOOTPIN_CONFIG and BOOTDEF values.

Note

The locations Z2-OTP-BOOTDEF-LOW and Z2-OTP-BOOTDEF-HIGH will be used instead of Z1-OTP-BOOTDEF-LOW and Z1-OTP-BOOTDEF-HIGH locations when Z2-OTP-BOOTPIN-CONFIG is configured. Refer to [Configuring Boot Mode Pins](#) for more details on BOOTPIN_CONFIG usage.

Table 7-11. BOOTDEF Bit Fields

| BOOTDEF NAME | BYTE POSITION | NAME | DESCRIPTION |
|--------------|---------------|------------------------|---|
| BOOT_DEF0 | 7:0 | BOOT_DEF0 Mode/Options | Set the boot mode for index 0 of the boot table. Different boot modes and their options can include, for example, a boot mode that uses different GPIOs for a specific bootloader or a different flash entry point address. Any unsupported boot mode will cause the device to either go to wait boot or boot to flash. Refer to GPIO Assignments for valid BOOTDEF values to set in the table. |
| BOOT_DEF1 | 15:8 | BOOT_DEF1 Mode/Options | Refer to BOOT_DEF0 description |
| BOOT_DEF2 | 23:16 | BOOT_DEF2 Mode/Options | |
| BOOT_DEF3 | 31:24 | BOOT_DEF3 Mode/Options | |
| BOOT_DEF4 | 39:32 | BOOT_DEF4 Mode/Options | |
| BOOT_DEF5 | 47:40 | BOOT_DEF5 Mode/Options | |
| BOOT_DEF6 | 55:48 | BOOT_DEF6 Mode/Options | |
| BOOT_DEF7 | 63:56 | BOOT_DEF7 Mode/Options | |

7.11.2 GPIO Assignments

This section details the GPIOs and boot option values used for boot mode set in the BOOT_DEF memory location located at Z1-OTP-BOOTDEF-LOW/ Z2-OTP-BOOTDEF-LOW and Z1-OTP-BOOTDEF-HIGH/ Z2-OTP-BOOTDEF-HIGH. Refer to [Configuring Boot Mode Table Options](#) on how to configure BOOT_DEF. When selecting a boot mode option, make sure to verify that the necessary pins are available in the pin mux options for the specific device package being used.

Table 7-12. SCI Boot Options

| OPTION | BOOTDEF VALUE | SCITXDA GPIO | SCIRXDA GPIO |
|-------------|---------------|--------------|--------------|
| 0 (default) | 0x01 | GPIO29 | GPIO28 |
| 1 | 0x21 | GPIO16 | GPIO17 |
| 2 | 0x41 | GPIO8 | GPIO9 |
| 3 | 0x61 | GPIO2 | GPIO3 |
| 4 | 0x81 | GPIO16 | GPIO3 |

Table 7-13. MCAN Boot Options

| OPTION | BOOTDEF VALUE | CANTXA GPIO | CANRXA GPIO |
|-------------|---------------|-------------|-------------|
| 0 (default) | 0x08 | GPIO4 | GPIO5 |
| 1 | 0x28 | GPIO1 | GPIO0 |
| 2 | 0x48 | GPIO13 | GPIO12 |

Table 7-14. DCAN Boot Options

| OPTION | BOOTDEF VALUE | CANTXA GPIO | CANRXA GPIO |
|-------------|---------------|-------------|-------------|
| 0 (default) | 0x02 | GPIO4 | GPIO5 |
| 1 | 0x22 | GPIO32 | GPIO33 |
| 2 | 0x42 | GPIO2 | GPIO3 |
| 3 | 0x62 | GPIO13 | GPIO12 |

Table 7-15. I2C Boot Options

| OPTION | BOOTDEF VALUE | SDAA GPIO | SCLA GPIO |
|--------|---------------|-----------|-----------|
| 0 | 0x07 | GPIO32 | GPIO33 |
| 1 | 0x27 | GPIO0 | GPIO1 |
| 2 | 0x47 | GPIO10 | GPIO8 |

Table 7-16. RAM Boot Options

| OPTION | BOOTDEF VALUE | RAM ENTRY POINT (ADDRESS) |
|--------|---------------|---------------------------|
| 0 | 0x05 | 0x0000 0000 |

Table 7-17. Flash Boot Options

| OPTION | BOOTDEF VALUE | FLASH ENTRY POINT (ADDRESS) | FLASH SECTOR |
|-------------|---------------|-----------------------------|-------------------|
| 0 (default) | 0x03 | 0x0008 0000 | Bank0 Sector 0 |
| 1 | 0x23 | 0x0008 8000 | Bank 0 Sector 8 |
| 2 | 0x43 | 0x0008 FFF0 | Bank 0 Sector 15 |
| 3 | 0x63 | 0x0009 0000 | Bank 1, Sector 0 |
| 4 | 0x83 | 0x0009 7FF0 | Bank 1, Sector 7 |
| 5 | 0xA3 | 0x0009 FFF0 | Bank 1, Sector 15 |
| 6 | 0xC3 | 0x000A 0000 | Bank 2, Sector 0 |
| 7 | 0xE3 | 0x000A FFF0 | Bank 2, Sector 15 |

Table 7-18. LFU Flash Boot Options

| OPTION | BOOTDEF VALUE | FLASH ENTRY POINT (ADDRESS) | BANK |
|-------------|---------------|-----------------------------|-------|
| 0 (default) | 0x0B | 0x0008 0000 | Bank0 |
| | | 0x0009 0000 | Bank1 |
| | | 0x000A 0000 | Bank2 |
| 1 | 0x2B | 0x0008 8000 | Bank0 |
| | | 0x0009 8000 | Bank1 |
| | | 0x000A 8000 | Bank2 |
| 2 | 0x4B | 0x0008 FFF0 | Bank0 |
| | | 0x0009 FFF0 | Bank1 |
| | | 0x000A FFF0 | Bank2 |
| 3 | 0x6B | 0x0008 8000 | Bank0 |
| | | 0x0009 0000 | Bank1 |
| | | 0x000A 0000 | Bank2 |
| 4 | 0x8B | 0x0008 EFF0 | Bank0 |
| | | 0x0009 7FF0 | Bank1 |
| | | 0x000A 7FF0 | Bank2 |

Table 7-19. Wait Boot Options

| OPTION | BOOTDEF VALUE | WATCHDOG |
|--------|---------------|----------|
| 0 | 0x04 | Enabled |
| 1 | 0x24 | Disabled |

Table 7-20. SPI Boot Options

| OPTION | BOOTDEF VALUE | SPISIMOA | SPISOMIA | SPICLKA | SPISTEA |
|--------|---------------|----------|----------|---------|---------|
| 0 | 0x06 | GPIO2 | GPIO1 | GPIO3 | GPIO5 |
| 1 | 0x26 | GPIO16 | GPIO1 | GPIO3 | GPIO0 |
| 2 | 0x46 | GPIO8 | GPIO10 | GPIO9 | GPIO11 |
| 3 | 0x66 | GPIO8 | GPIO17 | GPIO9 | GPIO11 |

Table 7-21. Parallel Boot Options

| OPTION | BOOTDEF VALUE | D0-D7 GPIO | 28x(DSP) CONTROL GPIO | HOST CONTROL GPIO |
|-------------|---------------|-------------|-----------------------|-------------------|
| 0 (default) | 0x00 | D0 - GPIO28 | GPIO16 | GPIO29 |
| | | D1 - GPIO1 | | |
| | | D2 - GPIO2 | | |
| | | D3 - GPIO3 | | |
| | | D4 - GPIO4 | | |
| | | D5 - GPIO5 | | |
| | | D6 - GPIO6 | | |
| | | D7 - GPIO7 | | |
| 1 | 0x20 | D0 - GPIO0 | GPIO16 | GPIO11 |
| | | D1 - GPIO1 | | |
| | | D2 - GPIO2 | | |
| | | D3 - GPIO3 | | |
| | | D4 - GPIO4 | | |
| | | D5 - GPIO5 | | |
| | | D6 - GPIO6 | | |
| | | D7 - GPIO7 | | |

7.12 Security

Security features are enforced by the Dual Code Security Module (DCSM). The primary layer of defense is securing the boundary of the chip, which should always be enabled. Additionally, the Dual Zone Security feature is available to support code partitioning.

7.12.1 Securing the Boundary of the Chip

The following two features, along with authentication in the firmware update code, should be used to help to prevent unauthorized code from running on the device.

7.12.1.1 JTAGLOCK

Enabling the JTAGLOCK feature in the USER OTP disables JTAG access (for example, debug probe) to resources on the device.

7.12.1.2 Zero-pin Boot

Enabling the Zero-pin Boot option along with Flash Boot in the USER OTP blocks all pin-based external bootloader options (for example, SCI, CAN, Parallel).

7.12.2 Dual-Zone Security

The dual-zone security mechanism offers protection for two zones: Zone 1 (Z1) and Zone 2 (Z2). The security implementation for both zones is identical. Each zone has its own dedicated secure resource (OTP memory and secure ROM) and allocated secure resource (LSx RAM and flash sectors).

7.12.3 Disclaimer

Code Security Module Disclaimer

THE CODE SECURITY MODULE (CSM) INCLUDED ON THIS DEVICE WAS DESIGNED TO PASSWORD PROTECT THE DATA STORED IN THE ASSOCIATED MEMORY AND IS WARRANTED BY TEXAS INSTRUMENTS (TI), IN ACCORDANCE WITH ITS STANDARD TERMS AND CONDITIONS, TO CONFORM TO TI'S PUBLISHED SPECIFICATIONS FOR THE WARRANTY PERIOD APPLICABLE FOR THIS DEVICE.

TI DOES NOT, HOWEVER, WARRANT OR REPRESENT THAT THE CSM CANNOT BE COMPROMISED OR BREACHED OR THAT THE DATA STORED IN THE ASSOCIATED MEMORY CANNOT BE ACCESSED THROUGH OTHER MEANS. MOREOVER, EXCEPT AS SET FORTH ABOVE, TI MAKES NO WARRANTIES OR REPRESENTATIONS CONCERNING THE CSM OR OPERATION OF THIS DEVICE, INCLUDING ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

IN NO EVENT SHALL TI BE LIABLE FOR ANY CONSEQUENTIAL, SPECIAL, INDIRECT, INCIDENTAL, OR PUNITIVE DAMAGES, HOWEVER CAUSED, ARISING IN ANY WAY OUT OF YOUR USE OF THE CSM OR THIS DEVICE, WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO LOSS OF DATA, LOSS OF GOODWILL, LOSS OF USE OR INTERRUPTION OF BUSINESS OR OTHER ECONOMIC LOSS.

7.13 Watchdog

The watchdog module is the same as the one on previous TMS320C2000™ microcontrollers, but with an optional lower limit on the time between software resets of the counter. This windowed countdown is disabled by default, so the watchdog is fully backward-compatible.

The watchdog generates either a reset or an interrupt. It is clocked from the internal oscillator with a selectable frequency divider.

Figure 7-4 shows the various functional blocks within the watchdog module.

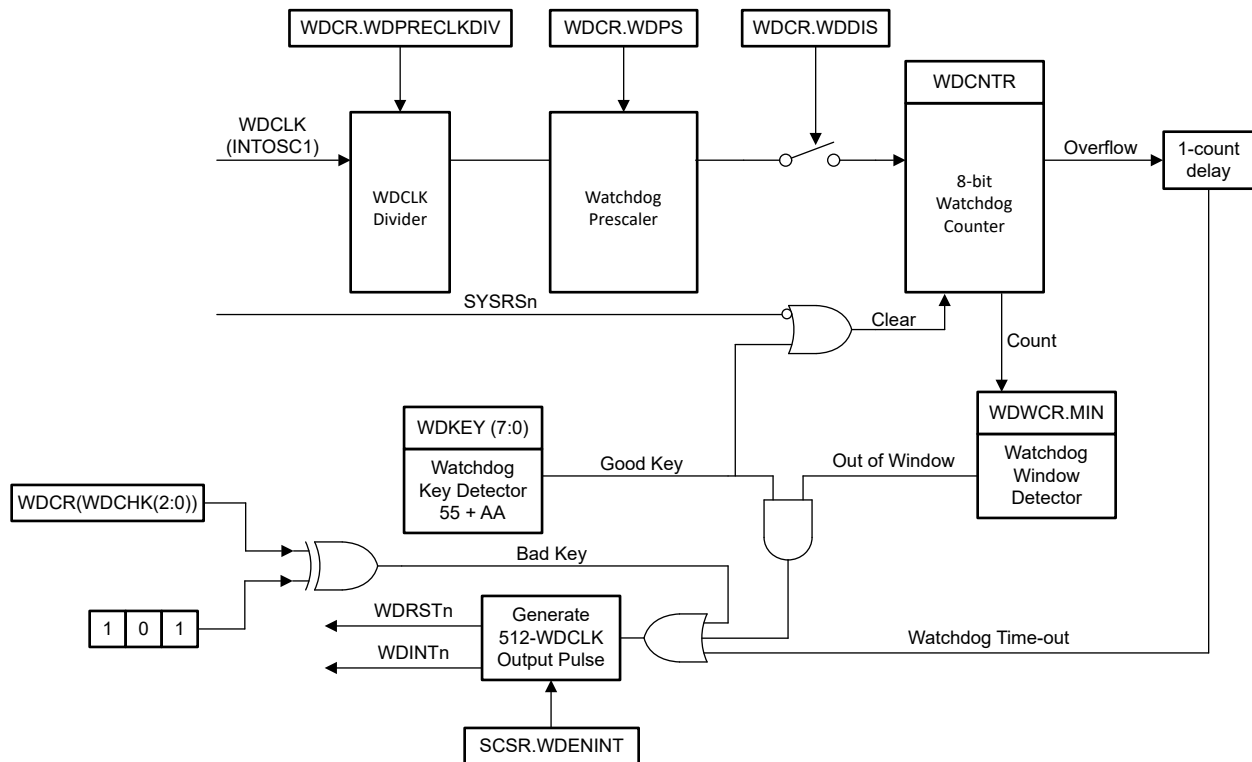


Figure 7-4. Windowed Watchdog

7.14 C28x Timers

CPU-Timers 0, 1, and 2 are identical 32-bit timers with presetable periods and with 16-bit clock prescaling. The timers have a 32-bit count-down register that generates an interrupt when the counter reaches zero. The counter is decremented at the CPU clock speed divided by the prescale value setting. When the counter reaches zero, it is automatically reloaded with a 32-bit period value.

CPU-Timer 0 is for general use and is connected to the PIE block. CPU-Timer 1 is also for general use and is connected to INT13 of the CPU. CPU-Timer 2 is reserved for TI-RTOS. It is connected to INT14 of the CPU. If TI-RTOS is not being used, CPU-Timer 2 is available for general use.

CPU-Timer 2 can be clocked by any one of the following:

- SYSCLK (default)
- Internal zero-pin oscillator 1 (INTOSC1)
- Internal zero-pin oscillator 2 (INTOSC2)
- X1 (XTAL)

7.15 Dual-Clock Comparator (DCC)

The DCC module is used for evaluating and monitoring the clock input based on a second clock, which can be a more accurate and reliable version. This instrumentation is used to detect faults in clock source or clock structures, thereby enhancing the system's safety metrics.

7.15.1 Features

The DCC has the following features:

- Allows the application to ensure that a fixed ratio is maintained between frequencies of two clock signals.
- Supports the definition of a programmable tolerance window in terms of the number of reference clock cycles.
- Supports continuous monitoring without requiring application intervention.
- Supports a single-sequence mode for spot measurements.
- Allows the selection of a clock source for each of the counters, resulting in several specific use cases.

7.15.2 Mapping of DCCx Clock Source Inputs

Table 7-22. DCCx Clock Source0 Table

| DCCxCLKSRC0[3:0] | CLOCK NAME |
|------------------|-------------------------------------|
| 0x0 | XTAL/X1 |
| 0x1 | INTOSC1 |
| 0x2 | INTOSC2 |
| 0x4 | TCK |
| 0x5 | CPU1.SYSCLK |
| 0x8 | AUXCLKIN |
| 0xC | INPUT XBAR (Output16 of input-xbar) |
| others | Reserved |

Table 7-23. DCCx Clock Source¹ Table

| DCCxCLKSRC1[4:0] | CLOCK NAME |
|------------------|---|
| 0x0 | PLLRAWCLK |
| 0x2 | INTOSC1 |
| 0x3 | INTOSC2 |
| 0x6 | CPU1.SYSCLK |
| 0x9 | Input XBAR (Output15 of the input-xbar) |
| 0xA | AUXCLKIN |
| 0xB | EPWMCLK |
| 0xC | LSPCLK |
| 0xD | ADCCLK |
| 0xE | WDCLK |
| 0xF | CAN0BITCLK |
| others | Reserved |

7.16 Configurable Logic Block (CLB)

The C2000 configurable logic block (CLB) is a collection of blocks that can be interconnected using software to implement custom digital logic functions or enhance existing on-chip peripherals. The CLB is able to enhance existing peripherals through a set of crossbar interconnections, which provide a high level of connectivity to existing control peripherals such as enhanced pulse width modulators (ePWM), enhanced capture modules (eCAP), and enhanced quadrature encoder pulse modules (eQEP). The crossbars also allow the CLB to be connected to external GPIO pins. In this way, the CLB can be configured to interact with device peripherals to perform small logical functions such as comparators, or to implement custom serial data exchange protocols. Through the CLB, functions that would otherwise be accomplished using external logic devices can now be implemented inside the MCU.

The CLB peripheral is configured through the CLB tool. For more information on the CLB tool, available examples, application reports and users guide, please refer to the following location in your [C2000Ware for C2000 MCUs](#) package (C2000Ware_2_00_00_03 and higher):

- **C2000WARE_INSTALL_LOCATION\utilities\clb_tool\clb_syscfg\doc**
- [CLB Tool User's Guide](#)
- [Designing With the C2000™ Configurable Logic Block \(CLB\) Application Report](#)
- [How to Migrate Custom Logic From an FPGA/CPLD to C2000™ Microcontrollers Application Report](#)

The CLB module and its interconnections are shown in [Figure 7-5](#).

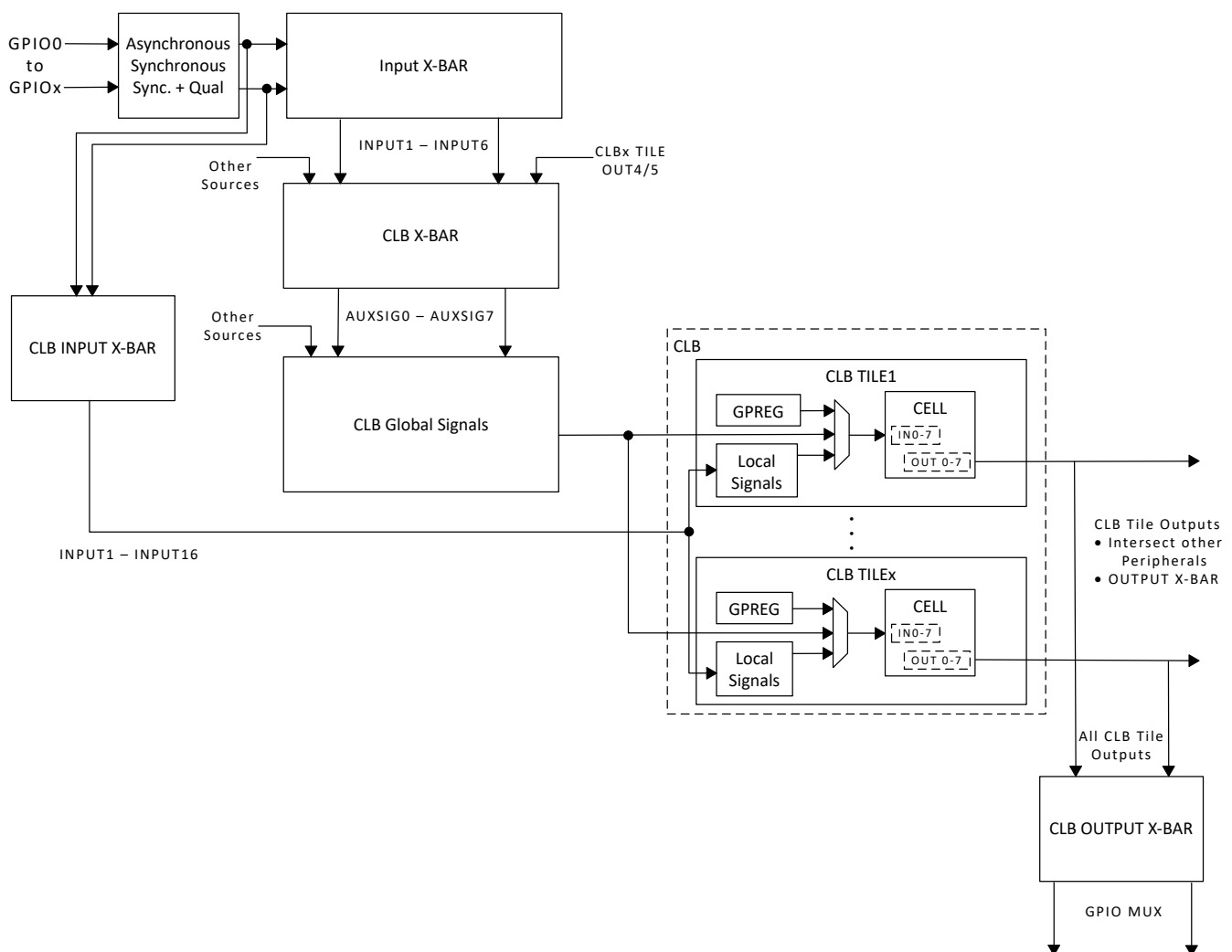


Figure 7-5. GPIO to CLB Tile Connections

Absolute encoder protocol interfaces are now provided as [Position Manager](#) solutions in the C2000Ware MotorControl SDK. Configuration files, application programmer interface (API), and use examples for such solutions are provided with [C2000Ware MotorControl SDK](#). In some solutions, the TI-configured CLB is used with other on-chip resources, such as the SPI port or the C28x CPU, to perform more complex functionality.

7.17 Functional Safety

Functional Safety-Compliant products are developed using an ISO 26262/IEC 61508-compliant hardware development process that is independently assessed and certified to meet ASIL D/SIL 3 systematic capability (see [certificate](#)). The TMS320F28003x has been certified to meet a component-level random hardware capability of ASIL B and SIL 2 (see [certificate](#)).

A functional safety manual that describes all of the hardware and software functional safety mechanisms is available. See the [Functional Safety Manual for TMS320F28003x Real-Time Microcontrollers](#).

A detailed, tunable, fault-injected, quantitative FMEDA that enables the calculation of random hardware metrics—as outlined in the International Organization for Standardization ISO 26262 and the International Electrotechnical Commission IEC 61508 for automotive and industrial applications, respectively—is also available. This tunable FMEDA must be requested; see the [C2000™ Safety Package for Automotive and Industrial Real-Time Microcontrollers User's Guide](#).

- A white paper outlining the value (or benefit) of a tunable FMEDA is available. See the [Functional Safety: A tunable FMEDA for C2000™ MCUs](#) publication.
- Part 1 and Part 2 of a five-part FMEDA tuning training are available from the [TI Video Library](#). Part 1 is [Basics of FMEDA and how it is useful in system level safety analysis](#). Part 2 is [Introduction to the C2000™ Tunable FMEDA](#). Parts 3, 4, and 5 are packaged with the tunable FMEDA, and must be requested.

Two diagnostic libraries designed for the F28003x series of devices are available to aid in the development of functionally safe systems—the CLA Self-Test Library (CLA_STL) and the Software Diagnostic Library (SDL). The CLA_STL provides software tests of the CLA and has been independently assessed and certified. It is available upon request only, see the [C2000™ Safety Package for Automotive and Industrial Real-Time Microcontrollers User's Guide](#). The SDL is a set of reference software providing example implementations of several safety mechanisms described in the device safety manual, such as HWBIST, software tests of SRAMs, software tests of Missing Clock Detect functionality, clock integrity checks using CPU Timers, and several other key features. The SDL is provided as part of [C2000Ware](#).

C2000 real-time MCUs are also equipped with a TI release validation-based C28x and CLA Compiler Qualification Kit (CQKIT), which is available for free and may be requested at the [Safety compiler qualification kit web page](#).

Additional details about how to develop functionally safe systems with C2000 real-time MCUs can be found in the following documents:

- [Automotive Functional Safety for C2000™ Real-Time Microcontrollers](#) summarizes the available functional safety products, documentation, software, and support available for aiding in the ISO 26262 certification process.
- [Industrial Functional Safety for C2000™ Real-Time Microcontrollers](#) summarizes the available functional safety products, documentation, software, and support available for aiding in the IEC 61508 certification process.
- [C2000™ Hardware Built-In Self-Test](#) discusses the Hardware Built-In Self-Test (HWBIST) feature in C2000™ real-time microcontrollers. The HWBIST provides a method of reaching a high level of diagnostic coverage on the C28x CPU, which is often needed to satisfy safety standards.
- [Error Detection in SRAM Application Report](#) provides technical information about the nature of the SRAM bit cell and bit array, as well as the sources of SRAM failures. It then presents methods for managing memory failures in electronic systems. This discussion is intended for electronic system developers or integrators who are interested in improving the robustness of the embedded SRAM.
- [C2000™ CPU Memory Built-In Self-Test](#) describes embedded memory validation using the C28x central processing unit (CPU) during an active control loop. It discusses system challenges to memory validation as well as the different solutions provided by C2000 devices and software. Finally, it presents the applicable Software Diagnostic Library features for memory testing.

8 Applications, Implementation, and Layout

8.1 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

The [Hardware Design Guide for F2800x C2000™ Real-Time MCU Series Application Note](#) is an essential guide for hardware developers using C2000 devices, and helps to streamline the design process while mitigating the potential for faulty designs. Key topics discussed include: power requirements; general-purpose input/output (GPIO) connections; analog inputs and ADC; clocking generation and requirements; and JTAG debugging among many others.

8.2 Key Device Features

Table 8-1. Key Device Features

| MODULE | FEATURE | SYSTEM BENEFIT |
|--|---|---|
| PROCESSING | | |
| Real-time control CPUs | Up to 120 MIPS C28x: 120 MIPS CLA: 120MIPs Flash: Up to 384KB RAM : Up to 69KB 32-bit Floating-Point Unit (FPU32) Trigonometric Math Unit (TMU) CRC engine and instructions (VCRC) | Provides 120 MHz of signal-processing performance for floating- or fixed-point code running from either on-chip flash or SRAM. CLA: 32-bit floating point Control Law Accelerator, parallel execution to C28x CPU FPU32: Native hardware support for IEEE-754 single-precision floating-point operations TMU: Accelerators used to speed up execution of trigonometric and arithmetic operations for faster computation (such as PLL and DQ transform) optimized for control applications. Helps in achieving faster control loops, resulting in higher efficiency and better component sizing. Special instructions to support nonlinear PID control algorithms VCRC: Provides a straightforward method for verifying data integrity over large data blocks, communication packets, or code sections. |
| SENSING | | |
| Analog-to-Digital Converter (ADC) (12-bit) | Up to 3 ADC modules 4 MSPS Up to 23 channels | ADC provides precise and concurrent sampling of all three-phase currents and DC bus with zero jitter. ADC post-processing – On-chip hardware reduces ADC ISR complexity and shortens current loop cycles. More ADCs help in multiphase applications. Provide better effective MSPS (oversampling) and typical ENOB for better control-loop performance. |

Table 8-1. Key Device Features (continued)

| MODULE | FEATURE | SYSTEM BENEFIT |
|--|--|--|
| Comparator Subsystem (CMPSS) | <p>CMPSS</p> <p>4 windowed comparator</p> <p>Dual 12-bit DACs</p> <p>DAC ramp generation</p> <p>Digital filters</p> <p>60-ns detection to trip time</p> <p>Slope compensation</p> | <p>System protection without false alarms:</p> <p>Comparator Subsystem (CMPSS) modules are useful for applications such as peak-current mode control, switched-mode power, power factor correction, and voltage trip monitoring.</p> <p>PWM trip-triggering and removal of unwanted noise are easy with blanking window and filtering features provided with the analog comparator subsystems.</p> <p>Provides better control accuracy. No need for further CPU configuration to control the PWM with the comparator and 12-bit DAC (CMPSS)</p> <p>Enables protection(CMPSS) and control(ADC) using the same pin.</p> |
| Enhanced Quadrature Encoder Pulse (eQEP) | 2 eQEP modules | Used for direct interface with a linear or rotary incremental encoder to get position, direction, and speed information from a rotating machine used in a high-performance motion and position-control system. Support CW/CCW encoding. Also can be used in other applications to count input pulses from an external device (such as a sensor). |
| Enhanced Capture (eCAP) | <p>3 eCAP modules</p> <p>Measures elapsed time between events (up to 4 time-stamped events).</p> <p>Connects to any GPIO through the input X-BAR.</p> <p>When not used in capture mode, the eCAP module can be configured as a single-channel PWM output (APWM).</p> | <p>Applications for eCAP include:</p> <p>Speed measurements of rotating machinery (for example, toothed sprockets sensed through Hall sensors)</p> <p>Elapsed time measurements between position sensor pulses</p> <p>Period and duty cycle measurements of pulse train signals</p> <p>Decoding current or voltage amplitude derived from duty-cycle encoded current/voltage sensors</p> |

Table 8-1. Key Device Features (continued)

| MODULE | FEATURE | SYSTEM BENEFIT |
|--|---|---|
| ACTUATION | | |
| Enhanced Pulse Width Modulation (ePWM) | Up to 16 ePWM channels Ability to generate high-side/low-side PWMs with deadband Supports Valley switching (ability to switch PWM output at valley point) and features like blanking window | Flexible PWM waveform generation with best power topology coverage. Shadowed Dead band itself and shadowed action qualifier enable adaptive PWM generation and protection for improved control accuracy and reduced power loss. Enables improvement in Power Factor (PF) and Total Harmonic Distortion (THD), which is especially relevant in Power Factor Correction (PFC) applications. Improves light load efficiency. |
| | One-shot and global reload feature | Critical for variable-frequency and multiphase DC-DC applications and helps in attaining high-frequency control loops (>2 MHz). Enables control of interleaved LLC topologies at high frequencies |
| | Independent PWM action on a Cycle-by-Cycle (CBC) trip event and an One-Shot Trip (OST) trip event | Provides cycle-by-cycle protection and complete shutoff of PWM under fault condition. Helps implement multiphase PFC or DC-DC control. |
| | Load on SYNC (support for shadow-to-active load on a SYNC event) | Enables variable-frequency applications (allows LLC control in power conversion). |
| | Ability to shut down the PWMs without software intervention (no ISR latency) | Fast protection under fault condition |
| | Delayed Trip Functionality | Helps implement the deadband with Peak Current Mode Control (PCMC) Phase-Shifted Full Bridge (PSFB) DC-DC easily without occupying much CPU resources (even on trigger events based on comparator, trip, or sync-in events). |
| | Dead band Generator (DB) submodule | Prevents simultaneous ON conditions of High and Low side gates by adding programmable delay to rising (RED) and falling (FED) PWM signal edges. |
| | Flexible PWM Phase Relationships and Timer Synchronization | Each ePWM module can be synchronized with other ePWM modules or other peripherals. Keeps PWM edges perfectly in synchronization with certain events. Supports flexible ADC scheduling with specific sampling window in synchronization with power device switching. |
| High-Resolution Pulse Width Modulation (HRPWM) | 8 channels with high-resolution capability (150 ps) Provides 150-ps steps for duty cycle, period, Dead band, and phase offsets for 99% greater precision | Beneficial for accurate control and enables better-performance high-frequency power conversion. Achieves cleaner waveforms and avoids oscillations/limit cycle at output. |
| CONNECTIVITY | | |
| Serial Peripheral Interface (SPI) | 2 high-speed SPI port | Supports 30 MHz |
| Serial Communication Interface (SCI) | 2 SCI (UART) modules | Interfaces with controllers |
| Local Interconnect Network (LIN) | 2 LIN | Provides a low-cost solution where the bandwidth and fault tolerance of a Controller Area Network (CAN) are not required Can also be used as simple UART |
| Controller Area Network (CAN/DCAN) | 1 DCAN module | Provides compatibility with classic CAN modules |

Table 8-1. Key Device Features (continued)

| MODULE | FEATURE | SYSTEM BENEFIT |
|---------------------------------------|---|--|
| Controller Area Network (CAN FD/MCAN) | 1 CAN FD/MCAN module | CAN FD (flexible data-rate) is an enhancement to the classic CAN protocol. CAN FD facilitates dynamic switching to higher bit rates (>1 Mbps) for the data segment and allows for up to 64 bytes compared to 8 bytes in classic CAN. This is done without having to change the physical layer. This results in a bandwidth gain over traditional CAN. Systems using CAN-FD benefit from faster in-the-field flash updates. |
| Inter-Integrated Circuit (I2C) | 2 I2C modules | Interfaces with external EEPROMs, sensors, or controllers |
| Power-Management Bus (PMBus) | 1 PMBus module Compliance with the SMI Forum PMBus Specification (Part I v1.0 and Part II v1.1) | Seamless HW-based host communication |
| OTHER SYSTEM FEATURES | | |
| Security enhancers | Dual-zone Code Security Module (DCSM) Watchdog Write Protection on Register Missing Clock Detection Logic (MCD) Error Correction Code (ECC) and parity Dual-Clock Comparator (DCC) | DCSM: Prevents duplication and reverse-engineering of proprietary code Watchdog: Generates reset if CPU gets stuck in endless loops of execution Write Protection on Registers: LOCK protection on system configuration registers Protection against spurious CPU writes MCD: Automatic clock failure detection ECC and parity: Single-bit error correction and double-bit error detection DCC: Used to detect faults in clock source |
| Crossbars (XBARs) | Provides flexibility to connect device inputs, outputs, and internal resources in a variety of configurations. <ul style="list-style-type: none"> • Input X-BAR • Output X-BAR • ePWM X-BAR | Enhances hardware design versatility: Input X-BAR: Routes signals from any GPIO to multiple IP blocks within the chip Output XBAR: Routes internal signals onto designated GPIO pins ePWM X-BAR: Routes internal signals from various IP blocks to EPWM |

8.3 Application Information

8.3.1 Typical Application

The *Typical Applications* section details *some* applications of this device. For a more extensive list of applications, see the *Applications* section of this data sheet.

8.3.1.1 Automotive Pump

Fluid or fuel control pumps are typically used in automotive engine management systems based on the type of powertrain required. Depending on the type of system and load, these actuators are in open loop or closed loop, complete with precise control.

All vehicles—internal combustion engine, electric, or hybrid (ICE/EV/HEV)—need various types of pumps (such as fuel pumps; coolant or water pumps; and oil pumps). Although the purpose of each pump is different, the function of the pump is the same: to move fluid, fuel, or oil from one place to another. In the example of a fuel pump, the pump transfers fuel from the fuel tank to the engine chamber for the engine to use. Depending on the function, pumps can be variable-speed pumps or fixed-speed pumps.

The vehicle's battery provides the current required to run the fuel pump. An electronic control unit (ECU) regulates the output pressure and volume of the gasoline, as well as meters the incoming fuel from the tank. The ECU assists the car in conserving fuel, resulting in improved economy and power.

8.3.1.1.1 System Block Diagram

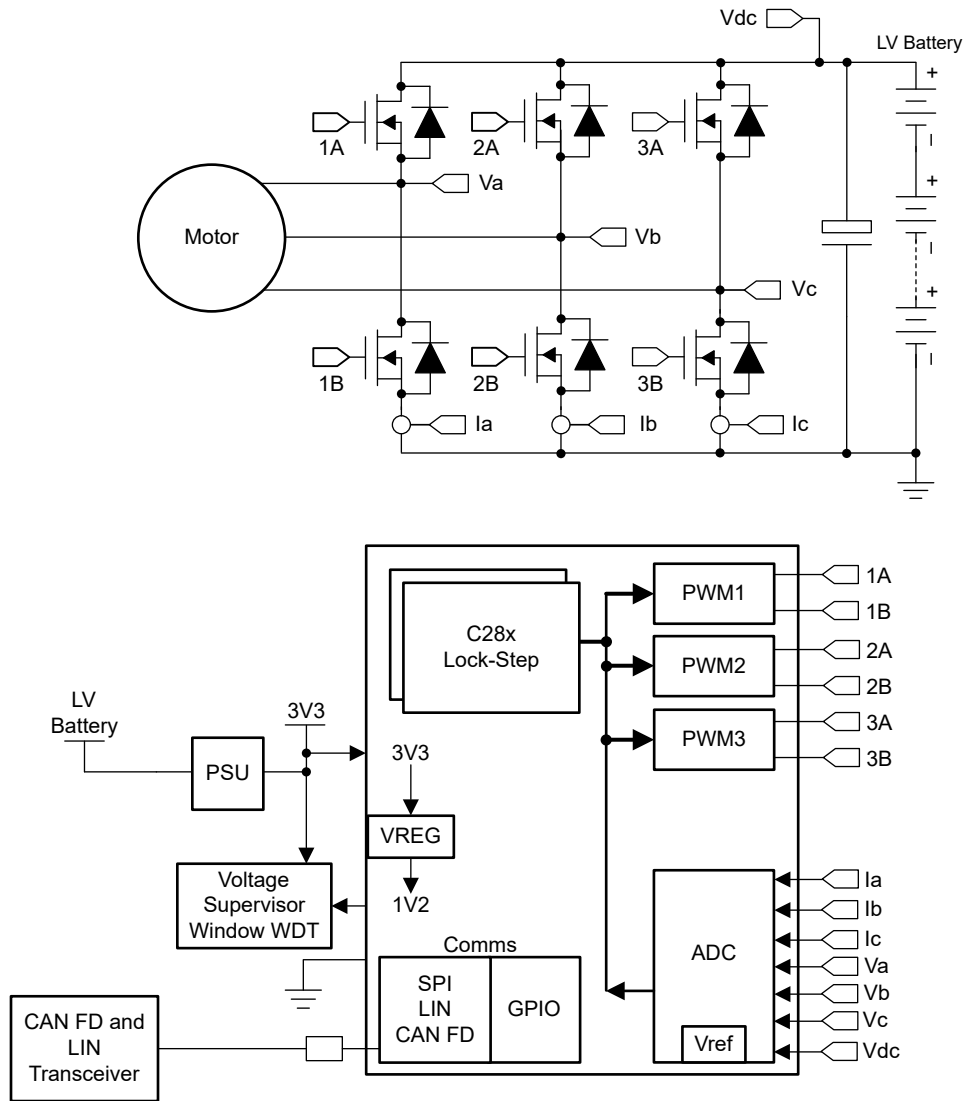


Figure 8-1. Automotive Pump

8.3.1.1.2 Automotive Pump Resources

Reference Designs and Associated Training Videos

[C2000™ MCUs - Electric vehicle \(EV\) training videos](#) (Video)

This collection of C2000™ MCU videos covers electric vehicle (EV)-specific training in both English and Chinese.

8.3.1.2 Automotive HVAC Compressor

In a vehicle, the purpose of a conventional HVAC compressor is to cool the cabin. In hybrid and electric vehicles (HEVs and EVs), the compressor system not only cools the cabin but also the battery which powers the vehicle.

In HEV/EVs, the sizing or the absence of a combustion engine requires the introduction of two additional components that play a key role in the HVAC system:

- A brushless DC (BLDC) motor is a type of DC motor that rotates the AC compressor, instead of the engine.

- A positive temperature coefficient (PTC) heater or alternatively, a heat pump, heats the coolant, rather than the engine.

Automotive HVAC compressor module designs require:

- Minimized number of isolated components.
- Reduced EMI to optimize system performance.
- Comprehensive diagnostics for fault identification.
- High efficiency and sensorless torque control even at low speeds.

8.3.1.2.1 System Block Diagram

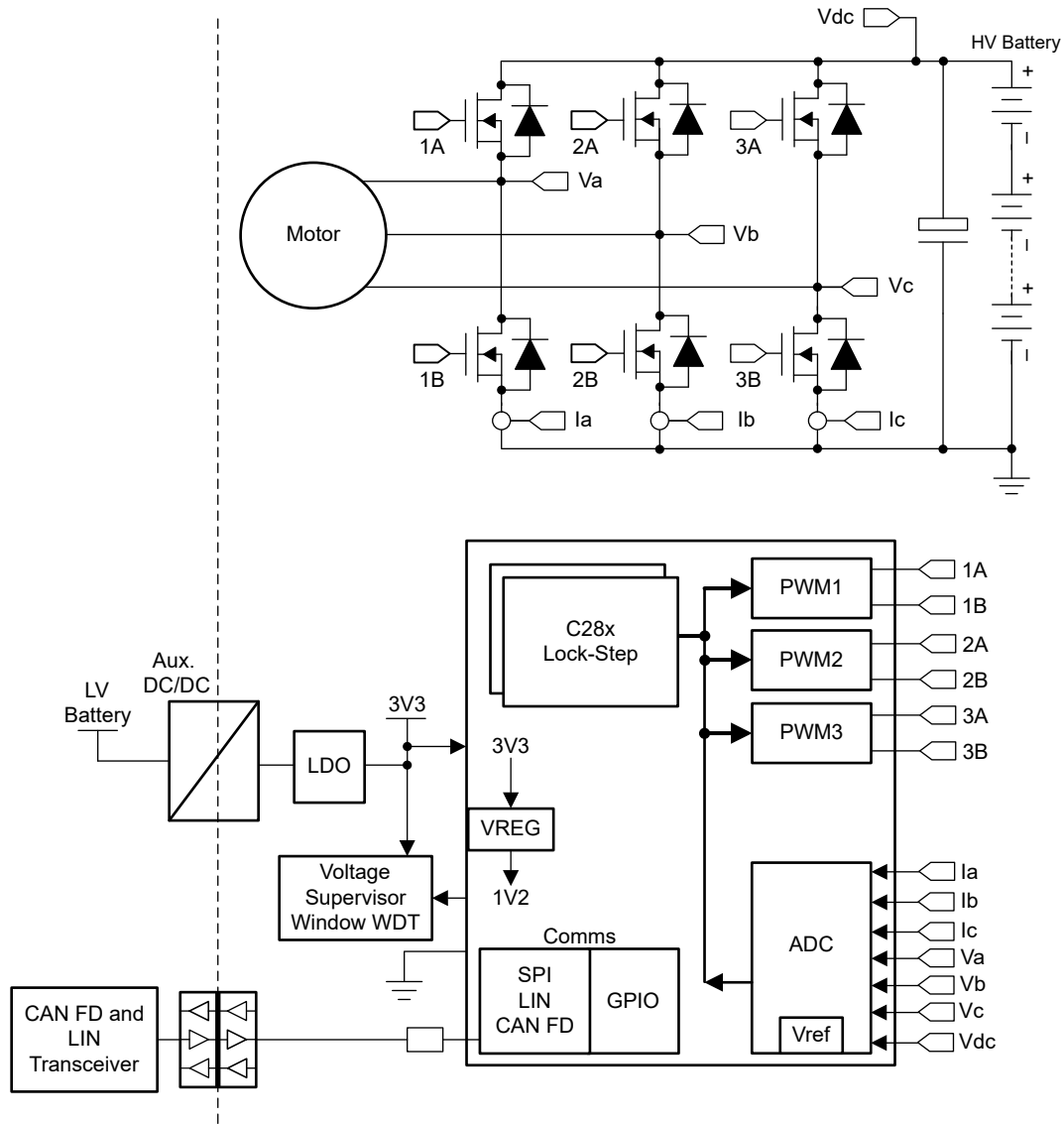


Figure 8-2. Automotive HVAC Compressor

8.3.1.2.2 HVAC Resources

Reference Designs and Associated Training Videos

[How to optimize your automotive HVAC design in the growing HEV/EV market](#)

In this article, we'll overview the design challenges associated with these electronic HVAC applications, and discuss how real-time control performance, scalability and cost can help address those challenges.

[C2000™ MCUs - Electric vehicle \(EV\) training videos](#) (Video)

This collection of C2000™ MCU videos covers electric vehicle (EV)-specific training in both English and Chinese.

[How to design heating and cooling systems for HEV/EVs](#)

In this white paper, we will describe the new heating and cooling control modules in 48-V, 400-V or 800-V HEVs and EVs. From there, you will learn about the unique subsystems in these modules with examples and system diagrams, and we will finish by reviewing functional solutions for these subsystems to help you start planning your implementation

[Reliable real-time control in automotive HVAC compressor applications for HEVs and EVs](#)

In this article, we focus on the design challenges of HVAC compressor subsystems within HEV and EV heating and cooling systems and discuss how real-time control can address those challenges.

8.3.1.3 On-Board Charger (OBC)

In the OBC and High-Voltage DC-DC charger (HV DCDC) markets, the modular-based design and the combo-box-based design are the two primary architectures adopted. The modular approach provides flexibility in manufacturing and after-service; and the combo-box approach seeks to integrate multiple functions into one enclosure for compactness. F28003x targets the modular-based control architecture and cost-sensitive solutions, which require limited controller performance (≤ 120 MIPS) with the element functional safety of ASIL B (D) for the controller.

An on-board charger consists of two power stages: PFC (AC-DC) power converter and a subsequent DC-DC power converter. Each power stage is controlled with a single MCU.

OBC-charging design requirements are as follows:

- High-performance and fast digital control loops enabling highly efficient power conversion and increased power density.
- Enabling precise control and fast shutdown in an overcurrent scenario by high bandwidth and fast response current sensing.
- Safely and efficiently controlling and protecting the power switch [insulated-gate bipolar transistor/silicon carbide (IGBT/SiC)].

8.3.1.3.1 System Block Diagram

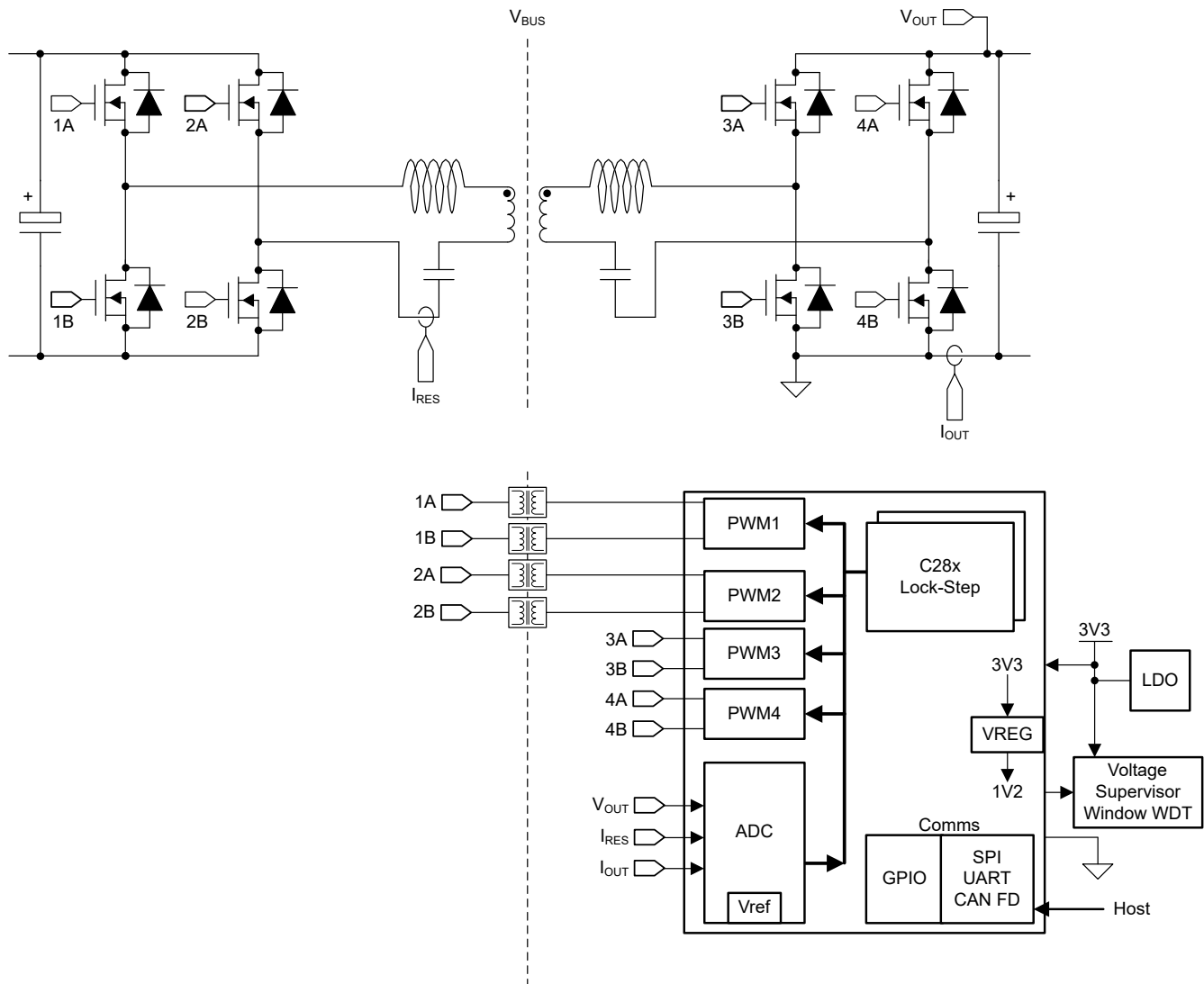


Figure 8-3. OBC - DC - DC

8.3.1.3.2 OBC Resources

Reference Designs and Associated Training Videos

[C2000 Digital Power Training videos](#)

This training series covers the basics of digital power control and how to implement it on C2000™ microcontrollers.

[C2000™ MCUs - Electric vehicle \(EV\) training videos \(Video\)](#)

This collection of C2000™ MCU videos covers electric vehicle (EV)-specific training in both English and Chinese.

[TIDUEG2C TIDM-02002 Bidirectional CLLC resonant dual active bridge \(DAB\) reference design for HEV/EV onboard charger](#)

The CLLC resonant DAB with bidirectional power flow capability and soft switching characteristics is an ideal candidate for Hybrid Electric Vehicle/Electric Vehicle (HEV/EV) on-board chargers and energy storage applications. This design illustrates control of this power topology using a C2000™ MCU in closed voltage and

closed current-loop mode. The hardware and software available with this design help accelerate your time to market.

[TIDUEG3A TIDM-1022 Valley switching boost power factor correction \(PFC\) reference design](#)

This reference design illustrates a digital control method to significantly improve Boost Power Factor Correction (PFC) converter performance such as the efficiency and Total Harmonic Distortion (THD) under light load condition where efficiency and THD standards are difficult to meet. This is achieved using the integrated digital control feature of the C2000™ microcontroller (MCU). The design supports phase-shedding, valley-switching, valley-skipping, and Zero Voltage Switching (ZVS) for different load and instantaneous input voltage conditions. The software available with this reference design accelerates time to market.

8.3.1.4 Servo Drive Control Module

Servo drives require high precision current and voltage sensing for accurate torque control and often supports interfaces for multiple encoder types along with communication interfaces. This C2000 device can be used either as single chip solution for standalone servo drive (shown in [Figure 8-4](#)) or can be used in decentralized systems (shown in [Figure 8-5](#)). In the later case, the F28P65x C2000 device functions as the controller which samples all the voltage and current inputs and generates the correct PWM signals for inverter. Each C2000 device serves as real-time controller for a target axis, running motor current control loop. Using the Fast Serial Interface (FSI) peripheral, up to 16 axes can be managed with one C2000 device. As an outer loop controller, the C2000 device executes main axis motor control, controls data exchange with all secondary axis over FSI and communicates with a host or PLC through EtherCAT.

8.3.1.4.1 System Block Diagram

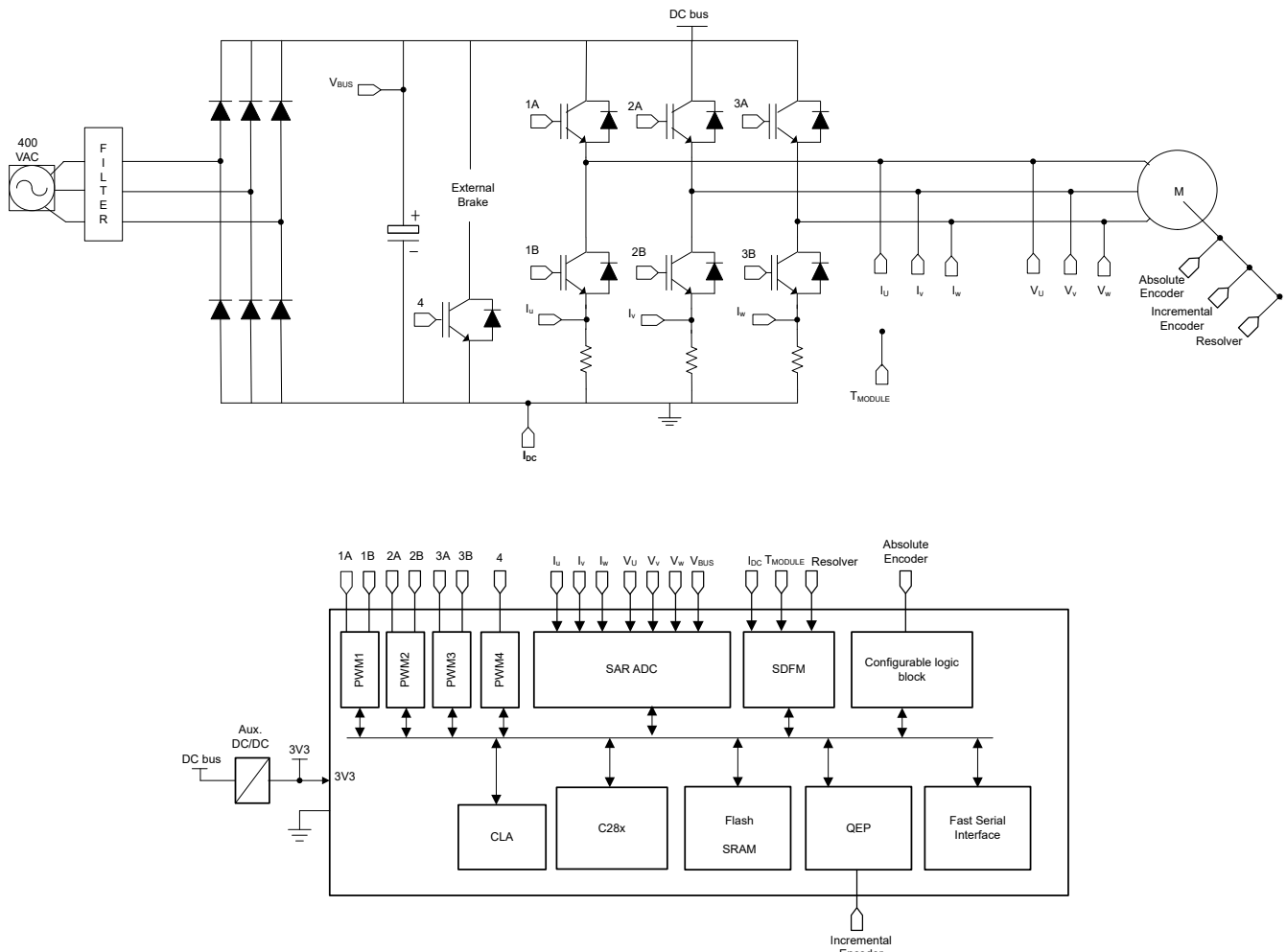


Figure 8-4. Servo Drive Control Module

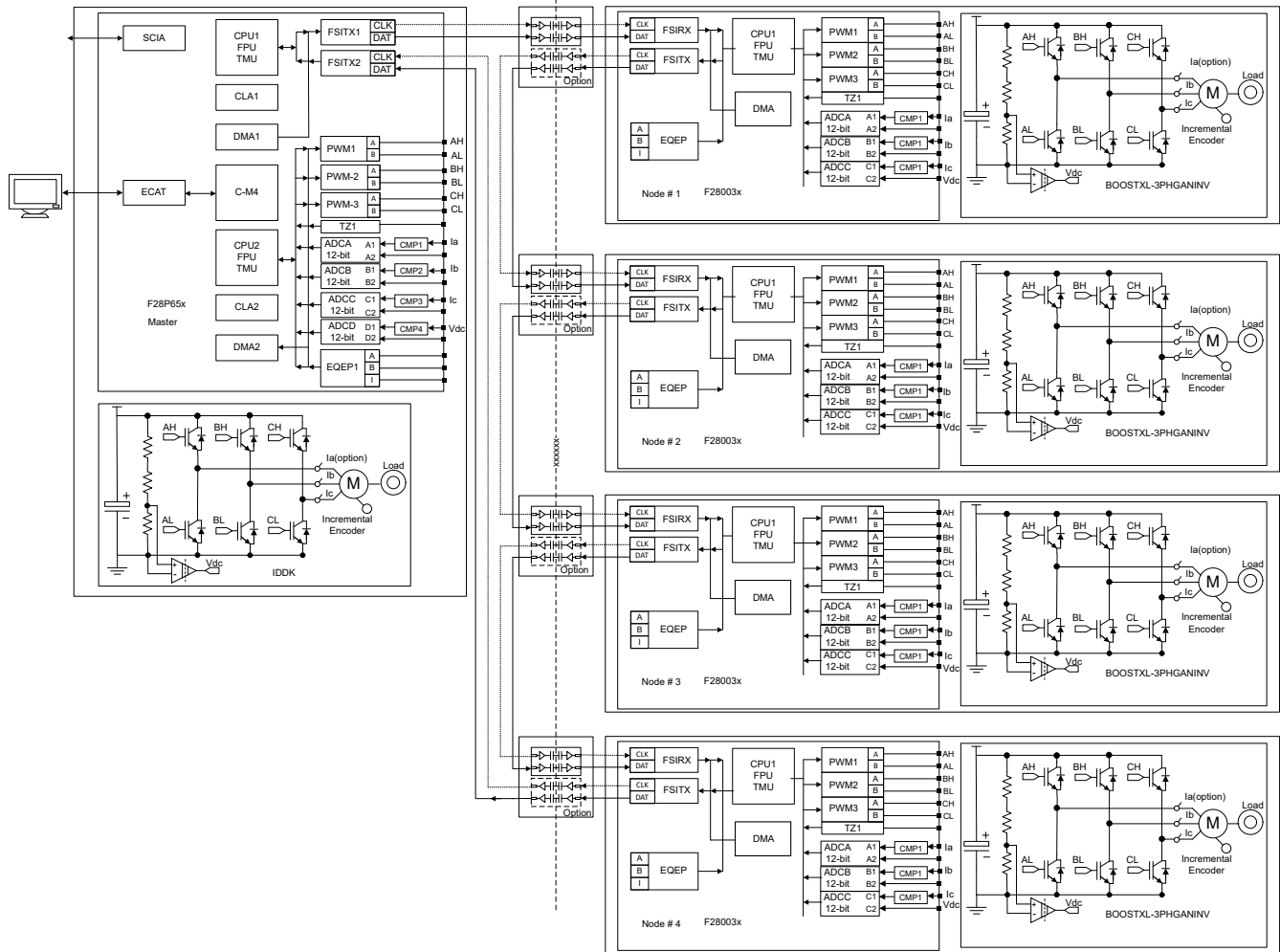


Figure 8-5. Distributed Multi-Axis Servo Drive

8.3.1.4.2 Servo Drive Control Module Resources

Reference Designs and Associated Training Videos

[48-V Three-Phase Inverter With Shunt-Based In-Line Motor Phase Current Sensing Evaluation Module](#)

The BOOSTXL-3PHGANINV evaluation module features a 48-V/10-A three-phase GaN inverter with precision in-line shunt-based phase current sensing for accurate control of precision drives such as servo drives.

[C2000 DesignDRIVE Development Kit for Industrial Motor Control](#)

The DesignDRIVE Development Kit (IDDK) hardware offers an integrated servo drive design with full power stage to drive a high voltage three-phase motor and eases the evaluation of a range of position feedback, current sensing and control topologies.

[C2000 DesignDRIVE position manager BoosterPack™ plug-in module](#)

The PositionManager BoosterPack is a flexible low voltage platform intended for evaluating interfaces to absolute encoders and analog sensors like resolvers and SinCos transducers. When combined with the DesignDRIVE Position Manager software solutions this low-cost evaluation module becomes a powerful tool for interfacing many popular position encoder types such as EnDat, BiSS and T-format with C2000 Real-Time Control devices. C2000 Position Manager technology integrates interfaces to the most popular digital and analog position sensors onto C2000 Real-Time Controller, thus eliminating the need for external FPGAs for these functions.

[C2000Ware MotorControl SDK](#)

MotorControl SDK for C2000™ microcontrollers (MCU) is a cohesive set of software infrastructure, tools, and documentation designed to minimize C2000 real-time controller based motor control system development time targeted for various three-phase motor control applications. The software includes firmware that runs on C2000 motor control evaluation modules (EVMs) and TI designs (TIDs) which are targeted for industrial drives, robotics, appliances, and automotive applications. MotorControl SDK provides all the needed resources at every stage of development and evaluation for high performance motor control applications.

[TIDM-02006 Distributed multi-axis servo drive over fast serial interface \(FSI\) reference design](#)

This reference design presents an example distributed or decentralized multi-axis servo drive over Fast Serial Interface (FSI) using C2000™ real-time controllers. Multi-axis servo drives are used in many applications such as factory automation and robots. The cost per axis, performance and ease of use are always high concerns for such systems. FSI is a cost-optimized and reliable high speed communication interface with low jitter that can daisy-chain multiple C2000 microcontrollers. In this design, each TMS320F280039 or TMS320F280025 real-time controller serves as a real-time controller for a distributed axis, running motor current control loop. A single TMS320F28388D runs position and speed control loops for all axes. The same F2838x also executes a centralized motor control axis plus EtherCAT communication, leveraging its multiple cores. The design uses our existing EVM kits, the software is released within C2000WARE MotorControl SDK.

[TIDM-02007 Dual-axis motor drive using fast current loop \(FCL\) and SFRA on a single MCU reference design](#)

This reference design presents a dual-axis motor drive using fast current loop (FCL) and software frequency response analyzer (SFRA) technologies on a single C2000 controller. The FCL utilizes dual core (CPU, CLA) parallel processing techniques to achieve a substantial improvement in control bandwidth and phase margin, to reduce the latency between feedback sampling and PWM update, to achieve higher control bandwidth and maximum modulation index, to improve DC bus utilization by the drive and to increase speed range of the motor. The integrated SFRA tool enables developers to quickly measure the frequency response of the application to tune speed and current controllers. Given the system-level integration and performance of C2000 series, MCUs have the ability to support dual-axis motor drive requirements simultaneously that delivers very robust position control with higher performance. The software is released within C2000Ware MotorControl SDK.

[TIDM-02010 Dual motor control with digital interleaved PFC for HVAC reference design](#)

The TIDM-02010 reference design is a 1.5-kW dual motor drive and PFC control reference design for variable frequency air conditioner outdoor unit controller in HVAC applications, which illustrates a method to implement sensorless 3-phase PMSM vector control for compressor and fan motor drive, and digital interleaved boost PFC for meeting new efficiency standards with a single C2000™ microcontroller. The hardware and software available with this reference design are tested and ready-to-use to help accelerate development time to market. The reference design includes hardware design files and software codes.

[TIDM-02012 High-voltage HEV/EV HVAC eCompressor motor control reference design](#)

The TIDM-02012 is a high-voltage, 5-kW reference design built for HEV/EV compressor (eCompressor) applications controlled by a mid-performance C2000™ TMS320F28003x real-time MCU. It is designed to evaluate with both 400-V and 800-V DC-bus, covering the market-trending of higher battery voltage. A controlCARD-based design enables users to evaluate multiple MCU and gate driver options, and is scalable to support other devices within the C2000™ portfolio including future roadmap devices to meet growing cybersecurity, functional safety, and other automotive market needs.

8.3.1.5 Solar Micro Inverter

A Solar Micro Inverter consists of a DC-AC inverter power stage and one or more Maximum Power Point Tracking (MPPT) DC-DC power stages. Typical switching frequency for the inverter (DC-AC) is between 20kHz-50kHz and for DC-DC side can be in the range 100kHz-200kHz. A variety of power stage topologies can be used to achieve this and the diagram only depicts a typical power stage and the control & communication requirements. A C2000 microcontroller has on-chip EPWM, ADC and analog comparator modules to implement complete digital control of such micro inverter system.

8.3.1.5.1 System Block Diagram

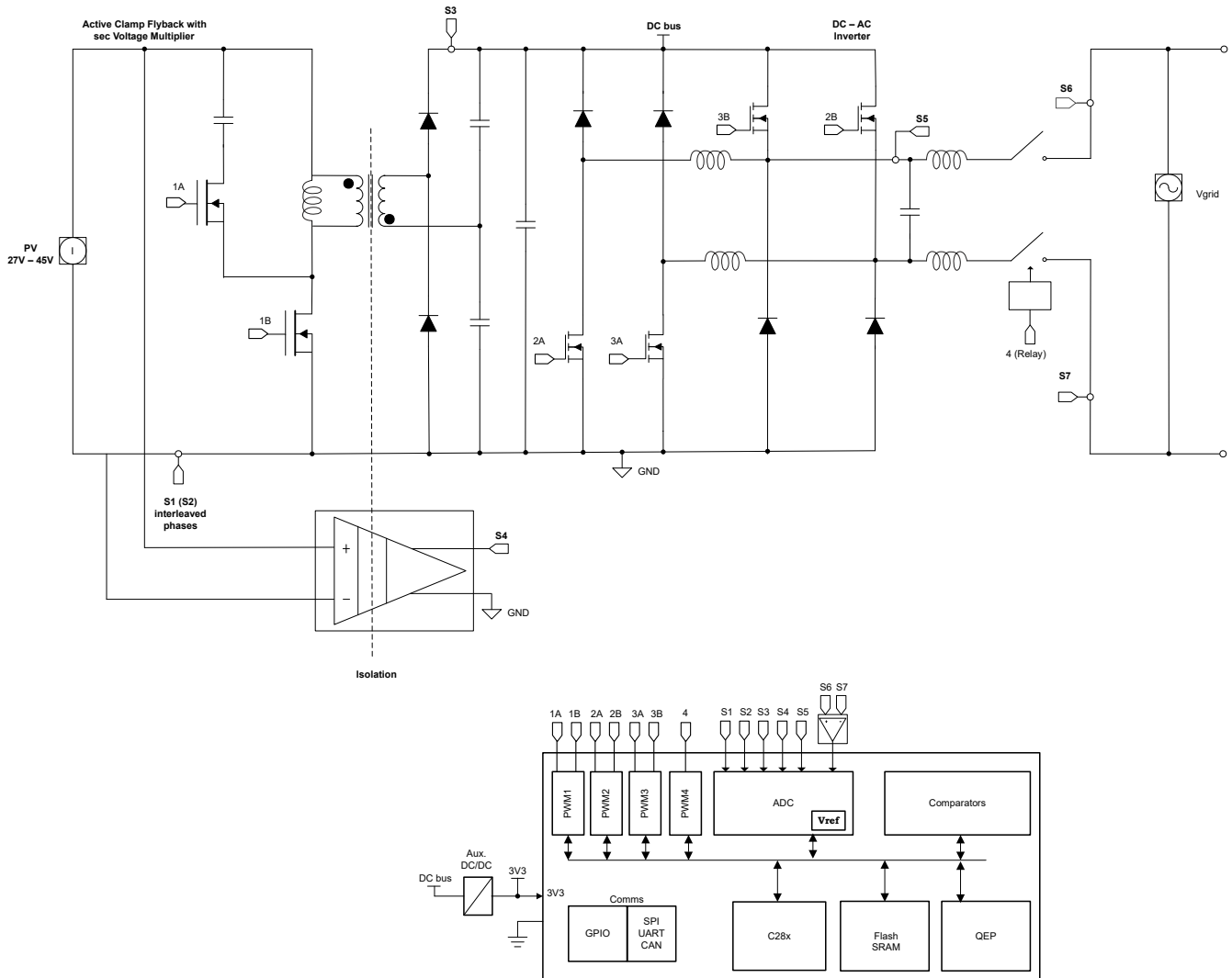


Figure 8-6. Solar Micro Inverter

8.3.1.5.2 Solar Micro Inverter Resources

Reference Designs and Associated Training Videos

[TIDM-SOLARUINV Grid-tied Solar Micro Inverter with MPPT](#)

This C2000 Solar Micro Inverter EVM hardware consists of two stages. These are: (1) an active clamp fly-back DC/DC converter with secondary voltage multiplier and, (2) a DC-AC inverter. A block diagram of this system is shown in Figure 1b. The DC-DC converter draws dc current from the PV panel such that the panel operates at its maximum power transfer point. This requires maintaining the panel output, that is, the DC-DC converter input at a level determined by the MPPT algorithm. The MPPT algorithm determines the panel output current (reference current) for maximum power transfer. Then a current control loop for the fly-back converter ensures that the converter input current tracks the MPPT reference current. The fly-back converter also provides high frequency isolation for the DC-DC stage. The output of the fly-back stage is a high voltage DC bus which drives the DC-AC inverter. The inverter stage maintains the DC bus at a desired set point and injects controlled sine wave current into the grid. The inverter also implements grid synchronization in order to maintain its current waveform locked to phase and frequency of the grid voltage. A C2000 piccolo microcontroller with its on-chip

PWM, ADC and analog comparator modules is able to implement complete digital control of such micro inverter system.

[C2000™ digital power training series](#) (Video)

This training series covers the basics of digital power control and how to implement it on C2000 microcontrollers.

[Calculating Useful Lifetimes of Embedded Processors](#)

This application report provides a methodology for calculating the useful lifetime of TI embedded processors (EP) under power when used in electronic systems. It is aimed at general engineers who wish to determine if the reliability of the TI EP meets the end system reliability requirement. Electromigration is the primary failure mechanism being modeled

[Digitally Controlled Solar Micro Inverter Design using C2000™ Piccolo Microcontroller](#)

This document presents the implementation details of a digitally-controlled solar micro inverter using the C2000 microcontroller. A 250-W isolated micro inverter design presents all the necessary PV inverter functions using the Piccolo-B (F28035) control card. This document describes the power stages on the micro inverter board, as well as an incremental build level system that builds the software by verifying open loop operation and closed loop operation. This guide describes control structures and algorithms for controlling power flow, maximizing power from the PV panel (MPPT), and locking to the grid using phase locked loop (PLL), along with hardware details of Texas Instruments Solar Micro Inverter Kit (TMDSOLARUINVKIT)

[Software Phase Locked Loop Design Using C2000™ Microcontrollers for Single Phase Grid Connected Inverter Application Report](#)

Grid connected applications require an accurate estimate of the grid angle to feed power synchronously to the grid. This is achieved using a software phase locked loop (PLL). This application report discusses different challenges in the design of software phase locked loops and presents a methodology to design phase locked loops using C2000 controllers for single phase grid connection applications.

[C2000WARE-DIGITALPOWER-SDK](#)

DigitalPower SDK for C2000™ microcontrollers (MCU) is a cohesive set of software infrastructure, tools, and documentation designed to minimize C2000 MCU based digital power system development time targeted for various AC-DC, DC-DC and DC-AC power supply applications. The software includes firmware that runs on C2000 digital power evaluation modules (EVMs) and TI designs (TIDs) which are targeted for solar, telecom, server, electric vehicle chargers and industrial power delivery applications. DigitalPower SDK provides all the needed resources at every stage of development and evaluation in a digital power application

8.3.1.6 Merchant Telecom Rectifiers

Merchant telecom rectifier consists of a power factor correction (PFC) stage and a DC-DC converter stage. The Totem pole PFC is widely used as the PFC stage. For the DC-DC stage, LLC and phase-shifted full bridge (PSFB) are the two most popular topologies. Single-chip and two-chip architecture can be used in merchant telecom rectifier, as shown in [Figure 8-7](#) and [Figure 8-8](#).

The PFC stage draws sine-wave current from the AC mains in phase with the AC voltage, and maintains a steady DC bus voltage (VDC, typically +400 V) across its output. This output voltage is applied to the input of DC-DC stage, which converts it to an isolated low-output voltage Vout (usually 48 V).

8.3.1.6.1 System Block Diagram

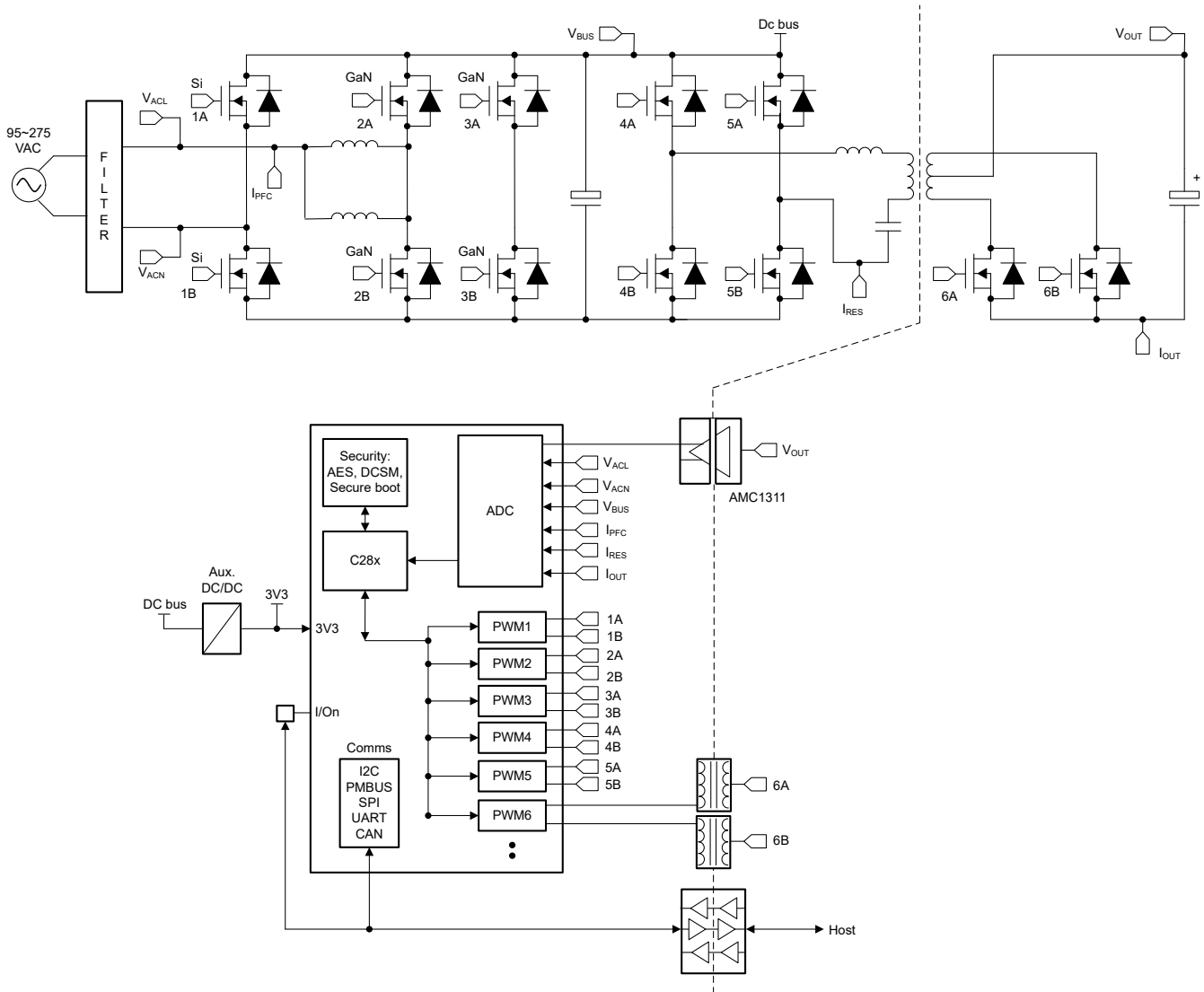


Figure 8-7. Merchant Telecom Rectifier Single-chip Architecture

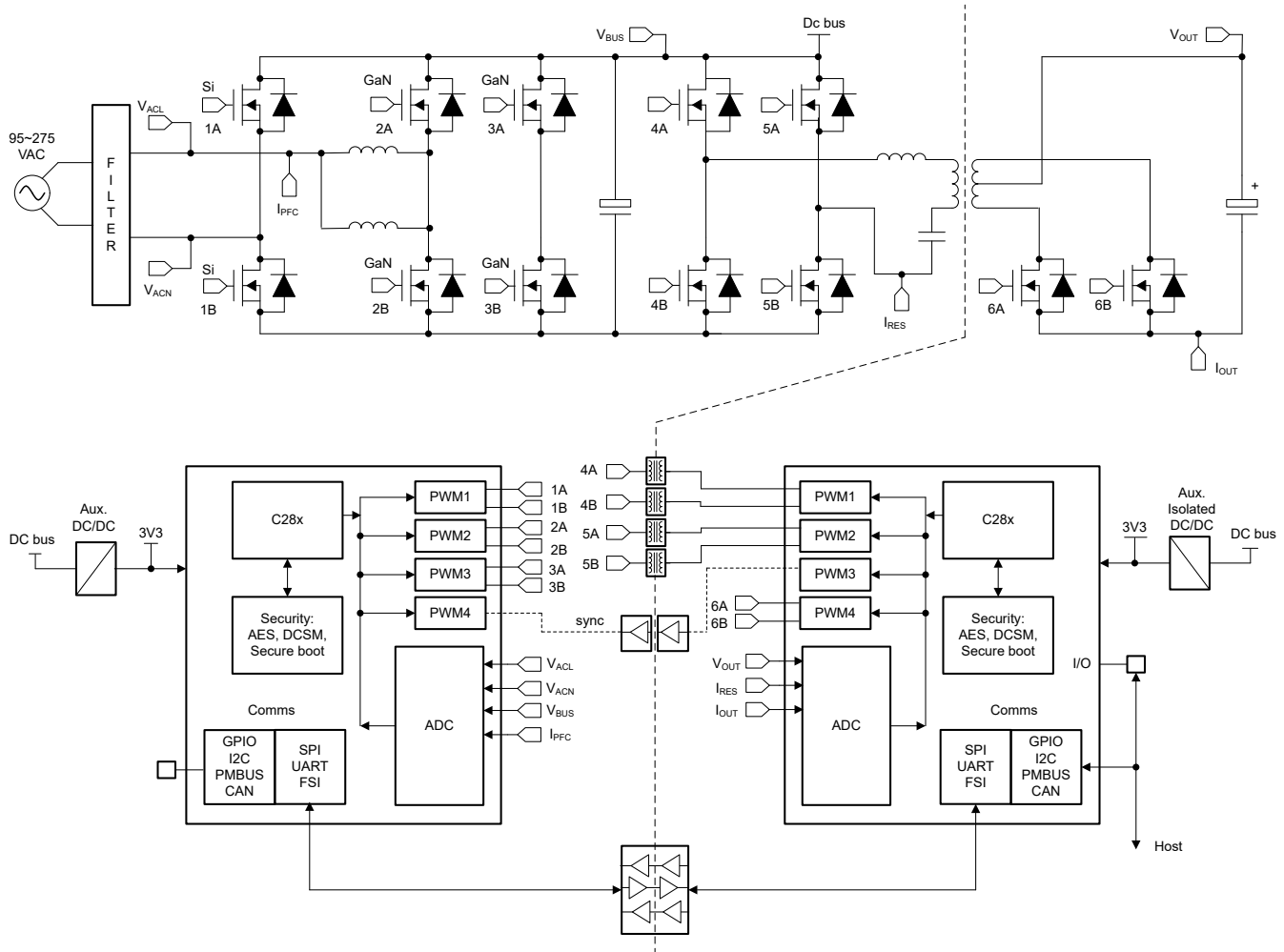


Figure 8-8. Merchant Telecom Rectifier Dual-chip Architecture

8.3.1.6.2 Merchant Telecom Rectifiers Resources

Reference Designs and Associated Training Videos

PMP41006 1-kW reference design with CCM totem pole PFC and current-mode LLC realized by C2000™ and GaN

This reference design demonstrates a hybrid hysteresis control (HHC) method, a kind of current-mode control method on half-bridge LLC stage with a C2000™ F28004x microcontroller. The hardware is based on TIDA-010062, which is 1-kW, 80-Plus titanium, GaN CCM totem pole bridgeless PFC and half-bridge LLC reference design. A separate sensing card is added for hybrid hysteresis control, which recreates the voltage on the resonant capacitor. This HHC LLC stage shows better transient response and ease-of-control loop design compared with the single-loop voltage-mode control method (VMC).

PMP23126 3-kW phase-shifted full bridge with active clamp reference design with > 270-W/in³ power density

This reference design is a GaN-based 3-kW phase-shifted full bridge (PSFB) targeting maximum power density. The design has an active clamp to minimize voltage stress on the secondary synchronous rectifier MOSFETs enabling use of lower voltage-rating MOSFETs with better figure-of-merit (FoM). PMP23126 uses our 30mΩ GaN on the primary side and silicon MOSFETs on the secondary side. The LMG3522 top-side cooled GaN with integrated driver and protection enables higher efficiency by maintaining ZVS over a wider range of operation compared to Si MOSFET. The PSFB operates at 100 kHz and achieves a peak efficiency of 97.74%.

PMP23069 [3.6-kW single-phase totem-pole bridgeless PFC reference design with a > 180-W/in³ power density](#)

This reference design is a GaN-based 3.6-kW single-phase continuous conduction mode (CCM) totem-pole power factor correction (PFC) converter targeting maximum power density. The power stage is followed by a small boost converter, which helps to reduce the size of the bulk capacitor. The LMG3522 top-side cooled GaN with integrated driver and protection enables higher efficiency and reduces power supply size and complexity. The F28003x, F28004x, or F28002x C2000™ controller is used for all the advanced controls that includes fast relay control; baby boost operation during AC dropout event; reverse-current-flow protection; and communication between the PFC and the housekeeping controller. The PFC operates at a switching frequency of 65 kHz and achieves peak efficiency of 98.7%.

1-kW reference design with CCM totem pole PFC and current-mode LLC realized by C2000™ and GaN (Video)

With the changing transient response requirements in the world of digital power, meeting stringent specs in applications like server power supply and other industrial ACDC power supplies has become challenging. This C2000 real-time MCU based digital hybrid hysteretic controlled (HHC) LLC converter design demonstrates how current mode control achieves better transient response compared to a traditional voltage mode control with least CPU resources yet achieving the needed performance.

TIDA-010203 [High efficiency PFC stage using GaN and C2000™ Real-time control MCUs](#) (Video)

GaN power FETs and C2000™ MCUs enable a totem-pole Power Factor Correction (PFC) topology, eliminating bridge rectifier power losses.

TIDA-010062 [1-kW, 80 Plus titanium, GaN CCM totem pole bridgeless PFC and half-bridge LLC reference design](#)

This reference design is a digitally controlled, compact 1-kW AC/DC power supply design for server power supply unit (PSU) and telecom rectifier applications. The highly efficient design supports two main power stages, including a front-end continuous conduction mode (CCM) totem-pole bridgeless power factor correction (PFC) stage. The PFC stage features an LMG341x GaN FET with integrated driver to provide enhanced efficiency across a wide load range and meet 80-plus titanium requirements. The design also supports a half-bridge LLC isolated DC/DC stage to achieve a +12-V DC output at 1-kW. Two control cards use C2000™ Entry-Performance MCUs to control both power stages.

TIDM-1001 [Two Phase Interleaved LLC Resonant Converter Reference Design Using C2000™ MCUs](#)

Resonant converters are popular DC-DC converters frequently used in server, telecom, automotive, industrial, and other power supply applications. Their high performance (efficiency, power density, etc.), improving requirements of the various industry standards, and the ever-increasing power density goals have made these converters a good choice for medium- to high-power applications. This design implements a digitally controlled 500-W two-phase interleaved LLC resonant converter. The system is controlled by a single C2000™ microcontroller (MCU), TMS320F280025C, which also generates PWM waveforms for all power electronic switching devices under all operating modes. This design implements a novel current-sharing technique to accurately achieve current-balancing between phases.

TIDM-1007 [Interleaved CCM Totem Pole PFC Reference Design](#) (Video)

This video covers the hardware aspects, the control aspects, and the software design that are required to control a totem-pole PFC using a C2000 microcontroller. The test results achieved on this reference design are also presented as part of this presentation.

Variable-frequency, ZVS, 5-kW, GaN-based, two-phase totem-pole PFC reference design

This reference design is a high-density and high-efficiency 5-kW totem-pole power factor correction (PFC) design. The design uses a two-phase totem-pole PFC operating with variable frequency and zero voltage switching (ZVS). The control uses a new topology and improved triangular current mode (iTCM) to achieve both small size and high efficiency. The design uses a high performance processing core inside a TMS320F280049C microcontroller to maintain efficiency over a wide operating range. The PFC operates with variable frequency between 100 kHz and 800 kHz. A peak system efficiency of 99% was achieved with an open-frame power density of 120 W/in³.

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Getting Started and Next Steps

The *Getting Started With C2000™ Real-Time Control Microcontrollers (MCUs) Getting Started Guide* covers all aspects of [development with C2000 devices](#) from hardware to support resources. In addition to key reference documents, each section provides relevant links and resources to further expand on the information covered.

For a quick overview of the device, features, comparisons to other devices, and package details, see [New Product Update: C2000™ real-time MCU family: F28003x overview](#).

9.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all TMS320 MCU devices and support tools. Each TMS320™ MCU commercial family member has one of three prefixes: TMX, TMP, or TMS (for example, **TMS320F280039C**). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (with TMX for devices and TMDX for tools) through fully qualified production devices and tools (with TMS for devices and TMDS for tools).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

TMP Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

TMS Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

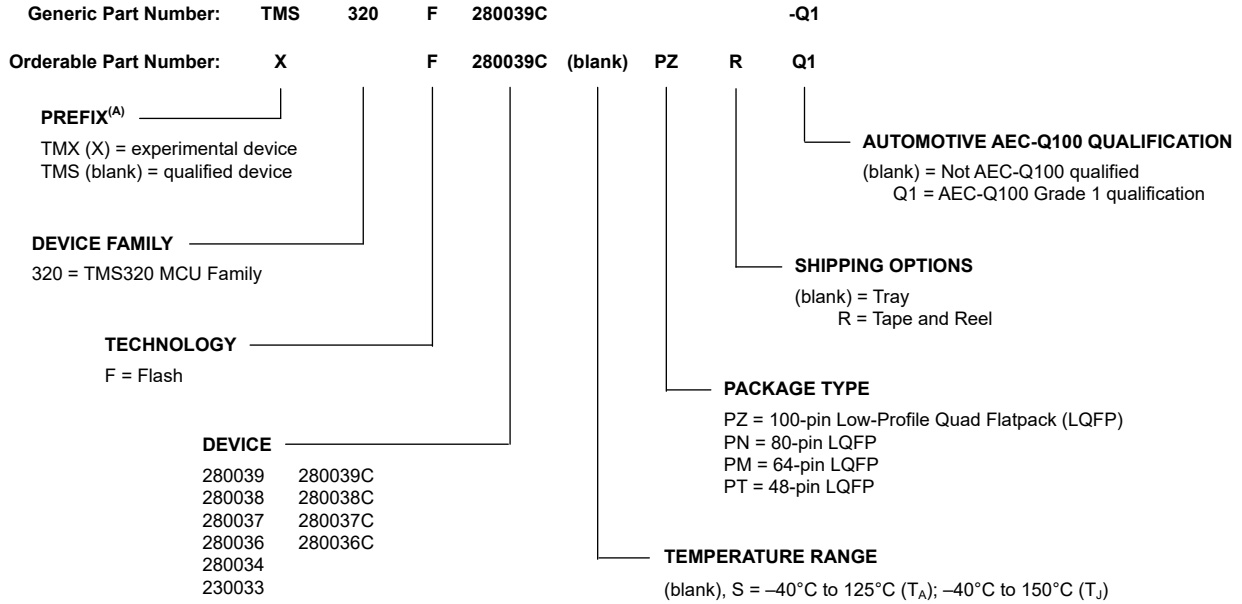
"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PN) and temperature range (for example, S).

For device part numbers and further ordering information, see the TI website (www.ti.com) or contact your TI sales representative.

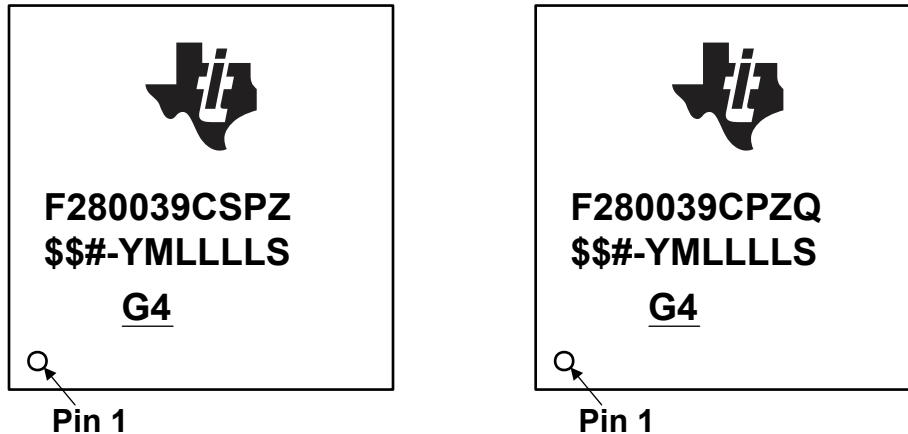


A. Prefix X is used in orderable part numbers.

Figure 9-1. Device Nomenclature

9.3 Markings

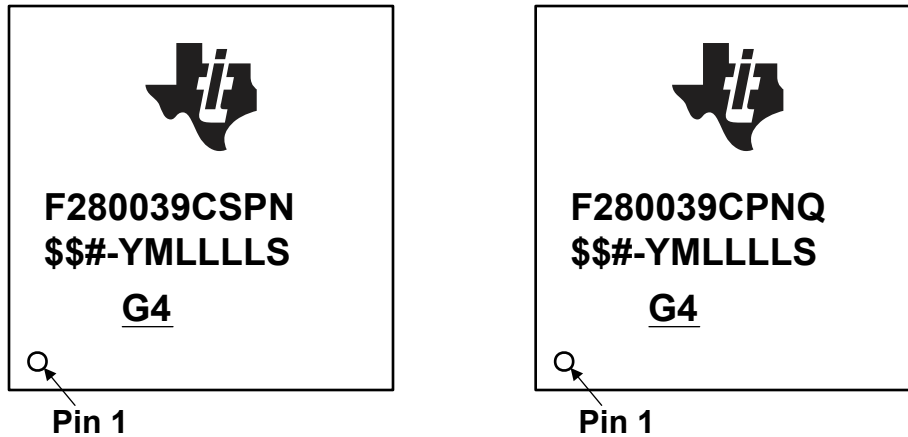
Figure 9-2, Figure 9-3, Figure 9-4, and Figure 9-5 show the package symbolization. Table 9-1 lists the silicon revision codes.



\$\$ = Wafer Fab Code (one or two characters)
= Silicon Revision Code
YM = 2-digit Year/Month Code
LLLL = Assembly Lot Code
S = Assembly Site Code per QSS 005-120

G4 = ECAT

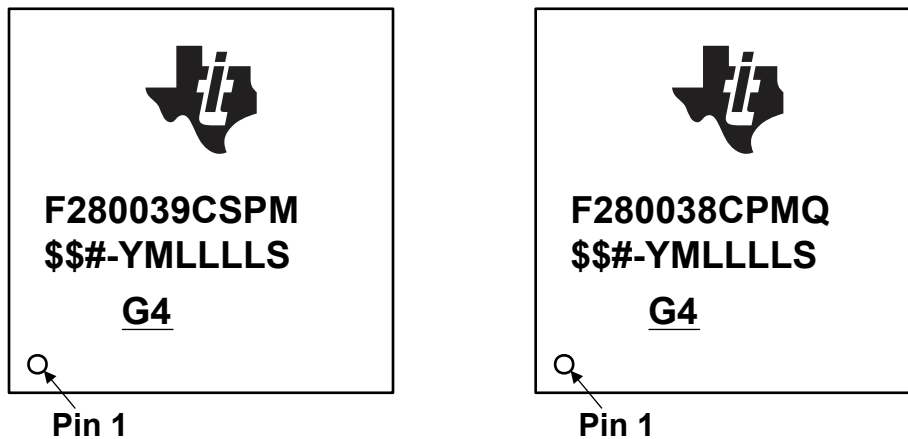
Figure 9-2. Package Symbolization for PZ Package



\$\$ = Wafer Fab Code (one or two characters)
= Silicon Revision Code
YM = 2-digit Year/Month Code
LLLL = Assembly Lot Code
S = Assembly Site Code per QSS 005-120

G4 = ECAT

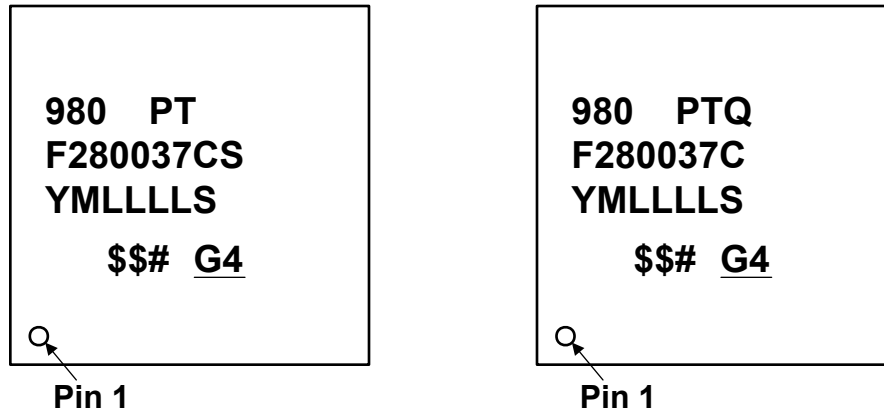
Figure 9-3. Package Symbolization for PN Package



\$\$ = Wafer Fab Code (one or two characters)
= Silicon Revision Code
YM = 2-digit Year/Month Code
LLLL = Assembly Lot Code
S = Assembly Site Code per QSS 005-120

G4 = ECAT

Figure 9-4. Package Symbolization for PM Package



980 = TI EIA Code
YM = 2-digit Year/Month Code
LLLL = Assembly Lot Code
S = Assembly Site Code per QSS 005-120
\$\$ = Wafer Fab Code (one or two characters)
= Silicon Revision Code

G4 = ECAT

Figure 9-5. Package Symbolization for PT Package

Table 9-1. Revision Identification

| SILICON REVISION CODE | SILICON REVISION | REVID ⁽¹⁾ ADDRESS: 0x5D00C | COMMENTS |
|-----------------------|------------------|--|--|
| Blank | 0 | 0x0000 0000 | This silicon revision is available as TMX and TMS. |

(1) Silicon Revision ID

9.4 Tools and Software

TI offers an extensive line of development tools. Some of the tools and software to evaluate the performance of the device, generate code, and develop solutions follow. To view all available tools and software for C2000™ real-time control MCUs, visit the [C2000 real-time control MCUs – Design & development](#) page.

Development Tools

[TMDSCNCD280039C Control Card](#)

The F280039C controlCARD is an HSEC180 controlCARD based evaluation and development tool for the C2000™ F28003x series of microcontroller products. controlCARDS are ideal to use for initial evaluation and system prototyping. controlCARDS are complete board-level modules that utilize one of two standard form factors (100-pin DIMM or 180-pin HSEC) to provide a low-profile single-board controller solution. For first evaluation controlCARDS are typically purchased bundled with a baseboard or bundled in an application kit.

[HSEC180 controlCARD Baseboard Docking Station](#)

TMDSHSECDOCK is a baseboard that provides header pin access to key signals on compatible HSEC180-based controlCARDS. A breadboard area is available for rapid prototyping. Board power can be provided by the provided USB cable or a 5-V barrel supply.

[XDS110 JTAG Debug Probe](#)

The Texas Instruments XDS110 is a new class of debug probe (emulator) for TI embedded processors. The XDS110 replaces the XDS100 family while supporting a wider variety of standards (IEEE1149.1, IEEE1149.7, SWD) in a single pod. Also, all XDS debug probes support Core and System Trace in all Arm® and DSP processors that feature an Embedded Trace Buffer (ETB). For Core Trace over pins the [XDS560v2 PRO TRACE Receiver & Debug Probe](#) is required.

[XDS200 USB Debug Probe](#)

The XDS200 is a debug probe (emulator) used for debugging TI embedded devices. The XDS200 features a balance of low cost with good performance as compared to the low cost XDS110 and the high performance XDS560v2. It supports a wide variety of standards (IEEE1149.1, IEEE1149.7, SWD) in a single pod. All XDS debug probes support Core and System Trace in all Arm® and DSP processors that feature an Embedded Trace Buffer (ETB). For Core Trace over pins the [XDS560v2 PRO TRACE Receiver & Debug Probe](#) is required.

[XDS560v2 System Trace USB Debug Probe](#)

The XDS560v2 is the highest performance of the XDS family of debug probes and supports both the traditional JTAG standard (IEEE1149.1) and cJTAG (IEEE1149.7). Note that it does not support serial wire debug (SWD).

Software Tools

[C2000™ Software Guide](#)

C2000™ real-time controllers are a portfolio of high-performance microcontrollers that are purpose-built to control power electronics and provide advanced digital signal processing for industrial and automotive applications. Software components to program various modules in C2000 MCUs are released as part of C2000 software releases. This guide provides an overview of various software components and available functionality.

[C2000Ware for C2000 MCUs](#)

C2000Ware for C2000™ MCUs is a cohesive set of software and documentation created to minimize development time. It includes device-specific drivers, libraries, and peripheral examples.

[Digital Power SDK](#)

Digital Power SDK is a cohesive set of software infrastructure, tools, and documentation designed to minimize C2000 MCU-based digital power system development time targeted for various AC-DC, DC-DC and DC-AC power supply applications. The software includes firmware that runs on C2000 digital power evaluation modules (EVMs) and reference designs, which are targeted for solar, telecom, server, electric vehicle chargers and industrial power delivery applications. Digital Power SDK provides all the needed resources at every stage of development and evaluation in a digital power applications.

[Motor Control SDK](#)

Motor Control SDK is a cohesive set of software infrastructure, tools, and documentation designed to minimize C2000 MCU-based motor control system development time targeted for various three-phase motor control applications. The software includes firmware that runs on C2000 motor control evaluation modules (EVMs) and reference designs, which are targeted for industrial drive and other motor control, Motor Control SDK provides all the needed resources at every stage of development and evaluation for high-performance motor control applications.

[Code Composer Studio™ \(CCS\) Integrated Development Environment \(IDE\) for C2000 microcontrollers](#)

Code Composer Studio is an integrated development environment (IDE) that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking the user through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

[TI Resource Explorer](#)

To enhance your experience, be sure to check out the TI Resource Explorer to browse examples, libraries, and documentation for your applications.

[SysConfig System configuration tool](#)

SysConfig is a comprehensive collection of graphical utilities for configuring pins, peripherals, radios, subsystems, and other components. SysConfig helps you manage, expose and resolve conflicts visually so that you have more time to create differentiated applications. The tool's output includes C header and code files that can be used with software development kit (SDK) examples or used to configure custom software. The SysConfig tool automatically selects the pinmux settings that satisfy the entered requirements. The SysConfig tool is delivered integrated in CCS, as a standalone installer, or can be used via the [dev.ti.com](#) cloud tools portal. For more information about the SysConfig system configuration tool, visit the [System configuration tool](#) page.

[C2000 Third-party search tool](#)

TI has partnered with multiple companies to offer a wide range of solutions and services for TI C2000 devices. These companies can accelerate your path to production using C2000 devices. Download this search tool to quickly browse third-party details and find the right third-party to meet your needs.

[UniFlash Standalone Flash Tool](#)

UniFlash is a standalone tool used to program on-chip flash memory through a GUI, command line, or scripting interface.

[C2000 code generation tools - compiler](#)

The TI C2000 C/C++ Compiler and Assembly Language Tools support development of applications for TI C2000 Microcontroller platforms, including the Concerto (F28M3xx), Entry-Performance (280xx), Premium-Performance Floating-Point (283xx), and C2000 Fixed-Point (2823x/280x/281x) Microcontroller devices.

Models

Various models are available for download from the product Design & development pages. These models include I/O Buffer Information Specification (IBIS) Models and Boundary-Scan Description Language (BSDL) Models. To view all available models, visit the Design tools & simulation subsection of the Design & development section of each device product page.

Training

To help assist design engineers in taking full advantage of the C2000 microcontroller features and performance, TI has developed a variety of training resources. Utilizing the online training materials and downloadable hands-on workshops provides an easy means for gaining a complete working knowledge of the C2000 microcontroller family. These training resources have been designed to decrease the learning curve, while reducing development time, and accelerating product time to market. For more information on the various training resources, visit the [C2000™ real-time control MCUs – Support & training](#) site. Additionally, the [C2000 Academy](#) course provides new users with a way to ramp quickly with C2000 devices and their many features. This is a great entry point for users getting started with C2000, and is available at the [C2000 Academy](#) resource explorer page.

9.5 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the processor, related peripherals, and other technical collateral follows.

Errata

[TMS320F28003x Real-Time MCUs Silicon Errata](#) describes known advisories on silicon and provides workarounds.

Technical Reference Manual

[TMS320F28003x Real-Time Microcontrollers Technical Reference Manual](#) details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the F28003x real-time microcontrollers.

CPU User's Guides

[TMS320C28x CPU and Instruction Set Reference Guide](#) describes the central processing unit (CPU) and the assembly language instructions of the TMS320C28x fixed-point digital signal processors (DSPs). This Reference Guide also describes emulation features available on these DSPs.

[TMS320C28x Extended Instruction Sets Technical Reference Manual](#) describes the architecture, pipeline, and instruction set of the TMU, VCU-II, and FPU accelerators.

Peripheral Guides

[C2000 Real-Time Control Peripherals Reference Guide](#) describes the peripheral reference guides of the 28x DSPs.

Tools Guides

[TMS320C28x Assembly Language Tools v22.6.0.LTS User's Guide](#) describes the assembly language tools (assembler and other tools used to develop assembly language code), assembler directives, macros, common object file format, and symbolic debugging directives for the TMS320C28x device.

[TMS320C28x Optimizing C/C++ Compiler v22.6.0.LTS User's Guide](#) describes the TMS320C28x C/C++ compiler. This compiler accepts ANSI standard C/C++ source code and produces TMS320 DSP assembly language source code for the TMS320C28x device.

Application Reports

The [SMT & packaging application notes](#) website lists documentation on TI's surface mount technology (SMT) and application notes on a variety of packaging-related topics.

[Semiconductor Packing Methodology](#) describes the packing methodologies employed to prepare semiconductor devices for shipment to end users.

[Calculating Useful Lifetimes of Embedded Processors](#) provides a methodology for calculating the useful lifetime of TI embedded processors (EPs) under power when used in electronic systems. It is aimed at general engineers who wish to determine if the reliability of the TI EP meets the end system reliability requirement.

[An Introduction to IBIS \(I/O Buffer Information Specification\) Modeling](#) discusses various aspects of IBIS including its history, advantages, compatibility, model generation flow, data requirements in modeling the input/output structures, and future trends.

[Serial Flash Programming of C2000™ Microcontrollers](#) discusses using a flash kernel and ROM loaders for serial programming a device.

[Fast Integer Division – A Differentiated Offering From C2000™ Product Family](#) provides an overview of the different division and modulo (remainder) functions and its associated properties.

[The Essential Guide for Developing With C2000™ Real-Time Microcontrollers](#) provides a deeper look into the components that differentiate the C2000 Microcontroller Unit (MCU) as it pertains to Real-Time Control Systems.

9.6 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.7 Trademarks

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9.8 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.9 Glossary

[TI Glossary](#)

This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

Changes from November 30, 2022 to December 7, 2023

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| • Global: Information on the TMS320F280039-Q1, TMS320F280039, TMS320F280038-Q1, TMS320F280037-Q1, TMS320F280036C-Q1, TMS320F280036-Q1, TMS320F280034-Q1, and TMS320F280033 devices is now Production Data..... | 1 |
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| • <i>Features</i> section: Updated "Functional Safety-Compliant" feature and "Safety-related certification" feature.... | 1 |
| • <i>Package Information</i> table: Added table..... | 3 |
| • <i>Functional Block Diagram</i> figure: Updated "Buses Legend" by changing "CLU" to "CLA"..... | 6 |
| • <i>Device Comparison</i> table: Changed "Code security for on-chip flash and RAM" to "Security: JTAGLOCK, Zero-pin boot, Dual-zone security"..... | 8 |
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11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

To learn more about TI packaging, visit the [Packaging information](#) website.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| F280033SPM | ACTIVE | LQFP | PM | 64 | 160 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280033SPM | Samples |
| F280033SPN | ACTIVE | LQFP | PN | 80 | 119 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280033SPN | Samples |
| F280033SPT | ACTIVE | LQFP | PT | 48 | 250 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280033S PT | Samples |
| F280033SPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280033SPZ | Samples |
| F280034PTRQ1 | ACTIVE | LQFP | PT | 48 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280034 PTQ | Samples |
| F280034SPM | ACTIVE | LQFP | PM | 64 | 160 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280034SPM | Samples |
| F280034SPN | ACTIVE | LQFP | PN | 80 | 119 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280034SPN | Samples |
| F280034SPT | ACTIVE | LQFP | PT | 48 | 250 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280034S PT | Samples |
| F280034SPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280034SPZ | Samples |
| F280036CPMRQ1 | ACTIVE | LQFP | PM | 64 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280036CPMQ | Samples |
| F280036PMRQ1 | ACTIVE | LQFP | PM | 64 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280036PMQ | Samples |
| F280037CPTQ1 | ACTIVE | LQFP | PT | 48 | 250 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280037C PTQ | Samples |
| F280037CPTRQ1 | ACTIVE | LQFP | PT | 48 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280037C PTQ | Samples |
| F280037CPZRQ1 | ACTIVE | LQFP | PZ | 100 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280037CPZQ | Samples |
| F280037CSPM | ACTIVE | LQFP | PM | 64 | 160 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280037CSPM | Samples |
| F280037CSPN | ACTIVE | LQFP | PN | 80 | 119 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280037CSPN | Samples |
| F280037CSPT | ACTIVE | LQFP | PT | 48 | 250 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280037CS PT | Samples |
| F280037CSPTR | ACTIVE | LQFP | PT | 48 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280037CS PT | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| F280037CSPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280037CSPZ | Samples |
| F280037PTRQ1 | ACTIVE | LQFP | PT | 48 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280037 PTQ | Samples |
| F280037PZRQ1 | ACTIVE | LQFP | PZ | 100 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280037PZQ | Samples |
| F280037SPM | ACTIVE | LQFP | PM | 64 | 160 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280037SPM | Samples |
| F280037SPMR | ACTIVE | LQFP | PM | 64 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | | F280037SPM | Samples |
| F280037SPN | ACTIVE | LQFP | PN | 80 | 119 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280037SPN | Samples |
| F280037SPNR | ACTIVE | LQFP | PN | 80 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280037SPN | Samples |
| F280037SPT | ACTIVE | LQFP | PT | 48 | 250 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280037S PT | Samples |
| F280037SPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280037SPZ | Samples |
| F280038CPMQ1 | ACTIVE | LQFP | PM | 64 | 160 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280038CPMQ | Samples |
| F280038CPMRQ1 | ACTIVE | LQFP | PM | 64 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280038CPMQ | Samples |
| F280038PMRQ1 | ACTIVE | LQFP | PM | 64 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280038PMQ | Samples |
| F280039CPNQ1 | ACTIVE | LQFP | PN | 80 | 119 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280039CPNQ | Samples |
| F280039CPZQ1 | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280039CPZQ | Samples |
| F280039CPZRQ1 | ACTIVE | LQFP | PZ | 100 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280039CPZQ | Samples |
| F280039CSPM | ACTIVE | LQFP | PM | 64 | 160 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280039CSPM | Samples |
| F280039CSPMR | ACTIVE | LQFP | PM | 64 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280039CSPM | Samples |
| F280039CSPN | ACTIVE | LQFP | PN | 80 | 119 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280039CSPN | Samples |
| F280039CSPNR | ACTIVE | LQFP | PN | 80 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280039CSPN | Samples |
| F280039CSPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280039CSPZ | Samples |
| F280039CSPZR | ACTIVE | LQFP | PZ | 100 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280039CSPZ | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| F280039PZRQ1 | ACTIVE | LQFP | PZ | 100 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280039PZQ | Samples |
| F280039SPM | ACTIVE | LQFP | PM | 64 | 160 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280039SPM | Samples |
| F280039SPN | ACTIVE | LQFP | PN | 80 | 119 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280039SPN | Samples |
| F280039SPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | F280039SPZ | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TMS320F280034, TMS320F280034-Q1, TMS320F280037, TMS320F280037-Q1, TMS320F280037C, TMS320F280037C-Q1, TMS320F280039, TMS320F280039-Q1, TMS320F280039C, TMS320F280039C-Q1 :

- Catalog : [TMS320F280034](#), [TMS320F280037](#), [TMS320F280037C](#), [TMS320F280039](#), [TMS320F280039C](#)
- Automotive : [TMS320F280034-Q1](#), [TMS320F280037-Q1](#), [TMS320F280037C-Q1](#), [TMS320F280039-Q1](#), [TMS320F280039C-Q1](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| F280034PTRQ1 | LQFP | PT | 48 | 1000 | 330.0 | 16.4 | 9.6 | 9.6 | 1.9 | 12.0 | 16.0 | Q2 |
| F280036CPMRQ1 | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| F280036PMRQ1 | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| F280037CPTRQ1 | LQFP | PT | 48 | 1000 | 330.0 | 16.4 | 9.6 | 9.6 | 1.9 | 12.0 | 16.0 | Q2 |
| F280037CPZRQ1 | LQFP | PZ | 100 | 1000 | 330.0 | 32.4 | 16.9 | 16.9 | 2.0 | 24.0 | 32.0 | Q2 |
| F280037CSPTR | LQFP | PT | 48 | 1000 | 330.0 | 16.4 | 9.6 | 9.6 | 1.9 | 12.0 | 16.0 | Q2 |
| F280037PTRQ1 | LQFP | PT | 48 | 1000 | 330.0 | 16.4 | 9.6 | 9.6 | 1.9 | 12.0 | 16.0 | Q2 |
| F280037PZRQ1 | LQFP | PZ | 100 | 1000 | 330.0 | 32.4 | 16.9 | 16.9 | 2.0 | 24.0 | 32.0 | Q2 |
| F280037SPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| F280037SPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 16.0 | 16.0 | 2.0 | 24.0 | 24.0 | Q2 |
| F280038CPMRQ1 | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| F280038PMRQ1 | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| F280039CPZRQ1 | LQFP | PZ | 100 | 1000 | 330.0 | 32.4 | 16.9 | 16.9 | 2.0 | 24.0 | 32.0 | Q2 |
| F280039CSPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| F280039CSPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 16.0 | 16.0 | 2.0 | 24.0 | 24.0 | Q2 |
| F280039CSPZR | LQFP | PZ | 100 | 1000 | 330.0 | 32.4 | 16.9 | 16.9 | 2.0 | 24.0 | 32.0 | Q2 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| F280039PZRQ1 | LQFP | PZ | 100 | 1000 | 330.0 | 32.4 | 16.9 | 16.9 | 2.0 | 24.0 | 32.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| F280034PTRQ1 | LQFP | PT | 48 | 1000 | 336.6 | 336.6 | 31.8 |
| F280036CPMRQ1 | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |
| F280036PMRQ1 | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |
| F280037CPTRQ1 | LQFP | PT | 48 | 1000 | 336.6 | 336.6 | 31.8 |
| F280037CPZRQ1 | LQFP | PZ | 100 | 1000 | 367.0 | 367.0 | 55.0 |
| F280037CSPTR | LQFP | PT | 48 | 1000 | 336.6 | 336.6 | 31.8 |
| F280037PTRQ1 | LQFP | PT | 48 | 1000 | 336.6 | 336.6 | 31.8 |
| F280037PZRQ1 | LQFP | PZ | 100 | 1000 | 367.0 | 367.0 | 55.0 |
| F280037SPMR | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |
| F280037SPNR | LQFP | PN | 80 | 1000 | 367.0 | 367.0 | 55.0 |
| F280038CPMRQ1 | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |
| F280038PMRQ1 | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |
| F280039CPZRQ1 | LQFP | PZ | 100 | 1000 | 367.0 | 367.0 | 55.0 |
| F280039CSPMR | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |
| F280039CSPNR | LQFP | PN | 80 | 1000 | 367.0 | 367.0 | 55.0 |
| F280039CSPZR | LQFP | PZ | 100 | 1000 | 367.0 | 367.0 | 55.0 |
| F280039PZRQ1 | LQFP | PZ | 100 | 1000 | 367.0 | 367.0 | 55.0 |

TRAY

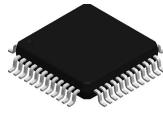

Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|--------------|--------------|--------------|------|-----|-------------------|----------------------|--------|--------|---------|---------|---------|---------|
| F280033SPM | PM | LQFP | 64 | 160 | 8 X 20 | 150 | 315 | 135.9 | 7620 | 15.2 | 13.1 | 13 |
| F280033SPN | PN | LQFP | 80 | 119 | 7 X 17 | 150 | 315 | 135.9 | 7620 | 17.9 | 14.3 | 13.95 |
| F280033SPT | PT | LQFP | 48 | 250 | 10 x 25 | 150 | 315 | 135.9 | 7620 | 12.2 | 11.1 | 11.25 |
| F280033SPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.4 |
| F280034SPM | PM | LQFP | 64 | 160 | 8 X 20 | 150 | 315 | 135.9 | 7620 | 15.2 | 13.1 | 13 |
| F280034SPN | PN | LQFP | 80 | 119 | 7 X 17 | 150 | 315 | 135.9 | 7620 | 17.9 | 14.3 | 13.95 |
| F280034SPT | PT | LQFP | 48 | 250 | 10 x 25 | 150 | 315 | 135.9 | 7620 | 12.2 | 11.1 | 11.25 |
| F280034SPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.4 |
| F280037CPTQ1 | PT | LQFP | 48 | 250 | 10 x 25 | 150 | 315 | 135.9 | 7620 | 12.2 | 11.1 | 11.25 |
| F280037CSPM | PM | LQFP | 64 | 160 | 8 X 20 | 150 | 315 | 135.9 | 7620 | 15.2 | 13.1 | 13 |
| F280037CSPN | PN | LQFP | 80 | 119 | 7 X 17 | 150 | 315 | 135.9 | 7620 | 17.9 | 14.3 | 13.95 |
| F280037CSPT | PT | LQFP | 48 | 250 | 10 x 25 | 150 | 315 | 135.9 | 7620 | 12.2 | 11.1 | 11.25 |
| F280037CSPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.4 |
| F280037SPM | PM | LQFP | 64 | 160 | 8 X 20 | 150 | 315 | 135.9 | 7620 | 15.2 | 13.1 | 13 |
| F280037SPN | PN | LQFP | 80 | 119 | 7 X 17 | 150 | 315 | 135.9 | 7620 | 17.9 | 14.3 | 13.95 |
| F280037SPT | PT | LQFP | 48 | 250 | 10 x 25 | 150 | 315 | 135.9 | 7620 | 12.2 | 11.1 | 11.25 |
| F280037SPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.4 |

| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|--------------|--------------|--------------|------|-----|-------------------|----------------------|--------|--------|---------|---------|---------|---------|
| F280038CPMQ1 | PM | LQFP | 64 | 160 | 8 X 20 | 150 | 315 | 135.9 | 7620 | 15.2 | 13.1 | 13 |
| F280039CPNQ1 | PN | LQFP | 80 | 119 | 7 X 17 | 150 | 315 | 135.9 | 7620 | 17.9 | 14.3 | 13.95 |
| F280039CPZQ1 | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.4 |
| F280039CSPM | PM | LQFP | 64 | 160 | 8 X 20 | 150 | 315 | 135.9 | 7620 | 15.2 | 13.1 | 13 |
| F280039CSPN | PN | LQFP | 80 | 119 | 7 X 17 | 150 | 315 | 135.9 | 7620 | 17.9 | 14.3 | 13.95 |
| F280039CSPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.4 |
| F280039SPM | PM | LQFP | 64 | 160 | 8 X 20 | 150 | 315 | 135.9 | 7620 | 15.2 | 13.1 | 13 |
| F280039SPN | PN | LQFP | 80 | 119 | 7 X 17 | 150 | 315 | 135.9 | 7620 | 17.9 | 14.3 | 13.95 |
| F280039SPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.4 |

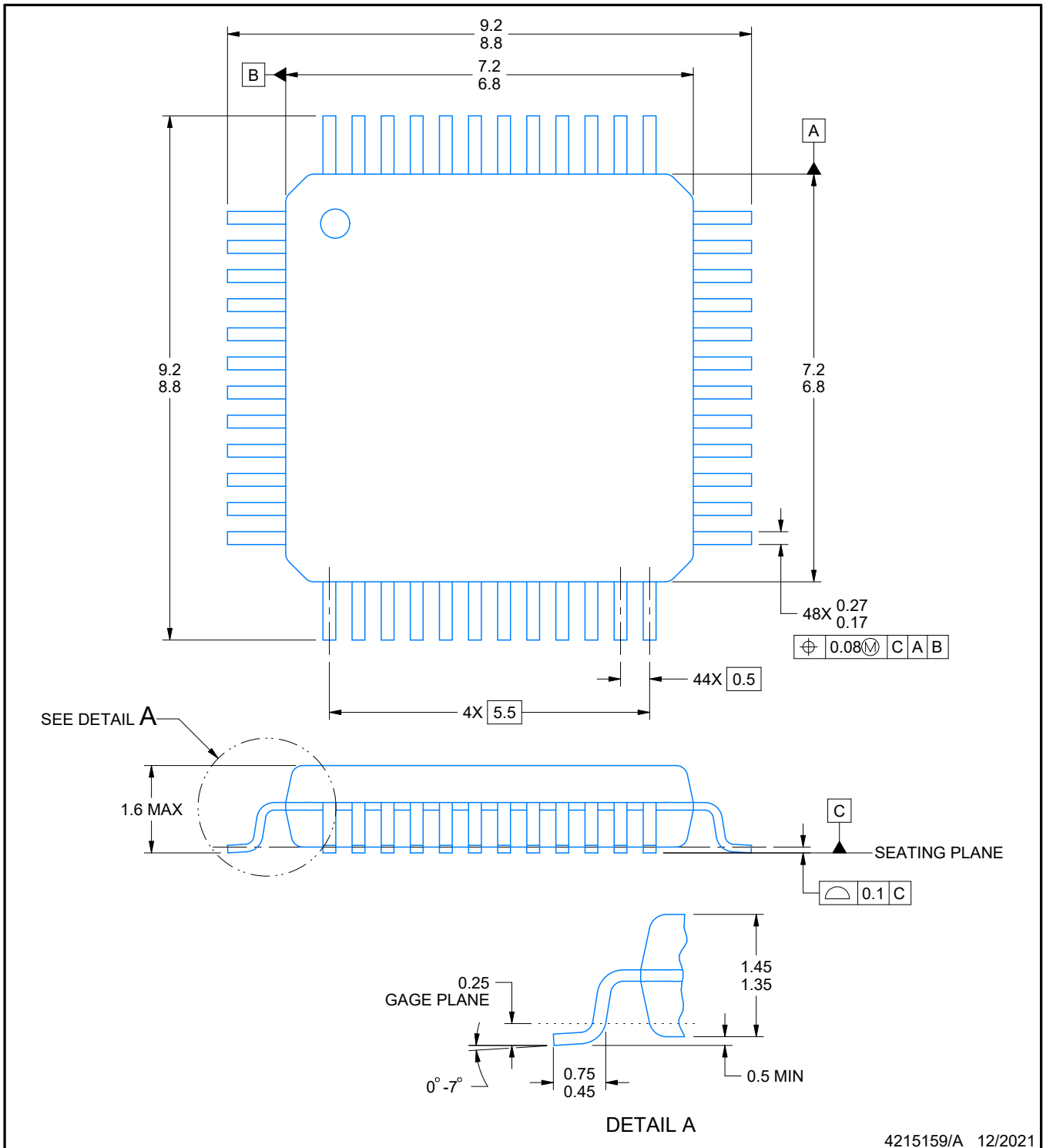
PT0048A



PACKAGE OUTLINE

LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK



NOTES:

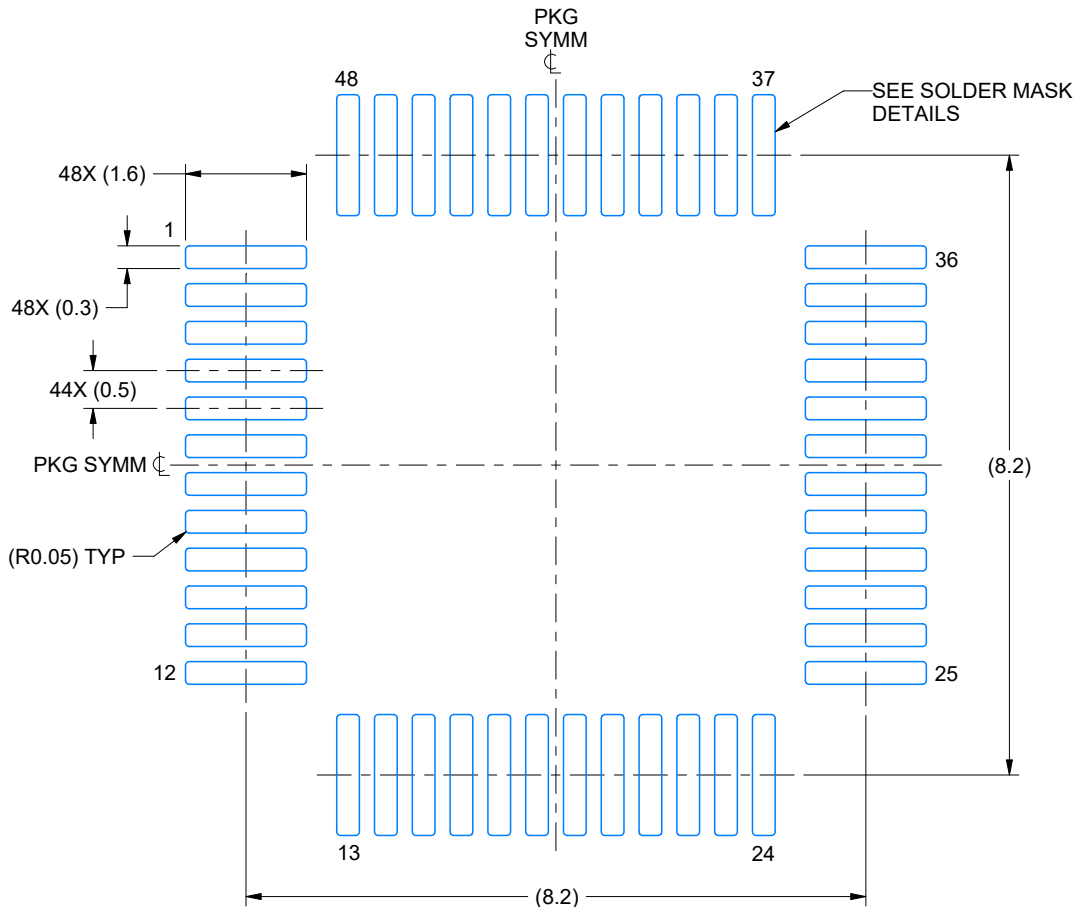
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.
4. This may also be a thermally enhanced plastic package with leads connected to the die pads.

EXAMPLE BOARD LAYOUT

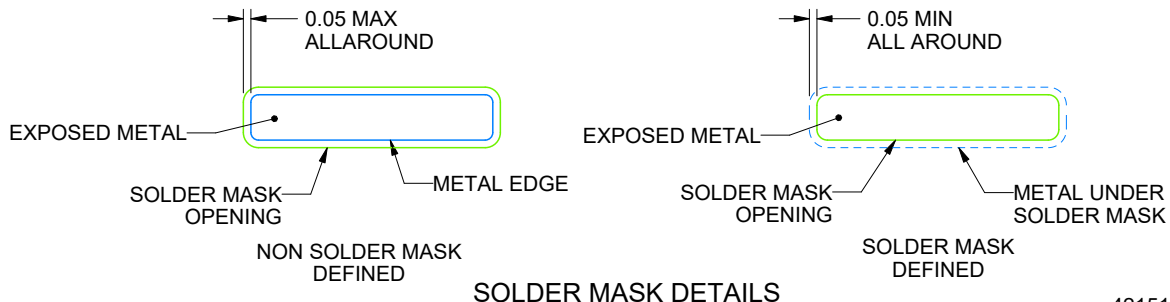
PT0048A

LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE 10.000



SOLDER MASK DETAILS

4215159/A 12/2021

NOTES: (continued)

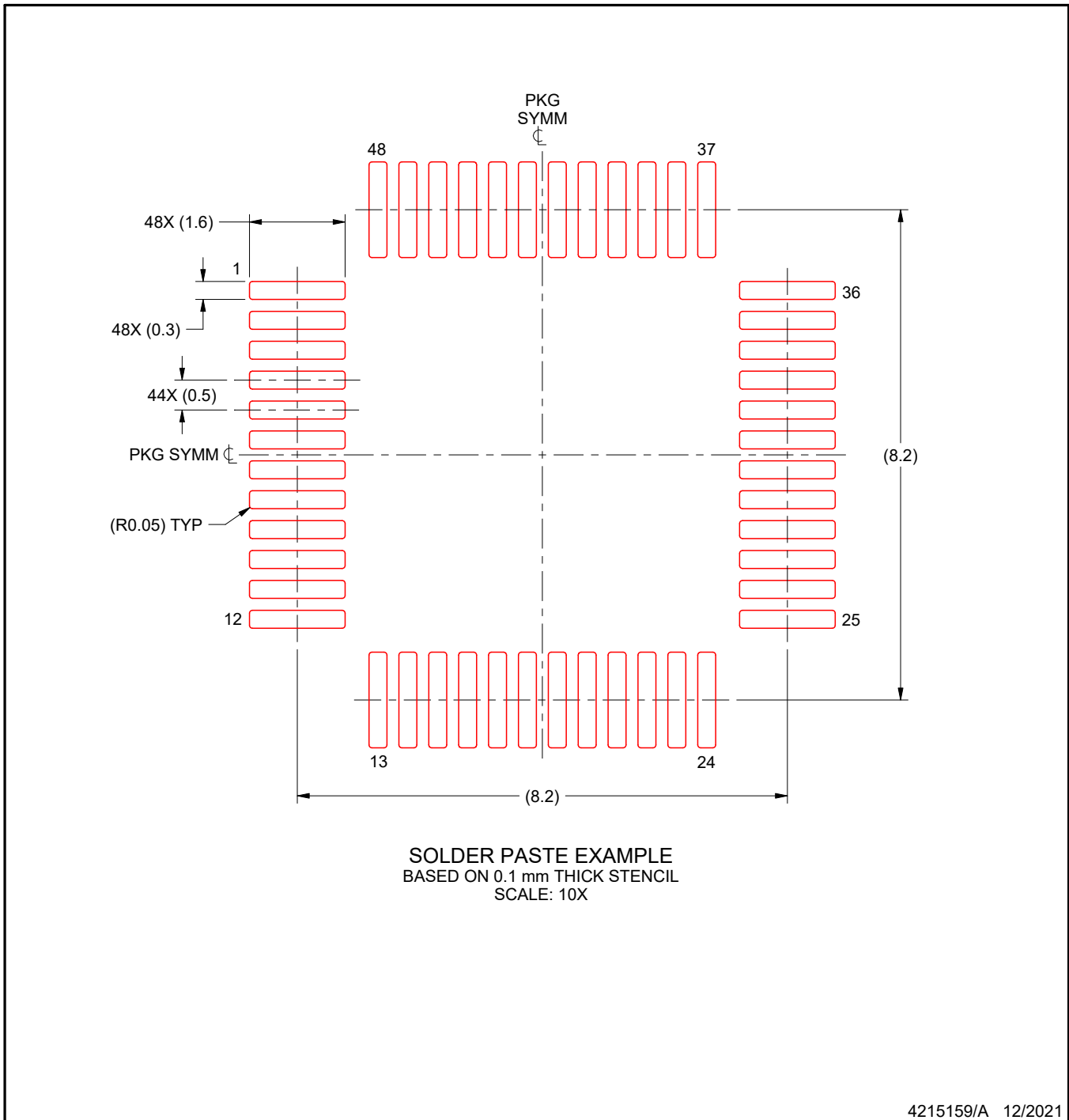
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PT0048A

LQFP - 1.6 mm max height

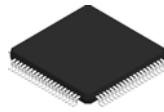
LOW PROFILE QUAD FLATPACK



NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

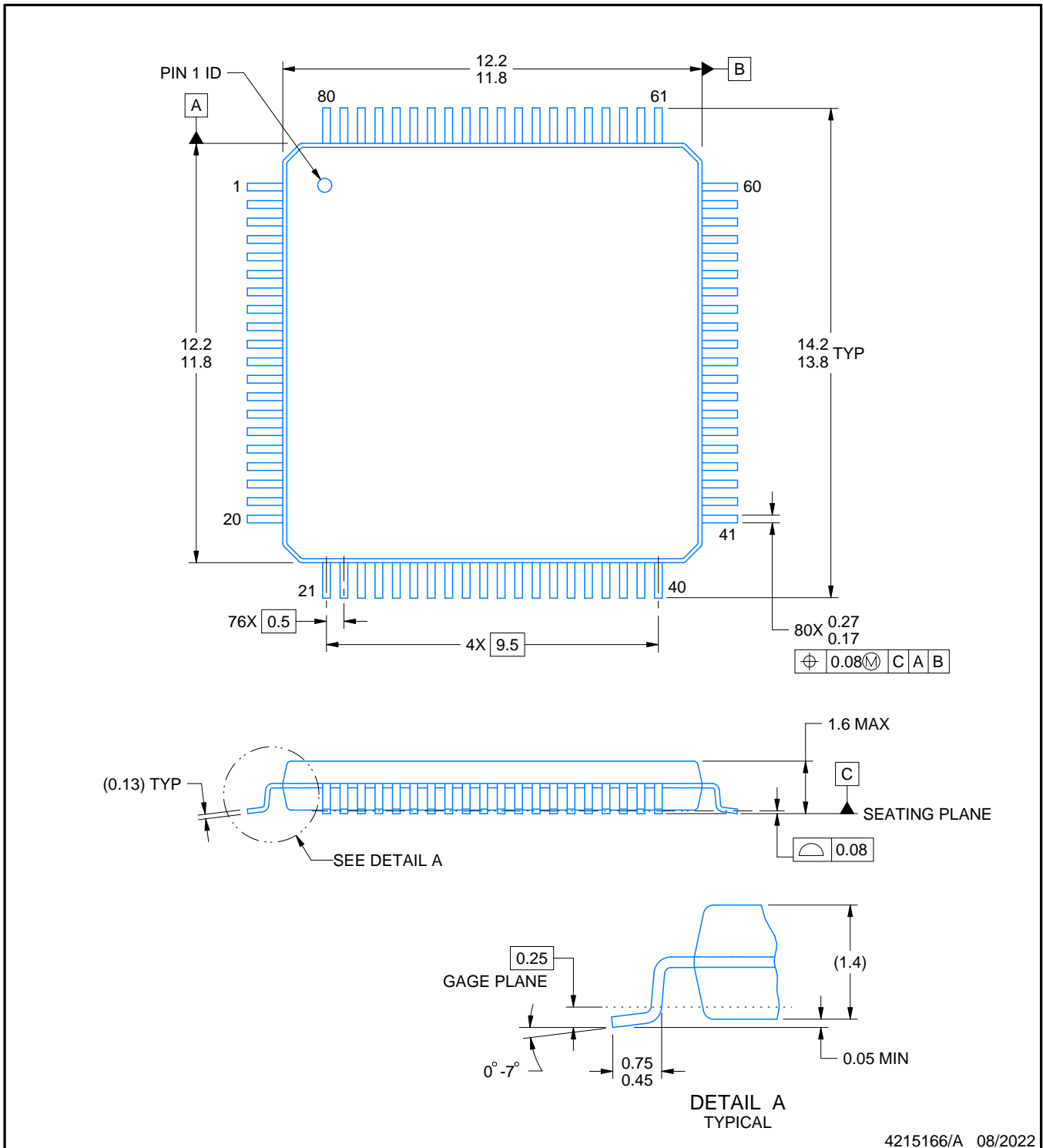
PN0080A



PACKAGE OUTLINE

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



NOTES:

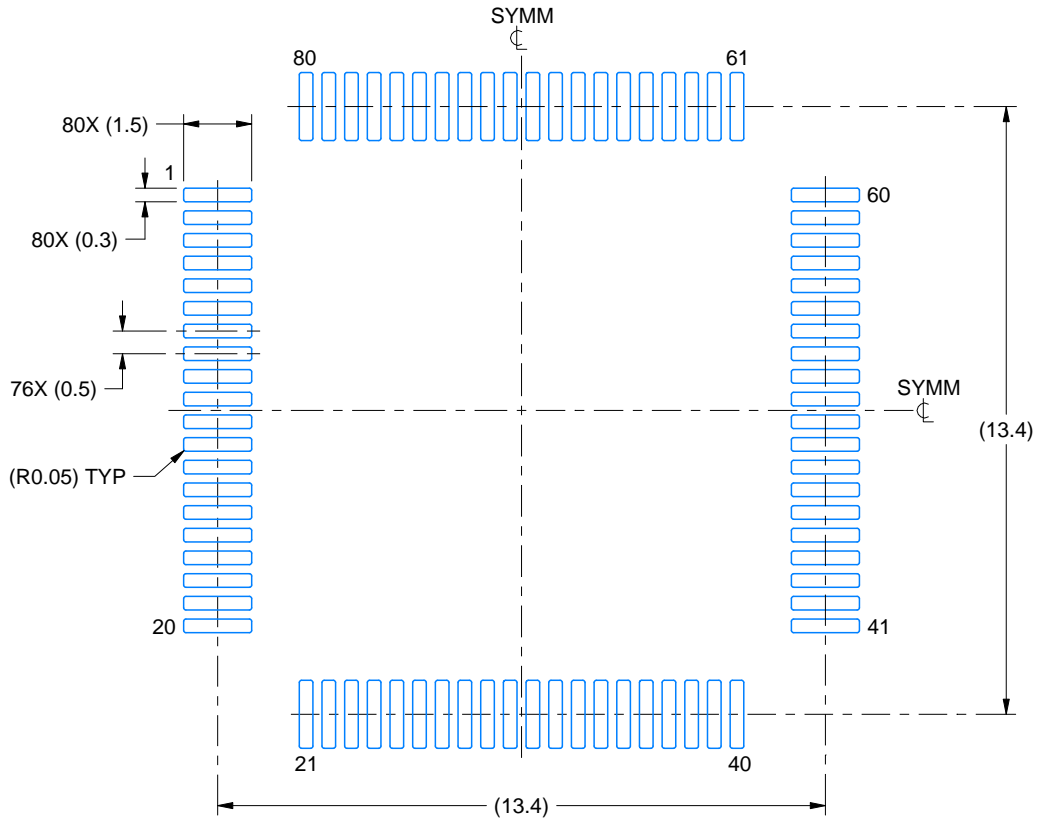
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.

EXAMPLE BOARD LAYOUT

PN0080A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS

4215166/A 08/2022

NOTES: (continued)

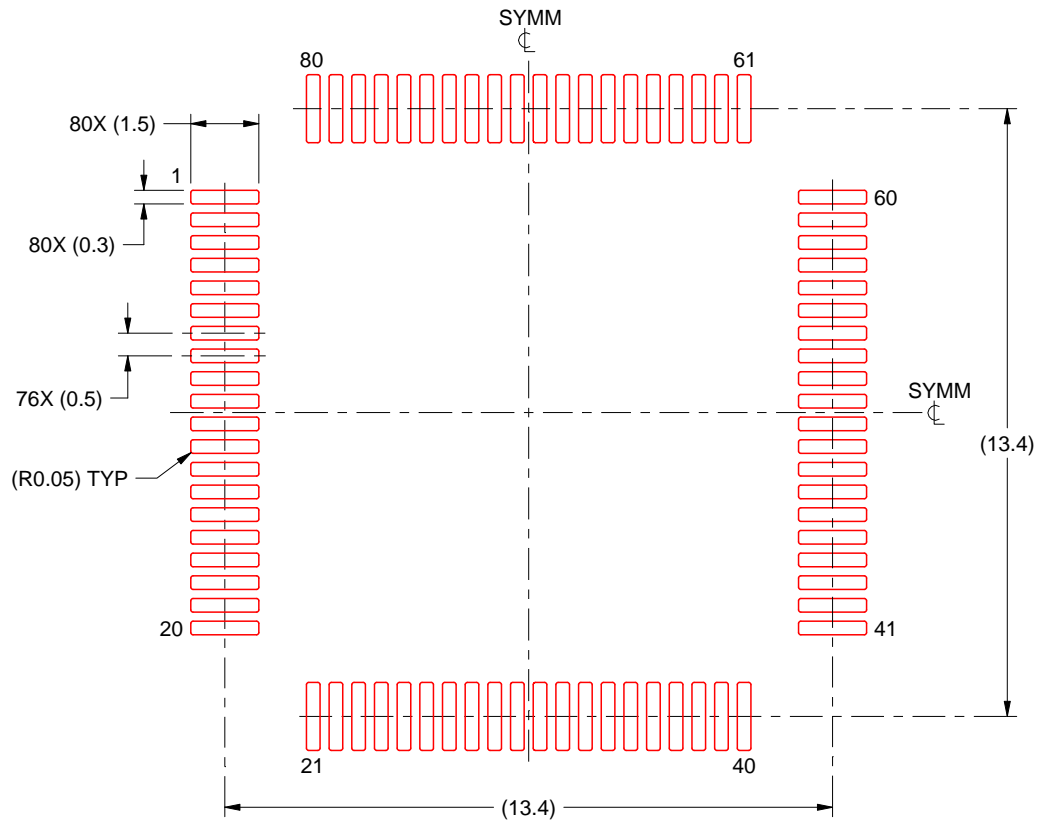
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).

EXAMPLE STENCIL DESIGN

PN0080A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:6X

4215166/A 08/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PM0064A



PACKAGE OUTLINE

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



4215162/A 03/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.

EXAMPLE BOARD LAYOUT

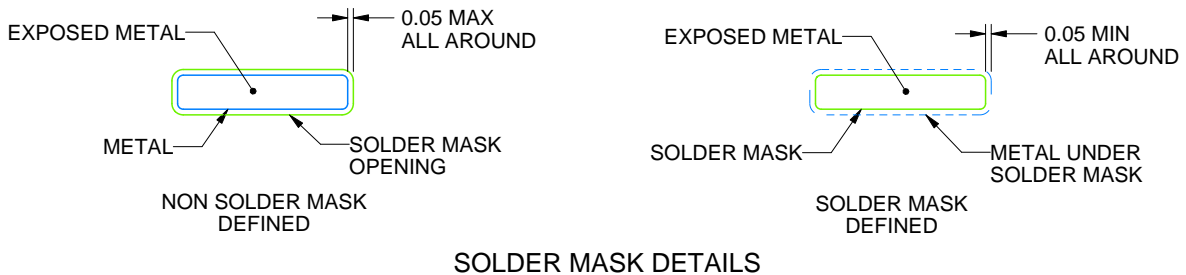
PM0064A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4215162/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).

EXAMPLE STENCIL DESIGN

PM0064A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK

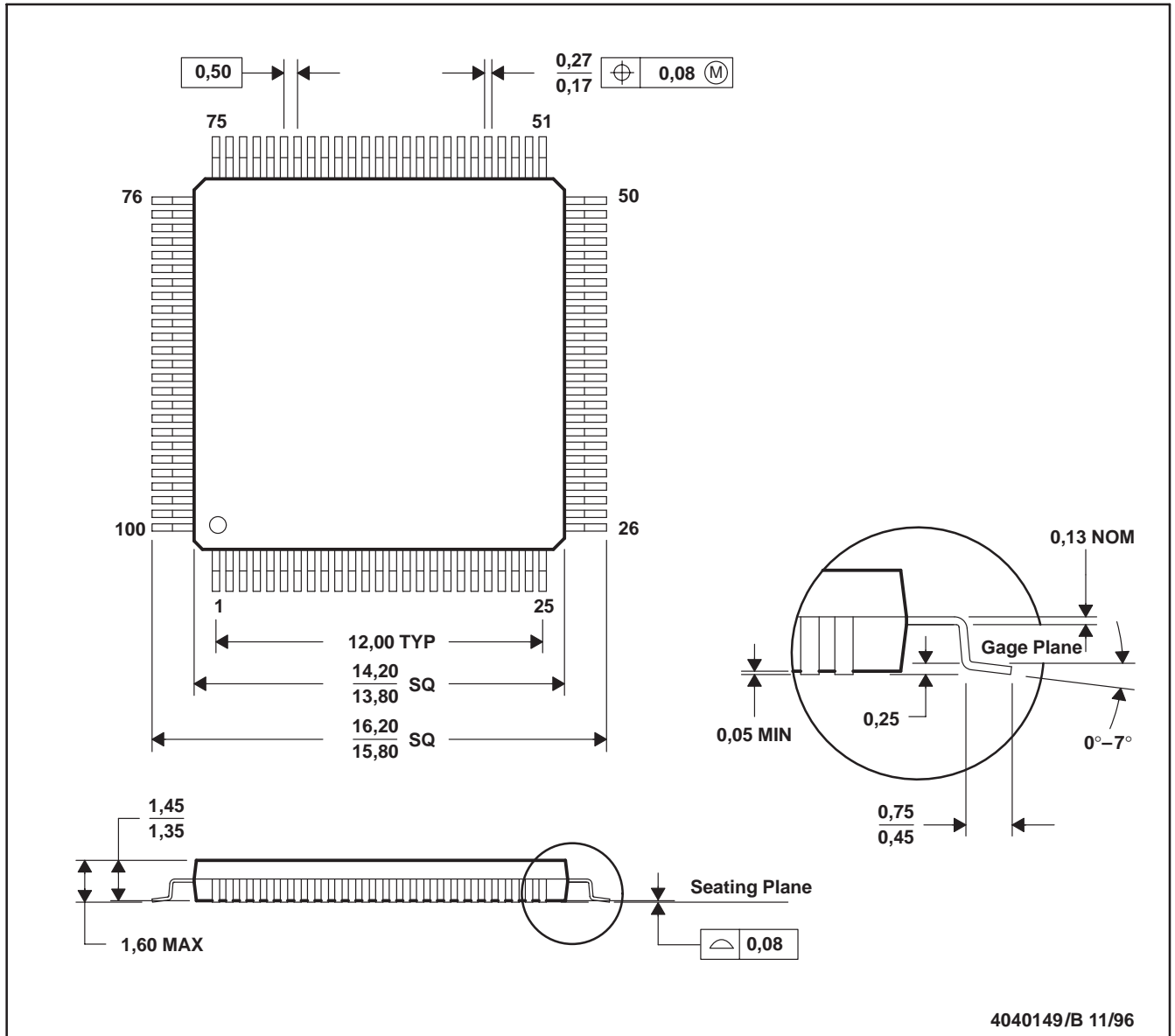


NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PZ (S-PQFP-G100)

PLASTIC QUAD FLATPACK

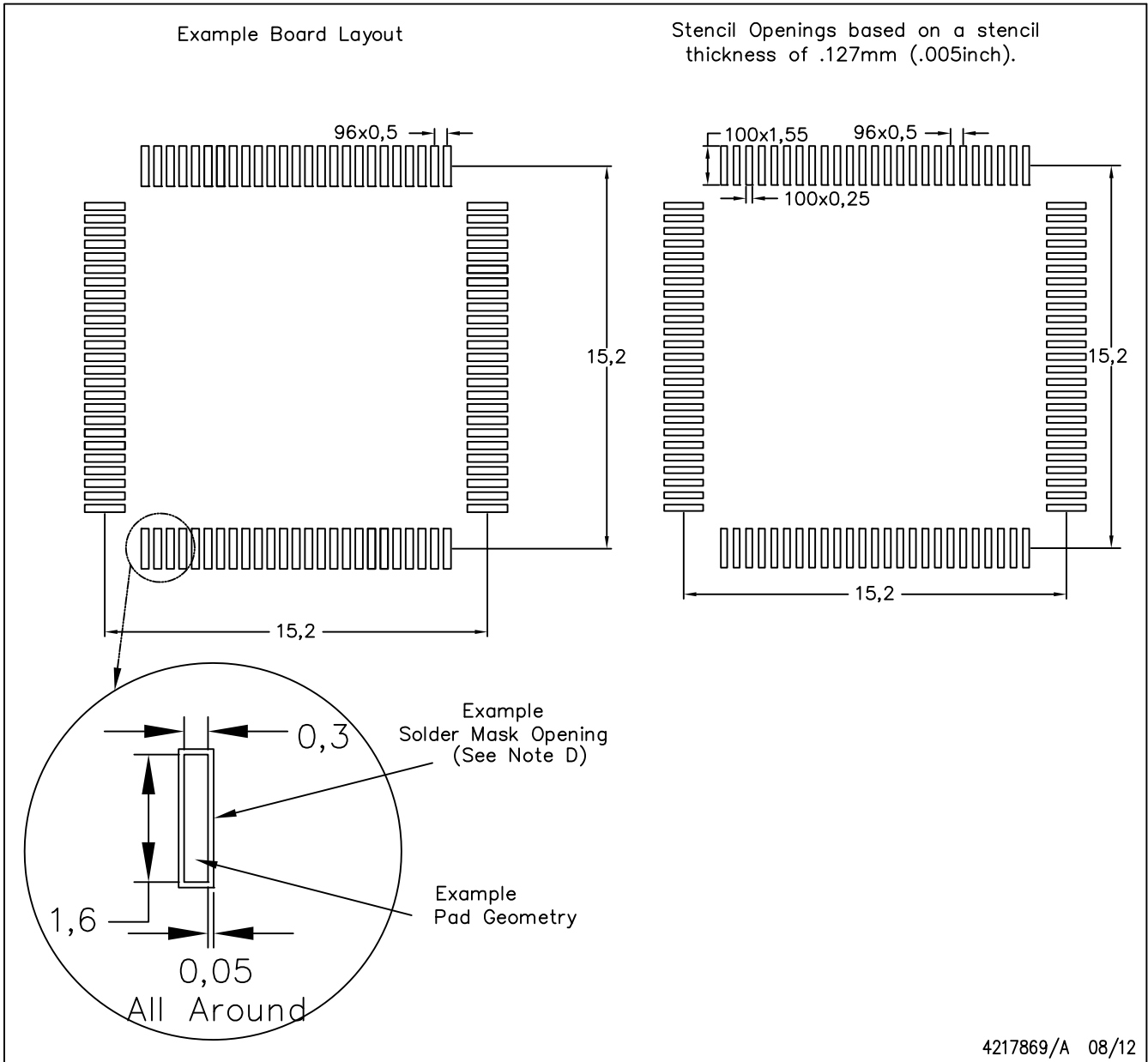


4040149/B 11/96

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-026

PZ (S-PQFP-G100)

PLASTIC QUAD FLAT PACK



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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