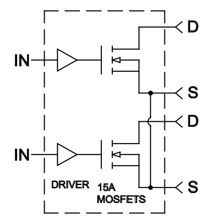
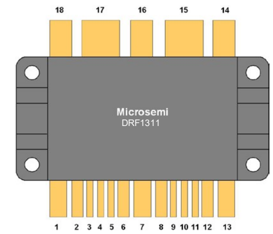
DATASHEET

DRF1311

DATASHEET

1000V, 15A, 30MHz





MOSFET Push-Pull Hybrid

The DRF1311 is a push-pull hybrid containing two high power gate drivers and two power MOSFETs. It was designed to provide the system designer increased flexibility, higher performance, and lowered cost over a non-integrated solution. This low parasitic approach, coupled with the Schmitt trigger input, Kelvin signal ground, provide improved stability and control in Kilowatt to Multi-Kilowatt, High Frequency ISM applications.

Features

- Switching Frequency: DC TO 30MHz
- Low Pulse Width Distortion
- Single Power Supply (Per Section)
- 1V CMOS Schmitt Trigger Input 1V Hysteresis
- Inverting Non-Inverting Select
- RoHS Compliant
- Switching Speed 3-4ns
- B_{Vds} = 1Kv
- I_{ds} = 26A avg.
- $R_{DS(on)}$ ≤ .55 Ohm
- P_D = 1000W Per-section

Typical Applications

- Class C, D and E RF Generators
- Switch Mode Power Amplifiers
- Pulse Generators
- Ultrasound Transducer Drivers
- Acoustic Optical Modulators

Driver Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Unit
V_{dd}	Supply Voltage	8		15	V
IN	Signal Input to Source Voltage	-0.5		V_{dd} + 0.3	
$I_{O\ PK}$	Output Current Peak			15	A
T_{JMAX}	Operating Temperature			150	°C

Driver Specifications (Per-Section) @ T_c = 25

Symbol	Parameter	Min	Typ	Max	Unit
V_{dd}	Supply Voltage	8	12		V
$IN_{(R)}$	Input Voltage Rising Edge		2.5		ns
$IN_{(F)}$	Input Voltage Falling Edge		2.5		
I_{DDQ}	Quiescent Current, V_{dd} = 12V		15	25	mA
I_O	Output Current		15		A
C_{oss}	Output Capacitance		2500		pF
C_{iss}	Input Capacitance Input		35		
R_{IN}	Input Parallel Resistance Vin= 5V, V_{dd} = 12V		1		MΩ
$V_{T(ON)}$	V Threshold On, V_{dd} = 12V, Vin= 0 to 5V Ramp	2.2		3.2	V
$V_{T(OFF)}$	V Threshold Off, V_{dd} = 12V, Vin= 5 to 0V Ramp	1.0		1.9	
t_r	Rise Time 10% to 90%, V_{dd} = 12V, Vin = 5 to 0V, R_L = 1.0Ω, C_L = 2nF	1.5	2.5	3.0	ns
t_f	Fall Time 90% to 10%, V_{dd} = 12V, Vin = 0 to 5V, R_L = 1.0Ω, C_L = 2nF	1.5	2.5	3.0	
$T_{D(ON)}$	On Delay Time, 50% to 50%, V_{dd} = 12V, Vin = 0 to 5V, RL = 1.0Ω, CL = 2nF		18		
$T_{D(OFF)}$	Off Delay Time, 50% to 50%, V_{dd} = 12V, Vin = 0 to 5V, RL = 1.0Ω, CL = 2nF		18		

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Driver Output Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
C_{out}	Output Capacitance		2500		pF
R_{out}	Output Resistance		0.5		Ω
L_{out}	Output Inductance	2	3	4	nH
F_{MAX}	Operating Frequency CL = 3nF + 50Ω			60	MHz

Driver Thermal Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$R_{\theta JC}$	Thermal Resistance Junction to Case		1.5		°C/W
T_j, T_{STG}	Operating and Storage Temperature	-55		150	°C
P_{DC}	Maximum Power Dissipation @ T_C = 25°C		80		W

MOSFET Absolutes Maximum Ratings (Per-Section)

Symbol	Parameter	Min	Typ	Max	Unit
BV_{DSS}	Drain Source Voltage	1000			V
I_D	Continuous Drain Current T_{HS} = 25°C			15	A
$R_{DS(on)}$	Drain-Source On State Resistance		1		Ω
T_{jmax}	Operating Temperature			175	°C

MOSFET Dynamic Characteristics (Per-Section)

Symbol	Parameter	Min	Typ	Max	Unit
C_{iss}	Input Capacitance, V_{DS} = 100V		1650		pF
C_{oss}	Output Capacitance, V_{DS} = 100V		158		
C_{rss}	Reverse Transfer Capacitance, V_{DS} = 100V		34		

MOSFET Thermal Characteristics (Total Package)

Symbol	Parameter	Min	Type	Max	Unit
$R_{\theta JC}$	Junction to Case Thermal Resistance		.06		°C/W
$R_{\theta JHS}$	Junction to Heat Sink Thermal Resistance		.14		
T_{JSTG}	Storage Junction Temperature	-55		150	°C
P_{DHS}	Maximum Power Dissipation @ T_{SINK} = 25°C		1.07		KW
P_{DC}	Total Power Dissipation @ T_C = 25°C		2.5		

Per Section Output Switching Performance, All Silicon Devices are Die Selected Temp = 25°C

ALL DATA IS COLLECTED USING THE TEST CIRCUIT AS SHOWN IN FIGURE 2

Symbol	Characteristic	Min	Typ	Max	Typ
t_f	Fall Time 90% to 10% V_{dd} = 12V, V_{in} = 0 to 5V , V_{DS} = 100V, RL = 16.6Ω, CL = 0.4μF	1		2.5	ns
t_r	Rise Time 10% to 90% V_{dd} = 12V, V_{in} = 0 to 5V , V_{DS} = 100V, RL = 16.6Ω, CL = 0.4μF	10		35	
$t_{DLY(ON)}$	ON Delay Time, 50% to 50% V_{dd} = 12V, V_{in} = 0 to 5V , V_{DS} = 100V, RL = 16.6Ω, CL = 0.4μF	35		55	
$t_{DLY(OFF)}$	OFF Delay Time, 50% to 50% V_{dd} = 12V, V_{in} = 0 to 5V, V_{DS} = 100V, RL = 16.6Ω, CL = 0.4μF	50		70	

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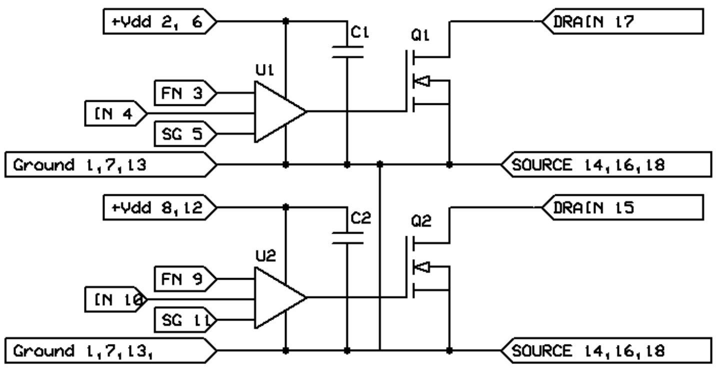

Figure 1, DRF1311 Circuit Diagram

The DRF1311 is configured as a Push Pull Hybrid incorporating two independent channels configured with a common source each consisting of a driver, a high voltage MOSFET and by-pass capacitors. The function of the by-pass capacitors C1 and C2 is to reduce the internal parasitic loop inductance. This coupled with the tight geometry of the hybrid allows optimal gate drive to the MOSFET. This low parasitic approach coupled with the Schmitt trigger input (IN), Kelvin signal ground (SG); provide improved stability and control in Kilowatt to Multi-Kilowatt high frequency applications. The IN pin should be referenced to the Kelvin Ground (SG) and is applied to a Schmitt Trigger. The SG pin is a Kelvin return for the IN pin only. The signal is then applied to the intermediate drivers and level shifters; this section contains proprietary circuitry designed specifically for ring abatement. To further increase the utility of the device the driver die and the MOSFET die are adjacent die selected. This provides a very close match in the turn on and propagation delays.

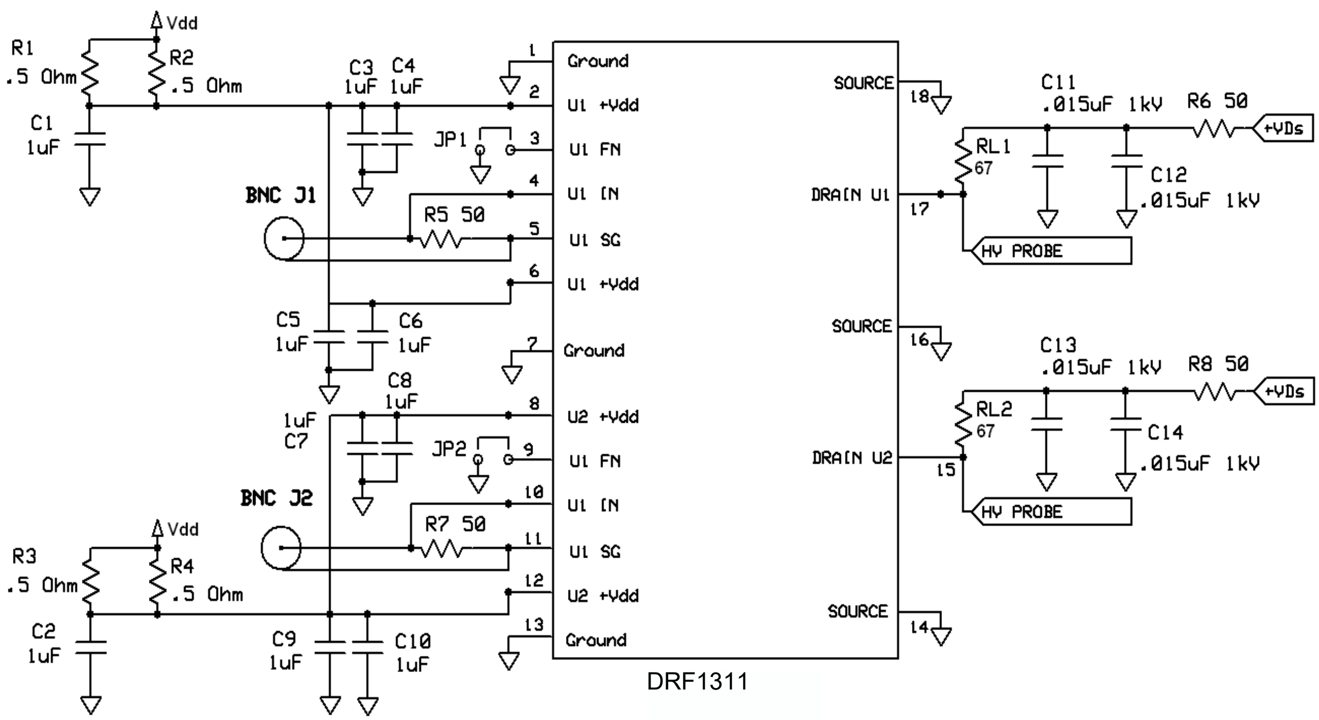

Figure 2, DRF1311 Test Circuit

The test circuit illustrated in Figure 2 was used to evaluate the DRF1311. The input control signal is applied via IN and SG pins using RG188. This provides excellent noise immunity and control of the signal ground currents. The $+V_{DD}$ inputs (pins 2, 6, 8 and 12) should be heavily by-passed by 1µF capacitors as close to the pins as possible. The capacitors used for this function must be capable of supporting the RMS currents and frequency of the gate load. R_L set for I_{DM} at V_{DS} max this load is used to evaluate the output performance.

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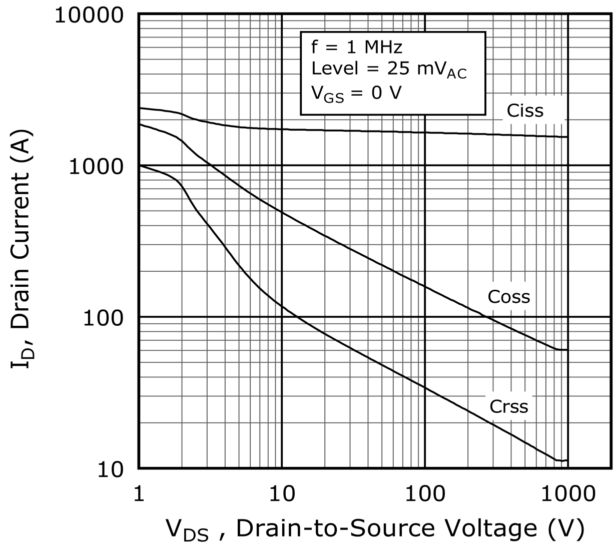

Figure 3, Typical Capacitance vs. Drain-to-Source Voltage

Pin Assignments	
Pin 1	Ground
Pin 2	U1 +Vdd
Pin 3	U1 FN
Pin 4	U1 IN
Pin 5	U1 SG
Pin 6	U1 +Vdd
Pin 7	Ground
Pin 8	U2 +Vdd
Pin 9	U2 FN
Pin 10	U2 IN
Pin 11	U2 SG
Pin 12	U2 +Vdd
Pin 13	Ground
Pin 14	Source
Pin 15	U2 Drain
Pin 16	Source
Pin 17	U1 Drain
Pin 18	Source

None of the inputs to U1 or U2 of the DRF1311 are isolated for direct connection to a ground referenced power supply or control circuitry. **Isolation appropriate to the application is the responsibility of the end user.** It is imperative that high output currents be restricted to the Source (14, 16, 18) and drain (15, 17) pins by design. See DRF100 for more information on Driver IC used in the device.

The Function (FN, pin 3 or pin 9) is the invert or non-invert select Pin, it is Internally held high.

Truth Table * Referenced to SG		
FN (pin 3)	**IN (pin 4)**	**MOSFET U1**
HIGH	**HIGH**	**ON**
HIGH	**LOW**	**OFF**
LOW	**HIGH**	**OFF**
LOW	**LOW**	**ON**

Truth Table * Referenced to SG		
FN (pin 9)	**IN (pin 10)**	**MOSFET U2**
HIGH	**HIGH**	**ON**
HIGH	**LOW**	**OFF**
LOW	**HIGH**	**OFF**
LOW	**LOW**	**ON**

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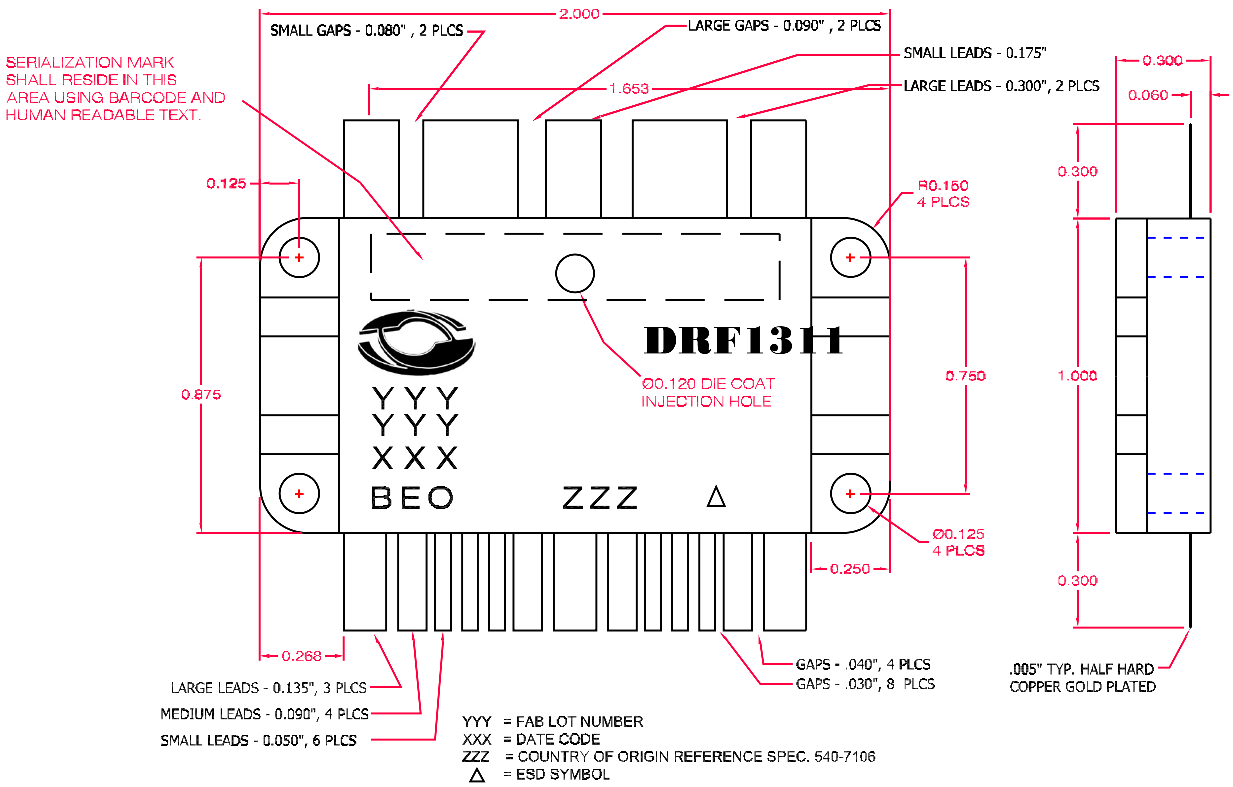

All dimensions are ± 0.010

Figure 4, DRF1311 Mechanical Outline

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