32V, 2A, SYNCHRONOUS DC-DC BUCK CONVERTER WITH ENHANCED EMI REDUCTION

DESCRIPTION

The AP63200Q is a 2A, synchronous buck converter with a wide input voltage range of 3.8V to 32V and fully integrates a 125mΩ high-side power MOSFET and a 68mΩ low-side power MOSFET to provide high-efficiency step-down DC-DC conversion.

The AP63200Q device is easily used by minimizing the external component count due to its adoption of peak current mode control along with its integrated compensation network.

The AP63200Q has designs optimized for Electromagnetic Interference (EMI) reduction. The converter features Frequency Spread Spectrum (FSS) with a switching frequency jitter of ±6%, which reduces EMI by not allowing emitted energy to stay in any one frequency for a significant period of time. It also has a proprietary gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off times, which further reduces high-frequency radiated EMI noise caused by MOSFET switching.

The device is available in a low-profile, TSOT26 package.

FEATURES

- VIN 3.8V to 32V
- 2A Continuous Output Current
- 0.8V ± 1% Reference Voltage
- 22µA Low Quiescent Current (Pulse Frequency Modulation)
- 500kHz Switching Frequency
- Supports Pulse Frequency Modulation (PFM) and Pulse Width Modulation (PWM)
- Proprietary Gate Driver Design for Best EMI Reduction
- Frequency Spread Spectrum (FSS) to Reduce EMI
- Low-Dropout (LDO) Mode
- Precision Enable Threshold to Adjust UVLO
- Protection Circuitry
    - Undervoltage Lockout (UVLO)
    - Cycle-by-Cycle Peak Current Limit
    - Thermal Shutdown

FUNCTIONAL BLOCK

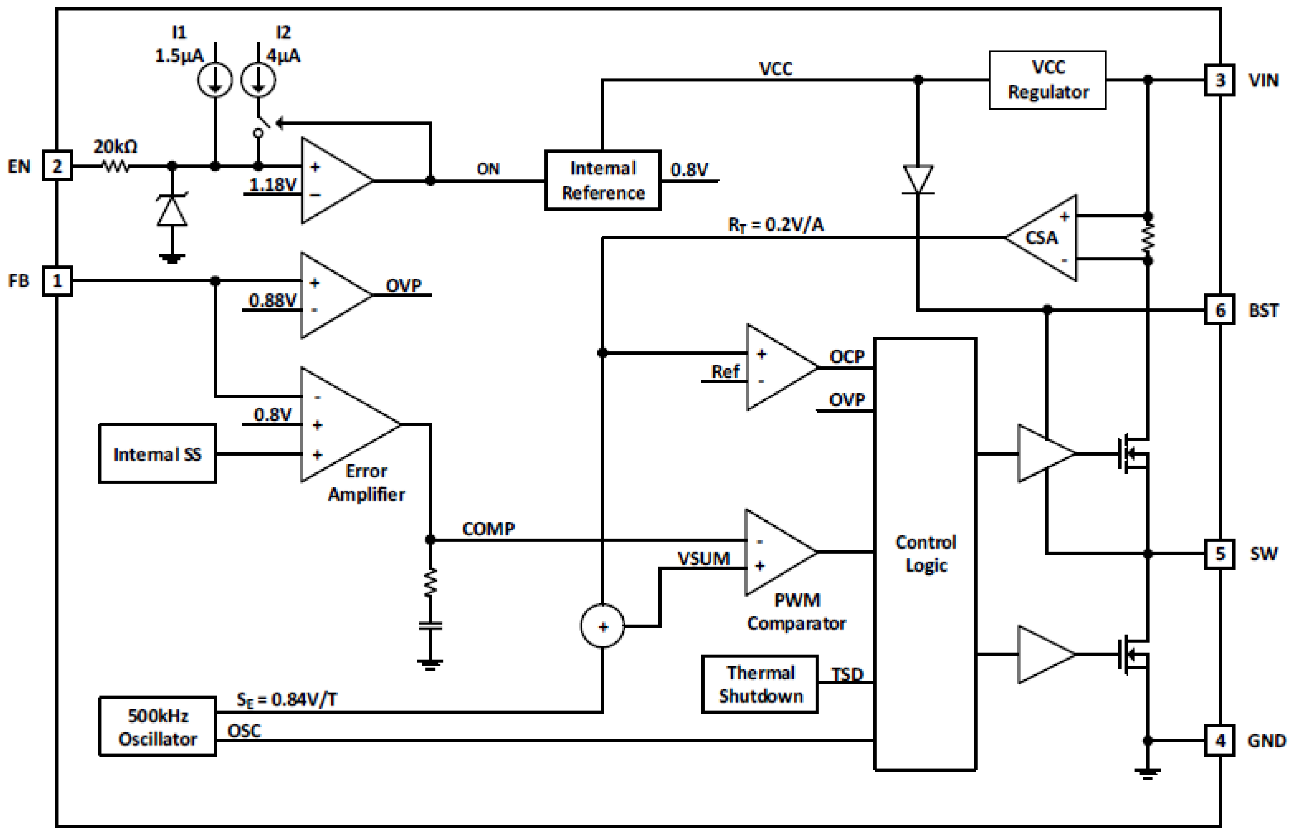

Figure 1. Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
VIN	Supply Voltage	-0.3 to +35.0 (DC)	V
		-0.3 to +40.0 (400ms)	
V_{SW}	Switch Node Voltage	-1.0 to VIN + 0.3 (DC)	V
		-2.5 to VIN + 2.0 (20ns)	
V_{BST}	Bootstrap Voltage	V_{SW} - 0.3 to V_{SW} + 6.0	V
V_{FB}	Feedback Voltage	-0.3 to +6.0	V
V_{EN}	Enable/UVLO Voltage	-0.3 to +35.0	V
T_{ST}	Storage Temperature	-65 to +150	°C
T_J	Junction Temperature	+160	°C
T_L	Lead Temperature	+260	°C

ESD Susceptibility			
HBM	Human Body Mode	2000	V
CDM	Charge Device Model	1500	V

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
VIN	Supply Voltage	3.8	32	V
T_A	Operating Ambient Temperature Range	-40	+125	°C
T_J	Operating Junction Temperature Range	-40	+150	°C

EVALUATION BOARD

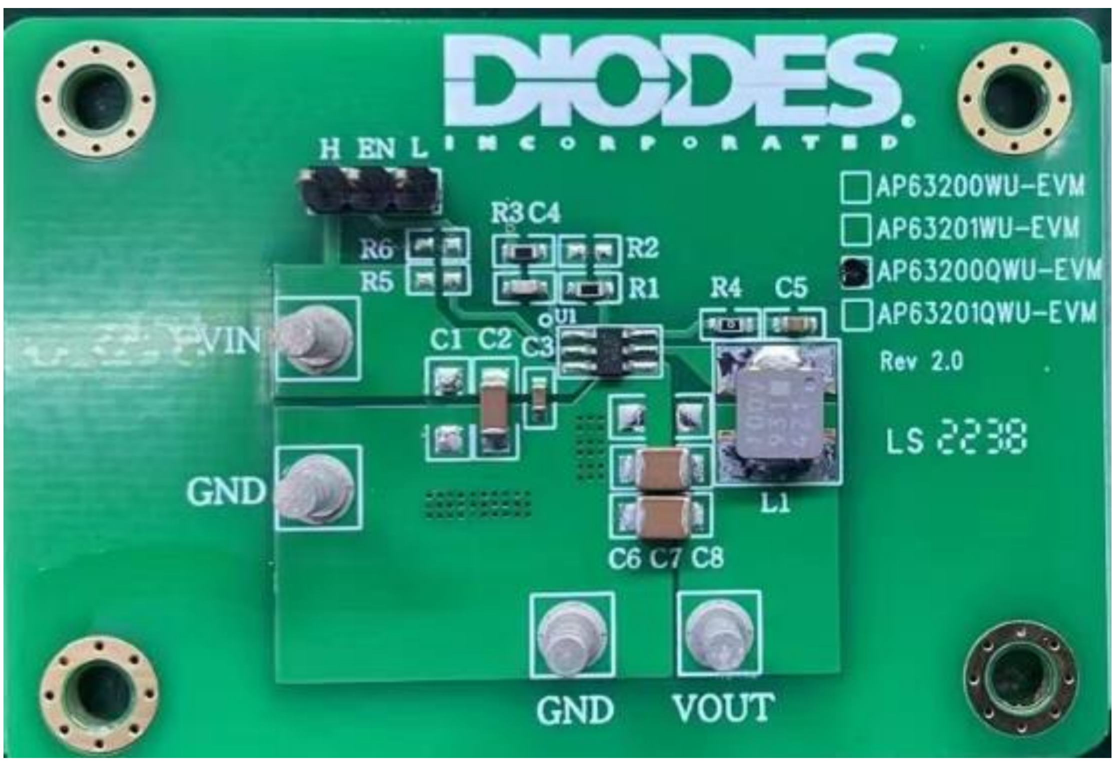

Figure 2. AP63200QWU-EVM

QUICK START GUIDE

The AP63200QWU-EVM has a simple layout and allows access to the appropriate signals through test points. To evaluate the performance of the AP63200QWU, follow the procedure below:

1. For evaluation board configured at V_{OUT}=5V, connect a power supply to the input terminals V_{IN} and GND. Set V_{IN} to 12V.
2. Connect the positive terminal of the electronic load to V_{OUT} and negative terminal to GND.
3. For Enable, place a jumper to "H" position to enable IC. Jump to "L" position to disable IC.
4. The evaluation board should now power up with a 5V output voltage.
5. Check for the proper output voltage of 5V (±1%) at the output terminals V_{OUT} and GND. Measurement can also be done with a multimeter with the positive and negative leads between V_{OUT} and GND.
6. Set the load to 2A through the electronic load. Check for the stable operation of the SW signal on the oscilloscope. Measure the switching frequency.

MEASUREMENT/PERFORMANCE GUIDELINES:

1) When measuring the output voltage ripple, maintain the shortest possible ground lengths on the oscilloscope probe. Long ground leads can erroneously inject high frequency noise into the measured ripple.
2) For efficiency measurements, connect an ammeter in series with the input supply to measure the input current. Connect an electronic load to the output for output current.

SETTING OUTPUT VOLTAGE:

(1) Setting the output voltage

The AP63200QWU features external programmable output voltage by using a resistor divider network R3 and R1 as shown in the typical application circuit. The output voltage is calculated as below,

$$V_{OUT} = 0.8 \times \left(\frac{R_1 + R_3}{R_1} \right)$$

First, select a value for R1 according to the value recommended in the table 1. Then, R3 is determined. The output voltage is given by Table 1 for reference. For accurate output voltage, 1% tolerance is required.

Table 1. Recommended Component Selections

AP63200Q							
Output Voltage (V)	R3 (kΩ)	R1 (kΩ)	L (µH)	C1 (µF)	C2 (µF)	C3 (nF)	C4 (pF)
1.2	15.0	30.1	3.3	10	3 x 22	100	100
1.5	26.1	30.1	4.7	10	3 x 22	100	100
1.8	37.4	30.1	4.7	10	2 x 22	100	100
2.5	63.4	30.1	6.8	10	2 x 22	100	100
3.3	93.1	30.1	6.8	10	2 x 22	100	100
5.0	158.0	30.1	10.0	10	2 x 22	100	100
12.0	422.0	30.1	15.0	10	2 x 22	100	56

(2) Output feed-forward capacitor selection

The AP63200QWU has the internal integrated loop compensation as shown in the function block diagram. The compensation network includes an 18k resistor and a 7.6nF capacitor. Usually, the type II compensation network has a phase margin between 60 and 90 degree. However, if the output capacitor has ultra-low ESR, the converter results in low phase margin. To increase the converter phase margin, a feed-forward cap C4 is used to boost the phase margin at the converter cross-over frequency, f_C. The feed-forward capacitor is given by Table 1 for reference. The feed-forward capacitor is calculated as below,

$$C_4 = \frac{1}{2\pi \times f_C \times R_3}$$

EVALUATION BOARD SCHEMATIC

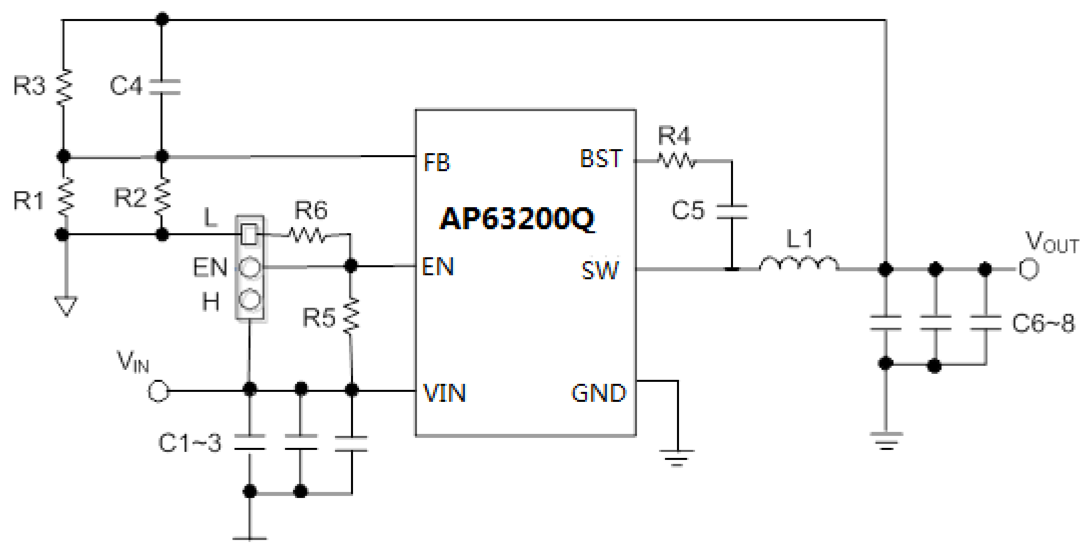

Figure 3. AP63200QWU-EVM Schematic

BILL OF MATERIALS for AP63200QWU-EVM (V_{OUT}=12V)

Item	Value	Type	Rating	Description	Description
C1				Input CAP	open
C2	10Uf	X7R, Ceramic/1206	50V	Input CAP	CGA5L1X7R1H106K160AC
C3	0.1Uf	Ceramic/0603	50V	Input CAP	GCM188L81H104KA57
C4	100pF	Ceramic/0603	100V	Feedback CAP	GCM1885G2A101JA16
C5	0.1Uf	Ceramic/0603	50V	Bootstrap CAP	GCM188L81H104KA57
C6	22Uf	X8L, Ceramic/1206	16V	Output CAP	CGA6P1X8L1C226M250AC
C7	22Uf	X8L, Ceramic/1206	16V	Output CAP	CGA6P1X8L1C226M250AC
C8				Output CAP	open
L1	10uH			Inductor	Panasonic ETQP3M100KVP
R1	30K	0603	1%		ERJ3EKF3002V
R2					open
R3	158K	0603	1%	Bootstrap RES	ERJ3EKF1583V
R4	0	0603	1%	Bootstrap RES	ERJ-3GEY0R00V
R5					open
R6					open
U1		AP63200QWU		TSOT23-6	Diodes BCD

***Note**: The present value of R3/R1 are based on Vout=5V

TYPICAL PERFORMANCE CHARACTERISTICS

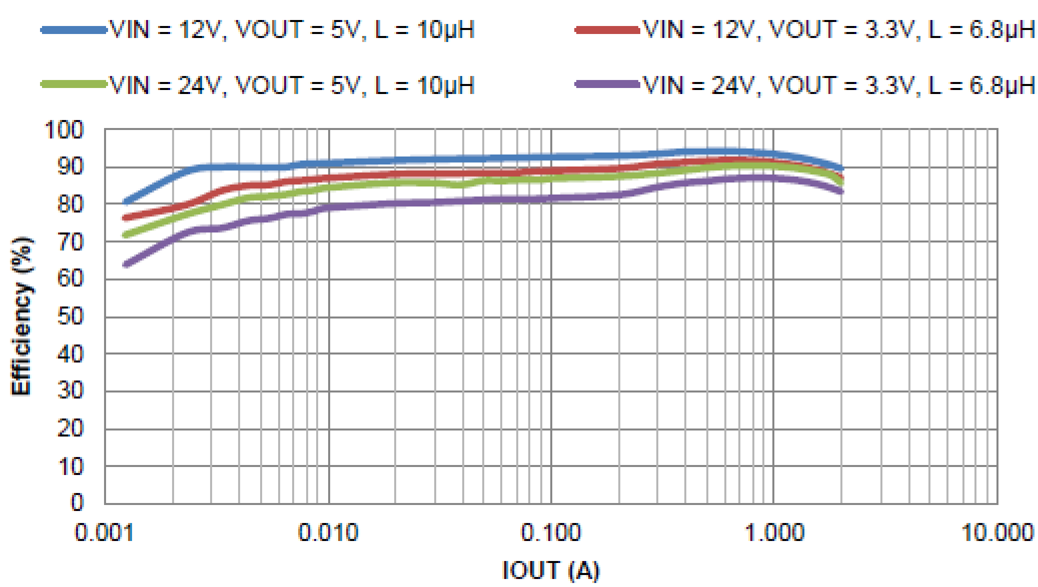

Figure 4. Efficiency vs Output Current

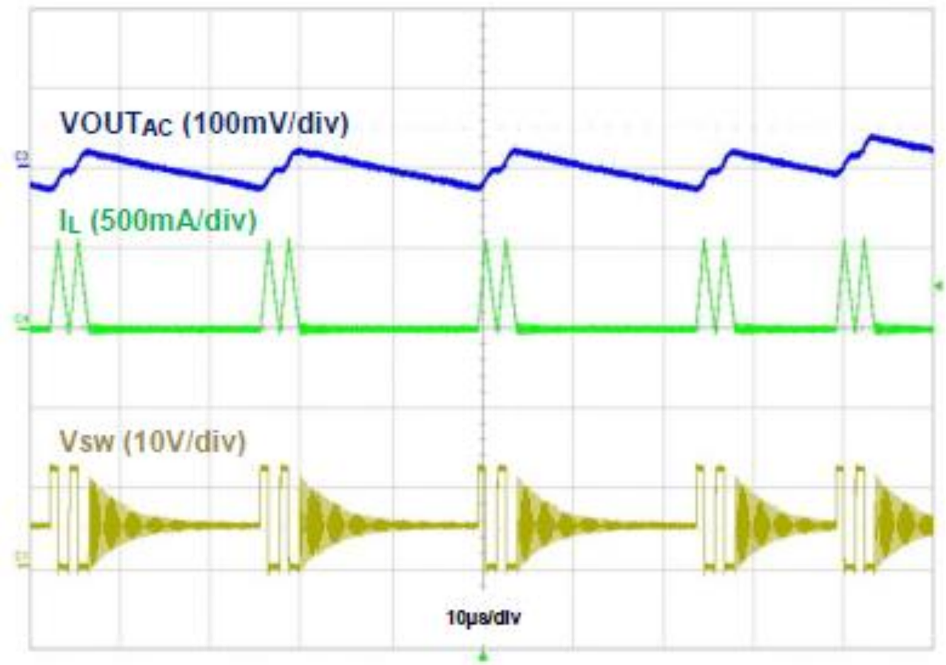

Figure 5. Output Ripple for V_{IN}=12V, V_{OUT}=5.0V, I_{OUT}=50mA

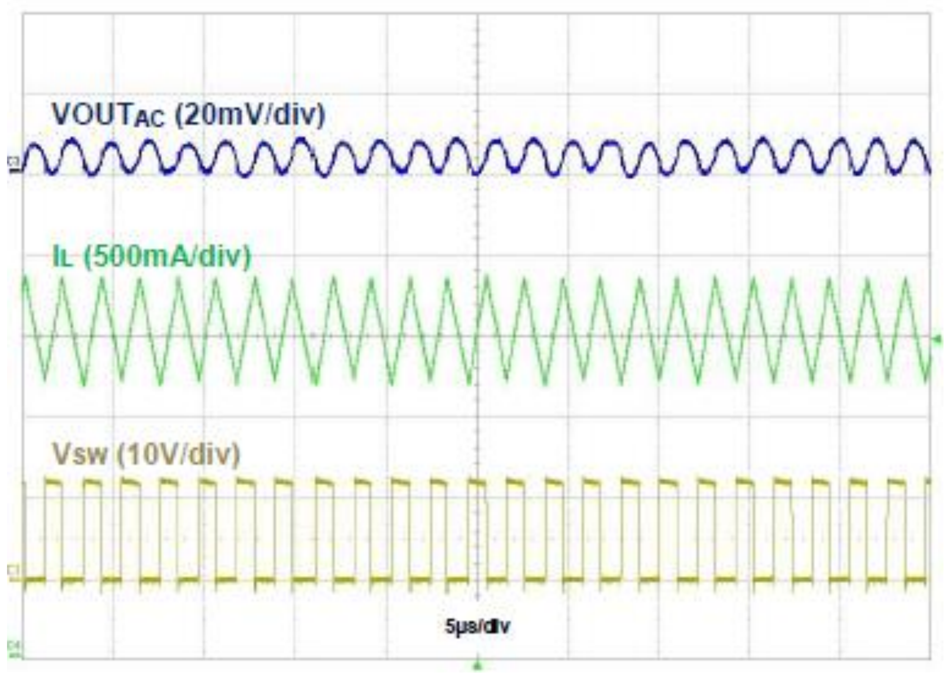

Figure 6. Output Ripple for V_{IN}=12V, V_{OUT}=5.0V, I_{OUT}=2A

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