

## J650-VB Datasheet

### P-Channel 60-V (D-S) MOSFET

#### PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)	$Q_g$ (Typ)
- 60	0.100 at $V_{GS} = -10$ V	- 20	12.5
	0.120 at $V_{GS} = -4.5$ V	- 15	

#### FEATURES

- Trench Power MOSFET
- 100 % UIS Tested

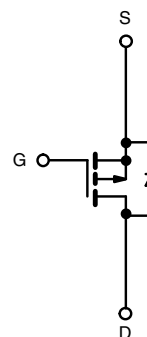
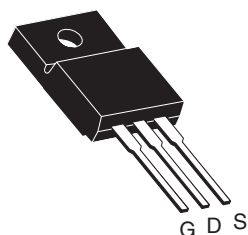
#### APPLICATIONS

- Load Switch



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

TO-220 FULLPAK



P-Channel MOSFET

#### ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ , unless otherwise noted

Parameter		Symbol	Limit	Unit
Gate-Source Voltage		$V_{GS}$	$\pm 20$	V
Continuous Drain Current ( $T_J = 175^\circ\text{C}$ )	$T_C = 25^\circ\text{C}$	$I_D$	- 20	A
	$T_C = 100^\circ\text{C}$		- 12	
Pulsed Drain Current		$I_{DM}$	- 60	
Continuing Source Current (Diode Conduction)		$I_S$	- 12	
Avalanche Current		$I_{AS}$	- 12	
Single Pulse Avalanche Energy	$L = 0.1$ mH	$E_{AS}$	7.2	mJ
Maximum Power Dissipation	$T_C = 25^\circ\text{C}$	$P_D$	30 <sup>a</sup>	W
	$T_A = 25^\circ\text{C}$		2 <sup>b</sup>	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	- 55 to 175	$^\circ\text{C}$

#### THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Junction-to-Ambient <sup>b</sup>	$t \leq 10$ sec	$R_{thJA}$	20	25	$^\circ\text{C/W}$
	Steady State		62	75	
Junction-to-Case		$R_{thJC}$	5	6	

Notes:

a. See SOA curve for voltage derating.

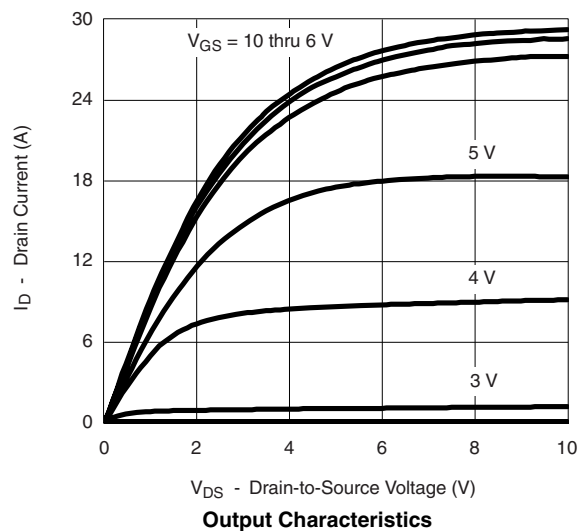
b. Surface Mounted on 1" x 1" FR-4 board.

SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Min	Typ <sup>a</sup>	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	- 60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	- 1.0	- 2.0	- 3.0	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -60\text{ V}, V_{GS} = 0\text{ V}$			- 1	$\mu\text{A}$
		$V_{DS} = -60\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^{\circ}\text{C}$			- 50	
		$V_{DS} = -60\text{ V}, V_{GS} = 0\text{ V}, T_J = 175\text{ }^{\circ}\text{C}$			- 150	
On-State Drain Current <sup>b</sup>	$I_{D(on)}$	$V_{DS} = -5\text{ V}, V_{GS} = -10\text{ V}$	- 10			A
Drain-Source On-State Resistance <sup>b</sup>	$r_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -5\text{ A}$		0.100		$\Omega$
		$V_{GS} = -10\text{ V}, I_D = -5\text{ A}, T_J = 125\text{ }^{\circ}\text{C}$		0.150		
		$V_{GS} = -10\text{ V}, I_D = -5\text{ A}, T_J = 175\text{ }^{\circ}\text{C}$		0.200		
		$V_{GS} = -4.5\text{ V}, I_D = -2\text{ A}$		0.120		
Forward Transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = -15\text{ V}, I_D = -5\text{ A}$		8		S
Dynamic						
Input Capacitance	$C_{iss}$	$V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		550		pF
Output Capacitance	$C_{oss}$			95		
Reverse Transfer Capacitance	$C_{rss}$			60		
Total Gate Charge	$Q_g$	$V_{DS} = -30\text{ V}, V_{GS} = -10\text{ V}, I_D = -8.4\text{ A}$		12.5	19	nC
Gate-Source Charge	$Q_{gs}$			2.3		
Gate-Drain Charge	$Q_{gd}$			3.2		
Gate Resistance	$R_g$	$f = 1\text{ MHz}$		8.0		$\Omega$
Turn-On Delay Time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = -30\text{ V}, R_L = 3.57\text{ }\Omega$ $I_D \cong -8.4\text{ A}, V_{GEN} = -10\text{ V}, R_G = 2.5\text{ }\Omega$		5	10	ns
Rise Time <sup>c</sup>	$t_r$			14	25	
Turn-Off Delay Time <sup>c</sup>	$t_{d(off)}$			15	25	
Fall Time <sup>c</sup>	$t_f$			7	12	
Source-Drain Diode Ratings and Characteristics ( $T_C = 25\text{ }^{\circ}\text{C}$ ) <sup>b</sup>						
Pulsed Current	$I_{SM}$				- 20	A
Forward Voltage <sup>b</sup>	$V_{SD}$	$I_F = -2\text{ A}, V_{GS} = 0\text{ V}$		- 0.9	- 1.3	V
Reverse Recovery Time	$t_{rr}$	$I_F = -8\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		50	80	ns
Reverse Recovery Time	$Q_{rr}$			80	120	nC

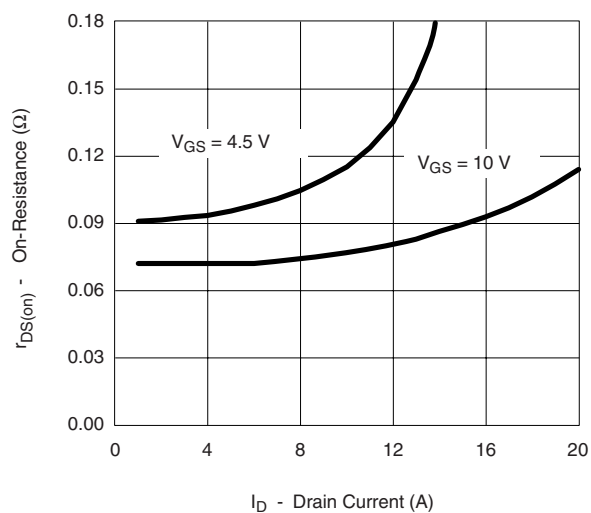
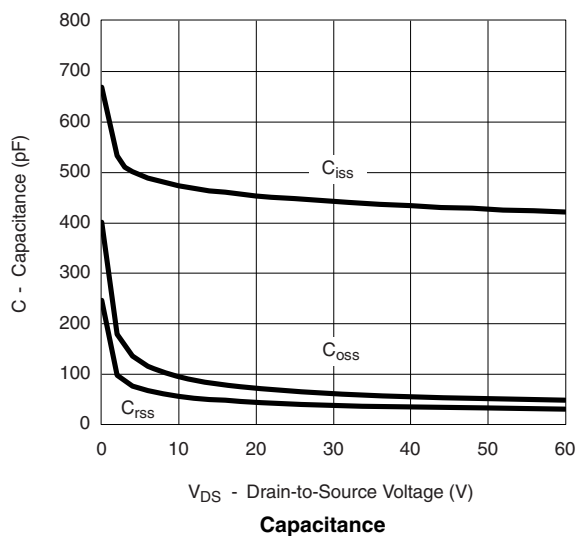
Notes:

- a. Guaranteed by design, not subject to production testing.  
 b. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
 c. Independent of operating temperature.

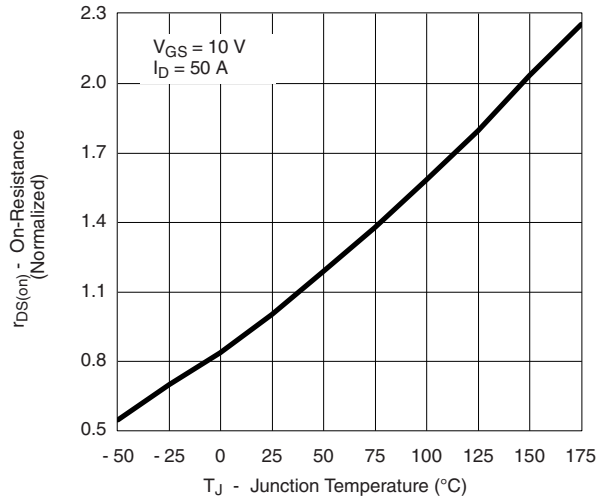
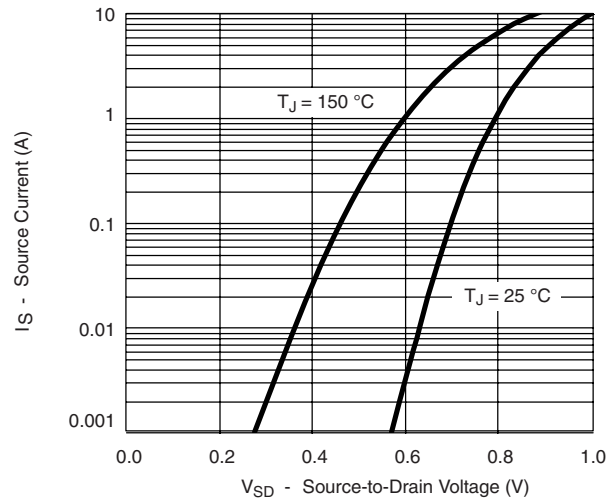
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

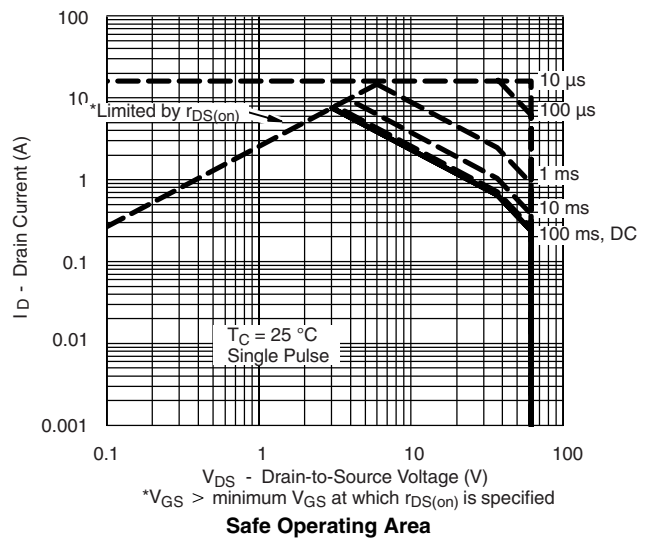
**TYPICAL CHARACTERISTICS** 25 °C unless noted

**Output Characteristics**

**Transfer Characteristics**

**Transconductance**

**On-Resistance vs. Drain Current**

**Capacitance**

**Gate Charge**

**TYPICAL CHARACTERISTICS** 25 °C unless noted

**On-Resistance vs. Junction Temperature**

**Source-Drain Diode Forward Voltage**
**THERMAL RATINGS**

**Drain Current vs. Case Temperature**

**Safe Operating Area**

**THERMAL RATINGS****Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Case**

**TO-220 FULLPAK**

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
e	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
Ø P	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
v	0.400	0.500	0.016	0.020

ECN: X09-0126-Rev. B, 26-Oct-09  
DWG: 5972

**Notes**

1. To be used only for process drawing.
2. These dimensions apply to all TO-220, FULLPAK leadframe versions 3 leads.
3. All critical dimensions should C meet  $C_{pk} > 1.33$ .
4. All dimensions include burrs and plating thickness.
5. No chipping or package damage.

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