带有 USB 接口，单端头戴式耳机输出和索尼和飞利浦数字接口 (S/PDIF) 输出的立体声音频数模转换器 (DAC)

查询样品: **PCM2704C**, **PCM2705C**, **PCM2706C**, **PCM2707C**

特性

- 片载 **USB** 接口：
  - 无需专用器件驱动器
  - 全速收发器
  - 完全与 **USB 2.0** 技术规格兼容
    - 具有 **USB** 音频类别支持的 **USB 1.1** 描述符
  - 经 **USB-IF** 认证
  - 部分可编程描述符
  - 用于回放的自适应同步传输
  - 总线供电或者自供电运行
- 采样速率：**32kHz**，**44.1kHz**，**48kHz**
- 带有 **12MHz** 时钟源的片载时钟生成器
- 单电源：
  - 总线供电时：**5V**，典型值 **(V_{BUS})**
  - 自供电时：**3.3V**，典型值
- **16** 位三角积分立体声 **DAC**
  - **5V**（总线供电），**3.3V**（自供电）时的模拟性能
    - 总谐波失真（**THD**）**+N**：自供电时，**0.006%** **R_L>10kΩ**
    - **THD+N**：**0.025%** **R_L=32Ω**
    - 信噪比 **(SNR)=98dB**
    - 动态范围：**98dB**
    - **P_O=12mW**，**R_L=32Ω**
  - 过采样数字滤波器
    - 通带纹波 **= ±0.04dB**
    - 抑制频带衰减 **= -50dB**
  - 单端电压输出
  - 包含模拟低通滤波器 **(LPF)**
- 多功能：
  - 多达 **8** 个人机接口器件 **(HID)** 接口（取决于模型类型和设置）
  - 挂起标志
  - 带有串行复制管理系统 **(SCMS)** 的 **S/PDIF** 输出
  - 外部 **ROM** 接口 **(PCM2704C/6C)**
  - 串行编程接口 **(PCM2705C/7C)**
  - **I^{2}S™** 接口（在 **PCM2706C/7C** 上可选）
- 封装：
  - **28** 引脚缩小型小外形尺寸封装 **(SSOP)(PCM2704C/5C)**
  - **32** 引脚薄型四方扁平封装 **(TQFP)(PCM2706C/7C)**

应用范围

- **USB** 头戴式耳机
- **USB** 音频扬声器
- **USB CRT/LCD** 显示器
- **USB** 音频接口盒
- 支持 **USB** 的消费类音频产品

说明

PCM2704C/5C/6C/7C 是具有 USB 2.0 接口的 TI 单芯片 USB 立体声音频模数转换器 (DAC) 兼容的全速协议控制器和 S/PDIF。 USB 协议控制器的运行无需软件代码支持，但是可使用一个外部 ROM (PCM2705C/7C) 或者串行外设接口 (SPI) (PCM2705C/7C) 来修改一些区域（例如，销售商 ID / 产品 ID）中的 USB 描述符。 PCM2704C/5C/6C/7C 还采用 SpAct™ 架构，这个 TI 所特有的系统能够从 USB 数据包中恢复音频时钟。 带有 SpAct 的片载模拟锁相环 (PLL) 能够在保证低时钟抖动的情况下启用回放。

English Data Sheet: SBFS036

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

For the most current specification and package information, refer to the Package Option Addendum located at the end of this data sheet or see the respective device product folders at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range unless otherwise noted.

		VALUE	UNIT
Supply voltage	V_{BUS}	–0.3 to 6.5	V
	V_{CCP}, V_{CCL}, V_{CCR}, V_{DD}	–0.3 to 4	V
Supply voltage differences	V_{CCP}, V_{CCL}, V_{CCR}, V_{DD}	±0.1	V
Ground voltage differences	PGND, AGNDL, AGNDR, DGND, ZGND	±0.1	V
Digital input voltage	HOST	–0.3 to 6.5	V
	D+, D–, HID0/MS, HID1/MC, HID2/MD, XTI, XTO, DOUT, $\overline{\text{SSPND}}$, CK, DT, PSEL, FSEL, TEST, TEST0, TEST1, FUNC0, FUNC1, FUNC2, FUNC3	–0.3 to (V_{DD} + 0.3) < 4	V
Analog input voltage	V_{COM}	–0.3 to (V_{CCP} + 0.3) < 4	V
	V_{OUT}R	–0.3 to (V_{CCR} + 0.3) < 4	V
	V_{OUT}L	–0.3 to (V_{CCL} + 0.3) < 4	V
Input current (any pins except supplies)		±10	mA
Ambient temperature under bias		–40 to +125	°C
Storage temperature		–55 to +150	°C
Junction temperature		+150	°C
Package temperature (IR reflow, peak)		+260	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range.

		MIN	NOM	MAX	UNIT
Supply voltage	V_{BUS}	4.35	5	5.25	V
	V_{CCP}, V_{CCL}, V_{CCR}, V_{DD}	3	3.3	3.6	
Digital input logic level			TTL-compatible		
Digital input clock frequency		11.994	12	12.006	MHz
Analog output load resistance		16	32		Ω
Analog output load capacitance				100	pF
Digital output load capacitance				20	pF
Operating free-air temperature, T_A		–25		85	°C

ELECTRICAL CHARACTERISTICS

All specifications at T_A = +25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, and 16-bit data (unless otherwise noted).

PARAMETER			TEST CONDITIONS	PCM2704CDB, PCM2705CDB PCM2706CPJT, PCM2707CPJT MIN	TYP	MAX	UNIT
DIGITAL INPUT/OUTPUT							
	Host interface			Apply USB revision 1.1, full-speed			
	Audio data format			USB isochronous data format			
INPUT LOGIC							
V_{IH}	Input logic level			2		3.3	V_{DC}
V_{IL}				–0.3		0.8	
V_{IH} (1)				2		5.5	
V_{IL} (1)				–0.3		0.8	
I_{IH} (2)	Input logic current		V_{IN} = 3.3 V			±10	μA
I_{IL} (2)			V_{IN} = 0 V			±10	
I_{IH}			V_{IN} = 3.3 V		65	100	
I_{IL}			V_{IN} = 0 V			±10	
OUTPUT LOGIC							
V_{OH} (3)	Output logic level		I_{OH} = –2 mA	2.8			V_{DC}
V_{OL} (3)			I_{OL} = 2 mA			0.3	
V_{OH}			I_{OH} = –2 mA	2.4			
V_{OL}			I_{OL} = 2 mA			0.4	
CLOCK FREQUENCY							
	Input clock frequency, XTI			11.994	12	12.006	MHz
f_S	Sampling frequency				32, 44.1, 48		kHz
DAC CHARACTERISTICS							
	Resolution				16		Bits
	Audio data channel				1, 2		Channel
DC ACCURACY							
	Gain mismatch, channel-to-channel				±2	±8	% of FSR
	Gain error				±2	±8	% of FSR
	Bipolar zero error				±3	±6	% of FSR
DYNAMIC PERFORMANCE (4)							
THD+N	Total harmonic distortion + noise	Line (5)	R_L > 10 kΩ, self-powered, V_{OUT} = 0 dB		0.006	0.01	%
			R_L > 10 kΩ, bus-powered, V_{OUT} = 0 dB		0.012	0.02	%
		Headphone	R_L = 32 Ω, self-/ bus-powered, V_{OUT} = 0 dB		0.025		%
THD+N	Total harmonic distortion + noise		V_{OUT} = –60 dB		2		%
	Dynamic range		EIAJ, A-weighted	90	98		dB
SNR	Signal-to-noise ratio		EIAJ, A-weighted	90	98		dB
	Channel separation			60	70		dB

(1) HOST pin.
(2) D+, D–, HOST, TEST, TEST0, TEST1, DT, PSEL, FSEL, XTI pins.
(3) FUNC0, FUNC1, FUNC2 pins.
(4) f_{IN} = 1 kHz, using the System Two™ Cascade audio measurement system by Audio Precision™ in RMS mode with a 20-kHz low-pass filter (LPF) and 400-Hz high-pass filter (HPF).
(5) THD+N performance varies slightly, depending on the effective output load, including dummy load R7, R8 in Figure 34.

ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, and 16-bit data (unless otherwise noted).

PARAMETER		TEST CONDITIONS	PCM2704CDB, PCM2705CDB PCM2706CPJT, PCM2707CPJT			UNIT
			MIN	TYP	MAX	
ANALOG OUTPUT						
Output voltage				0.55 V_{CCL}, 0.55 V_{CCR}		V_{PP}
Center voltage				0.5 V_{CCP}		V
Load impedance	Line	AC-coupling	10			kΩ
	Headphone	AC-coupling	16	32		Ω
LPF frequency response		–3 dB		140		kHz
		f = 20 kHz		–0.1		dB
DIGITAL FILTER PERFORMANCE						
Passband					0.454 f_S	Hz
Stop band			0.546 f_S			Hz
Passband ripple					±0.04	dB
Stop band attenuation			–50			dB
Delay time				20/f_S		s
POWER SUPPLY REQUIREMENTS						
Voltage range	V_{BUS}	Bus-powered	4.35	5	5.25	V_{DC}
	V_{CCP}, V_{CCL}, V_{CCR}, V_{DD}	Self-powered	3	3.3	3.6	
Supply current	Line	DAC operation		23	30	mA
	Headphone	DAC operation (R_L = 32 Ω)		35	46	
	Line/headphone	Suspend mode (6)		150	190	μA
Power dissipation (self-powered)	Line	DAC operation		76	108	mW
	Headphone	DAC operation (R_L = 32 Ω)		116	166	
	Line/headphone	Suspend mode (6)		495	684	μW
Power dissipation (bus-powered)	Line	DAC operation		115	158	mW
	Headphone	DAC operation (R_L = 32 Ω)		175	242	
	Line/headphone	Suspend mode (6)		750	998	μW
Internal power-supply voltage (7)	V_{CCP}, V_{CCL}, V_{CCR}, V_{DD}	Bus-powered	3.2	3.35	3.5	V_{DC}
TEMPERATURE RANGE						
Operating temperature			–25		+85	°C

(6) In USB suspended state.
(7) V_{DD}, V_{CCP}, V_{CCL}, V_{CCR} pins. These pins work as output pins of internal power supply for bus-powered operation.

THERMAL INFORMATION

THERMAL METRIC(1)		PCM2704C, PCM2705C	UNITS
		DB	
		32 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	68.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	27.2	
θ_{JB}	Junction-to-board thermal resistance	29.5	
ψ_{JT}	Junction-to-top characterization parameter	2.7	
ψ_{JB}	Junction-to-board characterization parameter	29.1	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	

(1) 有关传统和全新热度量的更多信息，请参阅 *IC 封装热度量* 应用报告 （文献号：SPRA953）。

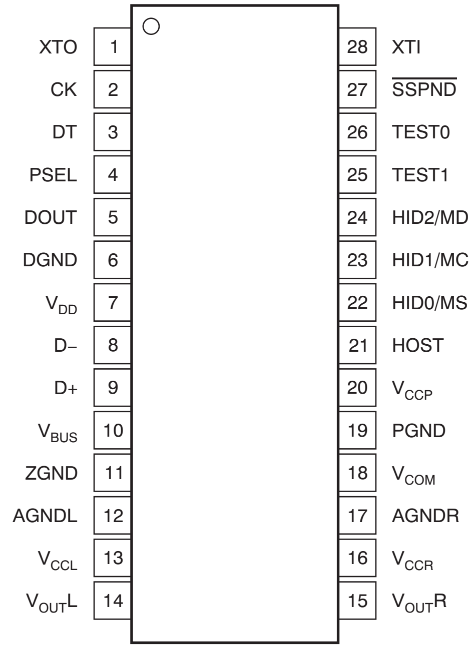
THERMAL INFORMATION

THERMAL METRIC(1)		PCM2706C, PCM2707C	UNITS
		PJT	
		32 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	TBD	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	TBD	
θ_{JB}	Junction-to-board thermal resistance	TBD	
ψ_{JT}	Junction-to-top characterization parameter	TBD	
ψ_{JB}	Junction-to-board characterization parameter	TBD	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	TBD	

(1) 有关传统和全新热度量的更多信息，请参阅 *IC 封装热度量* 应用报告 （文献号：SPRA953）。

DEVICE INFORMATION

PCM2704C, PCM2705C
DB PACKAGE
(TOP VIEW)



PCM2706C, PCM2707C
PJT PACKAGE
(TOP VIEW)

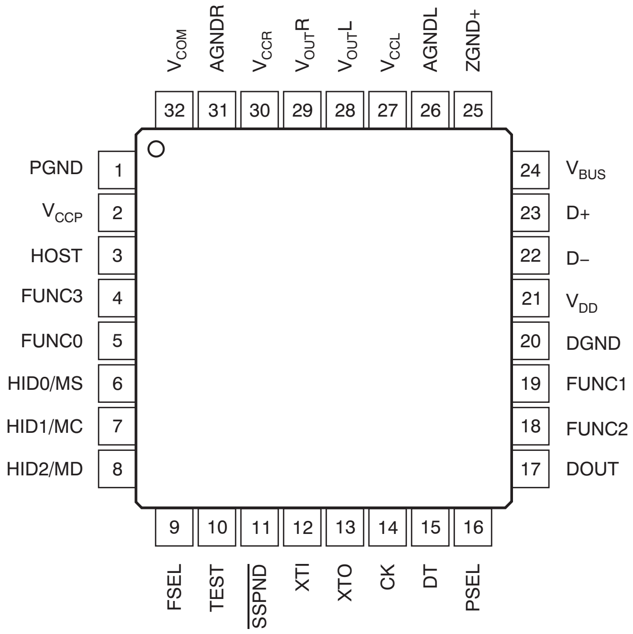


Table 1. Pin Descriptions: DB Package (PCM2704C/PCM2705C)

TERMINAL			
NAME	NO.	I/O	DESCRIPTION
AGNDL	12	—	Analog ground for headphone amplifier of L-channel
AGNDR	17	—	Analog ground for headphone amplifier of R-channel
CK	2	O	Clock output for external ROM (PCM2704C). Must be left open (PCM2705C).
D+	9	I/O	USB differential input/output plus(1)
D–	8	I/O	USB differential input/output minus(1)
DGND	6	—	Digital ground
DOUT	5	O	S/PDIF output
DT	3	I/O	Data input/output for external ROM (PCM2704C). Must be left open with pull-up resistor (PCM2705C).(1)
HID0/MS	22	I	HID key state input (mute), active high (PCM2704C). MS input (PCM2705C).(2)
HID1/MC	23	I	HID key state input (volume up), active high (PCM2704C). MC input (PCM2705C).(2)
HID2/MD	24	I	HID key state input (volume down), active high (PCM2704C). MD input (PCM2705C).(2)
HOST	21	I	Host detection during self-powered operation (connect to V_{BUS}). Max power select during bus-powered operation (low: 100 mA, high: 500 mA).(3)
PGND	19	—	Analog ground for DAC, OSC, and PLL
PSEL	4	I	Power source select (low: self-power, high: bus-power)(1)
$\overline{\text{SSPND}}$	27	O	Suspend flag, active low (low: suspend, high: operational)
TEST0	26	I	Test pin. Must be set high(1)
TEST1	25	I	Test pin. Must be set high(1)
V_{BUS}	10	—	Connect to USB power (V_{BUS}) for bus-powered operation. Connect to V_{DD} for self-powered operation.
V_{CCL}	13	—	Analog power supply for headphone amplifier of L-channel(4)
V_{CCP}	20	—	Analog power supply for DAC, OSC, and PLL(4)
V_{CCR}	16	—	Analog power supply for headphone amplifier of R-channel(4)
V_{COM}	18	—	Common voltage for DAC (V_{CCP}/2). Connect decoupling capacitor to PGND.
V_{DD}	7	—	Digital power supply(4)
V_{OUT}L	14	O	DAC analog output for L-channel
V_{OUT}R	15	O	DAC analog output for R-channel
XTI	28	I	Crystal oscillator input(1)
XTO	1	O	Crystal oscillator output
ZGND	11	—	Ground for internal regulator

(1) LV-TTL level.
(2) LV-TTL level with internal pulldown.
(3) LV-TTL level, 5-V tolerant.
(4) Connect decoupling capacitor to GND. Supply 3.3 V for self-powered applications.

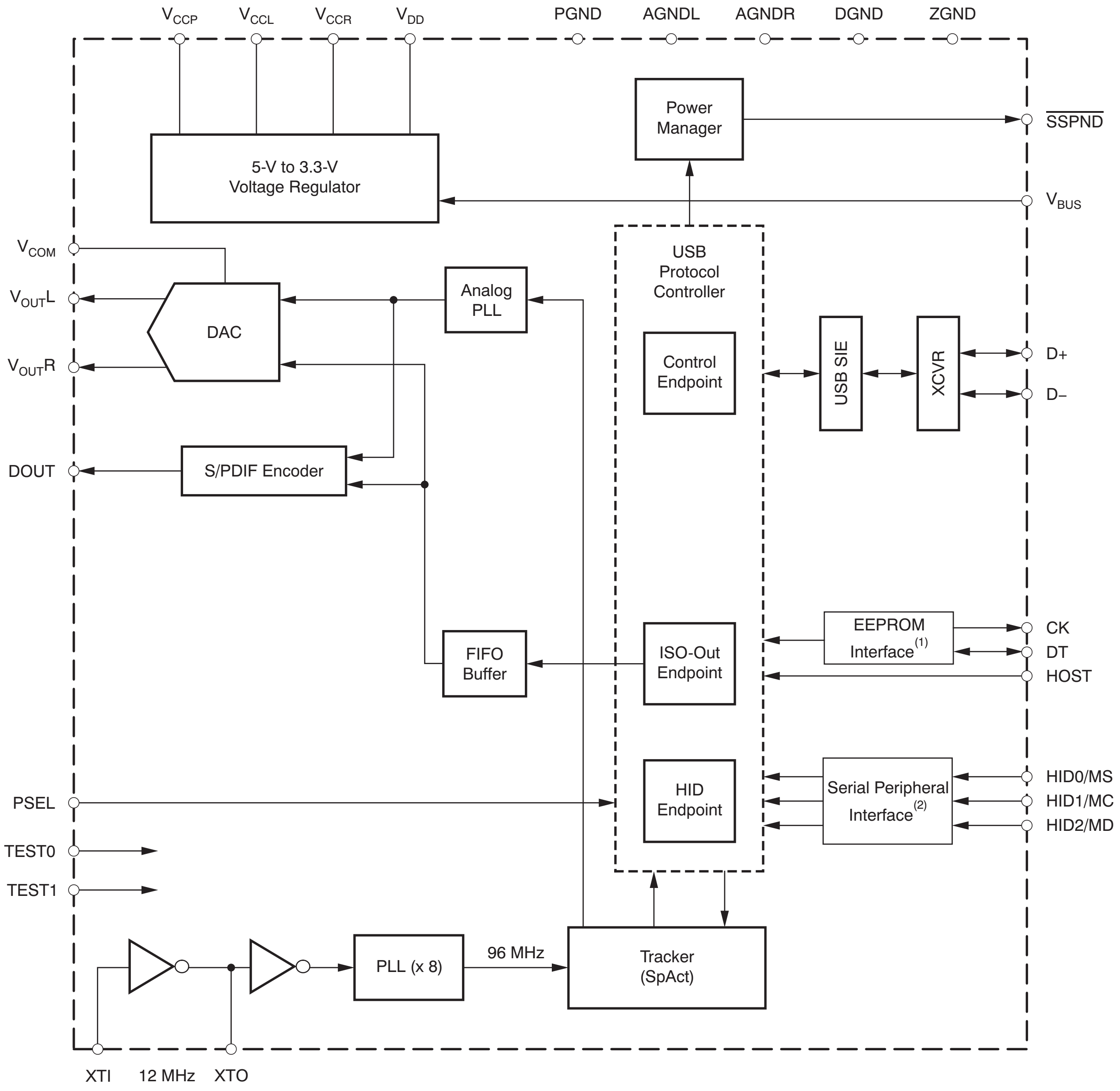
Table 2. Pin Descriptions: PJT Package (PCM2706C/PCM2707C)

TERMINAL			
NAME	NO.	I/O	DESCRIPTION
AGNDL	26	—	Analog ground for headphone amplifier of L-channel
AGNDR	31	—	Analog ground for headphone amplifier of R-channel
CK	14	O	Clock output for external ROM (PCM2706C). Must be left open (PCM2707C).
D+	23	I/O	USB differential input/output plus(1)
D–	22	I/O	USB differential input/output minus(1)
DGND	20	—	Digital ground
DOUT	17	O	S/PDIF output/I^{2}S data output
DT	15	I/O	Data input/output for external ROM (PCM2706C). Must be left open with pull-up resistor (PCM2707C).(1)
FSEL	9	I	Function select (low: I^{2}S data output, high: S/PDIF output)(1)
FUNC0	5	I/O	HID key state input (next track), active high (FSEL = 1). I^{2}S LR clock output (FSEL = 0).(2)
FUNC1	19	I/O	HID key state input (previous track), active high (FSEL = 1). I^{2}S bit clock output (FSEL = 0).(2)
FUNC2	18	I/O	HID key state input (stop), active high (FSEL = 1). I^{2}S system clock output (FSEL = 0).(2)
FUNC3	4	I	HID key state input (play/pause), active high (FSEL = 1). I^{2}S data input (FSEL = 0).(2)
HID0/MS	6	I	HID key state input (mute), active high (PCM2706C). MS input (PCM2707C).(2)
HID1/MC	7	I	HID key state input (volume up), active high (PCM2706C). MC input (PCM2707C).(2)
HID2/MD	8	I	HID key state input (volume down), active high (PCM2706C). MD input (PCM2707C).(2)
HOST	3	I	Host detection during self-powered operation (connect to V_{BUS}). Max power select during bus-powered operation. (low: 100 mA, high: 500 mA).(3)
PGND	1	—	Analog ground for DAC, OSC, and PLL
PSEL	16	I	Power source select (low: self-power, high: bus-power)(1)
$\overline{\text{SSPND}}$	11	O	Suspend flag, active low (low: suspend, high: operational)
TEST	10	I	Test pin. Must be set high(1)
V_{BUS}	24	—	Connect to USB power (V_{BUS}) for bus-powered operation. Connect to V_{DD} for self-powered operation.
V_{CCL}	27	—	Analog power supply for headphone amplifier of L-channel(4)
V_{CCP}	2	—	Analog power supply for DAC, OSC, and PLL(4)
V_{CCR}	30	—	Analog power supply for headphone amplifier of R-channel(4)
V_{COM}	32	—	Common voltage for DAC (V_{CCP}/2). Connect decoupling capacitor to PGND.
V_{DD}	21	—	Digital power supply(4)
V_{OUT}L	28	O	DAC analog output for L-channel
V_{OUT}R	29	O	DAC analog output for R-channel
XTI	12	I	Crystal oscillator input(1)
XTO	13	O	Crystal oscillator output
ZGND	25	—	Ground for internal regulator

(1) LV-TTL level.
(2) LV-TTL level with internal pulldown.
(3) LV-TTL level, 5-V tolerant.
(4) Connect decoupling capacitor to GND. Supply 3.3 V for self-powered applications.

FUNCTIONAL BLOCK DIAGRAMS

PCM2704C/PCM2705C

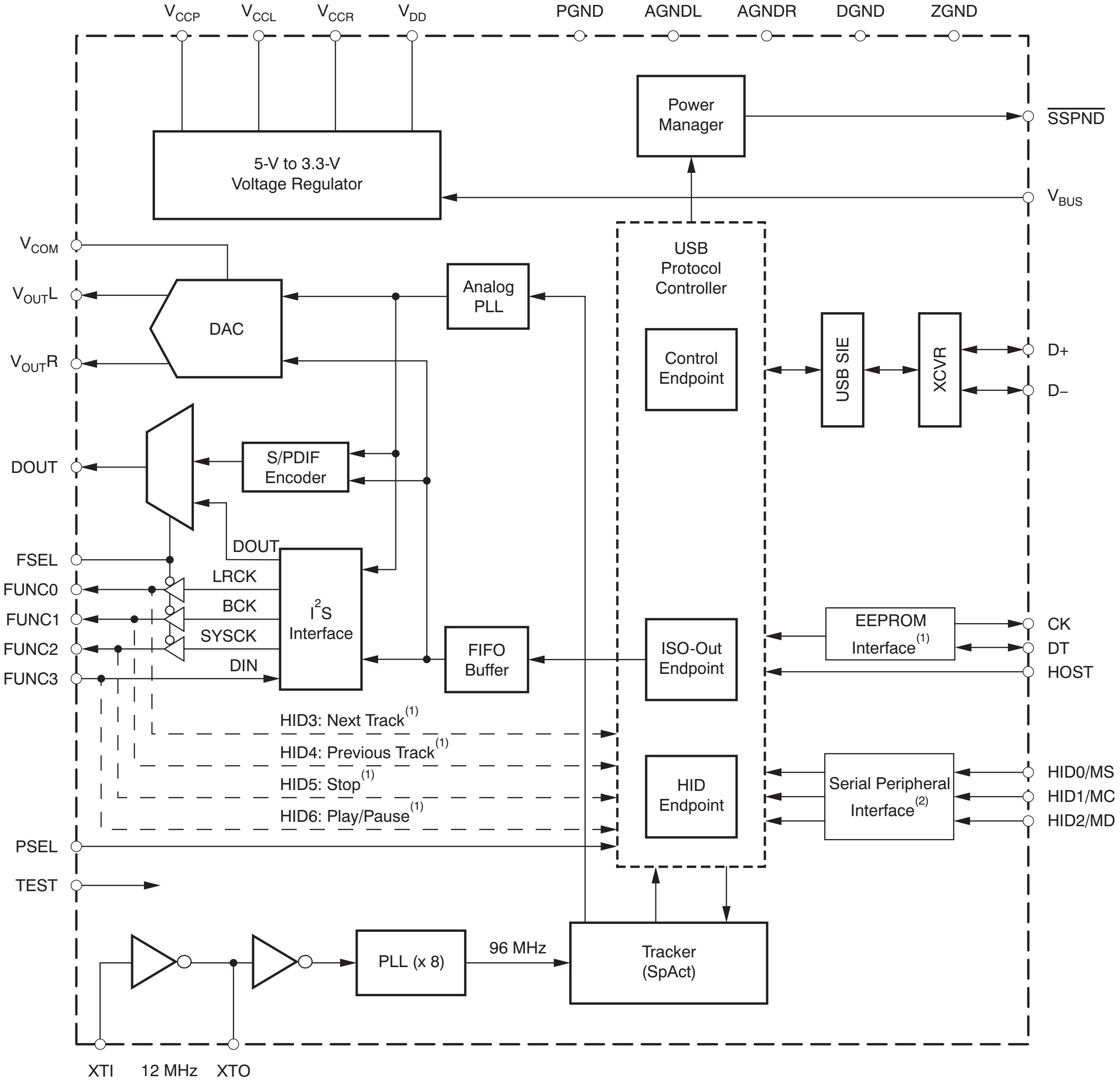


(1) Applies to PCM2704CDB.

(2) Applies to PCM2705CDB.

Figure 1.

PCM2706C/PCM2707C



(1) Applies to PCM2706CPJT.

(2) Applies to PCM2707CPJT.

Figure 2.

TYPICAL CHARACTERISTICS: INTERNAL FILTER

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data (unless otherwise noted).

DAC Digital Interpolation Filter Frequency Response

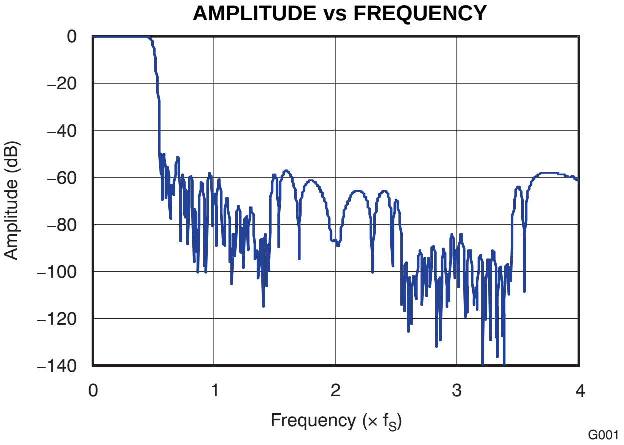


Figure 3. Frequency Response

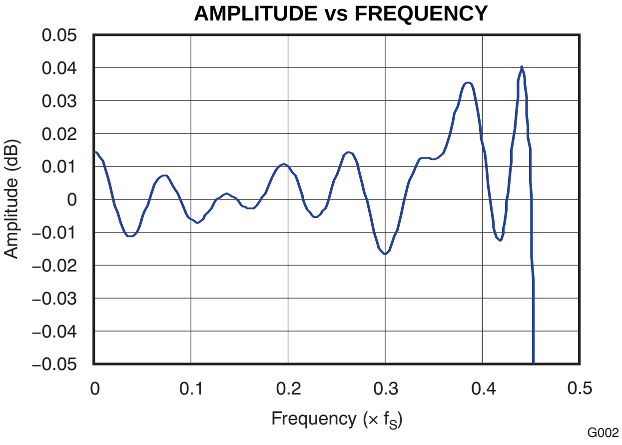


Figure 4. Passband Ripple

DAC Analog Low-Pass Filter Frequency Response

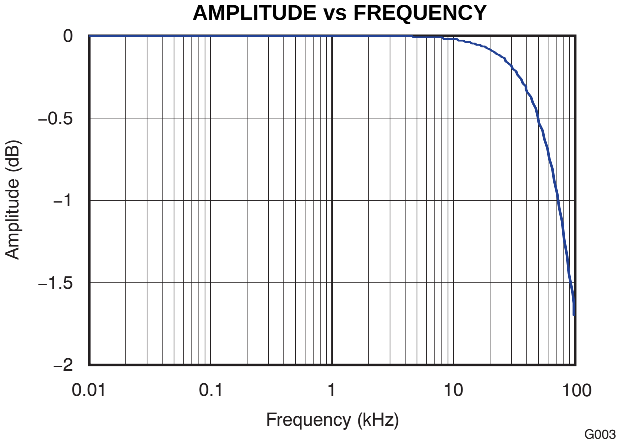


Figure 5. Passband Characteristics

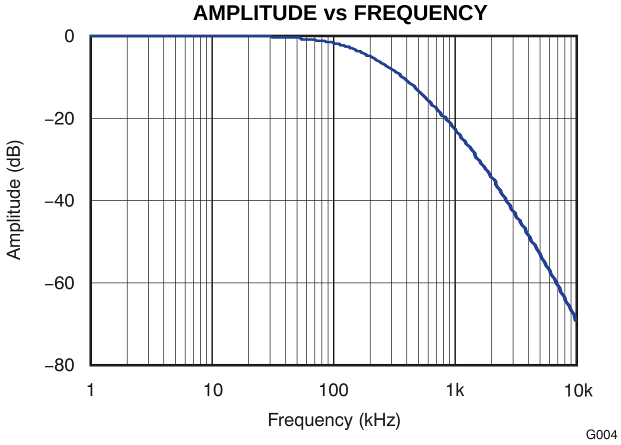


Figure 6. Stop Band Characteristics

TYPICAL CHARACTERISTICS: GENERAL

All specifications at T_A = +25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, and 16-bit data (unless otherwise noted).

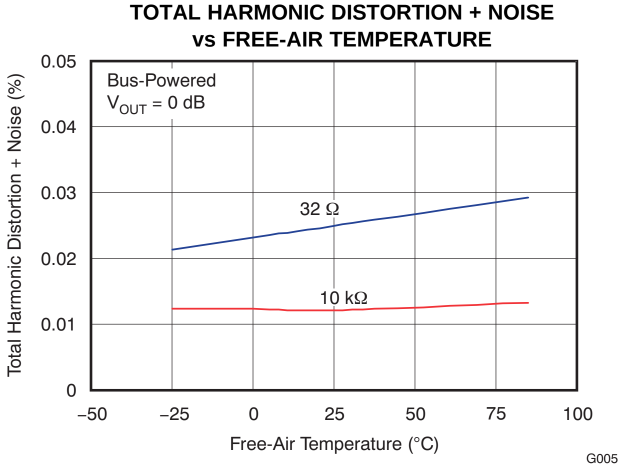

TOTAL HARMONIC DISTORTION + NOISE vs FREE-AIR TEMPERATURE

Figure 7.

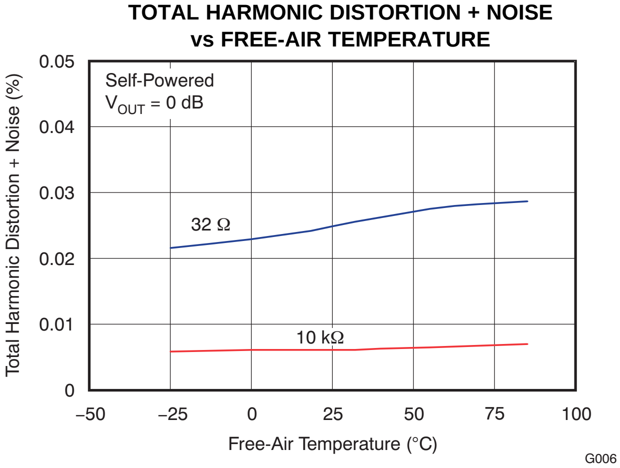

TOTAL HARMONIC DISTORTION + NOISE vs FREE-AIR TEMPERATURE

Figure 8.

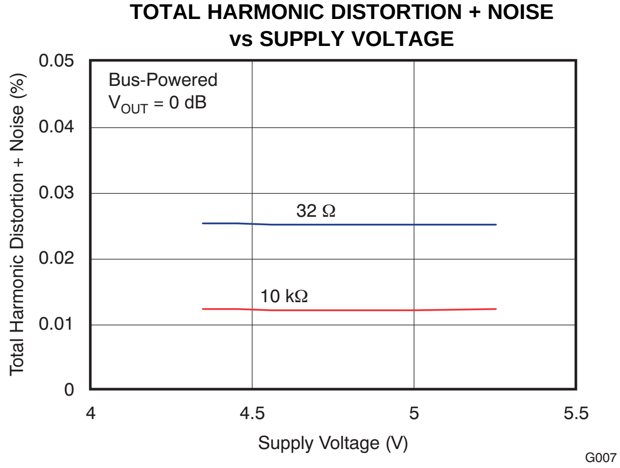

TOTAL HARMONIC DISTORTION + NOISE vs SUPPLY VOLTAGE

Figure 9.

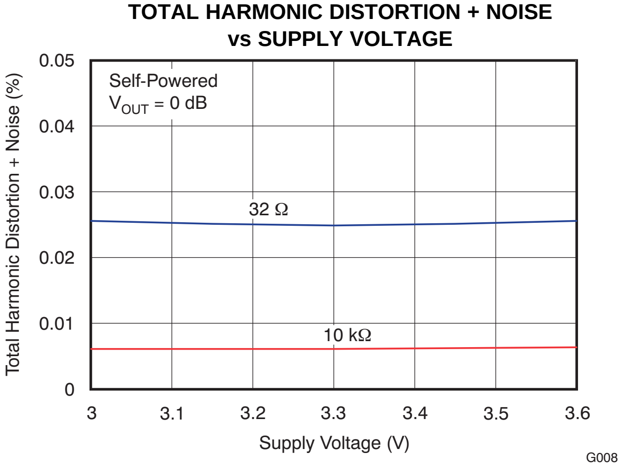

TOTAL HARMONIC DISTORTION + NOISE vs SUPPLY VOLTAGE

Figure 10.

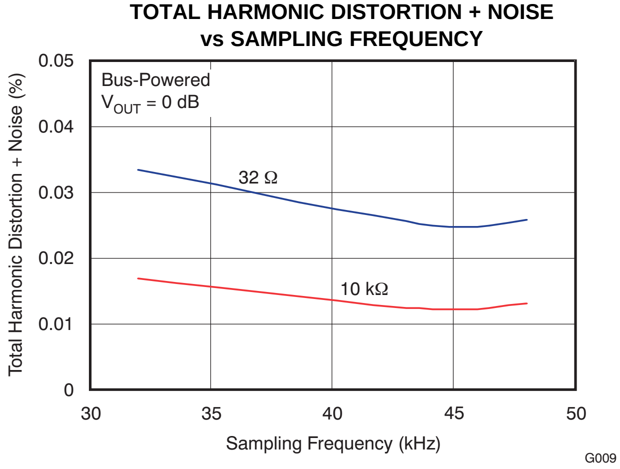

TOTAL HARMONIC DISTORTION + NOISE vs SAMPLING FREQUENCY

Figure 11.

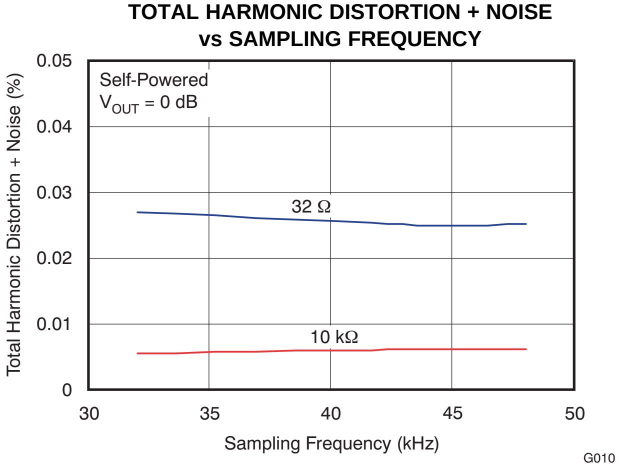

TOTAL HARMONIC DISTORTION + NOISE vs SAMPLING FREQUENCY

Figure 12.

TYPICAL CHARACTERISTICS: GENERAL (continued)

All specifications at $T_A = +25°C$, $V_{BUS} = 5$ V, $f_S = 44.1$ kHz, $f_{IN} = 1$ kHz, and 16-bit data (unless otherwise noted).

DYNAMIC RANGE and SNR
vs FREE-AIR TEMPERATURE

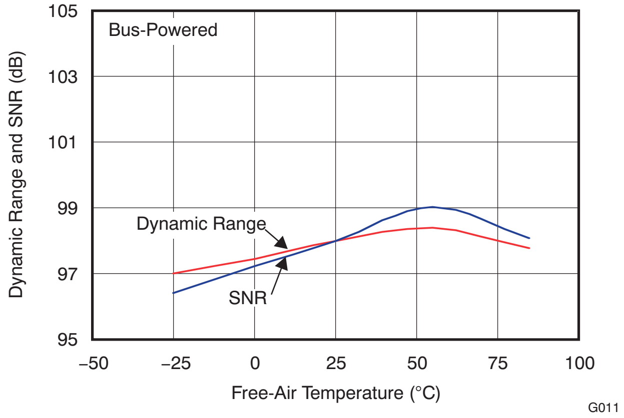


Figure 13.

DYNAMIC RANGE and SNR
vs FREE-AIR TEMPERATURE

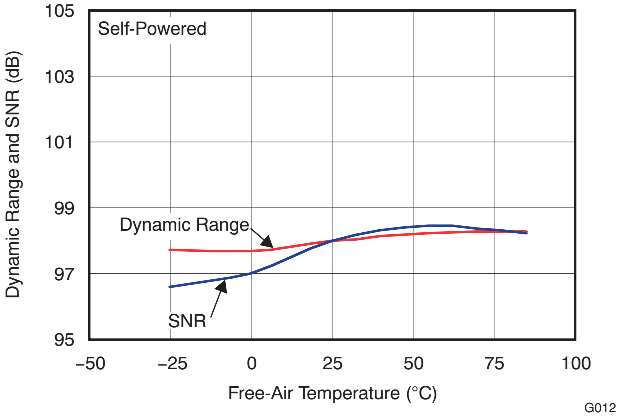


Figure 14.

DYNAMIC RANGE and SNR
vs SUPPLY VOLTAGE

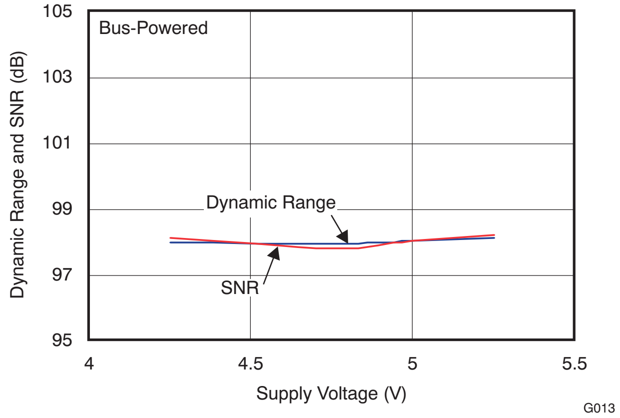


Figure 15.

DYNAMIC RANGE and SNR
vs SUPPLY VOLTAGE

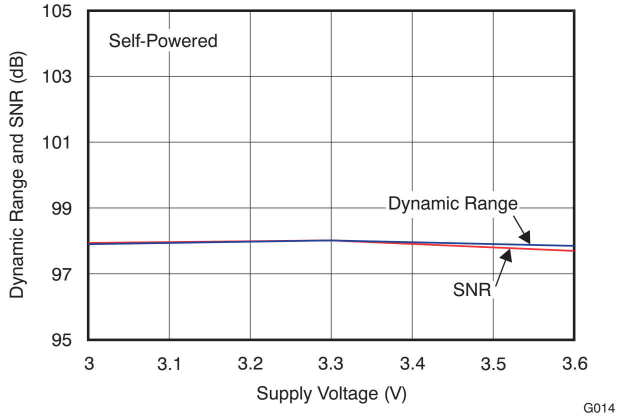


Figure 16.

DYNAMIC RANGE and SNR
vs SAMPLING FREQUENCY

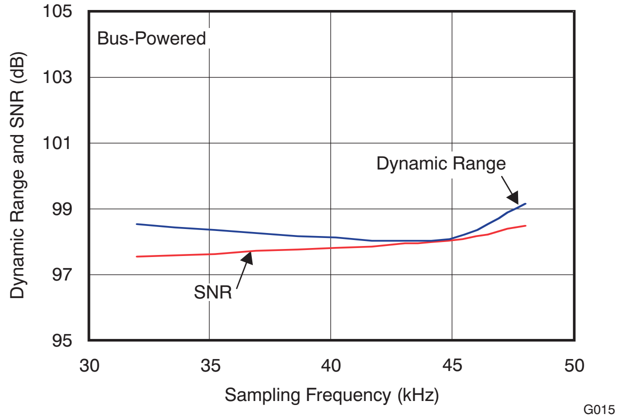


Figure 17.

DYNAMIC RANGE and SNR
vs SAMPLING FREQUENCY

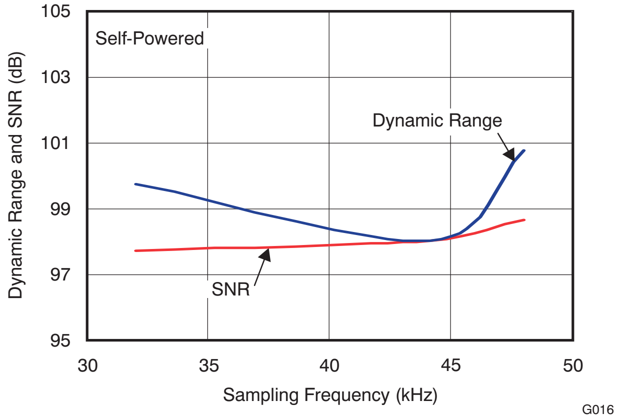


Figure 18.

TYPICAL CHARACTERISTICS: GENERAL (continued)

All specifications at T_A = +25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, and 16-bit data (unless otherwise noted).

SUSPEND CURRENT
vs SUPPLY VOLTAGE

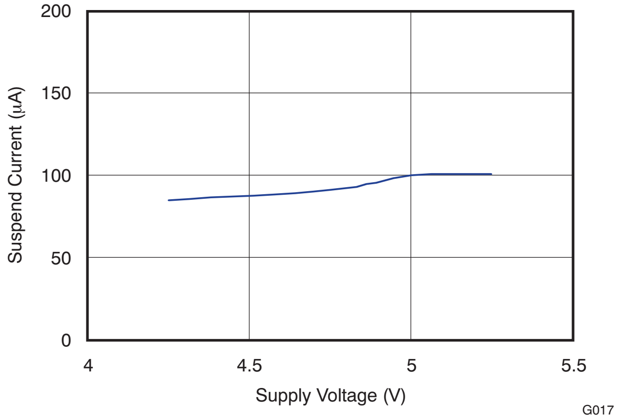


Figure 19.

SUSPEND CURRENT
vs FREE-AIR TEMPERATURE

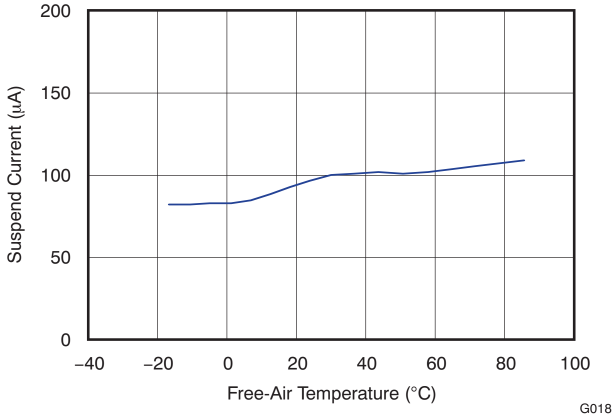


Figure 20.

AMPLITUDE vs FREQUENCY

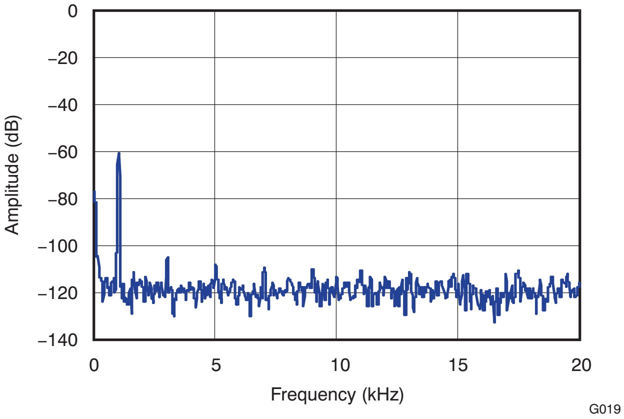


Figure 21. Output Spectrum (–60 dB, N = 8192)

AMPLITUDE vs FREQUENCY

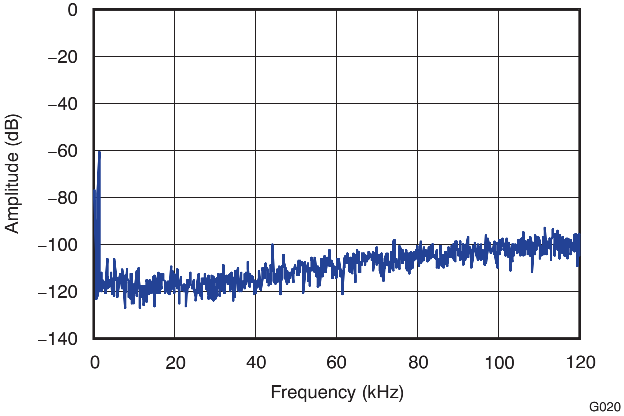


Figure 22. Output Spectrum (–60 dB, N = 8192)

DETAILED DESCRIPTION

Clock and Reset

For both USB and audio functions, the PCM2704C/5C/6C/7C require a 12-MHz (±500 ppm) clock that can be generated by the onboard oscillator using a 12-MHz crystal resonator. The 12-MHz crystal resonator must be connected to the XTI pin (pin 28 for the PCM2704C/5C, pin 12 for the PCM2706C/7C) and the XTO pin (pin 1 for the PCM2704C/5C, pin 13 for the PCM2706C/7C) with one large (1-MΩ) resistor and two small capacitors; the capacitance of these components depends on the specified load capacitance of the crystal resonator. An external clock can be supplied from XTI (pin 28 for the PCM2704C/5C, pin 12 for the PCM2706C/7C). If an external clock is supplied, XTO (pin 1 for the PCM2704C/5C, pin 13 for the PCM2706C/7C) must be left open. No clock disabling pin is provided; therefore, it is not recommended to use the external clock supply. $\overline{\text{SSPND}}$ (pin 27 for the PCM2704C/5C, pin 11 for the PCM2706C/7C) cannot use clock disabling.

The PCM2704C/5C/6C/7C have an internal power-on reset circuit, and it works automatically when V_{DD} (pin 7 for the PCM2704C/5C, pin 21 for the PCM2706C/7C) exceeds 2-V typical (1.6 V to 2.4 V), which is equivalent to V_{BUS} (pin 10 for the PCM2704C/5C, pin 24 for the PCM2706C/7C) exceeding 3-V typical for bus-powered applications. Approximately 700 μs is required until an internal reset release occurs.

Operation Mode Selection

The PCM2704C/5C/6C/7C have the following mode-select pins.

Power Configuration Select/Host Detection

PSEL (pin 4 for the PCM2704C/5C, pin 16 for the PCM2706C/7C) is dedicated to selecting the power source. This selection affects the configuration descriptor. While in bus-powered operation, the maximum power consumption from V_{BUS} is determined by the HOST pin (pin 21 for the PCM2704C/5C, pin 3 for the PCM2706C/7C). For self-powered operation, the HOST pin must be connected to V_{BUS} of the USB bus with a pulldown resistor to detect attach and detach. (To avoid excessive suspend current, the pulldown should be a high-value resistor.) Table 3 summarizes the power configuration select options.

Table 3. Power Configuration Select

PSEL	DESCRIPTION
0	Self-powered
1	Bus-powered
HOST	**DESCRIPTION**
0	Detached from USB (self-powered)/100 mA (bus-powered)
1	Attached to USB (self-powered)/500 mA (bus-powered)

Function Select (PCM2706C/7C Only)

FSEL (pin 9) determines the function of the FUNC0–FUNC3 pins (pins 4, 5, 18, and 19) and DOUT (pin 17). When the I^2S interface is required, FSEL must be low. Otherwise, FSEL must be high. Table 4 lists the functionality of the FUNC0-FUNC3 pins, based on the FSEL pin.

Table 4. Function Select

FSEL	DOUT	FUNC0	FUNC1	FUNC2	FUNC3
0	Data out (I^2S)	LRCK (I^2S)	BCK (I^2S)	SYSCK (I^2S)	Data in (I^2S)
1	S/PDIF data	Next track (HID) (1)	Previous track (HID) (1)	Stop (HID) (1)	Play/pause (HID) (1)

(1) Valid on the PCM2706C only; no function assigned on the PCM2707C.

USB Interface

Control data and audio data are transferred to the PCM2704C/5C/6C/7C via the D+ pin (pin 9 for the PCM2704C/5C, pin 23 for the PCM2706C/7C) and D– pin (pin 8 for the PCM2704C/5C, pin 22 for the PCM2706C/7C). D+ should be pulled up with a 1.5-kΩ (±5%) resistor. To avoid back voltage in self-powered operation, the device must not provide power to the pull-up resistor on D+ while V_{BUS} of the USB port is inactive.

All data to/from the PCM2704C/5C/6C/7C are transferred at full speed. The information shown in Table 5 is provided in the device descriptor. Some parts of the device descriptor can be modified through external ROM (PCM2704C/6C) or SPI™ (PCM2705C/7C).

Table 5. Device Descriptor

DEVICE DESCRIPTOR	DESCRIPTION
USB revision	1.1 compliant
Device class	0x00 (device defined interface level)
Device subclass	0x00 (not specified)
Device protocol	0x00 (not specified)
Max packet size for endpoint 0	8 bytes
Vendor ID	0x08BB (default value, can be modified)
Product ID	0x27C4/0x27C5/0x27C6/0x27C7 (These values correspond to the model number, and the value can be modified.)
Device release number	1.0 (0x0100)
Number of configurations	1
Vendor strings	BurrBrown from Texas Instruments (default value, can be modified)
Product strings	USB AUDIO DAC (default value, can be modified)
Serial number	Not supported

The information given in Table 6 is contained in the configuration descriptor. Some parts of the configuration descriptor can be modified through external ROM (PCM2704C/6C) or SPI (PCM2705C/7C).

Table 6. Configuration Descriptor

CONFIGURATION DESCRIPTOR	DESCRIPTION
Interface	Three interfaces
Power attribute	0x80 or 0xC0 (bus-powered or self-powered, depending on PSEL; no remote wake up. This value can be modified.)
Max power	0x0A, 0x32, or 0xFA (20 mA for self-powered, 100 mA or 500 mA for bus-powered, depending on PSEL and HOST. This value can be modified.)

The information listed in Table 7 is contained in the string descriptor. Some parts of the string descriptor can be modified through external ROM (PCM2704C/6C) or SPI (PCM2705C/7C).

Table 7. String Descriptor

STRING DESCRIPTOR	DESCRIPTION
#0	0x0409
#1	BurrBrown from Texas Instruments (default value, can be modified)
#2	USB AUDIO DAC (default value, can be modified)

Device Configuration

Figure 23 illustrates the USB audio function topology. The PCM2704C/5C/6C/7C have three interfaces. Each interface is enabled by different alternative settings.

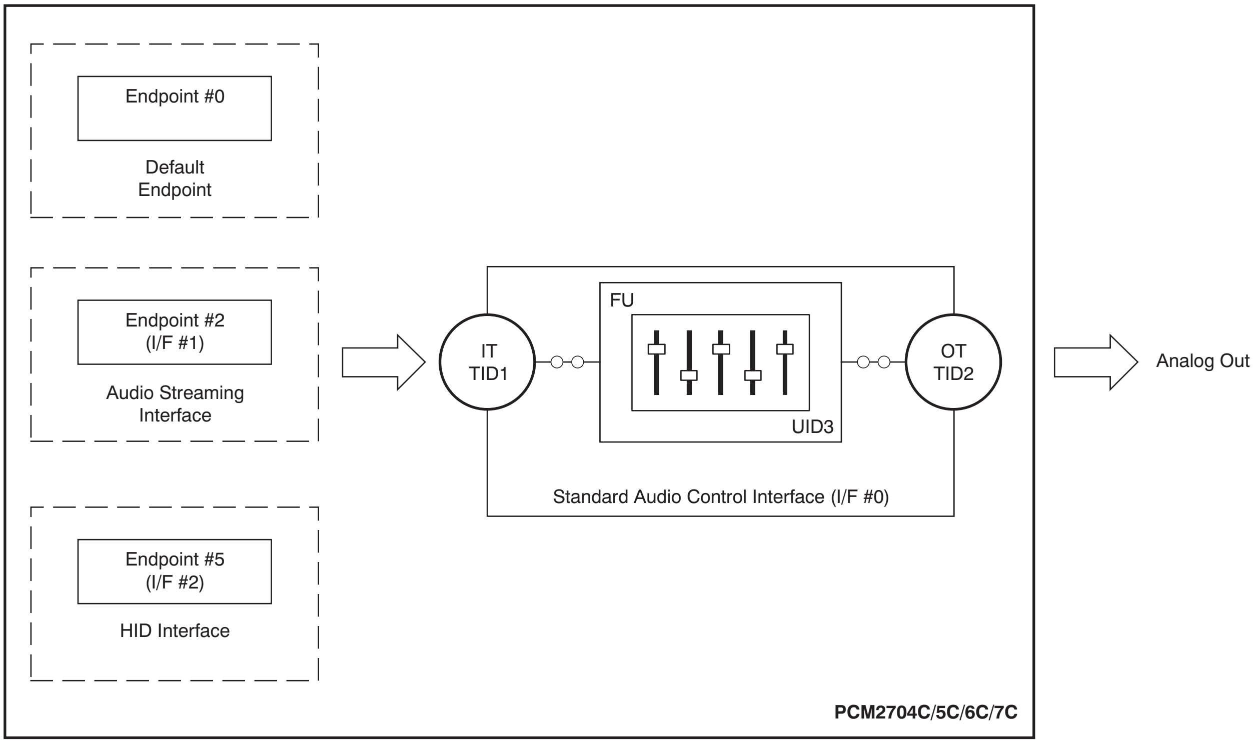


Figure 23. USB Audio Function Topology

Interface #0 (Default/Control Interface)

Interface #0 is the control interface. Setting #0 is the only possible setting for interface #0. Setting #0 describes the standard audio control interface. The audio control interface consists of a terminal. The PCM2704C/5C/6C/7C have three terminals:

- Input terminal (IT #1) for isochronous-out stream
- Output terminal (OT #2) for audio analog output
- Feature unit (FU #3) for DAC digital attenuator

Input terminal #1 is defined as a USB stream (terminal type 0x0101). Input terminal #1 can accept two-channel audio streams consisting of left and right channels. Output terminal #2 is defined as a speaker (terminal type 0x0301). Feature unit #3 supports these sound control features:

- Volume control
- Mute control

The built-in digital volume controller can be manipulated by an audio-class-specific request from 0 dB to –64 dB in steps of 1 dB. Changes are made by incrementing or decrementing one step (that is, 1 dB) for every $1/f_S$ time interval, until the volume level reaches the requested value. Each channel can be set to a separate value. The master volume control is not supported. A request to the master volume is stalled and ignored. The built-in digital mute controller can be manipulated by an audio-class-specific request. A master mute control request is acceptable. A mute control request to an individual channel is stalled and ignored. The digital volume control does not affect either the S/PDIF or I^2S outputs (PCM2706C/7C only).

Interface #1 (Isochronous-Out Interface)

Interface #1 is for the audio-streaming data-out interface. Interface #1 has the alternative settings described in Table 8. Alternative setting #0 is the zero-bandwidth setting. All other alternative settings are operational settings.

Table 8. Interface #1 Parameters

ALTERNATIVE SETTING	DATA FORMAT			TRANSFER MODE	SAMPLING RATE (kHz)
00	Zero bandwidth				
01	16-bit	Stereo	Twos complement (PCM)	Adaptive	32, 44.1, 48
02	16-bit	Mono	Twos complement (PCM)	Adaptive	32, 44.1, 48

Interface #2 (HID Interface)

Interface #2 is the interrupt-data-in interface. The HID consumer control device consists of interface #2. Alternative setting #0 is the only possible setting for interface #2.

On the HID device descriptor, eight HID items are reported for any model, in any configuration.

HID Items Reported

Basic HID Operation

Interface #2 can report these three key statuses for any model. These statuses can be set by the HID0–HID2 pins (PCM2704C/6C) or the SPI port (PCM2705C/7C).

- Mute (0xE2)
- Volume up (0xE9)
- Volume down (0xEA)

Extended HID Operation (PCM2705/6/7)

By using the FUNC0–FUNC3 pins (PCM2706C) or the SPI port (PCM2705C/7C), these additional conditions can be reported to the host.

- Play/Pause (0xCD)
- Stop (0xB7)
- Previous (0xB6)
- Next (0xB5)

Auxiliary HID Status Report (PCM2705C/7C)

One additional HID status can be reported to the host though the SPI port. This status flag is defined by SPI command or external ROM. This definition must be described as on the report descriptor with a three-byte usage ID. *AL A/V Capture* (0x0193) is assigned as the default value for this status flag.

Endpoints

The PCM2704C/5C/6C/7C has three endpoints:

- Control endpoint (EP #0)
- Isochronous-out audio data-stream endpoint (EP #2)
- HID endpoint (EP #5)

The control endpoint is a default endpoint. The control endpoint controls all functions of the PCM2704C/5C/6C/7C by standard USB request and USB audio-class-specific request from the host. The isochronous-out audio data-stream endpoint is an audio sink endpoint that receives the PCM audio data. The isochronous-out audio data-stream endpoint accepts the adaptive transfer mode. The HID endpoint is an interrupt-in endpoint. The HID endpoint reports HID status every 10 ms.

The HID endpoint is defined as a consumer-control device. The HID function is designed as an independent endpoint from the isochronous-out endpoint. This configuration means that the effect of HID operation depends on the host software. Typically, the HID function controls the primary audio-out device.

DAC

The PCM2704C/5C/6C/7C have a DAC that uses an oversampling technique with 128-f_S, second-order, multi-bit noise shaping. This technique provides extremely low quantization noise in the audio band, and the built-in analog low-pass filter removes the high-frequency components of the noise-shaping signal. The DAC analog outputs, $V_{OUT}L$ and $V_{OUT}R$, are sent through the headphone amplifier and can provide 12 mW at 32 Ω as well as 1.8 V_{PP} into a 10-kΩ load.

Digital Audio Interface: S/PDIF Output

The PCM2704C/5C/6C/7C employ S/PDIF output. Isochronous-out data from the host are encoded to S/PDIF output DOUT, as well as to DAC analog outputs $V_{OUT}L$ and $V_{OUT}R$. The interface format and timing follow the IEC-60958 standard. Monaural data are converted to the stereo format at the same data rate. S/PDIF output is not supported in the I^2S I/F enable mode. The implementation of this feature is optional. Note that it is the responsibility of the user to determine whether or not to implement this feature in the end application.

Channel Status Information

Channel status information is fixed, and includes consumer application, PCM mode, copyright, and digital/digital converter data. All other bits are fixed as 0s, except for the sample frequency, which is set automatically according to the data received through the USB.

Copyright Management

Digital audio data output always is encoded as original with SCMS control. Only one generation of digital duplication is allowed.

Digital Audio Interface: I^2S Interface Output (PCM2706C/7C)

The PCM2706C and PCM2707C can support the I^2S interface, which is enabled by the FSEL pin (pin 9). In the I^2S interface-enabled mode, pins 4, 18, 19, 5, and 17 are assigned as DIN, SYSCK, BCK, LRCK, and DOUT, respectively. These pins provide digital output/input data in the 16-bit I^2S format, which also is accepted by the internal DAC. I^2S interface format and timing are shown in Figure 24, Figure 25, and Figure 26. Table 9 and Table 10 list the audio interface timing and audio clock timing characteristics, respectively.

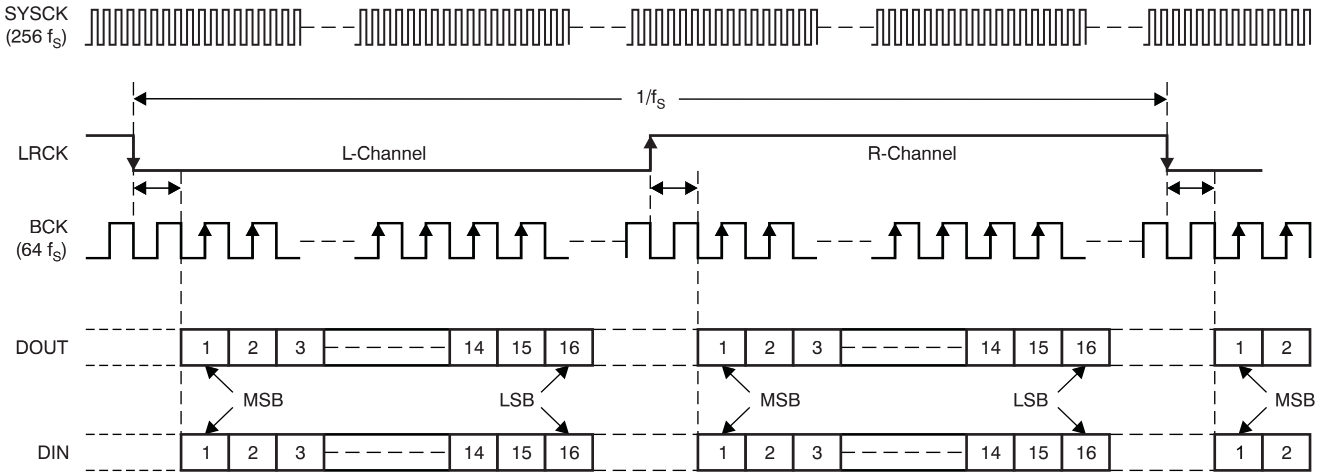


Figure 24. Audio Data Interface Format

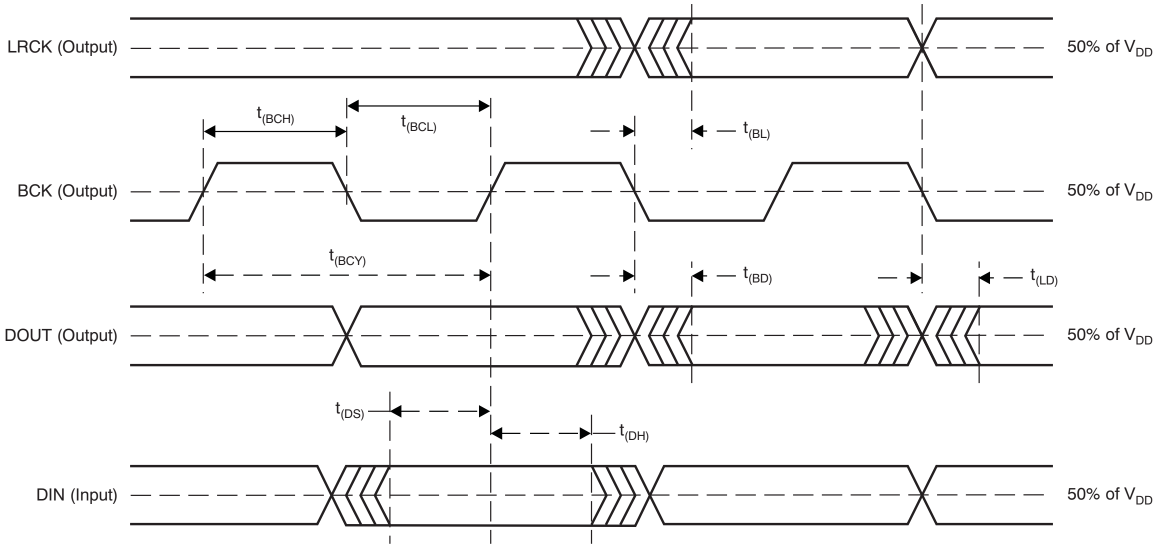


Figure 25. Audio Interface Timing

Table 9. Audio Interface Timing Characteristics(1)

SYMBOL	PARAMETER	MIN	MAX	UNIT
$t_{(BCY)}$	BCK pulse cycle time	300		ns
$t_{(BCH)}$	BCK pulse duration, high	100		ns
$t_{(BCL)}$	BCK pulse duration, low	100		ns
$t_{(BL)}$	LRCK delay time from BCK falling edge	–20	40	ns
$t_{(BD)}$	DOUT delay time from BCK falling edge	–20	40	ns
$t_{(LD)}$	DOUT delay time from LRCK edge	–20	40	ns
$t_{(DS)}$	DIN setup time	20		ns
$t_{(DH)}$	DIN hold time	20		ns

(1) Load capacitance of LRCK, BCK, and DOUT is 20 pF.

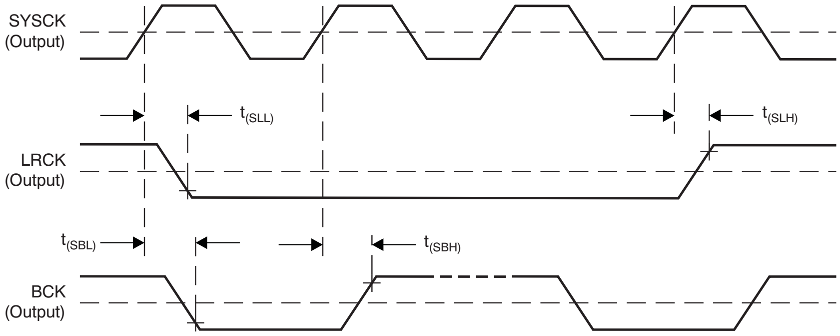


Figure 26. Audio Clock Timing

Table 10. Audio Clock Timing Characteristics(1)

SYMBOL	PARAMETER	MIN	MAX	UNIT
$t_{(SLL)}$, $t_{(SLH)}$	LRCK delay time from SYSCK rising edge	–5	10	ns
$t_{(SBL)}$, $t_{(SBH)}$	BCK delay time from SYSCK rising edge	–5	10	ns

(1) Load capacitance is 20 pF.

DESCRIPTOR DATA MODIFICATION

The descriptor data can be modified through the I^{2}C™ port by external ROM (PCM2704C/6C) or through the SPI port by an SPI host such as an MCU (PCM2705C/7C) under a particular configuration of the PSEL and HOST pins. Setting both the PSEL and the HOST pins high is necessary to modify the descriptor data; the D+ pin pull-up resistor must not be activated before programming the descriptor data through the external ROM or SPI port is completed. The descriptor data must be sent from an external ROM to the PCM2704C/6C or from the SPI host to the PCM2705C/7C in LSB first format, with a specified byte order. Additionally, the power attribute and max power contents must be consistent with the PSEL setting and the power usage from the USB V_{BUS} of the end application. Therefore, descriptor data modification in self-powered configuration (PSEL = low) is not supported.

External ROM Descriptor (PCM2704C/6C)

The PCM2704C/6C support an external ROM interface to override internal descriptors. Pin 3 (for the PCM2704C) or pin 15 (for the PCM2706C) is assigned as DT (serial data), and pin 2 (for the PCM2704C) or pin 14 (for the PCM2706C) is assigned as CK (serial clock) of the I^{2}C interface when using the external ROM descriptor. Descriptor data are transferred from the external ROM to the PCM2704C/6C through the I^{2}C interface the first time when the device is activate after a power-on reset. Before completing a read of the external ROM, the PCM2704C/6C reply with *NACK* for any USB command request from the host to the device itself. The descriptor data, which can be in the external ROM, must meet these parameters:

- String descriptors must be described in ANSI ASCII code (1 byte for each character).
- String descriptors are converted automatically to unicode strings for transmission to the host.
- The device address of the external ROM is fixed as 0xA0.

The data bits must be sent from LSB to MSB on the I^{2}C bus. This condition means that each byte of data must be stored with its bits in reverse order. A read operation is performed at a frequency of XTI/384 (approximately 30 kHz). The power attribute and max power contents must be consistent with the end application circuit configuration (the PSEL setting and the actual power usage from V_{BUS} of the USB connector); otherwise, it may cause improper or unexpected PCM2704C/6C operation.

The data must be stored from address 0x00 and must consist of 57 bytes, according to the parameters listed below:

- Vendor ID (2 bytes)
- Product ID (2 bytes)
- Product string (16 bytes in ANSI ASCII code)
- Vendor string (32 bytes in ANSI ASCII code)
- Power attribute (1 byte)
- Max power (1 byte)
- Auxiliary HID usage ID in report descriptor (3 bytes)

Figure 27 illustrates the timing for an external ROM read operation. The timing characteristics are summarized in Table 11.

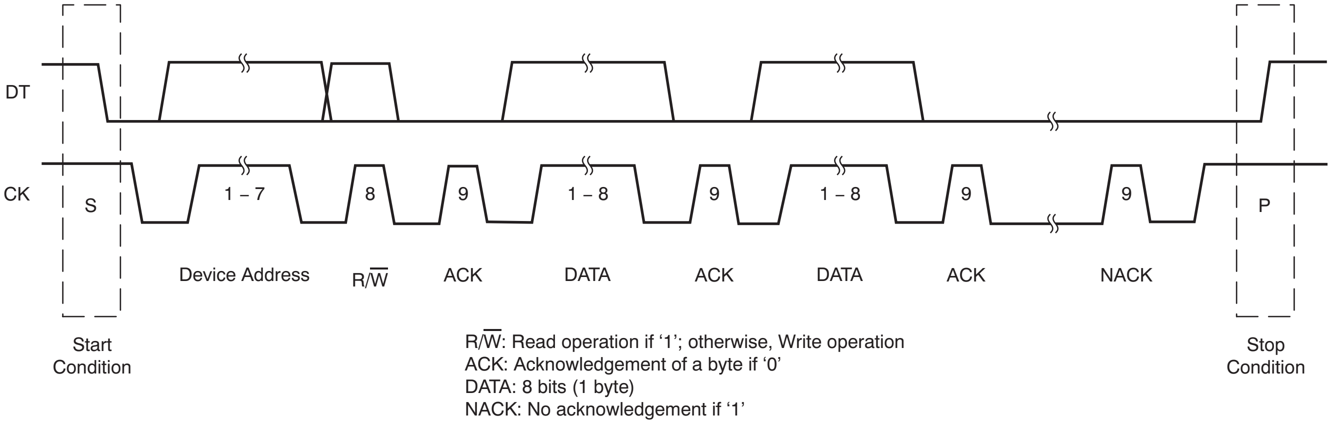


Figure 27. External ROM Read Operation

Table 11. External ROM Read Operation Characteristics

M	M	M	S	S	M	S	M	S	M	M
S	Device address	R/$\overline{W}$	ACK	DATA	ACK	DATA	ACK	. . .	NACK	P

Figure 28 shows the timing for an external ROM read interface. The respective timing characteristics are summarized in Table 12.

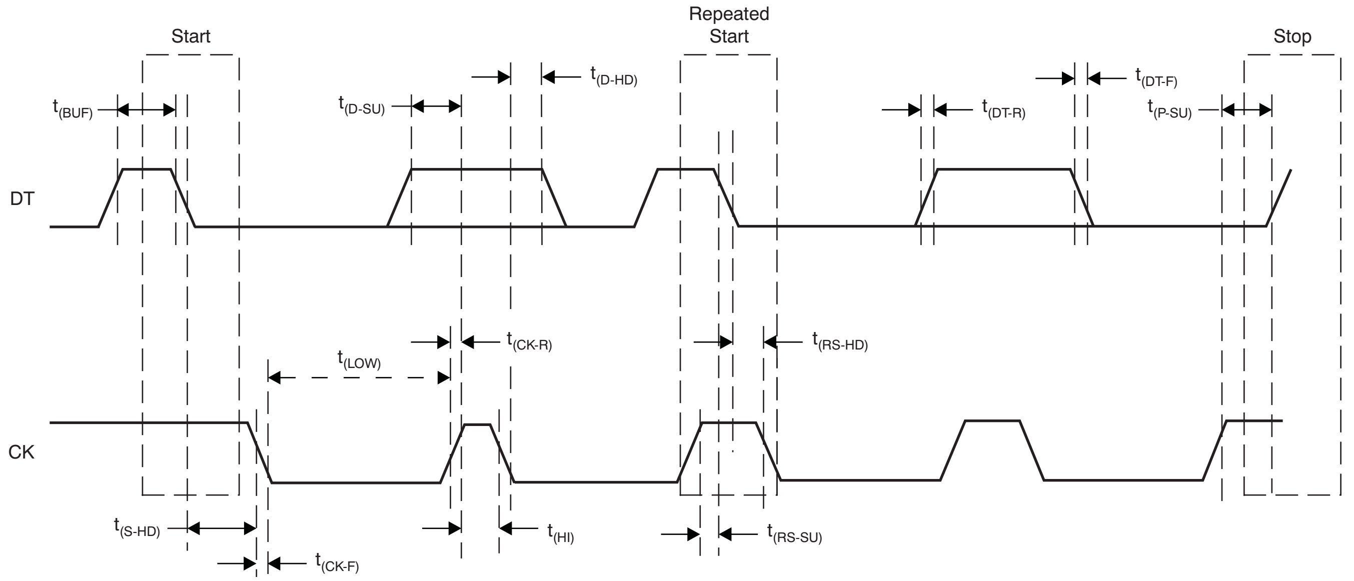


Figure 28. External ROM Read Interface Timing Requirements

Table 12. External ROM Read Interface Timing Characteristics

SYMBOL	PARAMETER	MIN	MAX	UNIT
$f_{(CK)}$	CK clock frequency		100	kHz
$t_{(BUF)}$	Bus free time between a STOP and a START condition	4.7		μs
$t_{(LOW)}$	Low period of the CK clock	4.7		μs
$t_{(HI)}$	High period of the CK clock	4		μs
$t_{(RS-SU)}$	Setup time for START/repeated START condition	4.7		μs
$t_{(S-HD)}$ $t_{(RS-HD)}$	Hold time for START/repeated START condition	4		μs
$t_{(D-SU)}$	Data setup time	250		ns
$t_{(D-HD)}$	Data hold time	0	900	ns
$t_{(CK-R)}$	Rise time of CK signal	$20 + 0.1\ C_B$	1000	ns
$t_{(CK-F)}$	Fall time of CK signal	$20 + 0.1\ C_B$	1000	ns
$t_{(DT-R)}$	Rise time of DT signal	$20 + 0.1\ C_B$	1000	ns
$t_{(DT-F)}$	Fall time of DT signal	$20 + 0.1\ C_B$	1000	ns
$t_{(P-SU)}$	Setup time for STOP condition	4		μs
C_B	Capacitive load for DT and CK lines		400	pF
V_{NH}	Noise margin at high level for each connected device (including hysteresis)	$0.2\ V_{DD}$		V

External ROM Example

External ROM data (sample set)

```
0xBB, 0x08, 0x04, 0x27,
0x50, 0x72, 0x6F, 0x64, 0x75, 0x63, 0x74, 0x20, 0x73, 0x74, 0x72, 0x69, 0x6E, 0x67, 0x73, 0x2E,
0x56, 0x65, 0x6E, 0x64, 0x6F, 0x72, 0x20, 0x73, 0x74, 0x72, 0x69, 0x6E, 0x67, 0x73, 0x20, 0x61,
0x72, 0x65, 0x20, 0x70, 0x6C, 0x61, 0x63, 0x65, 0x64, 0x20, 0x68, 0x65, 0x72, 0x65, 0x2E, 0x20,
0x80,
0x7D,
0x0A, 0x93, 0x01
```

Explanation

Data are stored beginning at address 0x00.

Vendor ID: 0x08BB

Product ID: 0x2704

Product string: Product strings (16 bytes).

Vendor string: Vendor strings are placed here (32 bytes, 31 visible characters are followed by 1 space).

Power attribute (bmAttribute): 0x80 (Bus-powered).

Max power (maxPower): 0x7D (250 mA).

Auxiliary HID usage ID: 0x0A, 0x93, 0x01 (AL A/V capture).

Note that the data bits must be sent from LSB to MSB on the I^{2}C bus. Therefore, each data byte must be stored with its bits in reverse order.

Serial Programming Interface (PCM2705C/7C)

The PCM2705C/7C supports a serial interface (SPI) to program the descriptor and to set the HID state. Descriptor data are described in the *External ROM Descriptor* section. Figure 29 illustrates the SPI timing; Table 13 lists the respective timing characteristics.

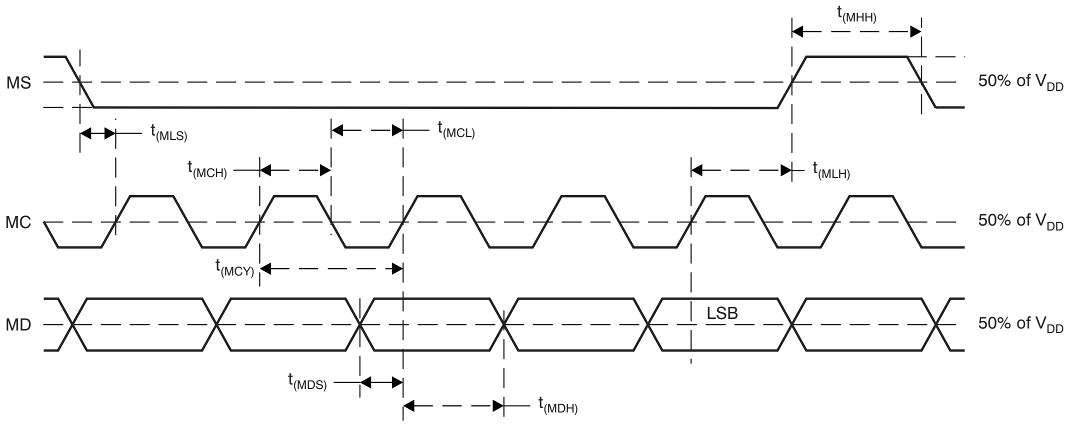


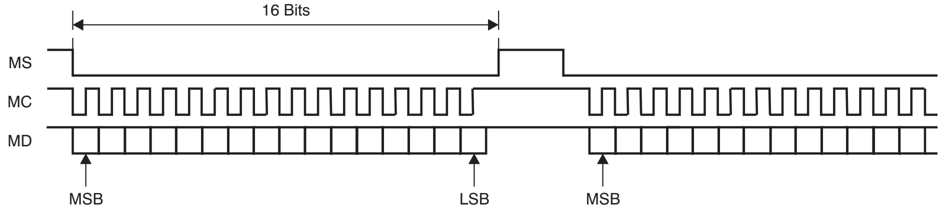
Figure 29. SPI Timing Diagram

Table 13. SPI Timing Characteristics

SYMBOL	PARAMETER	MIN	MAX	UNIT
$t_{(MCY)}$	MC pulse cycle time	100		ns
$t_{(MCL)}$	MC low-level time	50		ns
$t_{(MCH)}$	MC high-level time	50		ns
$t_{(MHH)}$	MS high-level time	100		ns
$t_{(MLS)}$	MS falling edge to MC rising edge	20		ns
$t_{(MLH)}$	MS hold time	20		ns
$t_{(MDH)}$	MD hold time	15		ns
$t_{(MDS)}$	MD setup time	20		ns

Figure 30 shows the SPI write timing sequence.

(1) Single Write Operation



(2) Continuous Write Operation

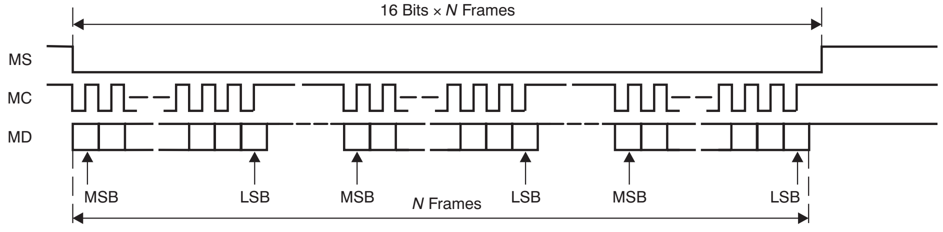


Figure 30. SPI Write Operation

SPI Register (PCM2705C/7C)

Table 14. SPI Register Description

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	ST	0	ADDR	0	D0	D1	D2	D3	D4	D5	D6	D7

D[7:0] **Function of the lower 8 bits depends on the value of the ST (B11) bit.**

ST = 0 (HID status write)

D7	Reports MUTE HID status to the host (active high)
D6	Reports volume-up HID status to the host (active high)
D5	Reports volume-down HID status to the host (active high)
D4	Reports next-track HID status to the host (active high)
D3	Reports previous-track HID status to the host (active high)
D2	Reports stop HID status to the host (active high)
D1	Reports play/pause HID status to the host (active high)
D0	Reports extended command status to the host (active high)

ST = 1 (ROM data write)

D[7:0] Internal descriptor ROM data, D0:LSB, D7:MSB

Contents of the power attribute and max power must be consistent with the actual application circuit configuration (the PSEL setting and the actual power usage from V_{BUS} of the USB connector); otherwise, it may cause improper or unexpected PCM2705C/7C operation.

ADDR **Starts write operation for internal descriptor reprogramming (active high)**

This bit resets the descriptor ROM address counter and indicates that subsequent words should be ROM data (described in the *External ROM Example* section). 456 bits of ROM data must be continuously followed after this bit has been asserted. The data bits must be sent from LSB (D0) to MSB (D7).

To set ADDR high, ST must be set low. Note that the lower 8 bits are still active as an HID status write when ST is set low.

ST **Determines the function of the lower 8-bit data**. Table 15 summarizes the functionality of ST and ADDR bit combinations.

0: HID status write

1: Descriptor ROM data write

Table 15. Functionality of ST and ADDR Bit Combinations

ST	ADDR	FUNCTION
0	0	HIS status write
0	1	HIS status write and descriptor ROM address reset
1	0	Descriptor ROM data write
1	1	Reserved

USB Host Interface Sequence

Power-On, Attach, and Playback Sequence

The PCM2704C/5C/6C/7C are ready for setup when the reset sequence has finished and the USB bus is attached. After a connection has been established (through the set-up process), the PCM2704C/5C/6C/7C are ready to accept USB audio data. While waiting for the audio data (that is, the device is in an idle state), the analog output is set to bipolar zero (BPZ).

Upon receiving the audio data, the PCM2704C/5C/6C/7C stores the first audio packet into the internal storage buffer. The packet contains 1 ms of audio data. The PCM2704C/5C/6C/7C start playing the audio data after detecting the next subsequent start-of-frame (SOF) packet. Figure 31 shows the initial operation sequence for the device.

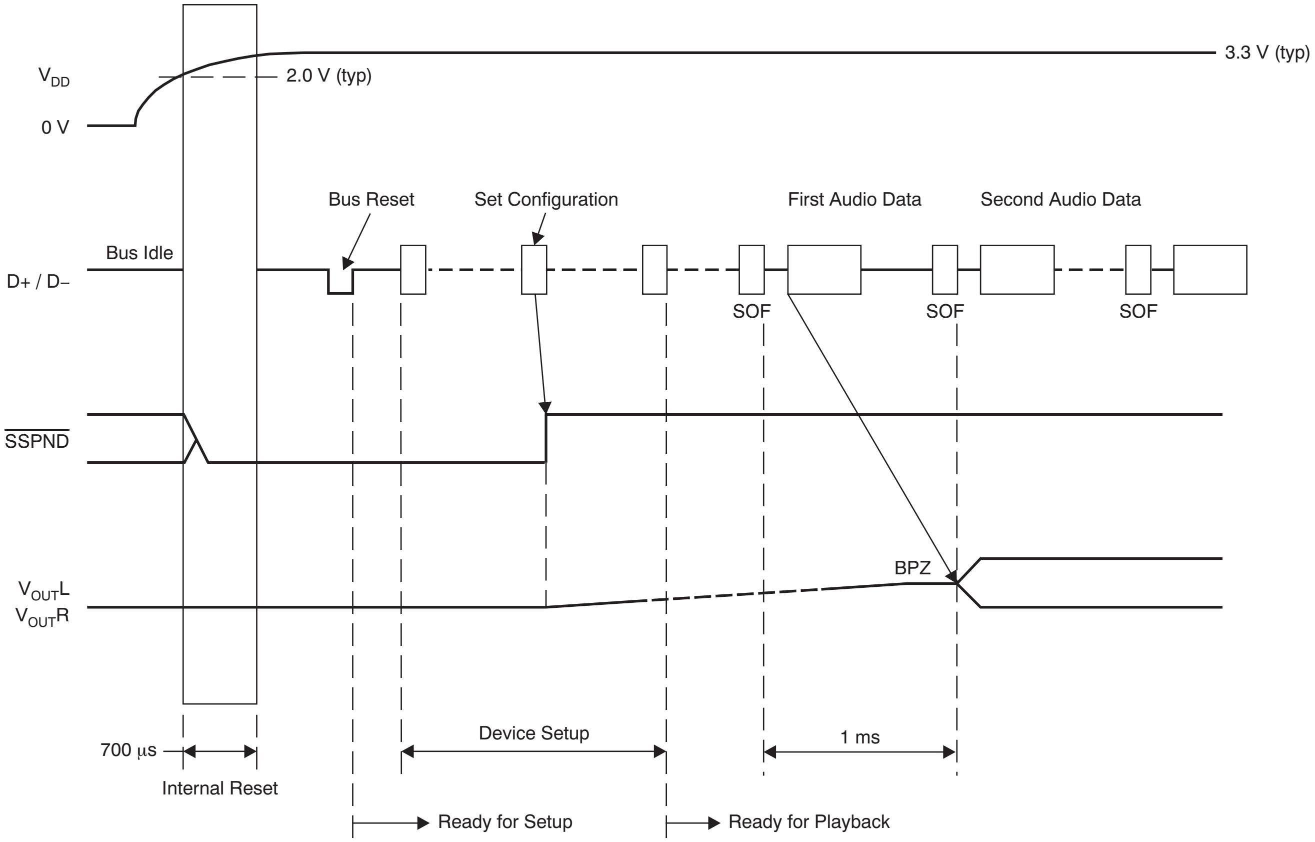


Figure 31. Initial Sequence

Play, Stop, and Detach Sequence

When the host finishes or aborts playback, the PCM2704C/5C/6C/7C stop playing after the last audio data output is complete. Figure 32 illustrates the play, stop, and detach sequence.

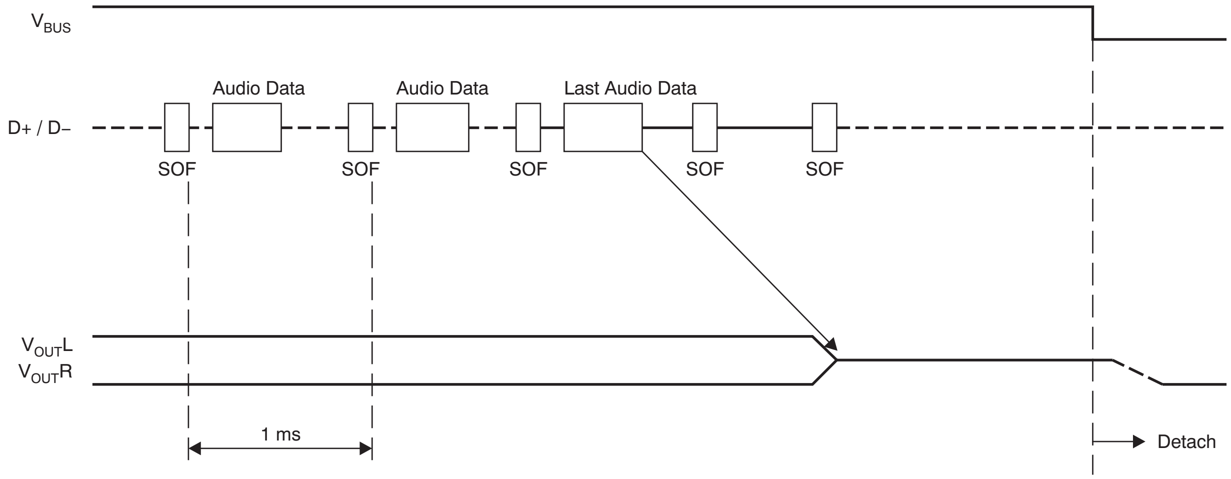


Figure 32. Play, Stop, and Detach Sequence

Suspend and Resume Sequence

The PCM2704C/5C/6C/7C enter a suspended state after the USB bus has been in a constant idle state for approximately 5 ms. While the PCM2704C/5C/6C/7C are in this suspended state, the $\overline{\text{SSPND}}$ flag (pin 27 for the PCM2704C/5C, pin 11 for the PCM2706C/7C) is asserted. The PCM2704C/5C/6C/7C wake up immediately when detecting a non-idle state on the USB bus. Figure 33 shows the operating sequence for the suspend and resume process.

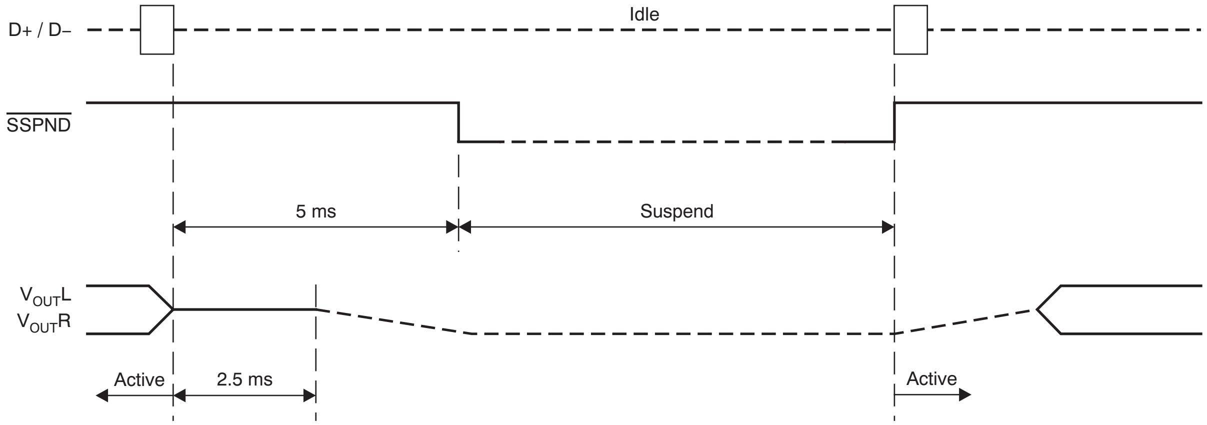


Figure 33. Suspend and Resume

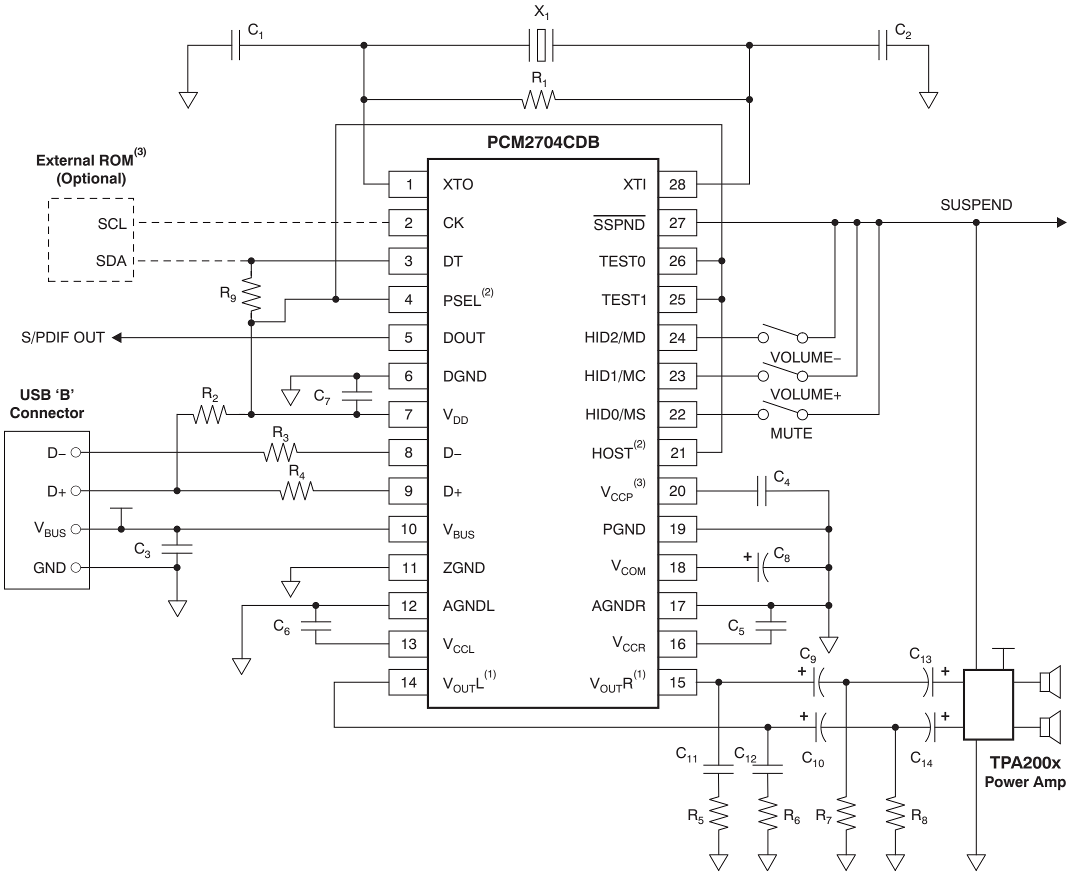
EXAMPLE CIRCUITS

Operating Environment

For current information on the PCM2704C/2705C/2706C/2707C operating environments, see the *Updated Operating Environments for PCM270X, PCM290X Applications* application report, SLAA374, available through the TI website at www.ti.com.

Typical Circuit Connection 1: USB Speaker

Figure 34 illustrates a typical circuit connection for an internal-descriptor, bus-powered, 500-mA application.



NOTE: X_1: 12-MHz crystal resonator. C_1, C_2: 10-pF to 33-pF capacitors (depending on load capacitance of crystal resonator). $C_3$to C_7: 1-μF ceramic capacitors. C_8: 10-μF electrolytic capacitor. C_9, C_{10}: 100-μF electrolytic capacitors (depending on tradeoff between required frequency response and discharge time for resume). C_{11}, C_{12}: 0.022-μF ceramic capacitors. C_{13}, C_{14}: 1-μF electrolytic capacitors. R_1: 1-MΩ resistor. R_2, R_9: 1.5-kΩ resistors. R_3, R_4: 22-Ω resistors. R_5, R_6: 16-Ω resistors. R_7, R_8: 330-Ω resistors (depending on tradeoff between required THD performance and pop-noise level for suspend).

(1) Output impedance of $V_{OUT}L$ and $V_{OUT}R$ during suspended mode or lack of power supply is 26 kΩ ±20%, which is the discharge path for C_9 and C_{10}.

(2) Descriptor programming through external ROM is only available when PSEL and HOST are high.

(3) External ROM power can be supplied from V_{CCP}, but any other active component must not use V_{CCP}, V_{CCL}, V_{CCR}, or V_{DD} as a power source.

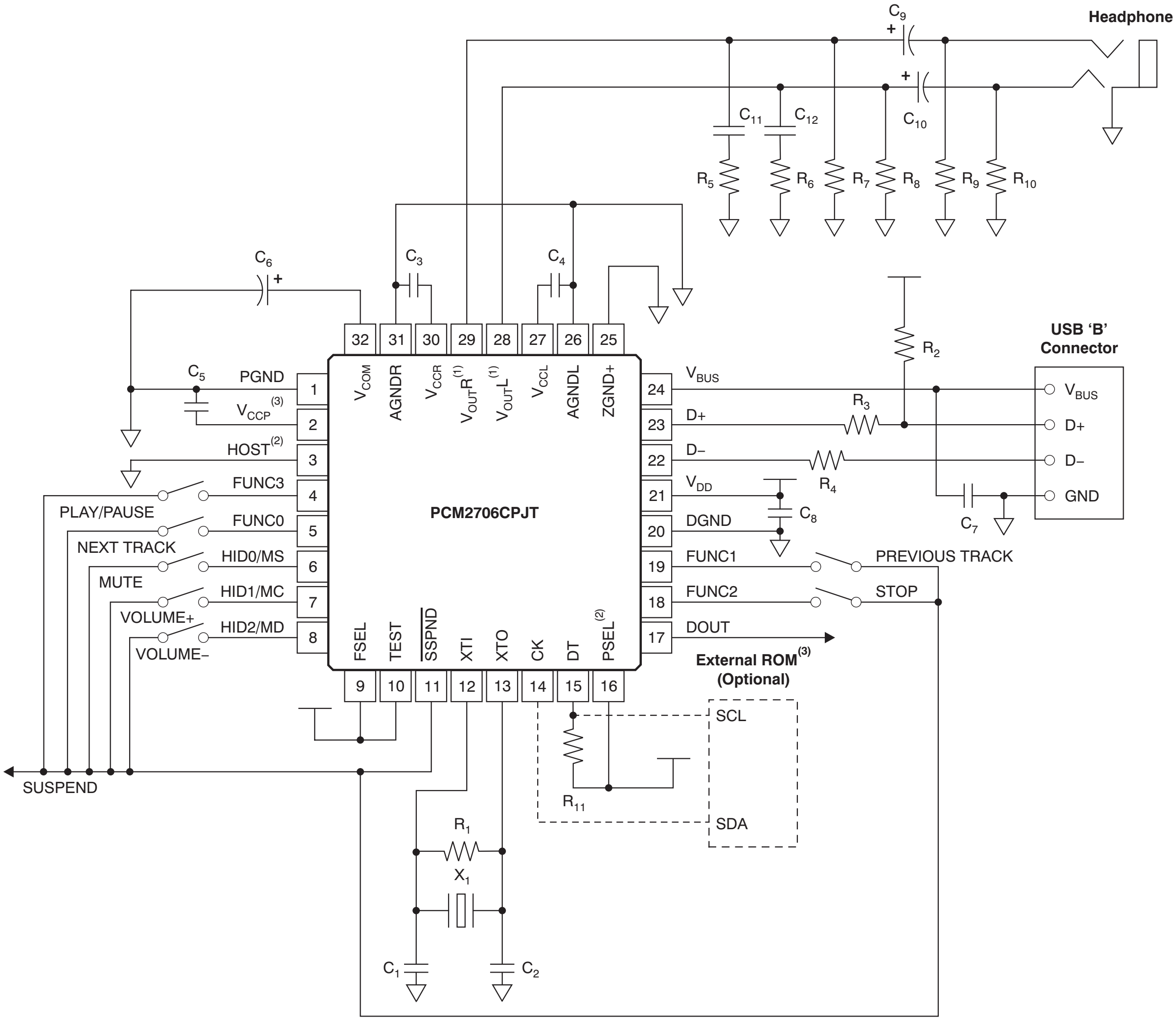
Figure 34. Bus-Powered Application

NOTE

The circuit illustrated in Figure 34 is for information only. The entire board design should be considered to meet the USB specification as a USB-compliant product.

Typical Circuit Connection 2: Remote Headphone

Figure 35 illustrates a typical circuit connection for a bus-powered, 100-mA headphone with seven HIDs.



NOTE: X_1: 12-MHz crystal resonator. C_1, C_2: 10-pF to 33-pF capacitors (depending on load capacitance of crystal resonator). C_3 to C_5, C_7, C_8: 1-μF ceramic capacitors. C_6: 10-μF electrolytic capacitor. C_9, C_{10}: 100-μF electrolytic capacitors (depending on required frequency response). C_{11}, C_{12}: 0.022-μF ceramic capacitors. R_1: 1-MΩ resistor. R_2, R_{11}: 1.5-kΩ resistors. R_3, R_4: 22-Ω resistors. R_5, R_6: 16-Ω resistors. R_7 to R_{10}: 3.3-kΩ resistors.

(1) Output impedance of $V_{OUT}L$ and $V_{OUT}R$ during suspend mode or lack of power supply is 26 kΩ ±20%, which is the discharge path for C_9 and C_{10}.

(2) Descriptor programming through external ROM is only available when PSEL and HOST are high.

(3) External ROM power can be supplied from V_{CCP}, but any other active component must not use V_{CCP}, V_{CCL}, V_{CCR}, or V_{DD} as a power source.

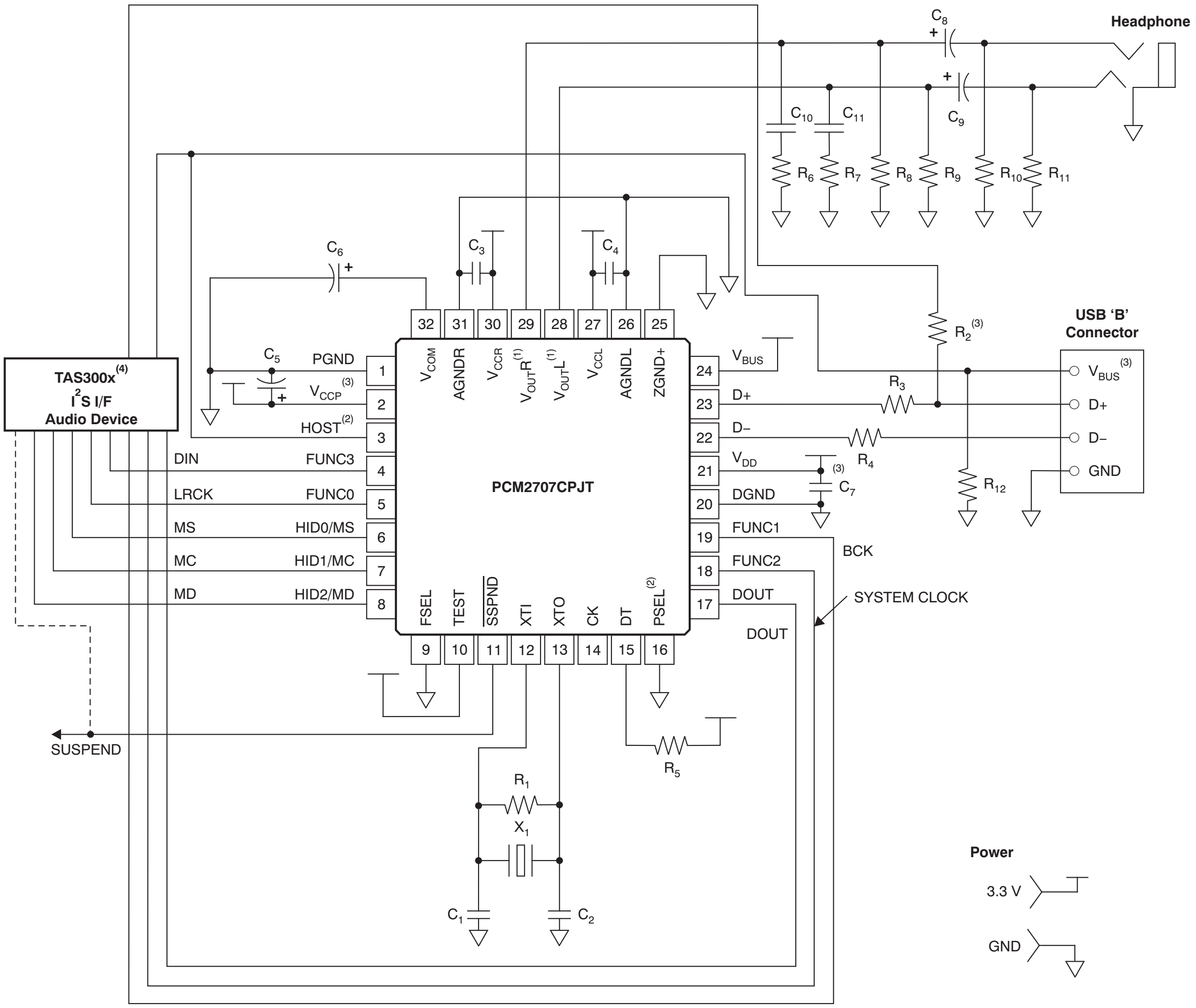
Figure 35. Bus-Powered Application

NOTE

The circuit illustrated in Figure 35 is for information only. The entire board design should be considered to meet the USB specification as a USB-compliant product.

Typical Circuit Connection 3: DSP Surround Processing Amplifier

Figure 36 illustrates a typical circuit connection for an I^{2}S- and SPI-enabled self-powered application.



NOTE: X_1: 12-MHz crystal resonator. C_1, C_2: 10-pF to 33-pF capacitors (depending on load capacitance of crystal resonator). C_3, C_4: 1-μF ceramic capacitors. C_5, C_7: 0.1-μF ceramic capacitor and 10-μF electrolytic capacitor. C_6: 10-μF electrolytic capacitors. C_8, C_9: 100-μF electrolytic capacitors (depending on required frequency response). C_{10}, C_{11}: 0.022-μF ceramic capacitors. R_1, R_{12}: 1-MΩ resistors. R_2, R_5: 1.5-kΩ resistors. R_3, R_4: 22-Ω resistors. R_6, R_7: 16-Ω resistors. $R_8$to R_{11}: 3.3-kΩ resistors.

(1) Output impedance of V_{OUT}L and V_{OUT}R during suspend mode or lack of power supply is 26 kΩ ±20%, which is the discharge path for C_8 and C_9.

(2) Descriptor programming through SPI is only available when PSEL and HOST are high.

(3) D+ pull-up must not be activated (high: 3.3 V) while the device is detached from USB or power supply is not applied on V_{DD} and V_{CCx}. V_{BUS} of USB (5 V) can be used to detect USB power status.

(4) MS must be high until the PCM2707C power supply is ready and the SPI host (the DSP) is ready to send data. Also, the SPI host must handle the D+ pull-up if the descriptor is programmed through the SPI. D+ pull-up must not be activated (high = 3.3 V) before programming of the PCM2707C through the SPI is complete.

Figure 36. Self-Powered Application

NOTE

The circuit illustrated in Figure 36 is for information only. The entire board design should be considered to meet the USB specification as a USB-compliant product.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August 2011) to Revision A	Page
• Changed 产品状态从混合状态改为生产数据	1
• Changed 特性部分显示与USB2.0技术规格完全兼容（但是仍使用USB1.1描述符）	1
• Changed 说明部分显示USB2.0兼容性（USB1.1已经被纳入2.0技术规范）	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
PCM2704CDB	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM2704C	Samples
PCM2704CDBR	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM2704C	Samples
PCM2705CDB	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM2705C	Samples
PCM2705CDBR	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM2705C	Samples
PCM2706CPJT	ACTIVE	TQFP	PJT	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM2706C	Samples
PCM2706CPJTR	ACTIVE	TQFP	PJT	32	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM2706C	Samples
PCM2707CPJT	ACTIVE	TQFP	PJT	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM2707C	Samples
PCM2707CPJTR	ACTIVE	TQFP	PJT	32	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM2707C	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

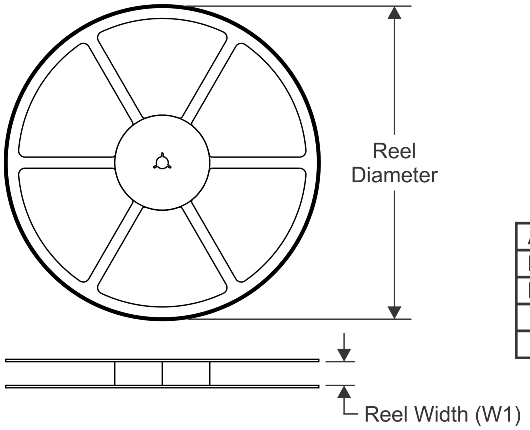
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

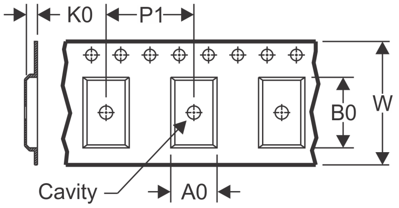
[4] Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

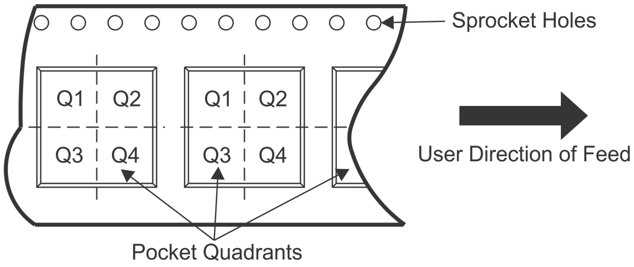


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

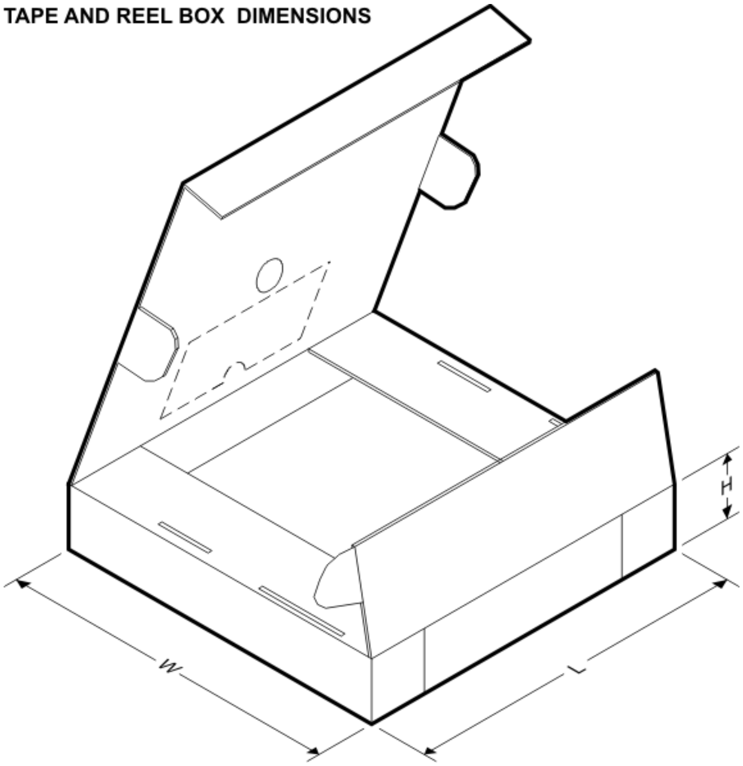
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM2705CDBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
PCM2706CPJTR	TQFP	PJT	32	1000	330.0	16.8	9.6	9.6	1.5	12.0	16.0	Q2
PCM2707CPJTR	TQFP	PJT	32	1000	330.0	16.8	9.6	9.6	1.5	12.0	16.0	Q2

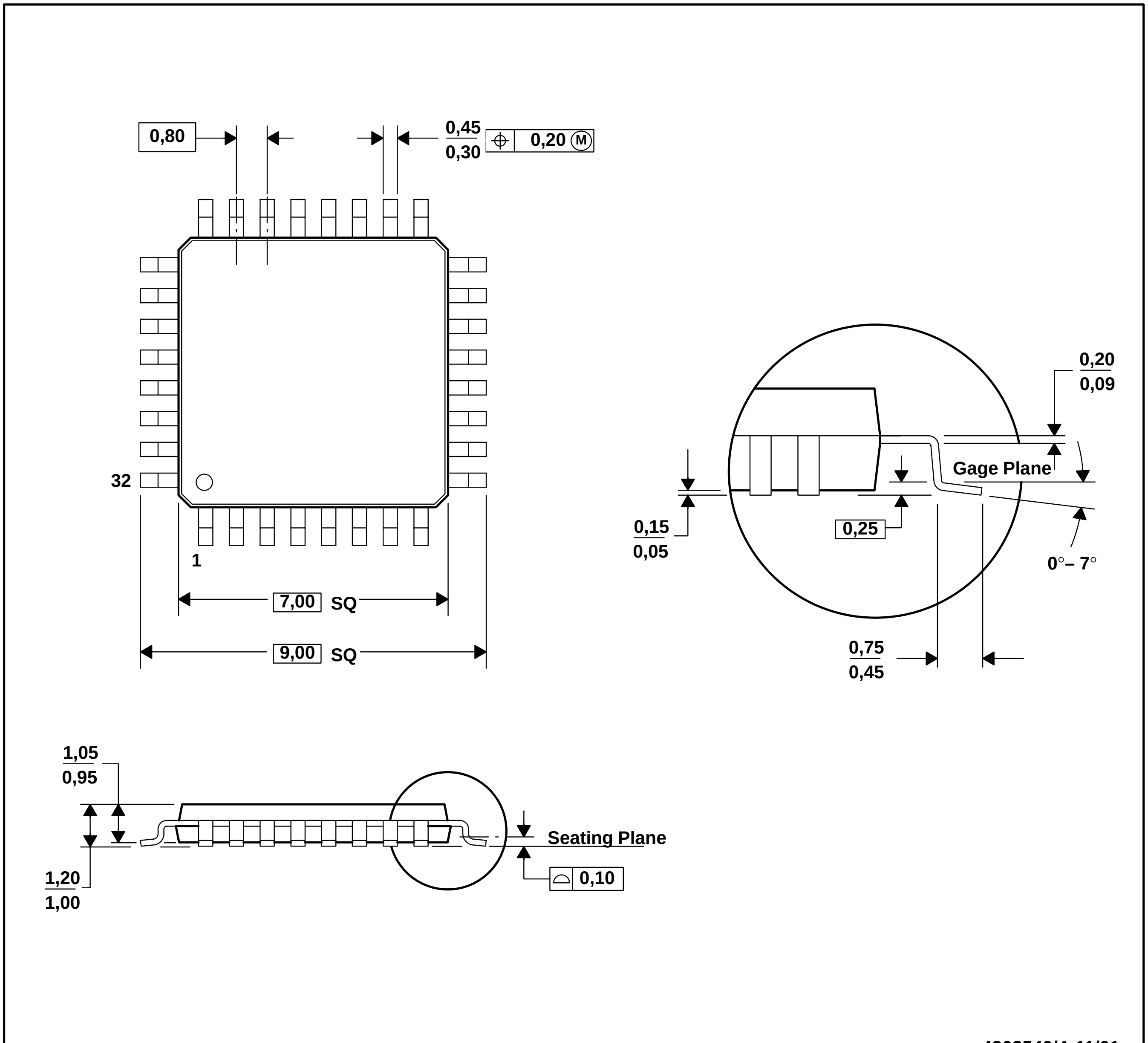
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM2705CDBR	SSOP	DB	28	2000	367.0	367.0	38.0
PCM2706CPJTR	TQFP	PJT	32	1000	367.0	367.0	38.0
PCM2707CPJTR	TQFP	PJT	32	1000	367.0	367.0	38.0

PJT (S-PQFP–N32) PLASTIC QUAD FLATPACK

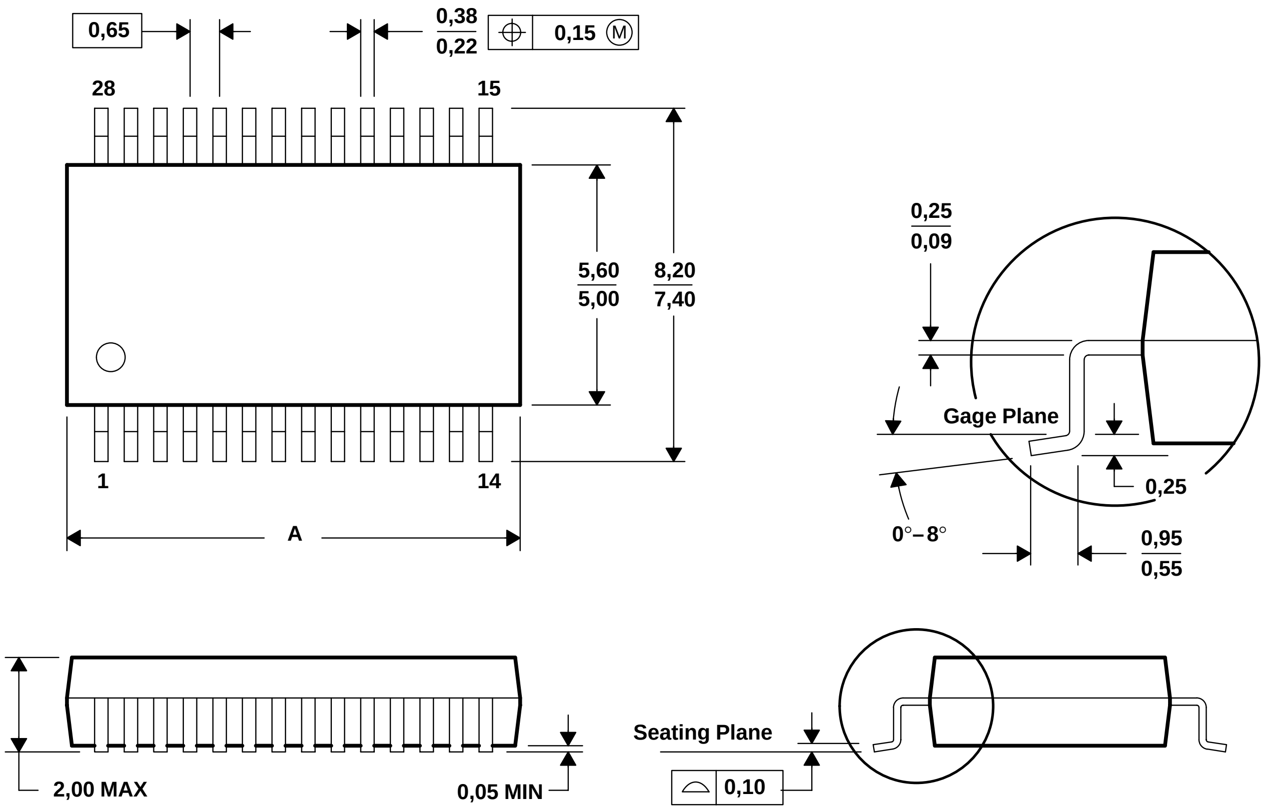


4203540/A 11/01

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-026

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



PINS ** / DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150

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