BLC9G20XS-160AV

Power LDMOS transistor

Rev. 3 — 24 May 2017

AMPLEON

Product data sheet

1. Product profile

1.1 General description

160 W LDMOS packaged asymmetric Doherty power transistor for base station applications at frequencies from 1805 MHz to 1990 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in an asymmetrical Doherty demo test circuit. V_{DS} = 30 V; I_{Dq} = 300 mA (main); $V_{GS(amp)peak}$ = 0.7 V, unless otherwise specified.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	ACPR
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
1-carrier W-CDMA	1805 to 1880	30	28	16.6	47	−30 [1]

[1] Test signal: 3GPP test model 1; 64 DPCH; PAR = 7.2 dB at 0.01% probability on CCDF per carrier.

1.2 Features and benefits

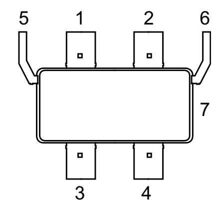
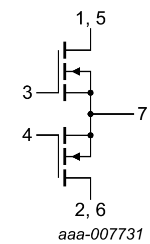
- Excellent ruggedness
- High-efficiency
- Low thermal resistance providing excellent thermal stability
- Designed for broadband operation (1805 MHz to 1990 MHz)
- Asymmetric design to achieve optimum efficiency across the band
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent digital pre-distortion capability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 1805 MHz to 1990 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1 (main)		
2	drain2 (peak)		
3	gate1 (main)		
4	gate2 (peak)		
5	video decoupling (main)		
6	video decoupling (peak)		
7	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLC9G20XS-160AV	-	air cavity plastic earless flanged package; 6 leads	SOT1275-1

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
$V_{GS(amp)main}$	main amplifier gate-source voltage		–5	+13	V
$V_{GS(amp)peak}$	peak amplifier gate-source voltage		–5	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	V_{DS} = 30 V; I_{Dq} = 300 mA (main); $V_{GS(amp)peak}$ = 0.5 V; T_{case} = 80 °C		
		P_L = 44.5 dBm	0.30	K/W
		P_L = 46.5 dBm	0.22	K/W

6. Characteristics

Table 6. DC characteristics
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Main device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.6 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 60 mA	1.5	2	2.5	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 30 V; I_D = 300 mA	1.65	2.2	2.75	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	12.2	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 3.0 A	-	4.56	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 2.1 A	-	237	385	mΩ
Peak device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 1.1 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 110 mA	1.5	2	2.5	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 30 V; I_D = 660 mA	1.6	2.1	2.6	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	21.7	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 5.5 A	-	8.16	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 3.85 A	-	129	214	mΩ

Table 7. RF characteristics
Test signal: 1-carrier W-CDMA; PAR = 7.2 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH; RF performance at V_{DS} = 30 V; I_{Dq} = 300 mA (main); $V_{GS(amp)peak}$ = 0.5 V; T_{case} = 25 °C; unless otherwise specified; in an asymmetrical Doherty production test circuit at frequencies from 1805 MHz to 1880 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 28 W	15.2	16.4	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = 28 W	-	−10	−5	dB
η_D	drain efficiency	$P_{L(AV)}$ = 28 W	41.4	46	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 28 W	-	−30	−23	dBc

Table 8. RF characteristics
Test signal: pulsed CW; t_p = 100 μs; δ = 10 %; RF performance at V_{DS} = 30 V; I_{Dq} = 300 mA (main); $V_{GS(amp)peak}$ = 0.5 V; T_{case} = 25 °C; unless otherwise specified; in an asymmetrical Doherty production test circuit at frequencies from 1805 MHz to 1880 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(M)}$	peak output power		160	190	-	W

7. Test information

7.1 Ruggedness in Doherty operation

The BLC9G20XS-160AV is capable of withstanding a load mismatch corresponding to a VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 30 V; I_{Dq} = 300 mA (main); $V_{GS(amp)peak}$ = 0.5 V; P_L = 135 W (CW); f = 1805 MHz.

7.2 Impedance information

Table 9. Typical impedance of main device
Measured load-pull data of main device; I_{Dq} = 360 mA (main); V_{DS} = 30 V.

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
1805	2.20 – j8.08	2.85 – j5.54	49.68	61.09	16.57
1843	3.40 – j8.84	2.85 – j5.54	49.56	60.83	16.55
1880	3.67 – j9.16	2.69 – j5.13	49.38	59.43	16.48
Maximum drain efficiency load					
1805	2.20 – j8.08	5.06 – j4.14	48.40	69.34	18.42
1843	3.40 – j8.84	4.84 – j2.59	47.52	68.53	18.61
1880	3.67 – j9.16	5.00 – j3.33	47.79	67.95	18.99

[1] Z_S and Z_L defined in Figure 1.

[2] at 3 dB gain compression.

Table 10. Typical impedance of peak device
Measured load-pull data of peak device; I_{Dq} = 660 mA (peak); V_{DS} = 30 V.

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
1805	1.76 – j7.22	2.61 – j6.60	51.62	54.98	15.72
1843	3.07 – j7.53	2.61 – j6.60	51.43	54.14	15.60
1880	3.44 – j8.15	2.61 – j6.60	51.29	53.36	15.75
Maximum drain efficiency load					
1805	1.76 – j7.22	4.65 – j3.75	50.09	66.75	18.39
1843	3.07 – j7.53	3.91 – j3.12	49.50	65.85	18.49
1880	3.44 – j8.15	3.94 – j3.76	49.80	64.54	18.55

[1] Z_S and Z_L defined in Figure 1.

[2] at 3 dB gain compression.

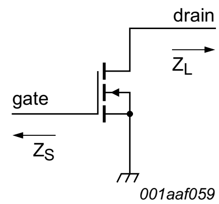


Fig 1. Definition of transistor impedance

7.3 Recommended impedances for Doherty design

Table 11. Typical impedance of main device at 1 : 1 load
Measured load-pull data of main device; I_{Dq} = 300 mA (main); V_{DS} = 30 V.

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [3]	G_p [3]
(MHz)	(Ω)	(Ω)	(dBm)	(%)	(dB)
1805	2.20 – j8.08	1.83 – j4.0	49.09	55.81	19.68
1843	3.40 – j8.84	1.80 – j3.7	49.15	56.21	19.40
1880	3.67 – j9.16	1.77 – j3.4	49.09	55.86	19.41

[1] Z_S and Z_L defined in Figure 1.

[2] at 3 dB gain compression.

[3] at $P_{L(AV)}$ = 44.5 dBm.

Table 12. Typical impedance of main device at 1 : 2.7 load
Measured load-pull data of main device; I_{Dq} = 300 mA (main); V_{DS} = 30 V.

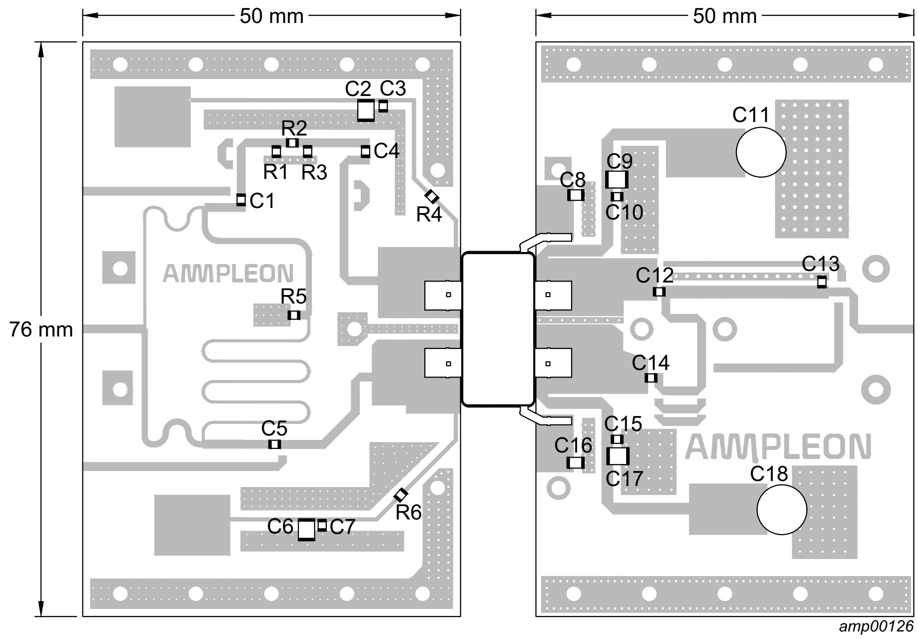
f	Z_S [1]	Z_L [1]	P_L [2]	η_D [3]	G_p [3]
(MHz)	(Ω)	(Ω)	(dBm)	(%)	(dB)
1805	2.20 – j8.08	4.30 – j2.46	47.11	64.24	22.15
1843	3.40 – j8.84	4.31 – j2.29	46.77	62.36	22.36
1880	3.67 – j9.16	4.31 – j2.12	46.61	60.79	22.70

[1] Z_S and Z_L defined in Figure 1.

[2] at 3 dB gain compression.

[3] at $P_{L(AV)}$ = 44.5 dBm.

7.4 Test circuit



Printed-Circuit Board (PCB): Rogers RO4350B; ε_r = 3.66; thickness = 0.508 mm; thickness copper plating = 35 μm.

See Table 13 for a list of components.

Fig 2. Component layout

Table 13. List of components

See Figure 2 for component layout.

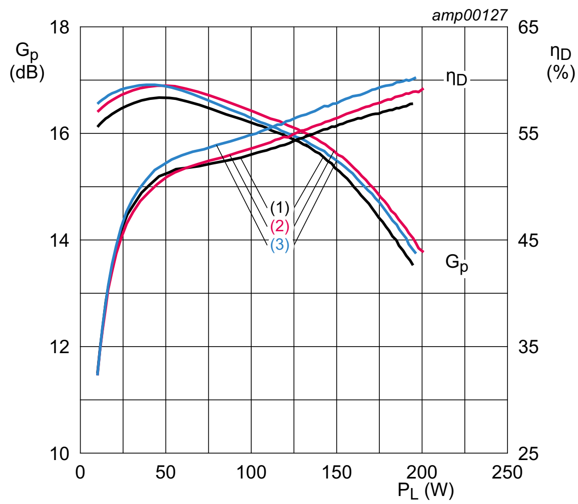
Component	Description	Value	Remarks
C1, C3, C4, C5, C7, C10, C14, C15	multilayer ceramic chip capacitor	36 pF [1]	
C2, C6, C8, C9, C16, C17	multilayer ceramic chip capacitor	10 μF, 50 V [2]	
C11, C18	electrolytic capacitor	1000 μF, 63 V [1]	
C12	multilayer ceramic chip capacitor	6.8 pF [1]	
C13	multilayer ceramic chip capacitor	0.2 pF [1]	
R1, R3	resistor	910 Ω	SMD 0805
R2, R4, R6	resistor	5.1 Ω	SMD 0805
R5	resistor	50 Ω	SMD 0805

[1] American Technical Ceramics type 600F or capacitor of same quality.

[2] Murata or capacitor of same quality.

7.5 Graphical data

7.5.1 Pulsed CW



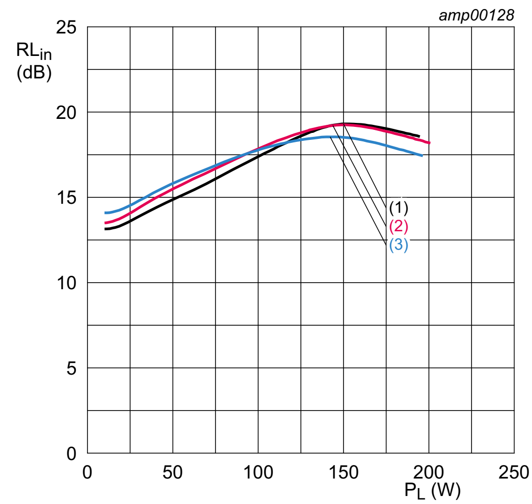
V_{DS} = 30 V; I_{Dq} = 300 mA (main device); $V_{GS(amp)peak}$ = 0.5 V.

(1) f = 1805 MHz

(2) f = 1842.5 MHz

(3) f = 1880 MHz

Fig 3. Power gain and drain efficiency as function of output power; typical values



V_{DS} = 30 V; I_{Dq} = 300 mA (main device); $V_{GS(amp)peak}$ = 0.5 V.

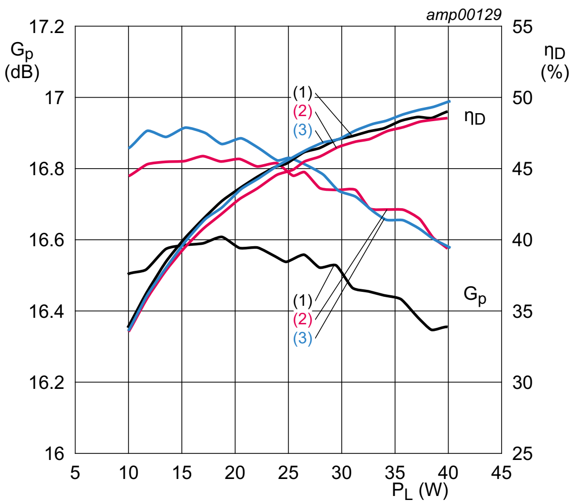
(1) f = 1805 MHz

(2) f = 1842.5 MHz

(3) f = 1880 MHz

Fig 4. Input return loss as a function of output power; typical values

7.5.2 1-Carrier W-CDMA



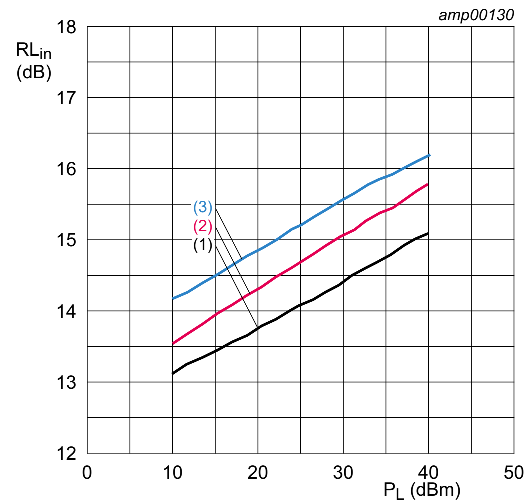
V_{DS} = 30 V; I_{Dq} = 300 mA (main device); $V_{GS(amp)peak}$ = 0.5 V.

(1) f = 1805 MHz

(2) f = 1842.5 MHz

(3) f = 1880 MHz

Fig 5. Power gain and drain efficiency as function of output power; typical values



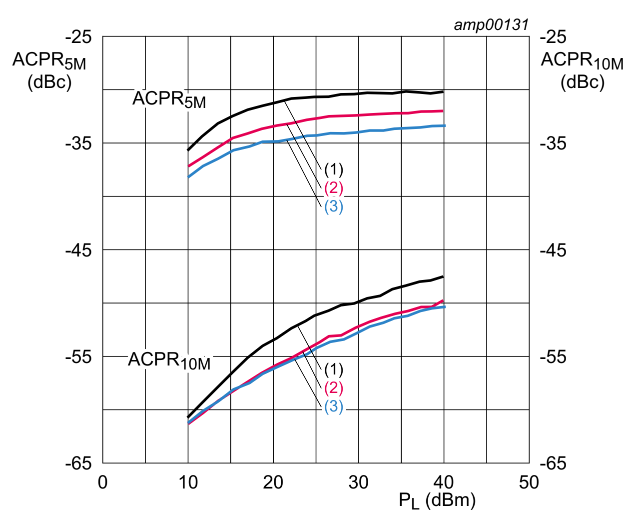
V_{DS} = 30 V; I_{Dq} = 300 mA (main device); $V_{GS(amp)peak}$ = 0.5 V.

(1) f = 1805 MHz

(2) f = 1842.5 MHz

(3) f = 1880 MHz

Fig 6. Input return loss as a function of output power; typical values



V_{DS} = 30 V; I_{Dq} = 300 mA (main device); $V_{GS(amp)peak}$ = 0.5 V.

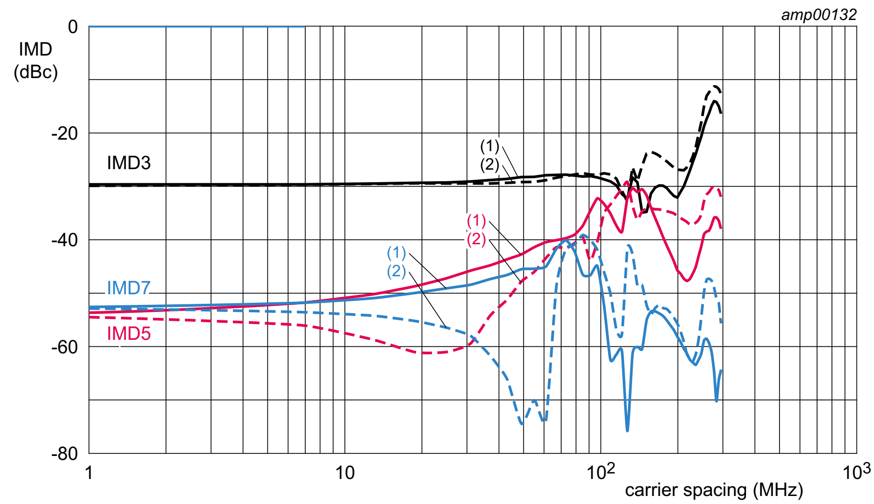
(1) f = 1805 MHz

(2) f = 1842.5 MHz

(3) f = 1880 MHz

Fig 7. Adjacent channel power ratio (5 MHz) and adjacent channel power ratio (10 MHz) as function of output power; typical values

7.5.3 2-Tone VBW



V_{DS} = 30 V; I_{Dq} = 300 mA (main device); $V_{GS(amp)peak}$ = 0.5 V; f_c = 1842.5 MHz.

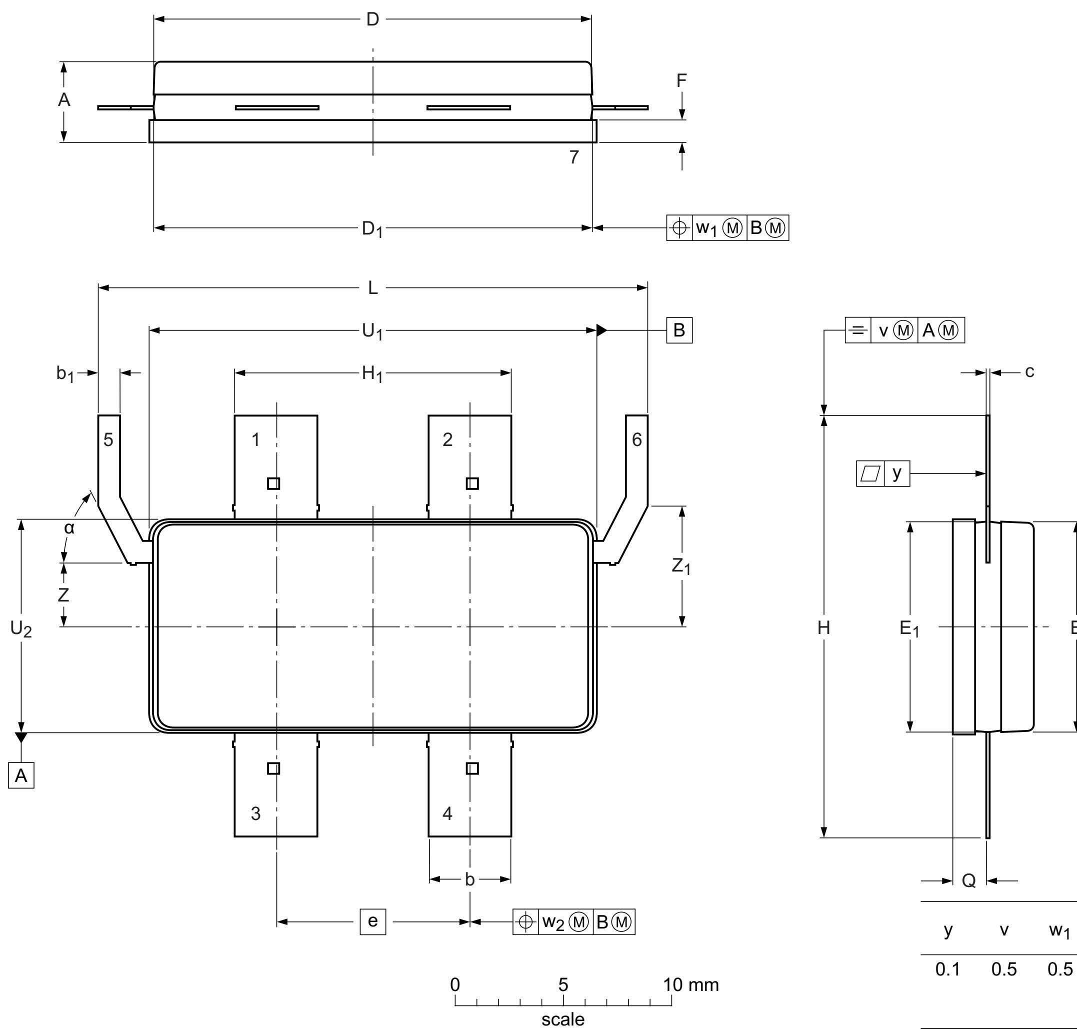
(1) IMD low

(2) IMD high

Fig 8. VBW capability in Doherty demo board

8. Package outline

Air cavity plastic earless flanged package; 6 leads **SOT1275-1**



y	v	w_1	w_2
0.1	0.5	0.5	0.5

Dimensions

Unit		A	b	b_1	c	D	D_1	E	E_1	e	F	H	H_1	L	Q[(1)]	U_1	U_2	Z	Z_1	α
mm	max	4.01	3.94	1.14	0.178	20.42	20.37	9.80	9.75		1.14	19.53	12.80	25.40	1.68	20.70	9.91	3.17	5.79	65°
	nom									8.89										
	min	3.40	3.68	0.89	0.127	20.12	20.17	9.50	9.55		0.94	19.33	12.60	25.20	1.45	20.50	9.70	2.67	5.29	61°

Note
1. Dimension Q is measured 0.1 mm away from the flange.
2. Ringframe and/or ringframe glue shall not overhang at the side of the flange.

sot1275-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1275-1						~~16-11-15~~ 17-04-13

Fig 9. Package outline SOT1275-1

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 14. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V, but fails after exposure to an ESD pulse of 750 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V, but fails after exposure to an ESD pulse of 4000 V.

10. Abbreviations

Table 15. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
PAR	Peak-to-Average Ratio
SMD	Surface Mounted Device
VBW	Video Bandwidth
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC9G20XS-160AV v.3	20170524	Product data sheet	-	BLC9G20XS-160AV v.2
Modifications:	• Table 2 on page 2: change simplified outline • Table 3 on page 2: change version to SOT1275-1 • Figure 9 on page 10: change package outline drawing to SOT1275-1			
BLC9G20XS-160AV v.2	20161220	Product data sheet	-	BLC9G20XS-160AV v.1
BLC9G20XS-160AV v.1	20161019	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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13. Contact information

For more information, please visit: **http://www.ampleon.com**

For sales office addresses, please visit: **http://www.ampleon.com/sales**

14. Contents

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