TDA38825

20 A synchronous Buck regulator

Features

- Wide Input Voltage Range: 4 V to 16 V with internal bias and 2.7 V to 16 V with external VCC (3.3 V)
- Precision Reference Voltage (0.6 V +/- 0.5%)
- Stable with Ceramic Output Capacitors
- No External Compensation
- Optional Forced Continuous Conduction Mode and Diode Emulation for Enhanced Light Load Efficiency
- Selectable Switching Frequency from 600 kHz, 800 kHz, and 1 MHz
- Programmable Soft-Start Time with a minimum of 1 ms & Enhanced Pre-Bias Start-Up
- Voltage Tracking with External Reference Input
- Programmable Over Current Protection Limit with internal thermal compensation
- Enable input with Voltage Monitoring Capability
- Power Good Output
- Non-Latch OCP, UVP, Thermal Shutdown, and Latch-Off OVP
- Operating Temp: -40 °C < T_j < 125 °C
- Small Size: 3 mm x 4 mm QFN-21
- Lead-free, Halogen-free and RoHS Compliant

Potential applications

- Server Applications
- Storage Applications
- Telecom & Datacom Applications
- Distributed Point of Load Power Architectures

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Description

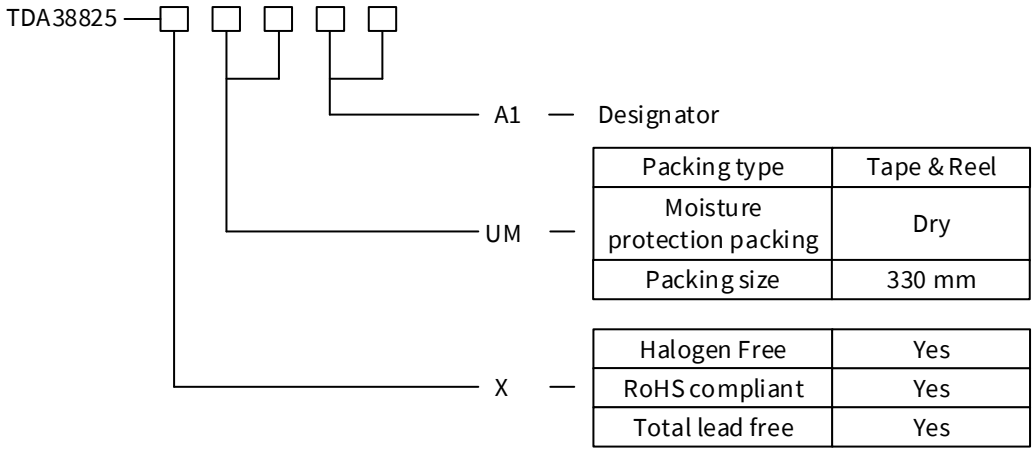
The TDA38825 is a 20 A fully integrated and highly efficient dc - dc Buck regulator. It uses a fast Constant On-Time (COT) control scheme, which simplifies the design efforts and achieves fast transient response while maintaining excellent line and load regulation. It can operate over a wide range of input voltage (2.7 V to 16 V) using an external bias supply.

TDA38825 is a versatile regulator, offering switching frequency selectable from 600 kHz, 800 kHz and 1 MHz, programmable current limit and soft-start time with a minimum of 1 ms, Forced Continuous Conduction Mode (FCCM) and Diode Emulation Mode (DEM) operation. The TDA38825 supports voltage tracking with an external reference input. It also features important protection functions, such as pre-bias start-up, thermally compensated current limit, over voltage and under voltage protection, and thermal shutdown to give required system level security in the event of fault conditions. The TDA38825 is available in a standard QFN-21 (3mm x 4mm) package and is able to operate over a wide temperature range (-40 °C < Tj < 125 °C).

Table of contents

1 Ordering Information

Base Part Number	Package Type	Standard Pack Form and Qty		Orderable Part Number
TDA38825	QFN-21	Tape and Reel	3000	TDA38825XUMA1



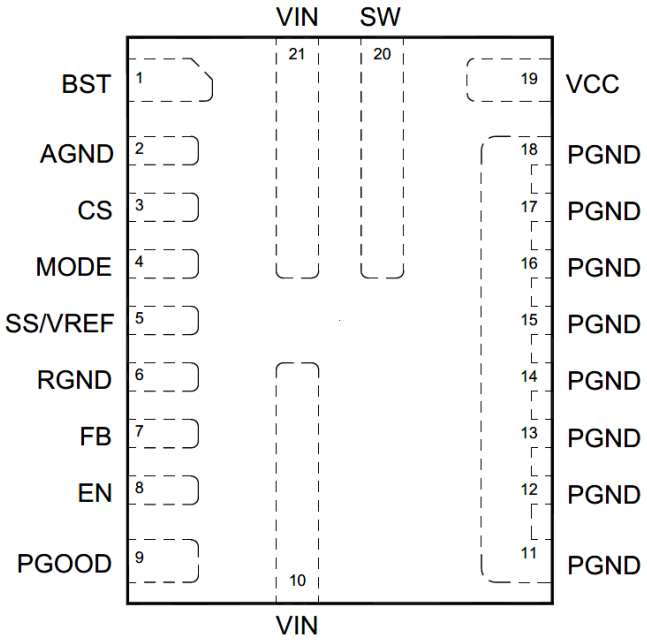


Figure 1 Package Top View

2 Functional Block Diagram

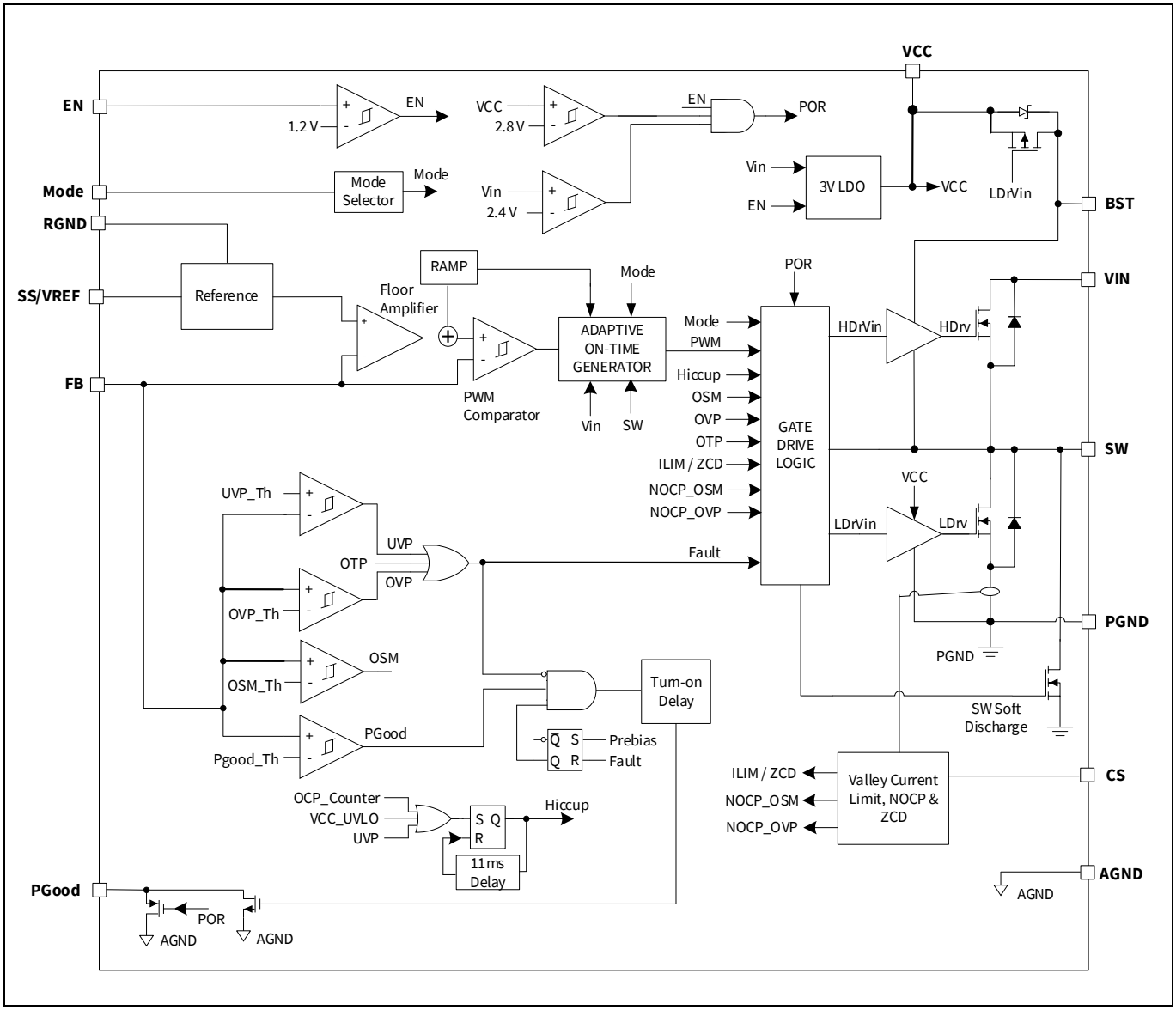


Figure 2 Block Diagram

3 Typical Application Diagram

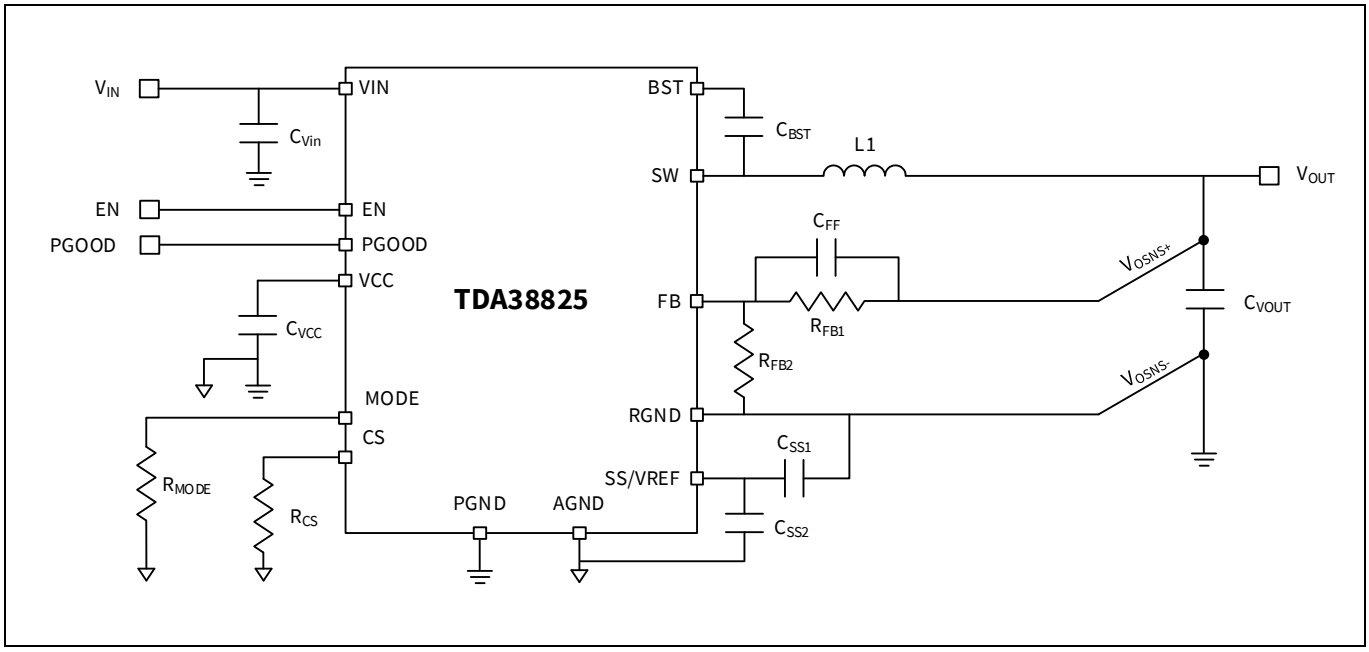


Figure 3 TDA38825 application circuit

4 Pin Descriptions

Note: *I = Input, O = Output*

Pin#	Pin Name	I/O	Type	Pin Description
1	BST	I	Analog	A capacitor connected between SW and BST is required to form a floating supply across the high-side switch driver.
2	AGND	-	Ground	Select AGND as the control circuit reference point.
3	CS	I	Analog	Current Limit; connect a resistor to AGND to set the current limit trip point.
4	MODE	I	Analog	Operation mode selection. Program MODE to select CCM, DEM, and the operating switching frequency.
5	SS/VREF	I	Analog	Input pin for external reference to support voltage tracking. Decouple with a ceramic capacitor as close to SS/VREF pin possible. The capacitance of this capacitor also determines the soft-start time.
6	RGND	-	Analog	Differential remote sense negative input. Connect this pin directly to the negative side of the voltage sense point. Short to GND if remote sense is not used.
7	FB	I	Analog	Feedback; An external resistor divider from the output to RGND (tapped to FB) sets the output voltage. It is recommended to place the resistor divider as close to FB as possible. Vias should be avoided on the FB traces. Place a feed-forward capacitor (Cff) between output and FB to optimize load transient response.
8	EN	I	Analog	Enable; EN is an input signal that turns the regulator on or off. Drive EN high to turn on the regulator, drive EN low to turn off the regulator. Connect EN to VIN through a pull-up resistor or a resistive voltage divider for automatic start-up.
9	PGOOD	O	Analog	Power good output. This is an open-drain signal. A pull-up resistor (connected to a DC voltage) is required to indicate high if the output voltage is within regulation. There is about 1 ms delay from FB ≥ 92.5% to PGOOD pull-high.
10, 21	VIN	I	Power	Input voltage. VIN supplies power for the internal MOSFET and regulator. The input capacitors are needed to decouple the input rail. Place decoupling capacitors close to VIN and PGND. Use wide PCB traces to make the connection.
11-18	PGND	-	Ground	System ground. PGND is the reference ground return. For this reason, care must be taken in PCB layout. Use wide PCB traces to make the connection.
19	VCC	I/O	Power	Internal 3V LDO output. The driver and control circuits are powered from this voltage. Decouple with a minimum 1 µF ceramic capacitor as close to VCC as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics.
20	SW	O	Power	Switch output. Connect SW to the inductor and bootstrap capacitor. SW is driven up to the VIN voltage by the high-side switch during the on-time of the PWM duty cycle. The inductor current drives SW low during the off-time. Use wide PCB traces to make the connection.

5 Absolute maximum ratings

Absolute maximum ratings

Description	Min	Max	Unit	Conditions
VIN	-0.3	18	V	Note **1**
VCC	-0.3	4.0	V	Note **1**
EN	-0.3	18	V	
SW to PGND	-0.3 (dc), -5 for 5 ns	VIN (dc) 25 for 5 ns	V	Note **1**
VIN to SW	-0.3 (dc), -5 for 5 ns	VIN (dc) 25 for 5 ns	V	Note **1**
BST to PGND	-0.3 (dc)	Vsw + 4.0	V	Note **1**
BST to SW	-0.3	4.0	V	
PGND to AGND	-0.3	0.3	V	
CS, FB, PGOOD, MODE, SS/VREF to GND	-0.3	4.0	V	Note **1**
Junction Temperature Range	-40	150	°C	
Storage Temperature Range	-55	150	°C	

Note:

1. PGND, RGND, and AGND pin are connected.

Attention: ***Stresses beyond these listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.***

6 Thermal Characteristics

Description	Symbol	Values	Test Conditions
Junction to Ambient Thermal Resistance	θ_{JA}	22.5 °C/W	Note **2**
Junction to PCB Thermal Resistance	$\theta_{JC\text{-}PCB}$	8.2 °C/W	Note **2**
Junction to Case Top Thermal Resistance	θ_{JC}	17.8 °C/W	Note **3**

Note:

2. *Simulated using TDA38825 evaluation board (Dimensions: 3in. x 4in., 6 Layer FR-4 PCB).*
3. *Simulated standalone thermal characteristics. Measured between junction and center on the package top.*

7 Electrical specifications

7.1 Recommended operating conditions

Description	Min	Max	Unit	Note
VIN Voltage Range with External VCC	2.7	16	V	Note **4**
VIN Voltage Range with Internal LDO	4	16	V	
VCC Supply Voltage Range	3.12	3.6	V	
Output Voltage Range	0.6	5.5	V	
Continuous Output Current Range		20	A	
OCP Limit (Valley)		24	A	
Peak current		28	A	
Operating Junction Temperature	-40	125	°C	

Note:

4. External bias voltage is connected to VCC pin.

7.2 Electrical characteristics

Note: Unless otherwise specified, the specifications apply over, Vin = 12 V, in -40 °C < Tj < 125 °C. Typical values are specified at Ta = 25 °C.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power Stage						
Top Switch	Rds(on)_top	V_{BST} – V_{SW} = 3.0 V, I_O = 10 A, Tj = 25 °C		8.5		mΩ
Bottom Switch	Rds(on)_bot	VCC = 3.0 V, Io = 10 A, Tj = 25 °C		2.7		
SW float voltage	Vsw	EN = 0 V			300	mV
		EN = high, No Switching			300	
Dead Band Time	Tdb	SW node rising edge, 10A, Note **5**		1.5		ns
		SW node falling edge, 10A, Note **5**		6		
Supply Current						
VIN Supply Current (standby)	Iin(standby)	EN = Low, No Switching, Tj = 25 °C		2.6	10	µA
VIN Supply Current (static)	Iin(static)	EN = 2 V, No Switching, Tj = 25 °C		1.04	1.2	mA
Soft Start						
Soft Start Sourcing current	Iss_source	SS = 0 V		42		uA
Soft Start Sinking current	Iss_sink	SS = 1 V		6.7		uA
Minimum SS time	Tss_min	Css = 1 nF, Tj = 25 °C	0.75	1	1.25	ms
Feedback Voltage						
Feedback Voltage	V_{REF}			0.6		V
Accuracy		0°C < Tj < 85 °C, Note **6**		0.5		%
		-40 °C < Tj < 125 °C, Note **6**		1		

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
On-Time Timer Control						
On Time	Ton	Vin = 12 V, Vout = 1 V, Fsw = 600 kHz Mode = VCC/GND, Note 7	133	142	149	ns
		Vin = 12 V, Vout = 1 V, Fsw = 800 kHz Mode = 243 kΩ/30.1 kΩ, Note 7	102	108	113	
		Vin = 12 V, Vout = 1 V, Fsw = 1000 kHz Mode = 121 kΩ/60.4 kΩ, Note 7	83	88.4	93	
Minimum On-Time	Ton(min)	Vfb = 500 mV		23		ns
Minimum Off-Time	Toff(min)	Vfb = 500 mV		180		ns
VCC LDO Output						
Output Voltage	Vcc		2.88	3.0	3.12	V
VCC load regulation		Icc = 25 mA, SS/VREF = 0V		0.5		%
Short Circuit current limit	Ishort	4 V ≤ Vin ≤ 16 V	135			mA
Foldback current limit	Ifoldback	Vin = 4 V, Tj = 25C		10		mA
Under Voltage Lockout						
VIN UVLO – Rising threshold	VIN_UVLO_Rise	Vcc = 3.2 V	2.1	2.4	2.7	V
VIN UVLO – Falling threshold	VIN_UVLO_Fall		1.55	1.85	2.15	
VCC-Start Threshold	Vcc_UVLO_Start	VCC Rising Trip Level	2.65	2.8	2.95	V
VCC-Stop Threshold	Vcc_UVLO_Stop	VCC Falling Trip Level	2.35	2.52	2.65	
Enable-Start-Threshold	En_UVLO_Start	ramping up	1.15	1.2	1.3	V
Enable Hysteresis	En_hysteresis			0.21		
Input Impedance	R_{EN}		500	1150	1800	kΩ
Over Current Limit						
Current Limit Threshold	Vcs		1.15	1.2	1.25	V
ICS to IOUT ratio	Gcs	Iout >= 5A	9	10	11	uA/A
Negative current limit	NOCP_OSM			-9		A
	NOCP_OVP			-10		A
Negative current limit timeout				Ton		ns
Output OVP and UVP						
OVP Trip Threshold	OVP_Vth	FB Rising	113	116	119	% V_{REF}
OSM Rising Threshold	OSM_Vth_Rising			104		
OSM Falling Threshold	OSM_Vth_Falling			102		
UVP Trip Threshold	UVP_Vth	FB Falling	77	80	83	
Hiccup Blanking Time	Tblk_Hiccup			11.5		ms
Power Good						
Pgood Turn on Threshold	VPG (upper)	FB Rising	89.5	92.5	95.5	% V_{REF}
Pgood Turn off Threshold	VPG (lower)	FB Falling	77	80	83	
		OVP Condition	113	116	119	
Pgood Voltage Low	VPG (low)	IPG = 10 mA, Powered ON			100	mV
		VIN = VCC = 0 V, IPG = 2 mA,		500	650	

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
		Rpull-up ≥ 2 kΩ to 3.3 V				
Pgood Turn on Delay	VPG (on)_Dly	FB Rising, see VPG (upper)	0.8	1	1.2	ms
Pgood Leakage Current		PG = 3.3 V			10	µA
Thermal Shutdown						
Thermal Shutdown		Note **5**		140	150	°C
Hysteresis		Note **5**		20		

Note:

5. *Guaranteed by construction and not tested in production.*
6. *Hot and cold temperature performance is guaranteed via correlation using statistical quality control. Not tested in production.*
7. *Ton is trimmed so that the target switching frequency of 800 kHz is achieved at around 4 A load current for a 12Vin and 1Vout operation.*

8 Typical efficiency and power loss curves

8.1 VIN = 12 V, Fsw = 800 kHz, Mode: DEM and FCCM

VIN = 12 V, VCC = internal LDO, Iout = 0 A – 20 A, Fsw = 800 kHz, room temperature, natural convection. Note that the efficiency and power loss curves include losses of the TDA38825, inductor losses, losses of the input and output capacitors, and PCB trace losses. The table below shows the inductors used for each of the output voltages in the efficiency measurement.

Table 1 Inductors for VIN = 12 V, Fsw = 800 kHz

Vout (V)	Lout (nH)	P/N	DCR (mΩ)	Size (mm)
0.6	100 nH	CMLB063T-R10MS	0.81	7.25 x 6.6 x 2.8
1.0	220 nH	CMLE063T-R22MS	1.15	7.25 x 6.6 x 2.8
1.8	240 nH	CMLE063T-R24MS	1.19	7.25 x 6.6 x 2.8
3.3	360 nH	CMLE063T-R36MS	2.3	6.95 x 6.6 x 2.8
5.0	470 nH	CMLE063T-R47MS	2.9	6.95 x 6.6 x 2.8

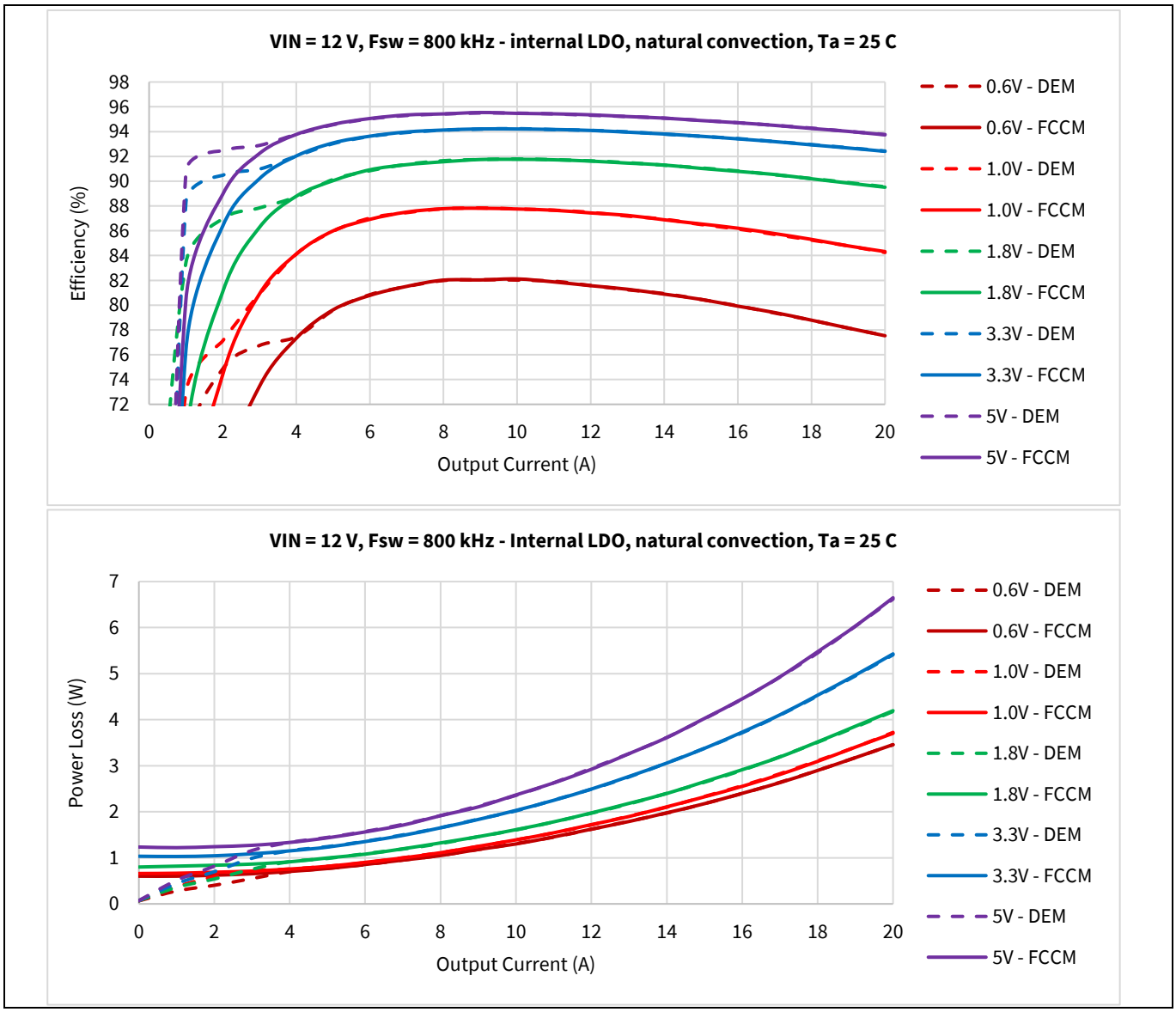


Figure 4 Efficiency and power loss

9 Thermal de-rating curves

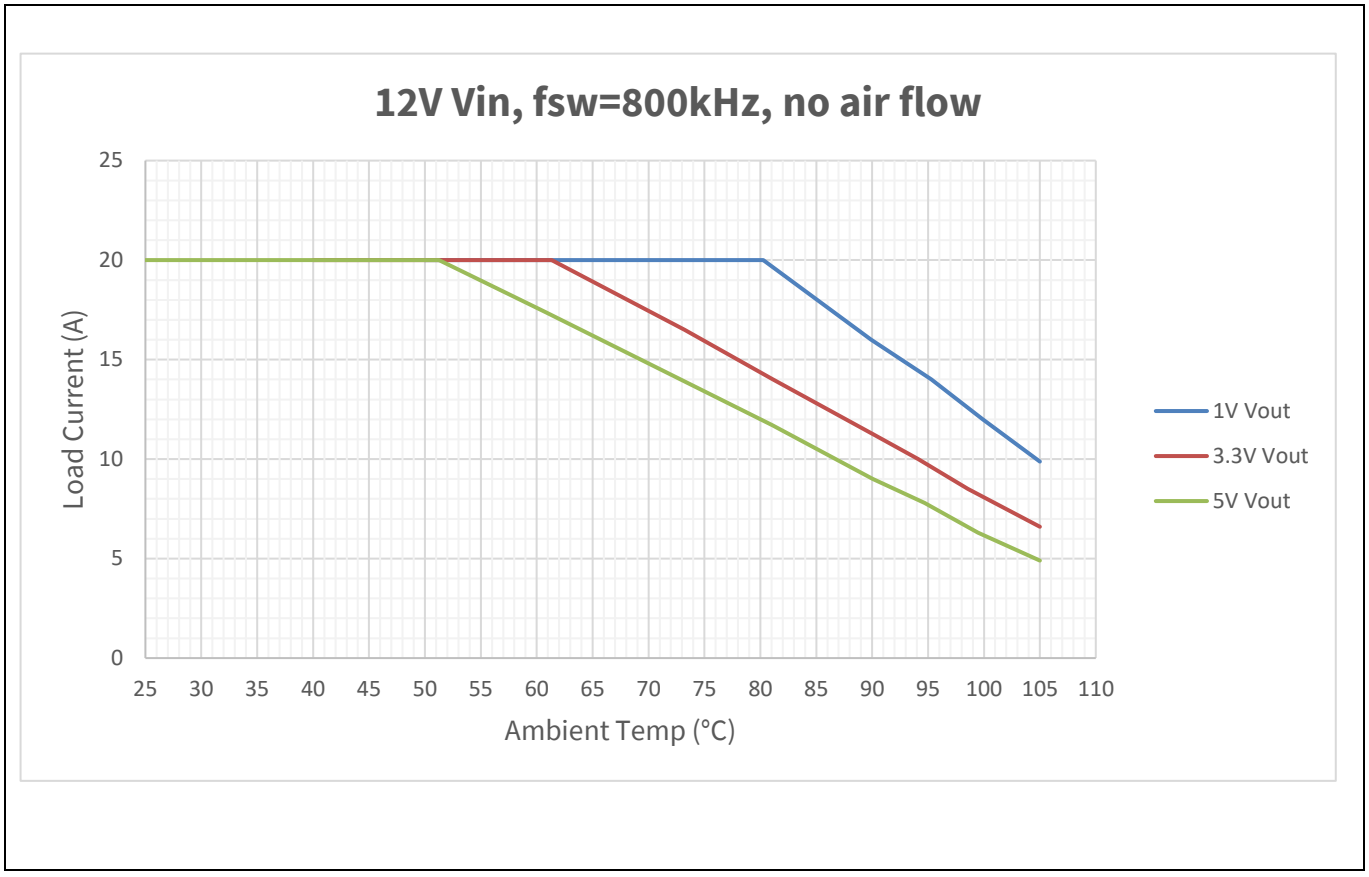


Figure 5 Thermal de-rating

10 $R_{DS(ON)}$ of MOSFET over temperature

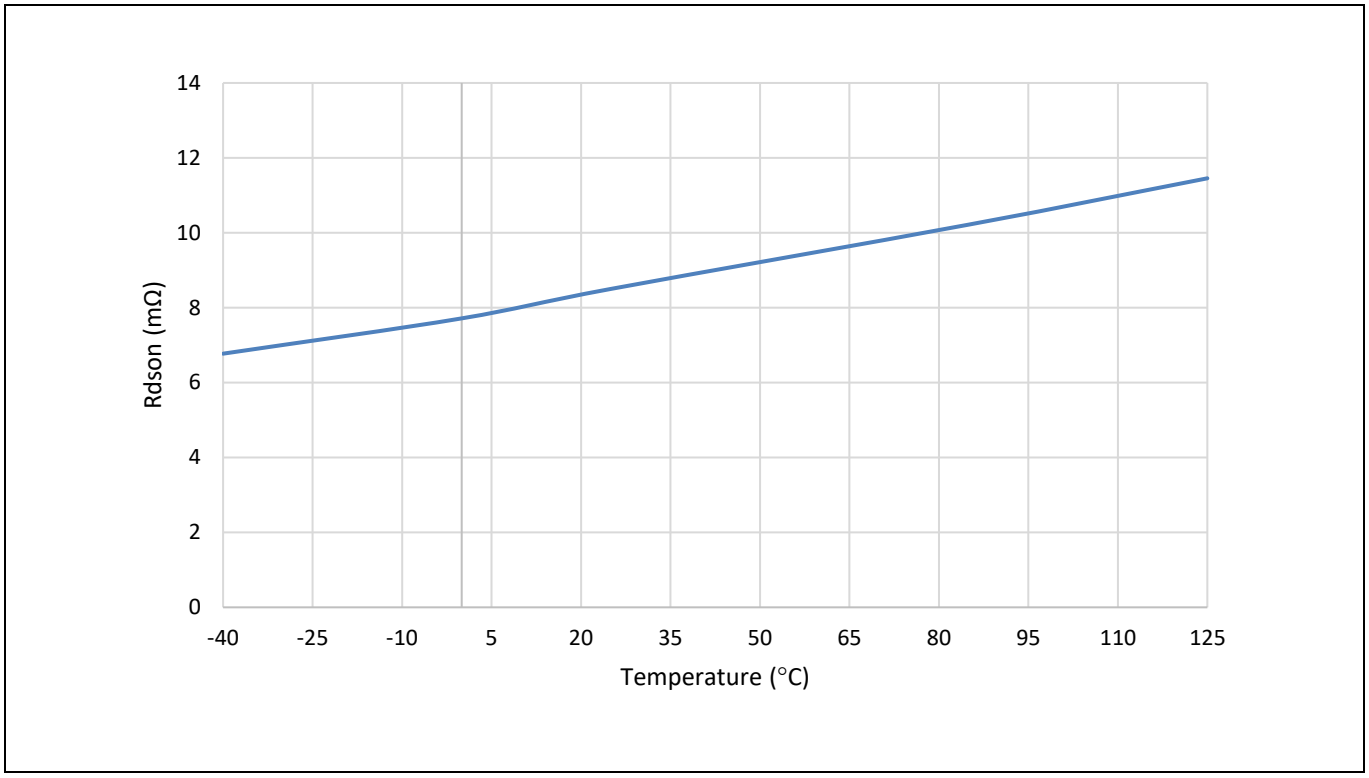


Figure 6 Control MOSFET (Q1) Rdson

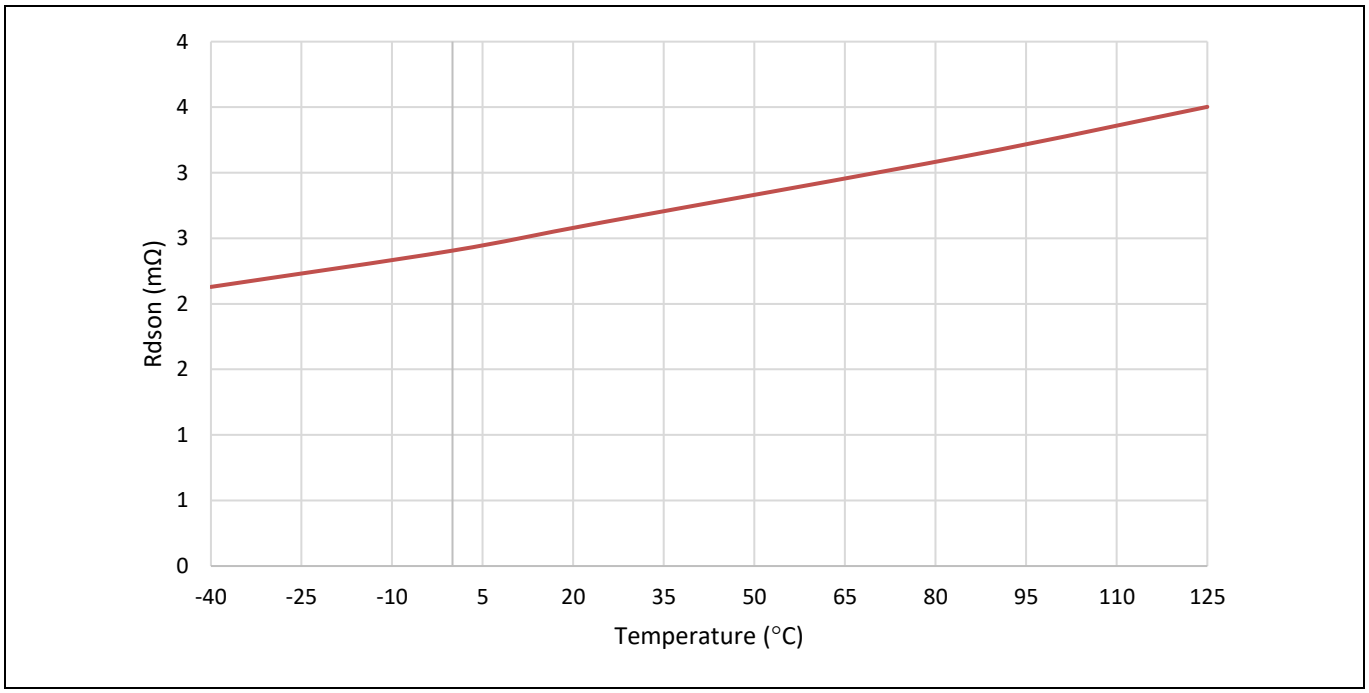


Figure 7 Synchronous MOSFET (Q2) Rdson

11 Theory of operation

11.1 Fast Constant On-Time Control

The TDA38825 features a proprietary fast Constant On-Time (COT) Control, which can provide fast load transient response, good output regulation and minimize the design effort. Fast COT control compares the output voltage (V_{OUT}) to a floor voltage combined with an internal ramp signal. When V_{OUT} drops below that signal, a PWM signal is initiated to turn on the high-side FET for a fixed on-time. The floor voltage is generated from an internal compensated error amplifier, which compares the V_{OUT} with a reference voltage. Compared to the traditional COT control, Fast COT control significantly improves output voltage regulation.

11.2 FCCM and DEM Operation

The TDA38825 offers two operation modes: Forced Continuous Conduction Mode (FCCM) and Diode Emulation Mode (DEM). With FCCM, the TDA38825 always operates as a synchronous buck converter with a pseudo-constant switching frequency leading to small output voltage ripple. In DEM, the synchronous FET is turned off when the inductor current is close to zero, reducing the switching frequency and improving efficiency at light load. At heavy load, both FCCM and DEM operate in the same way. The operation mode can be selected with the MODE pin, as shown in **Table 2**. It should be noted that the selection of the operation mode cannot be changed on the fly. To load a new MODE configuration, EN or VCC voltage must be cycled.

11.3 Pseudo-Constant Switching Frequency

The TDA38825 offers three programmable switching frequencies (F_{SW}) from 600 kHz to 1 MHz, by connecting an external resistor from the MODE pin to ground. Based on the selected F_{SW}, the TDA38825 generates the corresponding on-time of the Control FET (T_{ON}) for a given input voltage (V_{IN}) and V_{OUT}, as shown by the formula below.

$$T_{on} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{F_{SW}}$$

Where F_{SW} is the desired switching frequency. During operation, the TDA38825 monitors V_{IN} and V_{OUT}, and can automatically adjust the on-time to maintain the pre-selected F_{SW}. As load current increases, the switching frequency can increase to compensate for power losses.

Table 2 lists the configurations for MODE pin. In this table, E96 resistor with ±1% tolerance is used. To load a new MODE configuration, EN or VCC voltage must be cycled.

Table 2 Configuration of MODE Pin

MODE pin	Freq (kHz)	Mode
GND	600	FCCM
30.1 kΩ to GND	800	
60.4 kΩ to GND	1000	
VCC	600	DEM
243 kΩ to GND	800	
121 kΩ to GND	1000	

11.4 Enable

EN pin controls the on/off state of the TDA38825. An internal Under Voltage Lock-Out (UVLO) circuit monitors the EN voltage. When the EN voltage is above an internal threshold, the internal LDO starts to ramp up. When the VCC/LDO voltage rises above the VCC_UVLO_Start threshold, the soft-start sequence starts. The EN pin can be

configured in three ways, as shown in **Figure 8**. EN can be driven from an external source, as shown in Configuration 1. With configuration 2, the EN signal is derived from the VIN voltage by a resistor divider, R_{EN1} and R_{EN2}. By selecting different divider ratios, users can program a UVLO threshold for the bus voltage. This is a very desirable feature because it prevents the TDA38825 from operating until VIN is higher than a desired voltage level required to regulate the target output voltage. For some space-constrained designs, the EN pin can be directly connected to VIN without using the external resistor divider, as shown in Configuration 3. The EN pin should not be left floating. A pull-down resistor in the range of tens of kilohms is recommended.

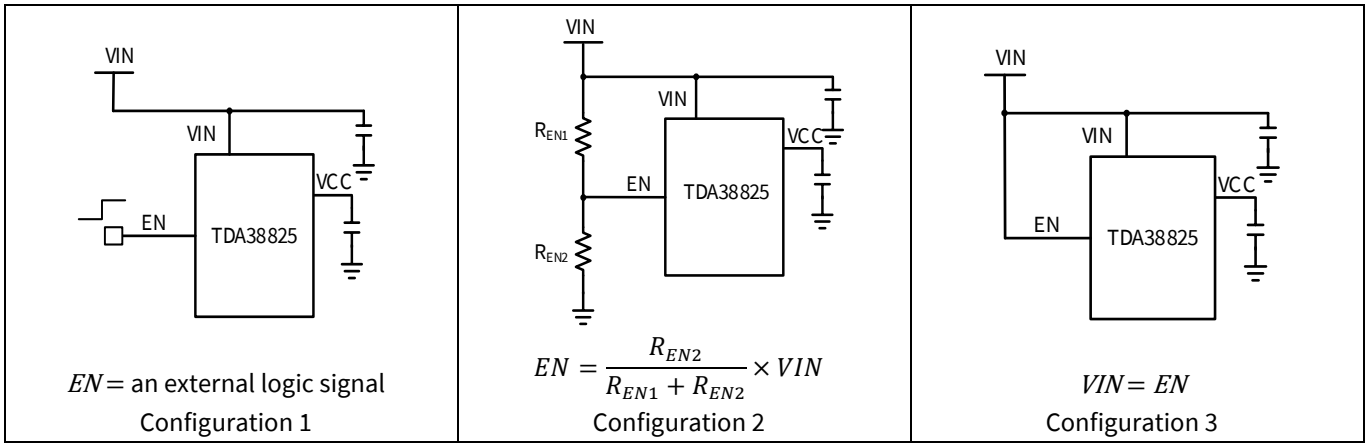


Figure 8 Enable Configurations

11.5 Soft start

The TDA38825 has an internal digital soft start to control the output voltage rise and to limit the current surge at start-up. To ensure proper start-up, the soft-start sequence initiates when the EN and VCC voltages rise above their respective thresholds. When EN and VCC rise above the threshold, the part does not soft start for 400 µs (typical) where it reads the MODE pin and any external reference voltage applied on SS/VREF pin. Then the internal soft start signal linearly rises from 0 V to 0.6 V in a defined time duration. The soft-start time does not change with the output voltage. During soft start, the TDA38825 operates in DEM until 0.9 ms after the output voltage ramps above the PGood turn-on threshold. The TDA38825 has a minimum soft start time of 1 ms. A longer soft start time can be set by adding capacitance between SS/VREF and GND. The soft start capacitance required can be calculated using,

$$C_{SS}\ (nF) = \frac{t_{SS}\ (ms) \times 36\mu A}{0.6\ (V)}$$

$$C_{SS} = C_{SS1} + C_{SS2}$$

where, C_{SS1} and C_{SS2} are recommended to be a minimum of 10 nF.

11.6 Pre-bias Start-up

The TDA38825 can start up into a pre-charged output without causing oscillations and disturbances of the output voltage. When the TDA38825 starts up with a pre-biased output voltage, both control FET and Sync FET are kept OFF until the SS/VREF voltage exceeds the FB voltage.

11.7 Voltage Tracking and External Reference

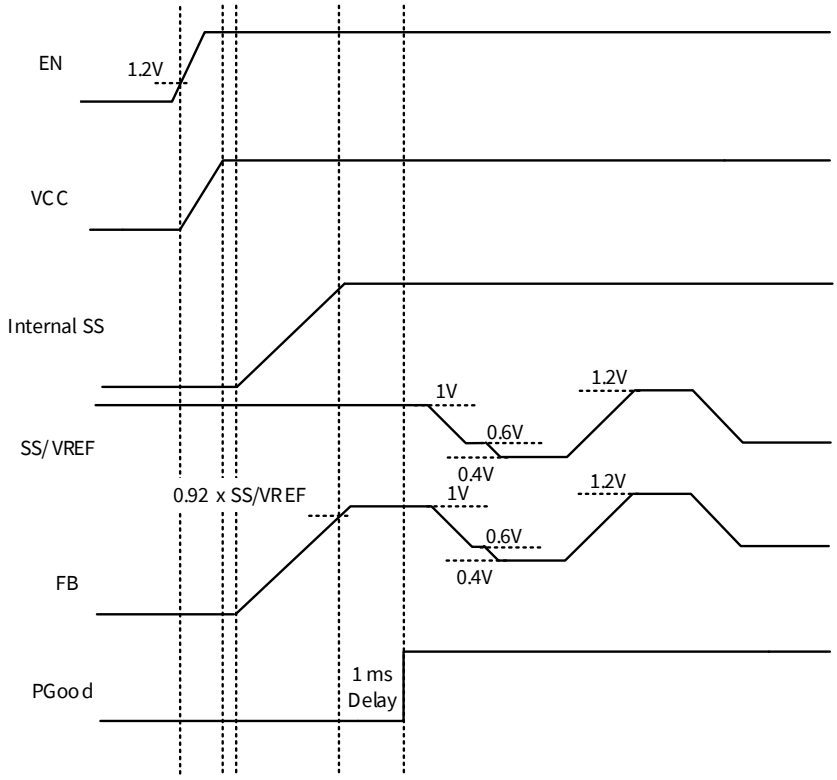
The TDA38825 supports voltage tracking and external reference voltage with the use of SS/VREF pin. When no external voltage is sensed on the SS/VREF pin, the part will use the internal reference voltage (0.6 V). When an external reference voltage is connected between SS/VREF and RGND, it acts as reference for the output voltage. The feedback (FB) voltage follows this external voltage signal.

During the power on delay, a detection circuit senses the voltage on the SS/VREF pin. Right before this sensing occurs, an internal 120 Ω resistor tries to discharge the voltage on SS/VREF pin for 100 µs. The discharge circuit makes sure that any left-over energy in the SS/VREF capacitor is not detected as the voltage reference. The detection circuit senses the SS/VREF voltage 40 µs after the discharge circuit is turned off. If the detection circuit senses the voltage on the SS/VREF pin to be higher than 92.5% of internal reference, it will use the SS/VREF pin voltage as the new reference for PGood, V_{OUT} OVP and UVP thresholds. The part powers up using internal soft start and PGood is high 1 ms after FB pin reaches the rising threshold.

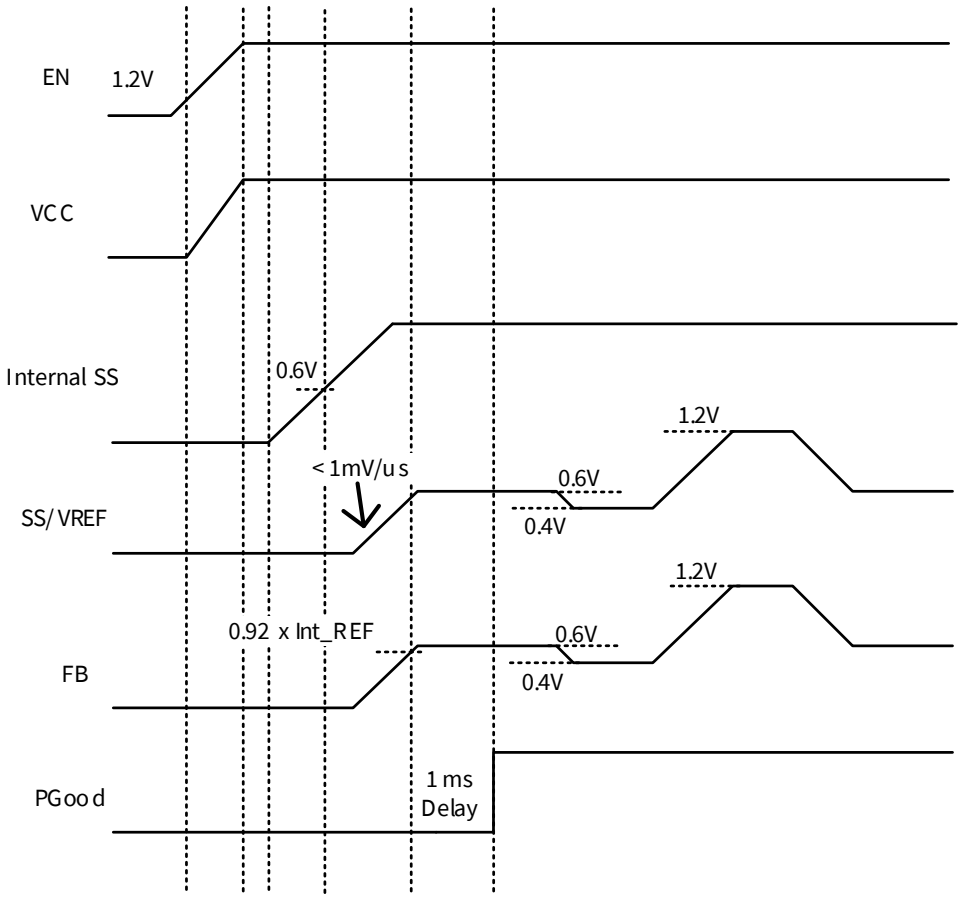
If the detection circuit senses the SS/VREF voltage to be lower than 92.5% of internal reference, it will use the internal reference voltage for the PGood, V_{OUT} OVP and UVP thresholds. For soft start, FB follows the slower one among the internal soft start or external SS/VREF pin. Once the Pgood is high, the reference voltage is transitioned from the internal reference to the voltage on SS/VREF pin.

During startup, the SS/VREF voltage must reach a minimum voltage equal to the internal reference (0.6 V) to ensure proper operation. After soft start is complete and PGood is high, the SS/VREF input signal can be in the range of 0.4 V to 1.2 V. The slew rate of the track voltage must be limited to 1 mV/us. To overdrive the SS/VREF during normal operation, the external source must be able to sink more than 36 µA of current when the external reference is lower than the internal reference. Or it should be able to source a current more than 12 µA when the external reference is higher than internal reference.

During ramping down of the external track voltage down to zero, the PGood goes low after the SS/VREF pin voltage reaches 100 mV. While tracking below 100 mV, the part would enter a latch off OVP and would require an EN or VCC recycle to power back up. During OCP/UVP hiccup retry or OTP retry, the part would sense the SS/VREF pin voltage and follow the typical startup procedure described above.



(a) Startup sequence with external reference

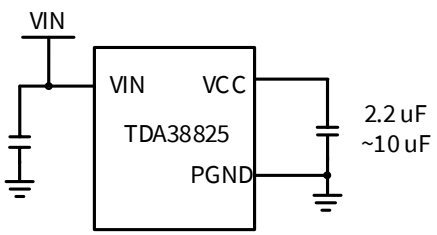


(b) Startup sequence with voltage tracking

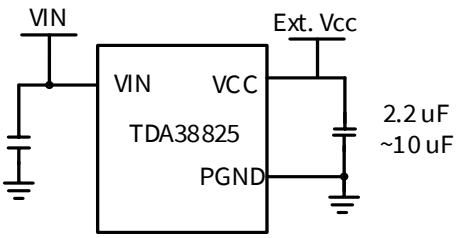
Figure 9 Startup sequence with external reference and voltage tracking

11.8 Internal Low-Dropout (LDO) Regulator

The TDA38825 has an integrated low-dropout (LDO) regulator, providing the bias voltage for the internal circuitry. To minimize standby current, the internal LDO is disabled when the EN voltage is pulled low. VIN pin is the input of the LDO. To save power losses on the LDO, an external bias voltage can be used by connecting directly to the VCC pin. Figure 10 illustrates the configuration of VCC, and VIN pin for internal LDO and external Vcc operation.



Single rail operation with the internal LDO



Use an external VCC

Figure 10 Configuration of using the internal LDO or an external VCC

Section **7.1** specified the recommended operating voltage range of VIN and VCC pin under different configurations. The following design guidelines are recommended when configuring the VCC.

- Place a bypass capacitor to minimize the disturbance on the VCC pin.
- For both operation using the internal LDO and external Vcc, a 2.2 uF~10 uF low ESR ceramic capacitor is required to be placed close to the VCC with reference to PGND.

The internal LDO has two current limits, i.e., a short circuit current limit and a foldback current limit. Foldback current limit is much lower than the short circuit current limit. The transition between the two limits is based on the VCC UVLO rising and falling thresholds. During startup, the LDO ramps up with the foldback current limit. Once the LDO voltage is above the VCC UVLO rising threshold, it transitions to the short circuit current limit. In case of short on LDO, the current is limited to short circuit current limit until the LDO voltage drops below the VCC UVLO falling threshold. Beyond which, the fold back current limit is enabled. These two limits help protect the LDO during any fault conditions.

11.9 Current Sense (CS) and Over Current Protection (OCP)

During the ON time of the Synchronous MOSFET, the inductor current is sensed and mirrored to CS pin with the ratio of G_{CS}. By using an external resistor (R_{CS}) from CS to AGND, the voltage on CS pin (V_{CS}) is proportional to the SW current cycle-by-cycle. The Control MOSFET is only allowed to turn on when V_{CS} is below the internal OCP voltage threshold of 1.2V (during the ON state of Synchronous MOSFET) to limit the SW valley current cycle-by-cycle. The resistor R_{CS} can be calculated as below.

$$R_{CS}(\Omega) = \frac{V_{CS}}{G_{CS} \times \left(I_{LIM} - \left(\frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \times \frac{1}{2 \times L \times F_{SW}} \right) \right)}$$

where, V_{CS} is 1.2 V, G_{CS} = 10 µA/A, and ILIM is the desired DC current limit.

OCP hiccup is active 3 ms after the device is enabled. Once OCP hiccup is active, if the device detects over current condition for consecutive 40 cycles, or if the FB drops below under voltage protection (UVP) threshold, it enters hiccup mode and Pgood flags low. In hiccup mode, the device latches off the Control MOSFET immediately, and latches off the Synchronous MOSFET after ZCD (zero crossing detection) is detected. Meanwhile, the SS/VREF capacitor is also discharged. After about 11 ms, the device will try to soft stat automatically. If the over current condition still holds after 3 ms of running, the device repeats this operation cycle until the over current condition disappears, and the output voltage rises smoothly back to the regulation level.

11.10 Under Voltage Protection (UVP)

Under Voltage Protection (UVP) provides additional protection during OCP fault or other faults. UVP protection is enabled when the soft-start reference rises above 160 mV. UVP circuitry monitors FB voltage. When FB is below the UVP threshold for 5 µs (typical), an undervoltage trip signal is triggered. PGood is pulled low after a delay of ~2 µs. The part continues to switch for ~5 µs after PGood is pulled low. Then the Control MOSFET is turned OFF and the Synchronous MOSFET is turned OFF after ZCD (zero crossing detection) is detected. Also, the SS/VREF capacitor is discharged. Then the TDA38825 enters hiccup mode with a blanking time of 11 ms, during which the Control MOSFET and the Synchronous MOSFET remain off. After the completion of blanking time, the TDA38825 attempts to recover to the nominal output voltage with a soft start, as shown in **Figure 11**. The TDA38825 will repeat hiccup mode and attempt to recover until the UVP condition is removed.

11.11 Output Voltage Discharge

The device enters output voltage discharge mode when it is disabled through EN. Both Control and Synchronous MOSFETs are latched OFF. A discharge FET connected between SW and PGND is turned on to discharge the output voltage. The typical switch ON resistance of the FET is about 80 Ω. Once FB voltage drops below 10% of SS/VREF, the discharge FET is turned OFF.

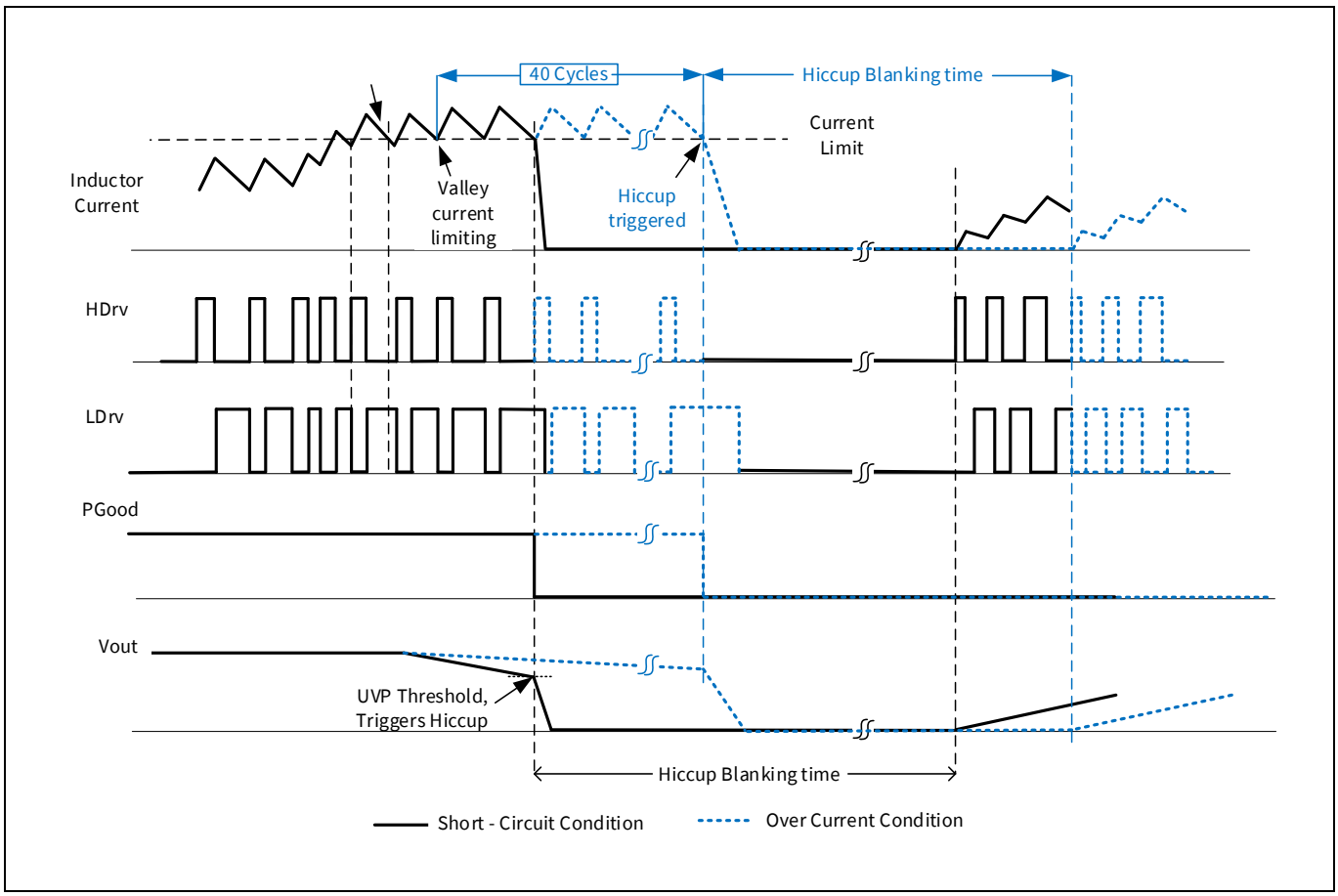


Figure 11 Cycle-by-cycle OCP response

11.12 Output Sinking Mode (OSM)

When the FB voltage is higher than 104% SS/VREF voltage but is below the OVP threshold, it triggers Output Sinking Mode. During OSM operation, the Synchronous MOSFET remains ON to discharge the output until it hits the -9 A negative current limit (NOCP_OSM). When it hits -9 A limit, the Synchronous MOSFET is turned OFF and Control MOSFET is turned ON for TON time. Then the Control MOSFET is turned OFF and Synchronous MOSFET is turned back ON. The device keeps this operation until the FB drops below 102% SS/VREF. Once FB drops below 102% SS/VREF, the device exits OSM.

11.13 Over Voltage Protection (OVP)

The OVP comparator becomes active after the SS/VREF voltage reaches 0.6 V. TDA38825 has a Latched OVP response, i.e., when OVP is triggered, the Control FET remains latched off until either VCC voltage or the EN signal is cycled.

Over Voltage Protection (OVP) is achieved by comparing the FB voltage to an OVP threshold voltage. When the FB voltage exceeds the OVP threshold, an over voltage trip signal is asserted after 4 µs (typical) delay. The Control MOSFET is latched OFF and PGood flags low. The Synchronous MOSFET remains ON to discharge the output until it hits the -10 A negative current limit (NOCP_OVP). When it hits -10 A limit, the Synchronous MOSFET is turned OFF and Control MOSFET is turned ON for TON time. Then the Control MOSFET is turned OFF and Synchronous MOSFET is turned back ON. This operation is repeated until the FB voltage drops below 50% of the SS/VREF voltage. When FB voltage drops below 50% of the reference voltage, Synchronous MOSFET is turned OFF if the part is operating in DEM. If operating in FCCM, it repeats the switching behavior (Synchronous MOSFET turned ON until the NOCP limit is hit, then turn OFF Synchronous MOSFET and turn control MOSFET ON for TON time) until FB is discharged to 10% of the reference voltage. After that Control MOSFET stays latched OFF. If ever the FB rises above the OVP threshold in this state, the response is repeated.

11.14 Negative Over Current Limit (NOCP)

The TDA38825 offers negative over current limit protection. When the device detects the current in the synchronous MOSFET is at the negative current limit, it turns off the Synchronous MOSFET to limit the negative current. Under normal operation or in the case of an OSM event, the negative current is limited at -9 A. In the case of an OVP event, the negative current is limited at -10 A.

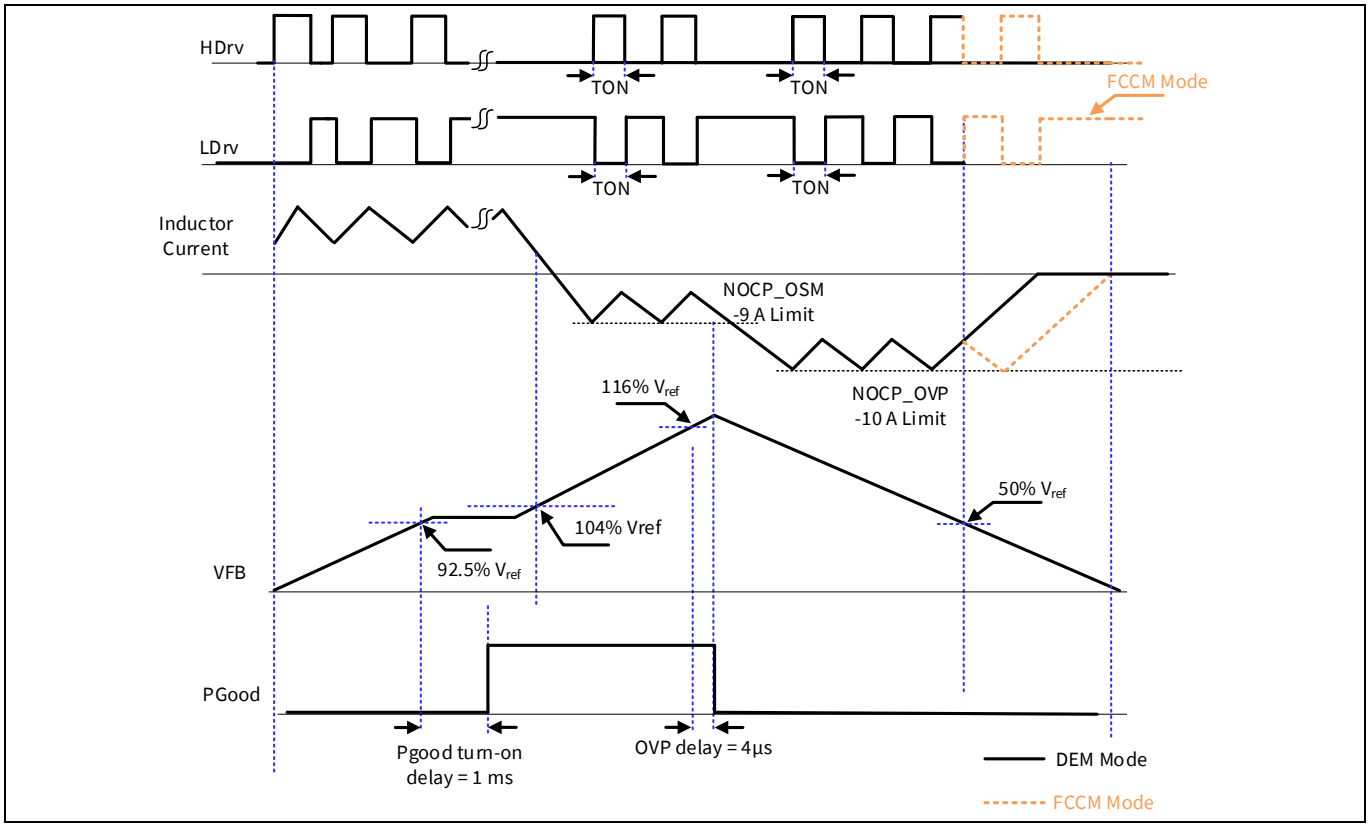


Figure 12 Over-voltage protection response

11.15 Over Temperature Protection (OTP)

Temperature is monitored internally on TDA38825. When the temperature exceeds the over temperature threshold, OTP circuitry turns off the Control MOSFET immediately and the Synchronous MOSFET is turned off after ZCD (zero crossing detection) is detected. Also, the SS/VREF capacitor is discharged. Automatic restart is initiated when the sensed temperature drops back into the operating range. The thermal shutdown threshold has a hysteresis of 20 °C.

11.16 Power Good (PGood) Output

The PGood pin is the open drain of an internal NFET and must be externally pulled high through a pull-up resistor. The PGood signal is high when three criteria are satisfied:

1. EN signal and VCC voltage are above their respective thresholds.

2. No over voltage or over temperature faults occur.

3. V_{OUT} is within regulation.

To detect if V_{OUT} is in regulation, the PGood comparator continuously monitors FB voltage. When FB voltage ramps up above the upper threshold, the PGood signal is pulled high after 1 ms. When FB voltage drops below the lower threshold or rises above the OVP threshold, the PGood signal is pulled low. **Figure 11** and **Figure 12** illustrate the PGood response. During start-up with a pre-biased output voltage, the PGood signal is held low

before the first PWM is generated and is then pulled high with 1 ms delay after FB voltage rises above the PGood threshold.

A 10 kΩ or higher pull-up resistor is needed for a PGood bias voltage of 3.3V to maintain the PGood signal at logic low (below 0.7 V) when VIN = VCC = 0 V.

11.17 Minimum ON - Time and Minimum OFF - Time

The minimum on-time refers to the shortest time for the Control MOSFET to be reliably turned on. The minimum off-time refers to the minimum time duration in which the Synchronous FET stays on before a new PWM pulse is generated. The minimum off-time is needed for TDA38825 to charge the bootstrap capacitor, and to sense the current of the Synchronous MOSFET for OCP.

For applications requiring a small duty cycle, it is important that the selected switching frequency results in an on-time larger than the maximum spec of the minimum on-time in Section **7.1**. Otherwise, the resulting switching frequency may be lower than the desired target. The following formula should be used to check for the minimum on-time requirement.

$$\frac{V_{OUT}}{k \times F_{SW} \times V_{IN}} > \max\ spec\ of\ T_{ON(\min)}$$

Where F_{SW} is the desired switching frequency. k is the variation of the switching frequency. As a rule of thumb, select k = 1.25 to ensure design margin.

For applications requiring a high duty cycle, it is important to make sure a proper switching frequency is selected so that the resulting off-time is longer than the maximum spec of the minimum off-time in Section **7.1**, which can be calculated as shown below.

$$\frac{V_{IN} - V_{OUT}}{k \times F_{SW} \times V_{IN}} > \max\ spec\ of\ T_{OFF(\min)}$$

Where F_{SW} is the desired switching frequency. k is the variation of the switching frequency. As a rule of thumb, select k = 1.25 to ensure design margin.

The resulting maximum duty cycle is therefore determined by the selected on-time and minimum off-time.

$$D_{max} = \frac{T_{on}}{T_{on} + T_{off(\min)}}$$

11.18 Selection of Feedforward Capacitor and Feedback Resistors

Output voltage can be programmed with an external voltage divider. The FB voltage is compared to an internal reference voltage of 0.6 V. The divider ratio is set to provide 0.6 V at the FB pin when the output is at its desired value. The calculation of the feedback resistor divider is shown below.

$$V_o = V_{ref} \times (1 + \frac{R_{FB1}}{R_{FB2}})$$

Where R_{FB1} and R_{FB2} are the top and bottom feedback resistors. Recommended feedback resistors values is from 1kΩ to 20kΩ.

A small MLCC capacitor, Cff, is preferred in parallel with the top feedback resistor, RFB1, to provide extra phase boost and to improve the transient load response. The value of Cff is recommended to be 10 pF to 1nF. For higher output voltage, lower cff capacitor value is recommended.

12 Design Example

In this section, an example is used to demonstrate how to design a buck regulator with the TDA38825. The application circuit is shown in **Figure 13.**The design specifications are given below:

- VIN = 12 V (±10 %)
- V_o = 1.0 V
- I_o = 20 A
- V_o ripple voltage = ±1 % of V_o
- Load transient response = ± 3 % of V_o with a step load current = 4 A and slew rate = 2.5 A/µs

12.1 Enabling the TDA38825

The TDA38825 has a precise Enable threshold voltage, which can be used to implement a higher UVLO on the input bus voltage by connecting the EN pin to VIN with a resistor divider, as shown in Configuration 2 of **Figure 8**. The Enable feedback resistor, R_{EN1} and R_{EN2}, can be calculated as follows.

$$VIN_{(\min)} \times \frac{R_{EN2}}{R_{EN1} + R_{EN2}} \geq V_{EN(\max)}$$

$$R_{EN2} \geq R_{EN1} \times \frac{V_{EN(\max)}}{VIN_{(\min)} - V_{EN(\max)}}$$

Where $V_{EN\ (max)}$ is the maximum spec of the Enable-start-threshold as defined in Section **7.1**. For $VIN_{(min)}$ = 10 V, select R_{EN1} = 49.9 kΩ and R_{EN2} = 7.5 kΩ.

12.2 Selecting Input Capacitors

Without input capacitors, the pulse current of the Control MOSFET is provided directly from the input supply. Due to the impedance of the cable, the pulse current can cause disturbance on the input voltage and potential EMI issues. The input capacitors filter the pulse current, resulting in almost constant current from the input supply. The input capacitors should be selected to tolerate the input pulse current, and to reduce the input voltage ripple. The RMS value of the input ripple current can be expressed by:

$$I_{RMS} = I_o \times \sqrt{D \times (1 - D)}$$

$$D = \frac{V_o}{VIN}$$

Where I_{RMS} is the RMS value of the input capacitor current. I_o is the output current, and D is the Duty Cycle. For I_o = 20 A and $D_{(max)}$ = 0.083, the resulting RMS current flowing into the input capacitor is I_{rms} = 5.52 A.

To meet the requirement of the input ripple voltage, the minimum input capacitance can be calculated as follows.

$$C_{in(\min)} > \frac{I_o \times (1 - D) \times D}{f_{sw} \times (\Delta VIN - ESR \times I_o \times (1 - D))}$$

Where ΔVIN is the maximum allowable peak-to-peak input ripple voltage, and ESR is the equivalent series resistance of the input capacitors. Ceramic capacitors are recommended due to low ESR, ESL and high RMS current capability. For I_o = 20 A, f_{sw} = 800 kHz, ESR = 2 mΩ, and VIN = 120 mV, $C_{in(min)}$ > 22 µF. To account for the

derating of ceramic capacitors under a bias voltage, ten 22 µF/0805/25V MLCC are used for the input capacitors. In addition, a bulk capacitor is recommended if the input supply is not located close to the voltage regulator.

12.3 Inductor Selection

The inductor is selected based on output power, operating frequency, and efficiency requirements. A low inductor value results in a large ripple current, lower efficiency, and high output noise, but helps with size reduction and transient load response. Generally, the desired peak-to-peak ripple current in the inductor (Δi) is found between 20% and 50% of the output current.

The inductor saturation current must be higher than the maximum spec of the OCP limit plus the peak-to-peak inductor ripple current. For some core material, inductor saturation current may decrease with increasing temperature. It is important to check the inductor saturation current at the maximum operating temperature.

The inductor value for the desired operating ripple current can be determined using the following relations:

$$L = (V_{in(\max)} - V_o) \times \frac{D_{min}}{\Delta i_{L(\max)} \times F_{sw}}$$

$$D_{min} = \frac{V_o}{V_{in(\max)}}$$

$$I_{sat} \geq OCP_{max} + \Delta i_{L(\max)}$$

Where: $VIN_{(max)}$ = Maximum input voltage; ΔiL_{max} = Maximum peak-to-peak inductor ripple current; OCP_{max} = maximum spec of the OCP limit as defined in Section **7.1**; and I_{sat} = inductor saturation current. In this case, select inductor L = 220 nH to achieve ΔiL_{max} = 26% of I_{omax}. The I_{sat} should be no less than 26 A.

12.4 Output Capacitor Selection

The output capacitor selection is mainly determined by the output voltage ripple and transient requirements.

To satisfy the V_o ripple requirement, C_o should satisfy the following criterion:

$$C_o > \frac{\Delta i_{Lmax}}{8 \times \Delta V_{or} \times f_{sw}}$$

Where ΔV_{or} is the desired peak-to-peak output ripple voltage. For ΔiL_{max} = 5.2 A, ΔV_{or} = 10 mV, f_{sw} = 800 kHz, C_o must be larger than 82 µF. The ESR and ESL of the output capacitors, as well as the parasitic resistance or inductance due to PCB layout, can also contribute to the output voltage ripple. It is suggested to use Multi-Layer Ceramic Capacitor (MLCC) for their low ESR, ESL and small size.

To meet the transient response requirements, the output capacitors should also meet the following criterion:

$$C_o > \frac{L \times \Delta I_{o(\max)}^2}{2 \times \Delta V_{oL} \times V_o}$$

Where ΔV_{OL} is the allowable V_o deviation during the load transient. $\Delta I_{o(max)}$ is the maximum step load current. Please note that the impact of ESL, ESR, control loop response, transient load slew rate, and PWM latency is not considered in the calculation shown above. Extra capacitance is usually needed to meet the transient requirements. As a rule of thumb, we can triple the C_o that is calculated above as a starting point, and then optimize the design based on bench measurement. In this case, to meet the transient load requirement (i.e. ΔV_{OL}= 30 mV, $\Delta I_{o(max)}$ = 10 A), select C_o = ~366 µF. For more accurate estimation of C_o, simulation tools should be used to aid the design.

12.5 Output Voltage Programming

Output voltage can be programmed with an external voltage divider. The FB voltage is compared to an internal reference voltage of 0.6 V. The divider ratio is set to provide 0.6 V at the FB pin when the output is at its desired value. The calculation of the feedback resistor divider is shown below.

$$V_o = V_{ref} \times (1 + \frac{R_{FB1}}{R_{FB2}})$$

Where R_{FB1} and R_{FB2} are the top and bottom feedback resistors. Select R_{FB1} = 10 kΩ and R_{FB2} = 15 kΩ, to achieve V_o = 1.0 V. The same resistor divider can be used at the VSNS pin to achieve the same voltage scaling factor.

12.6 Feedforward Capacitor

A small MLCC capacitor, C_{ff}, can be placed in parallel with the top feedback resistor, R_{FB1}, to improve the transient response. With Lo = 220 nH, Co = 470 µF and R_{FB1} = 10 kΩ, C_{ff} = ~220 pF. C_{ff} can be further optimized based on bench testing of transient load response.

12.7 Bootstrap Capacitor

For most applications, a 0.1 µF ceramic capacitor is recommended for bootstrap capacitor placed between SW and BOOT.

12.8 VCC bypass Capacitor

Please see the recommendation in **Section 11.8**. A 2.2 µF MLCC is selected for the VCC/LDO bypass capacitor and a 2.2 µF MLCC is selected for the VIN bypass capacitor.

12.9 Pgood Resistor

The recommended value for Pgood resistor is 10 kΩ and above. 10 kΩ resistor is selected for the Pgood resistor.

12.10 SS/Vref Capacitor

Soft start can be programmed with an external capacitor at SS/Vref pin. The calculation of the soft start capacitor is shown below.

$$C_{SS}\ (nF) = \frac{t_{SS}\ (ms) \times 36\mu A}{0.6\ (V)}$$

$$C_{SS} = C_{SS1} + C_{SS2}$$

For 2.2ms soft start, 68nF of two numbers of soft start capacitor are connected. Minimum value of 10nF capacitor value is recommended between SS/Vref pin to RGND and SS/Vref pin to AGND.

12.11 Current Sense Resistor

Following equation is used to calculate current sense resistor.

$$R_{CS}(\Omega) = \frac{V_{CS}}{G_{CS} \times \left(I_{LIM} - \left(\frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \times \frac{1}{2 \times L \times F_{SW}}\right)\right)}$$

where, V_{CS} is 1.2 V, G_{CS} = 10 µA/A, and ILIM is the desired DC current limit.

5.49kΩ resistor is selected for 24A current limit.

13 Application Information

13.1 Application Diagram

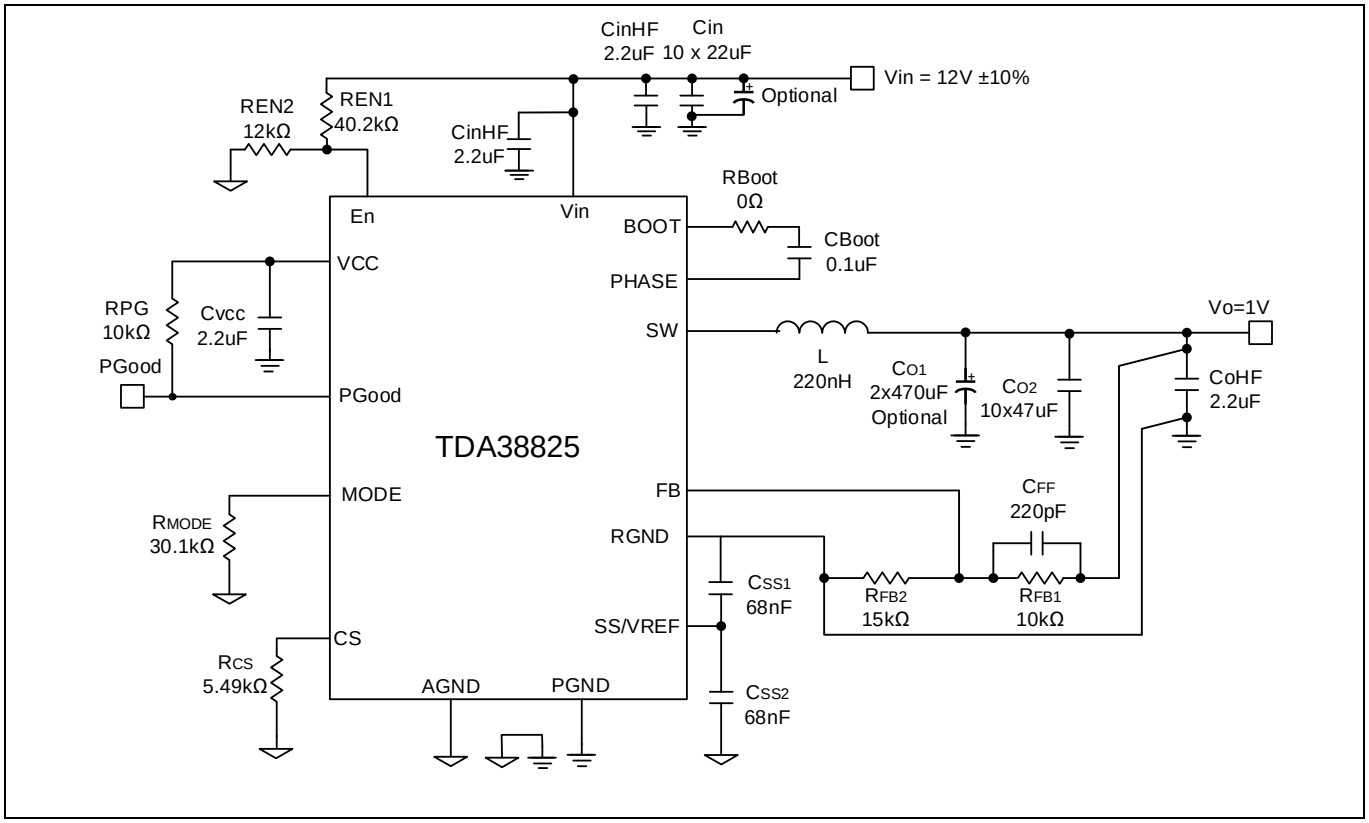


Figure 13 Typical application diagram of TDA38825. Vin = 12 V, Vo = 1V, Io = 20 A, Fsw = 800 kHz.

13.2 Typical Operating Waveforms

V_{in} = 12.0 V, Vo = 1 V, I_o = 20 A, F_{sw} = 800 kHz, Room Temperature, no airflow

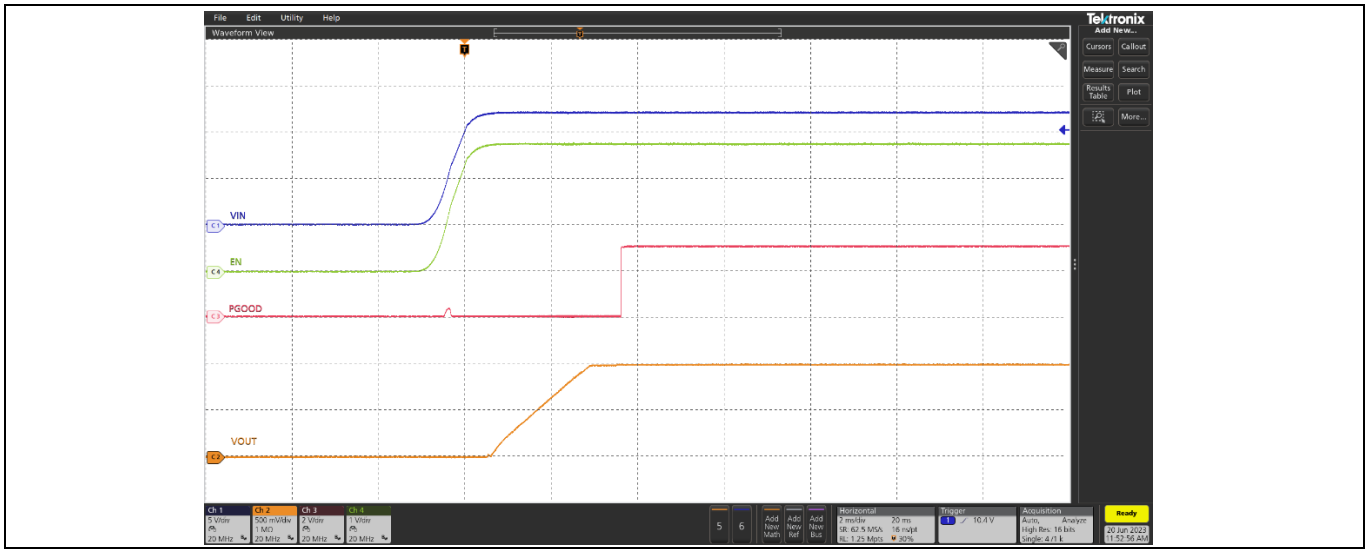


Figure 14 Start up at 20 A Load, (Ch1: Vin, Ch2: Vout, Ch3: PGood, Ch4: Enable)

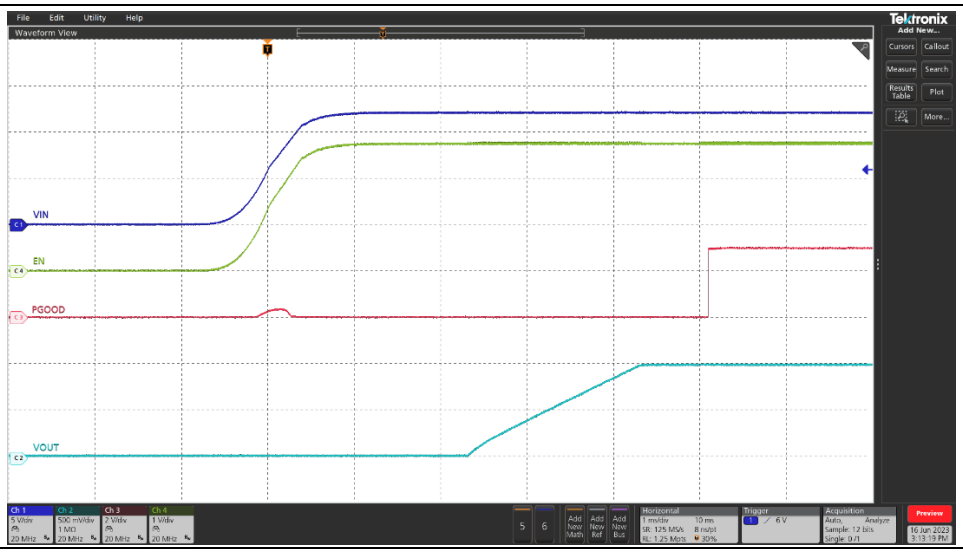


Figure 15 Start up at 0 A Load, (Ch1: Vin, Ch2: Vout, Ch3: PGood, Ch4: Enable)

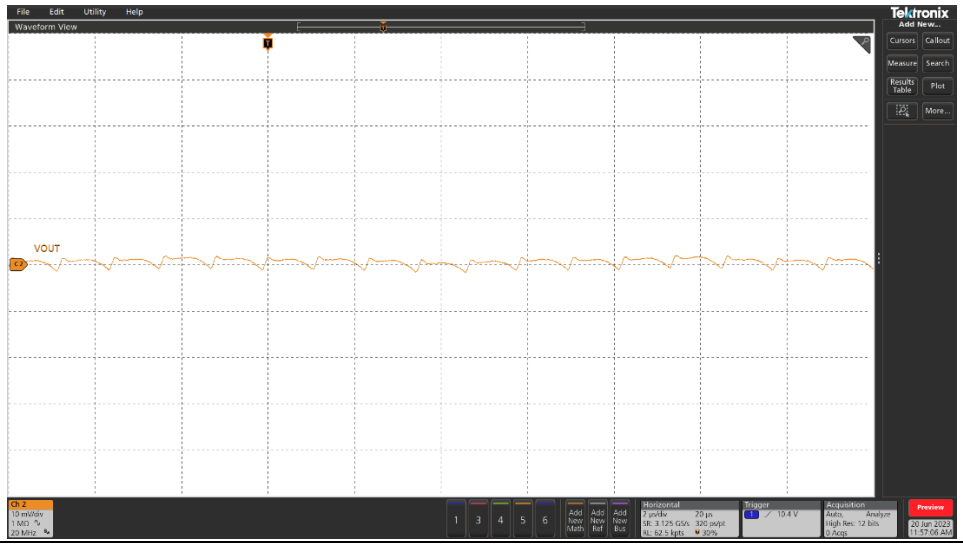


Figure 16 Vout ripple at 20A Load, Fsw = 800 kHz, (Ch2: Vo)

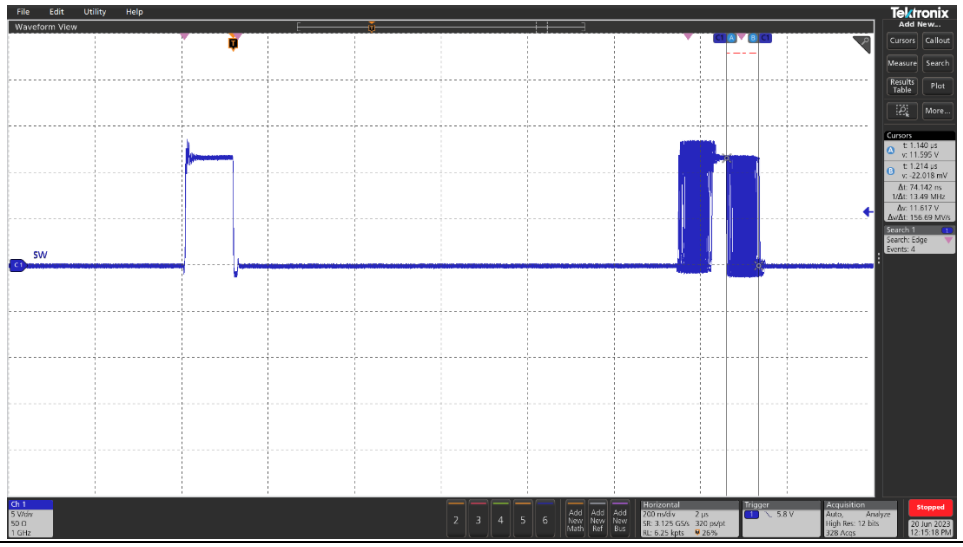


Figure 17 SW node jitter, 20A load, Fsw = 800 kHz

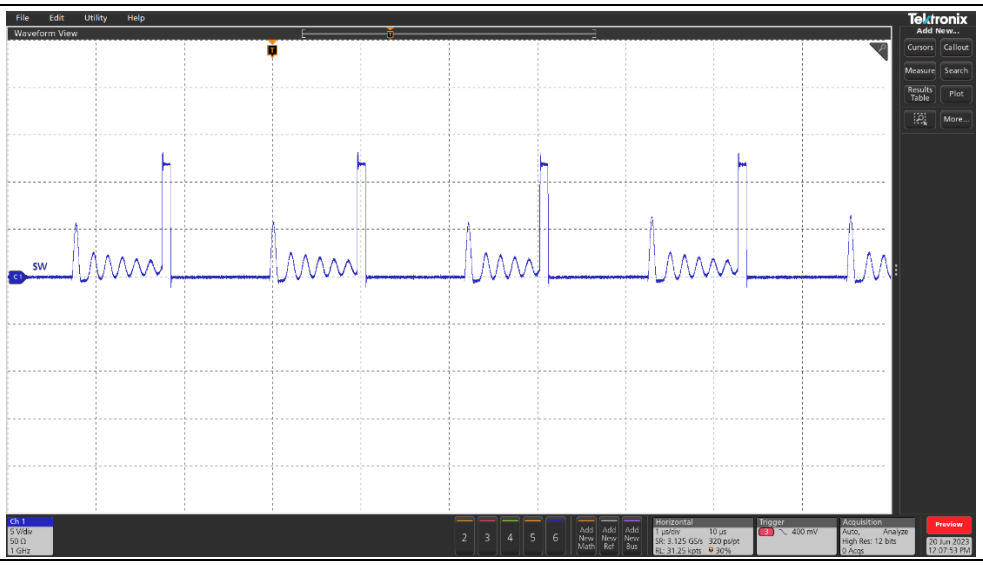


Figure 18 SW node (in DEM), 1 A load

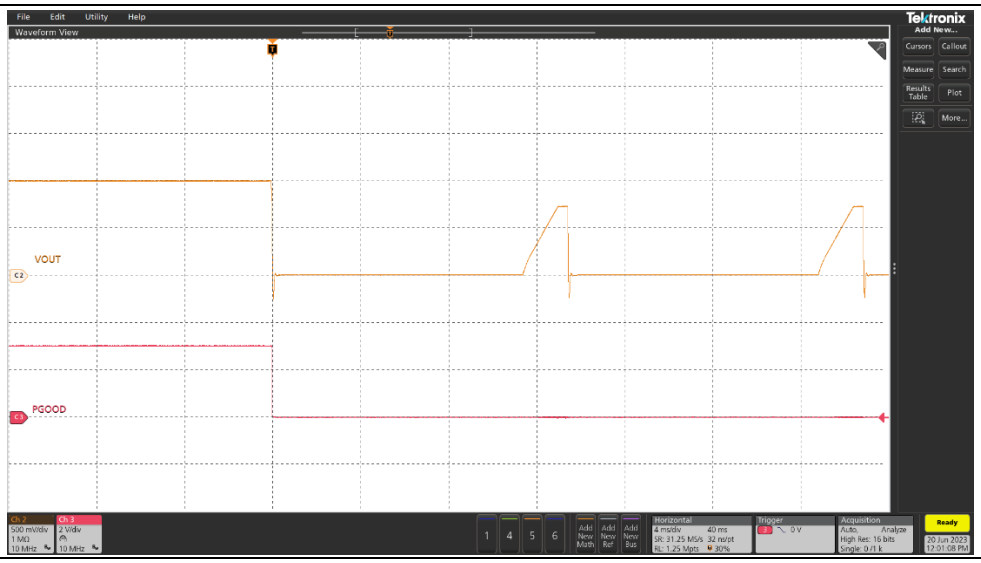


Figure 19 Short circuit and UVP (Hiccup), (Ch2: Vo, Ch3: PGood)

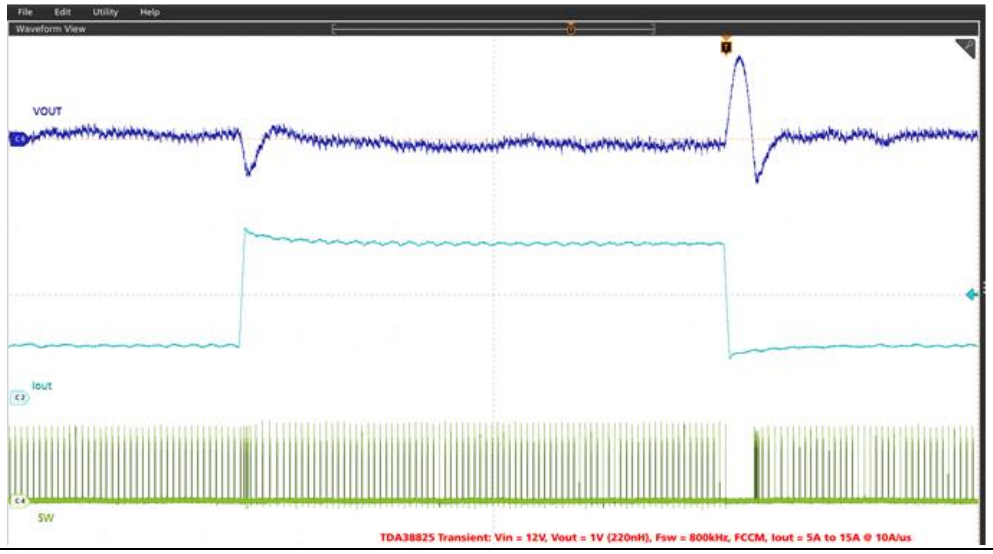


Figure 20 Transient response at 10 A step load current @ 10 A/µs slew rate: Io= 5 A – 15 A, (Ch6: Vo, Ch2: Io, Ch4: SW), pk-pk: 39.4 mV, Fsw = 800 kHz

14 Layout Recommendations

PCB layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results. Following design guidelines are recommended to achieve the best performance.

- Bypass capacitors, including input/output capacitors, VIN and VCC bypass capacitors, should be placed near the corresponding pins as close as possible.
- Place bypass capacitors from TDA38825 power input (Drain of Control MOSFET) to PGND (Source of Synchronous MOSFET) to reduce noise and ringing in the system. The output capacitors should be terminated to a ground plane that is away from the input PGND to mitigate the switching spikes on the Vout. The bypass capacitor shared by VCC should be terminated to PGND.
- Place a boot strap capacitor near the TDA38825 BST and SW pin as close as possible to minimize the loop inductance.
- SW node copper should only be routed on the top layer to minimize the impact of switching noise.
- Connect AGND pin to the PGND pad through a single point connection, using a wider trace. Keep the trace length to minimum and place it right underneath the AGND and PGND pins.
- Via holes can be placed on VIN and PGND pads to aid thermal dissipation.
- Wide copper polygons are desired for VIN and PGND connections in favor of power losses reduction and thermal dissipation. Sufficient via holes should be used to connect power traces between different layers.
- The EN pin and configuration pins including SS/VREF, MODE, and CS should be terminated to a quiet ground.

Following figures illustrate the PCB layout design of the TDA38825 standard demo board.

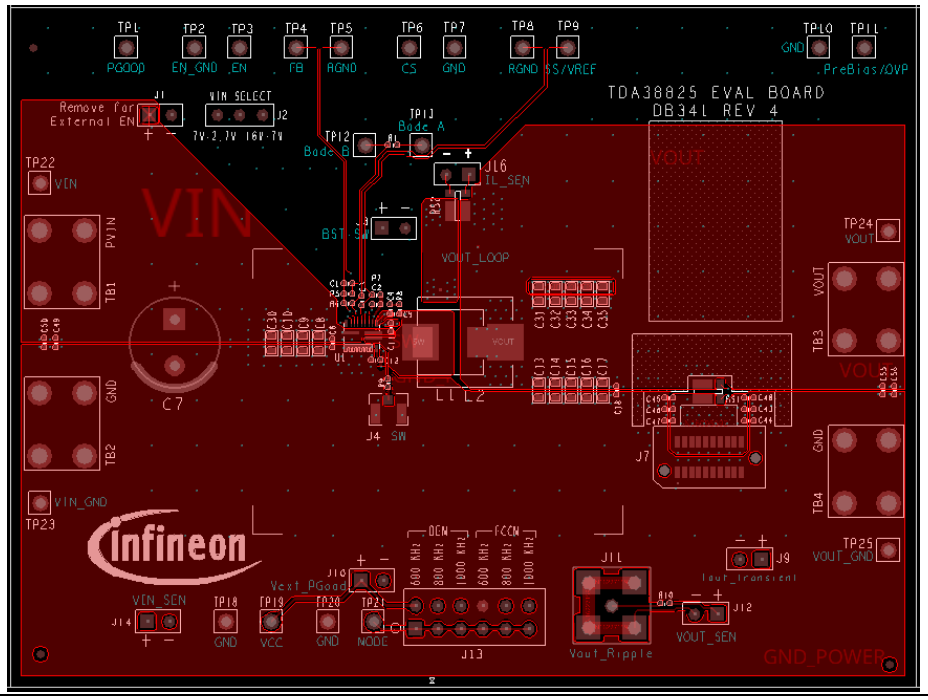


Figure 21 TDA38825 Demo Board – Top Layer

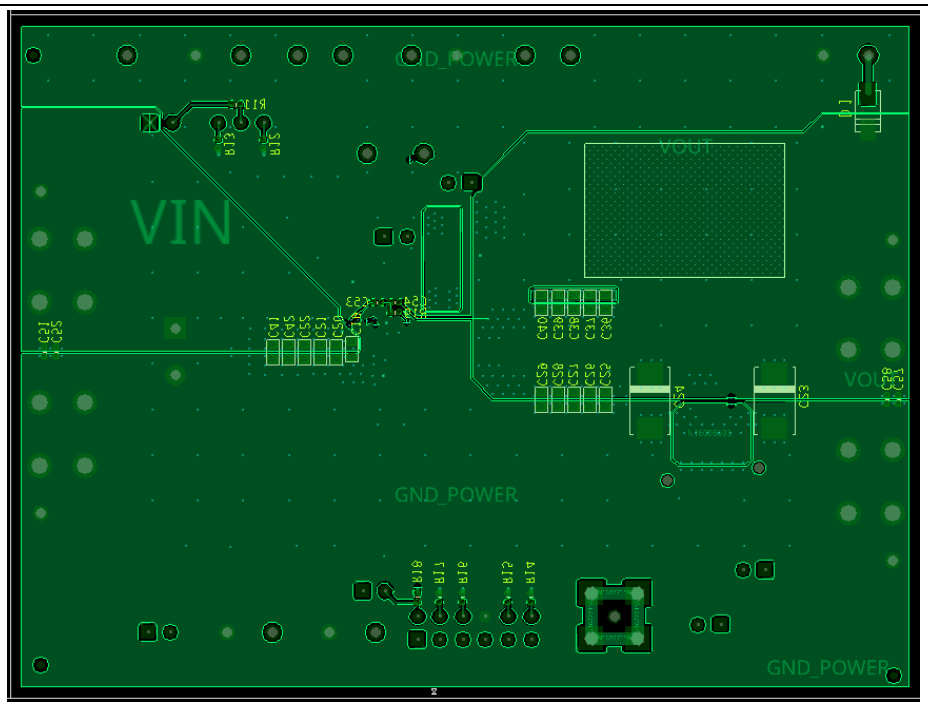


Figure 22 TDA38825 Demo Board – Bottom Layer

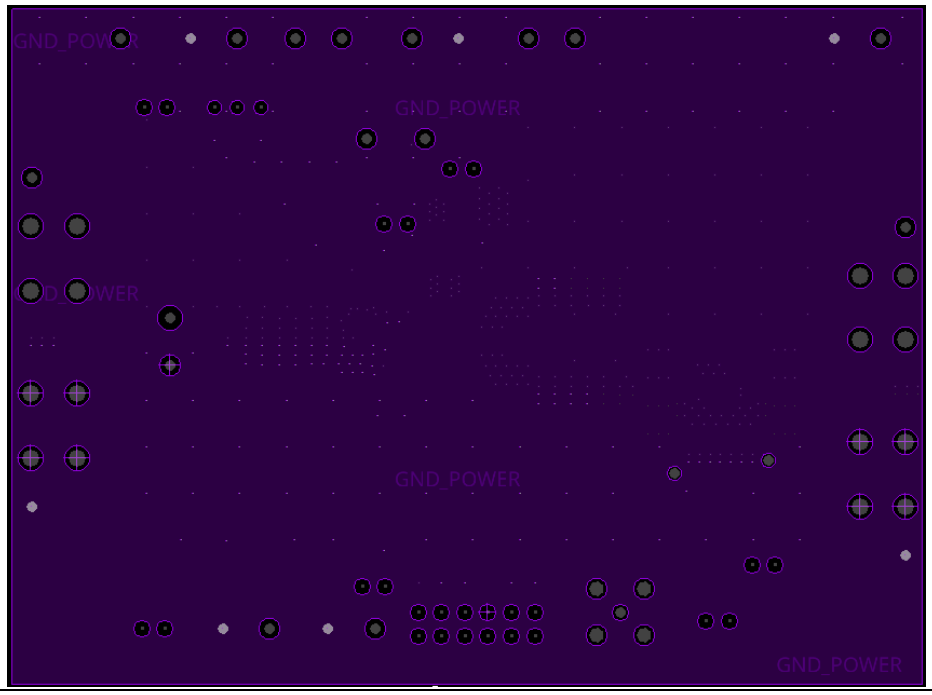


Figure 23 TDA38825 Demo Board – 2nd Layer (Ground)

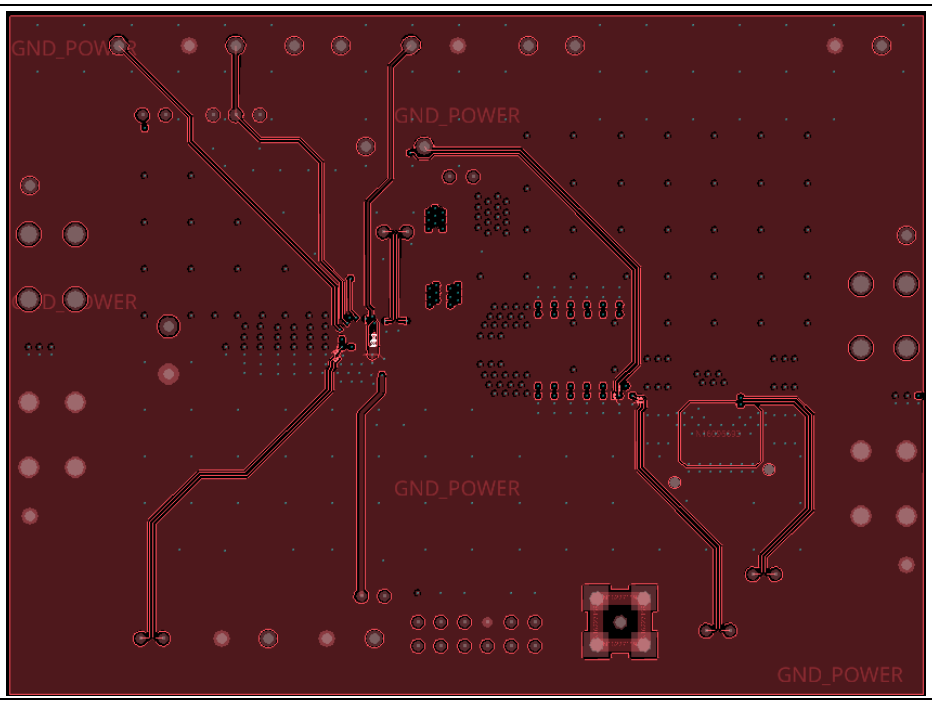


Figure 24 TDA38825 Demo Board – 3rd Layer (Ground & Signal)

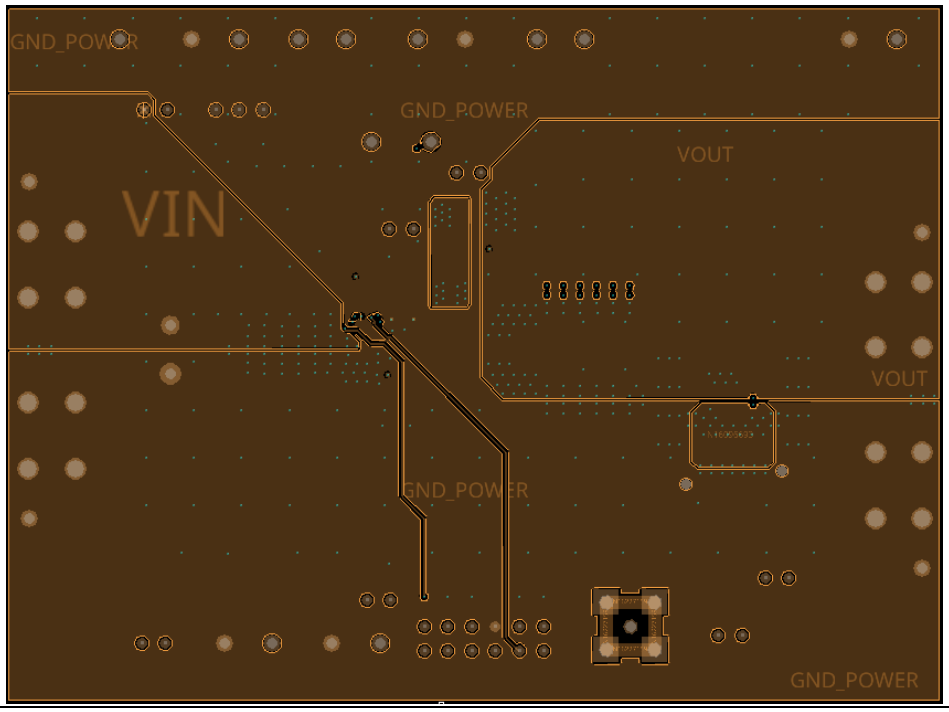


Figure 25 TDA38825 Demo Board – 4th Layer (Ground & Signal)

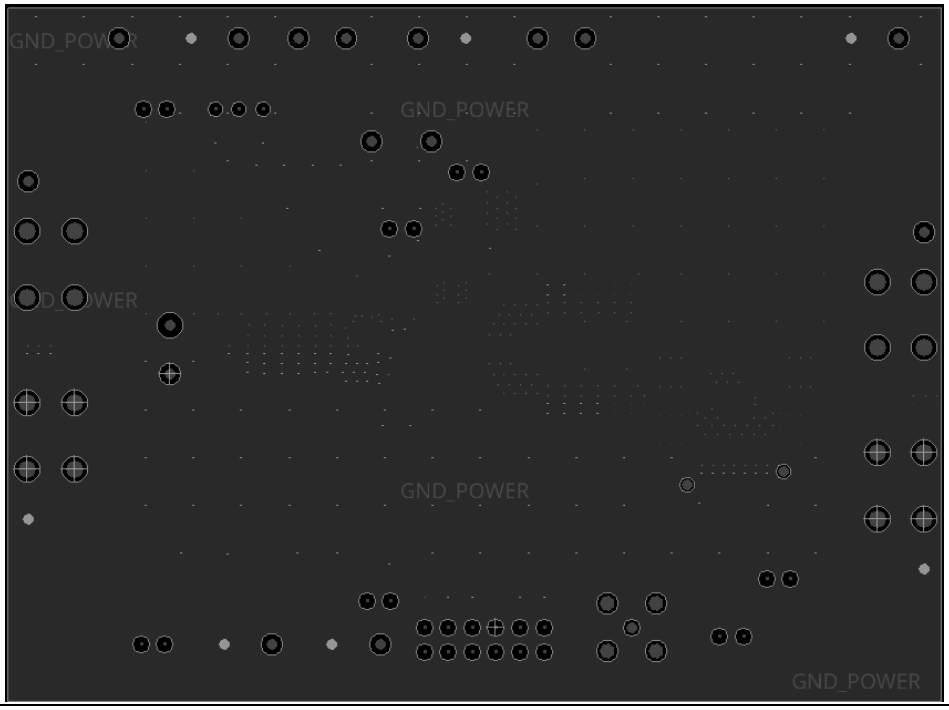


Figure 26 TDA38825 Demo Board – 5th Layer (Ground)

14.1 Solder mask

Evaluation has shown that the best overall performance is achieved using the substrate/PCB layout as shown in the following figures. PQFN devices should be placed to an accuracy of 0.050 mm on both X and Y axes. Self-centering behavior is highly dependent on solders and processes, and experiments should be run to confirm the limits of self-centering on specific processes.

Infineon recommends that larger Power or Land Area pads are Solder Mask Defined (SMD). This allows the underlying copper traces to be as large as possible, which helps in terms of current carrying capability and device cooling capability. When using SMD pads, the underlying copper traces should be at least 0.05 mm larger (on each edge) than the openings in the solder mask. This allows for layers to be misaligned by up to 0.1 mm on both axes. Ensure that the solder resist between the smaller signal lead areas is at least 0.15 mm wide due to the high x/y aspect ratio of the solder mask strip.

14.2 Stencil design

Stencils for QFN packages can be used with thicknesses of 0.100-0.250 mm (0.004-0.010”). Stencils thinner than 0.100 mm are unsuitable because they deposit insufficient solder paste to make good solder joints with the ground pad; high reductions sometimes create similar problems. Stencils in the range of 0.125 mm-0.200 mm (0.005-0.008”), with suitable reductions, give the best results. A recommended stencil design is shown below. This design is for a stencil thickness of 0.127 mm (0.005”). The reduction should be adjusted for stencils of other thicknesses.

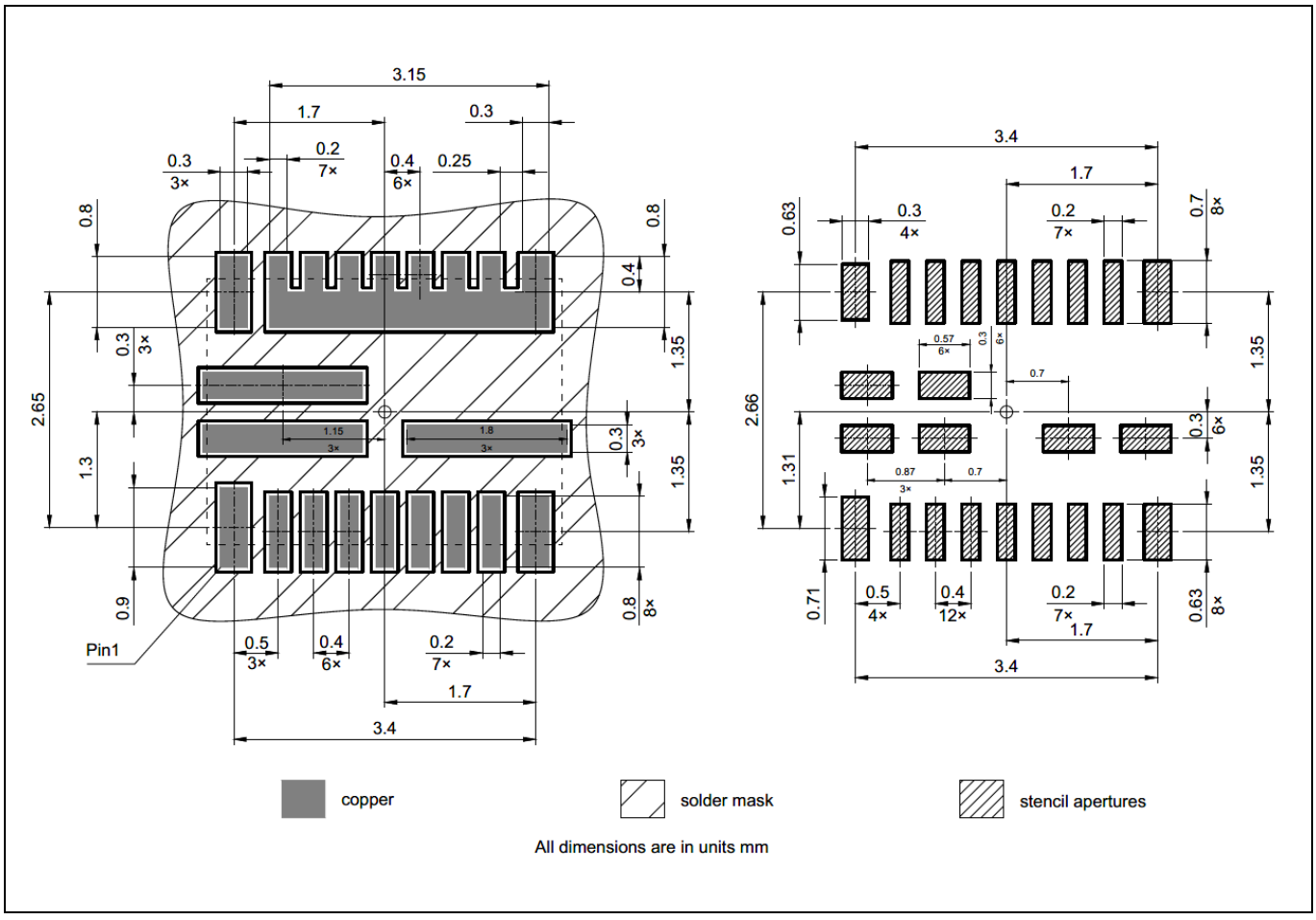
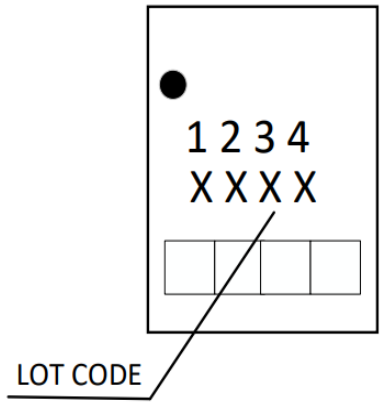


Figure 27 PCB metal, solder mask, and Stencil - pad size and spacing

15 Package

This section includes marking, mechanical and packaging information for TDA38825.

15.1 Marking Information



Dot:- Pin1 identifier
Line1:- Last four digit of part number – 8825
Line2:- Lot code
Line3:- Date code –EYWW [Y=Year, WW=Calender week]

Figure 28 Package Marking

15.2 Dimensions

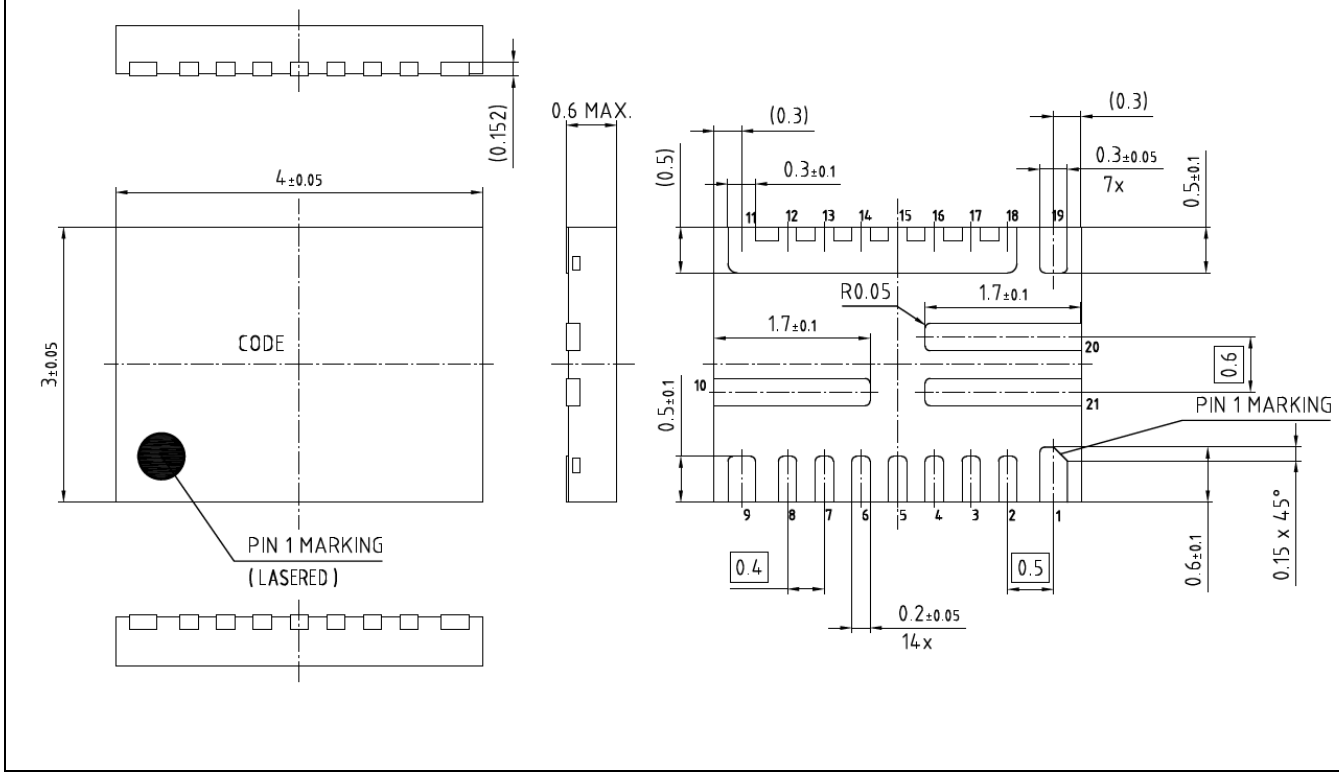


Figure 29 Package Dimensions (all dimensions in mm)

15.3 Tape and Reel information

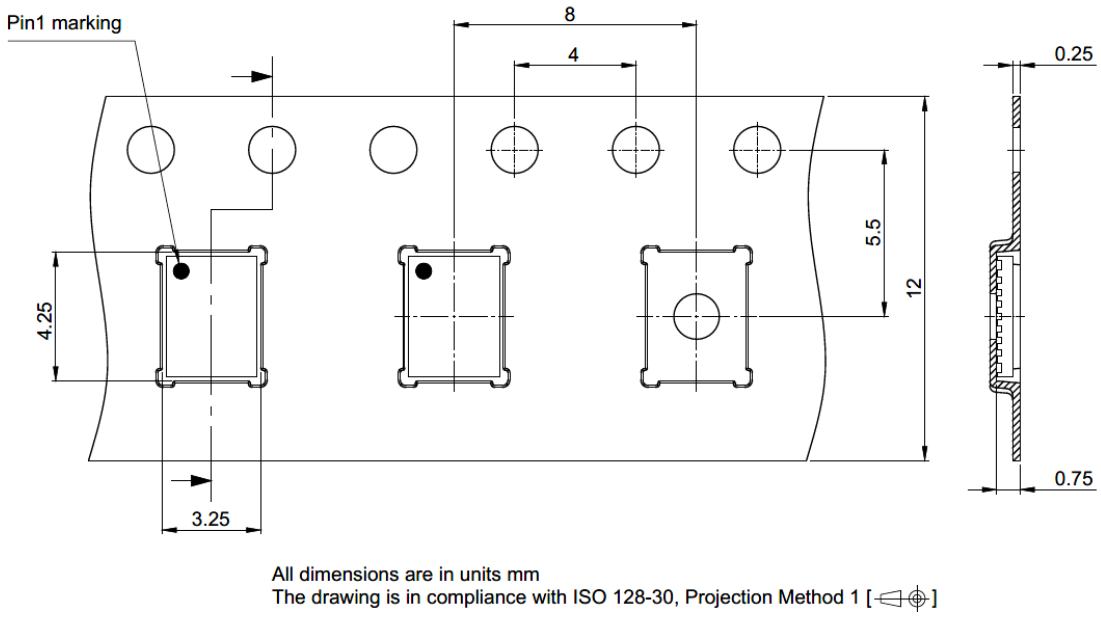


Figure 30 Tape and Reel packaging

16 Environmental Qualifications

Table 3 Environmental qualifications

Qualification Level		**Industrial**	
Moisture Sensitivity		QFN Package	JEDEC Level 2 @ 260 °C
ESD	Human Body Model	ANSI/ESDA/JEDEC JS-001, 2 (2000V to < 4000V)	
	Charged Device Model	ANSI/ESDA/JEDEC JS-002, C3 (≥ 1000V)	
RoHS Compliant		Yes	

Revision History

TDA38825

Revision 2024-08-05, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2023-07-19	Release of final version
2.1	2024-08-05	Added VDS Maximum specification for the High side MOSFET, Updated the Global condition of Vin for the EC table, Updated the IC Marking

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