

## F630FP-VB Datasheet

### N-Channel 200 V (D-S) MOSFET

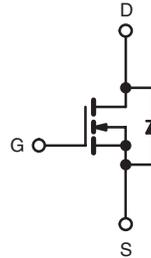
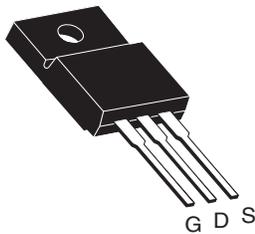
PRODUCT SUMMARY		
$V_{DS}$ (V)	200	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$	0.265
$Q_g$ (Max.) (nC)	16	
$Q_{gs}$ (nC)	5	
$Q_{gd}$ (nC)	8	
Configuration	Single	

#### FEATURES

- Isolated Package
- High Voltage Isolation = 2.5 kV<sub>RMS</sub> (t = 60 s; f = 60 Hz)
- Sink to Lead Creepage Distance = 4.8 mm
- 175 °C Operating Temperature
- Dynamic dV/dt Rating
- Low Thermal Resistance
- Lead (Pb)-free Available



TO-220 FULLPAK



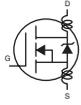
N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted					
PARAMETER	SYMBOL		LIMIT	UNIT	
Drain-Source Voltage	$V_{DS}$		200	V	
Gate-Source Voltage	$V_{GS}$		$\pm 20$		
Continuous Drain Current	$V_{GS}$ at 10 V	$T_C = 25\text{ }^\circ\text{C}$	10	A	
		$T_C = 100\text{ }^\circ\text{C}$	6.5		
Pulsed Drain Current <sup>a</sup>	$I_{DM}$		32		
Linear Derating Factor			0.24	W/ $^\circ\text{C}$	
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$		36	mJ	
Repetitive Avalanche Current <sup>a</sup>	$I_{AR}$		7.2	A	
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$		3.7	mJ	
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$		$P_D$	37	W
Peak Diode Recovery dV/dt <sup>c</sup>			dV/dt	5.5	V/ns
Operating Junction and Storage Temperature Range			$T_J, T_{stg}$	- 55 to + 175	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s			300 <sup>d</sup>	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 25\text{ V}$ , starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 1.0\text{ mH}$ ,  $R_G = 25\text{ }\Omega$ ,  $I_{AS} = 7.2\text{ A}$  (see fig. 12).
- $I_{SD} \leq 9.2\text{ A}$ ,  $dI/dt \leq 110\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 175\text{ }^\circ\text{C}$ .
- 1.6 mm from case.

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	65	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	4.1	

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		200	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$		-	0.13	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}$		-	-	25	$\mu\text{A}$
		$V_{DS} = 160\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 4.3\text{ A}^b$	-	0.265	-	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 4.3\text{ A}^b$		2.3	-	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$ , see fig. 5		-	560	-	pF
Output Capacitance	$C_{oss}$			-	260	-	
Reverse Transfer Capacitance	$C_{rss}$			-	110	-	
Drain to Sink Capacitance	$C$	$f = 1.0\text{ MHz}$		-	12	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 9.2\text{ A}, V_{DS} = 80\text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	16	nC
Gate-Source Charge	$Q_{gs}$			-	-	4.4	
Gate-Drain Charge	$Q_{gd}$			-	-	7.7	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 100\text{ V}, I_D = 9.2\text{ A}, R_G = 18\text{ }\Omega, R_D = 5.2\text{ }\Omega$ , see fig. 10 <sup>b</sup>		-	8.8	-	ns
Rise Time	$t_r$			-	30	-	
Turn-Off Delay Time	$t_{d(off)}$			-	19	-	
Fall Time	$t_f$			-	20	-	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal Source Inductance	$L_S$			-	7.5	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	10	-	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	32	-	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 7.2\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	2.5	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 9.2\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$		-	130	260	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	0.65	1.3	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

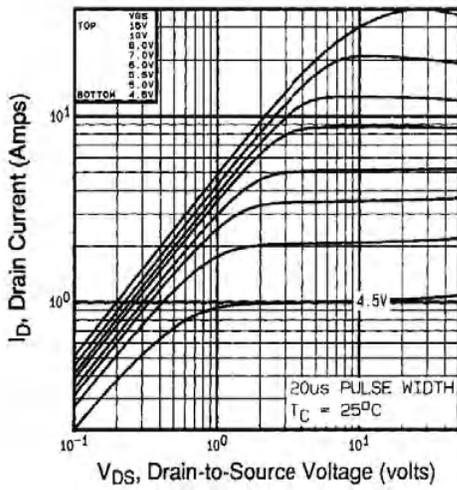


Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^\circ\text{C}$

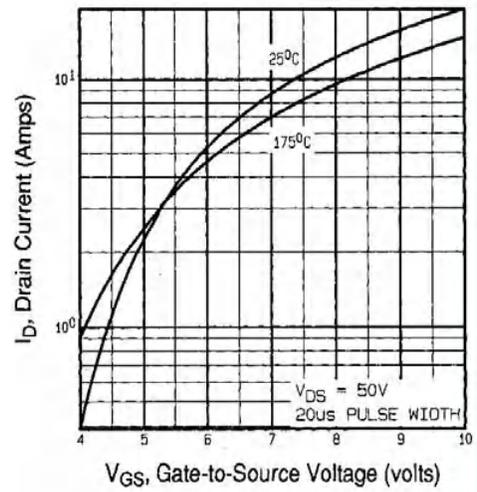


Fig. 3 - Typical Transfer Characteristics

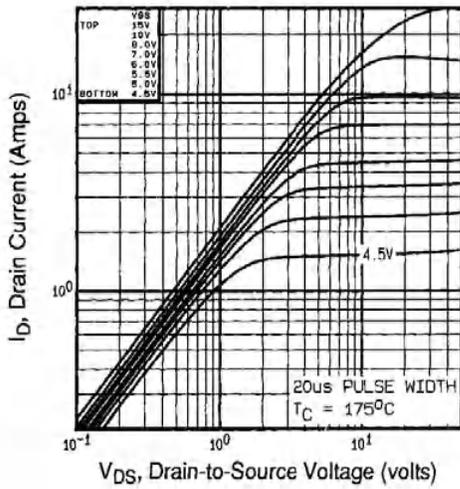


Fig. 2 - Typical Output Characteristics,  $T_C = 175\text{ }^\circ\text{C}$

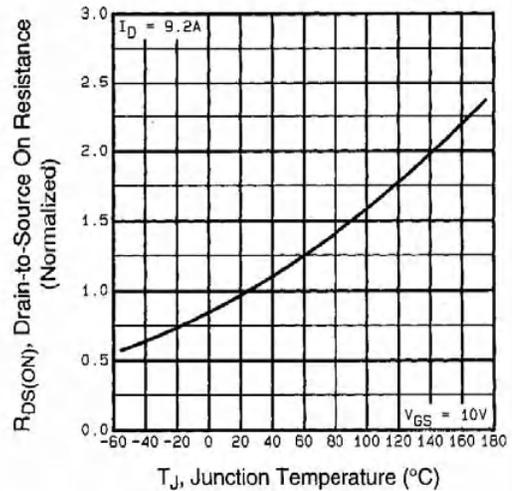


Fig. 4 - Normalized On-Resistance vs. Temperature

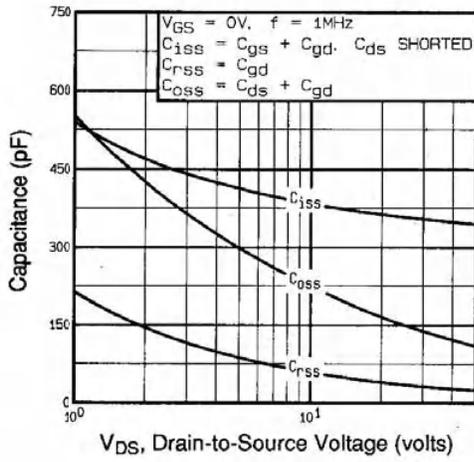


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

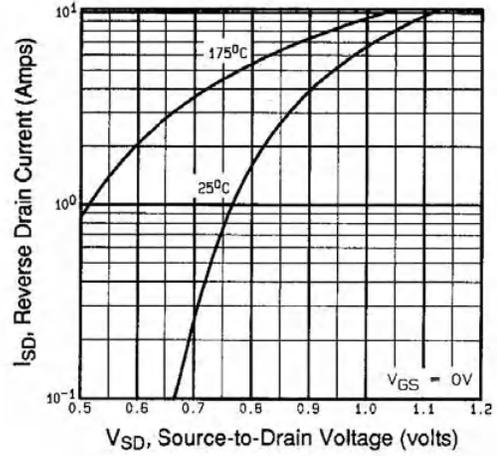


Fig. 7 - Typical Source-Drain Diode Forward Voltage

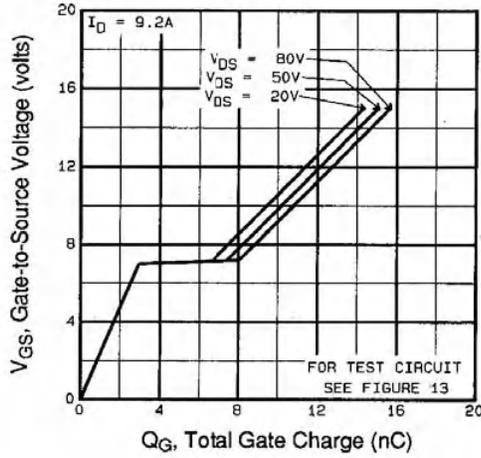


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

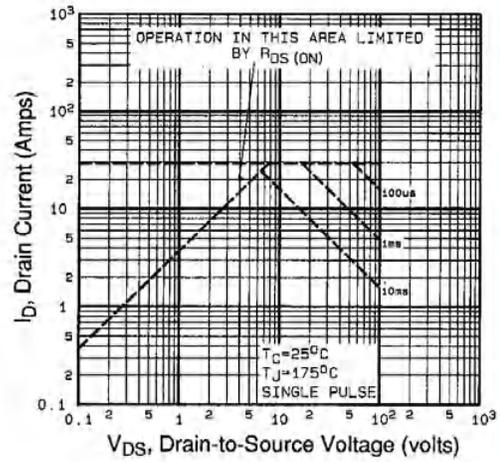


Fig. 5 - Fig. 8 - Maximum Safe Operating Area

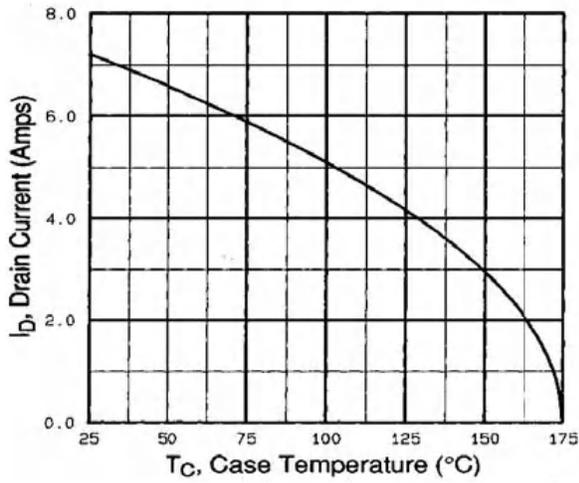


Fig. 9 - Maximum Drain Current vs. Case Temperature

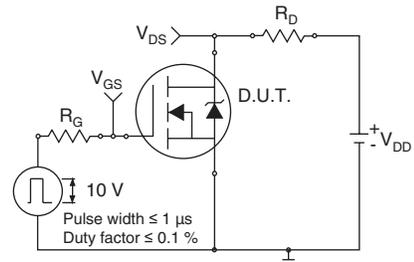


Fig. 10a - Switching Time Test Circuit

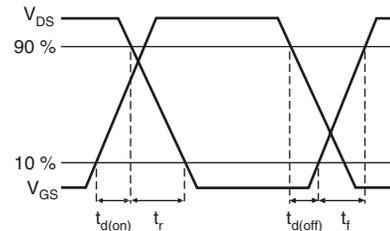


Fig. 10b - Switching Time Waveforms

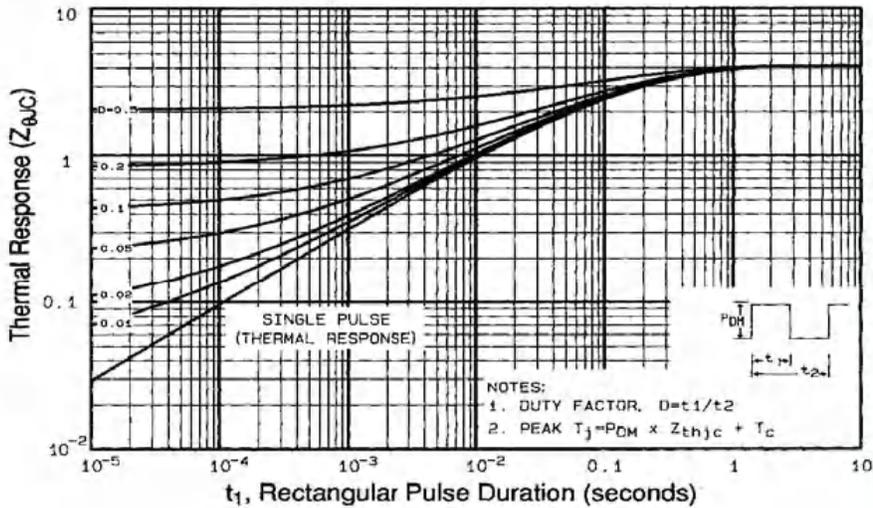


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

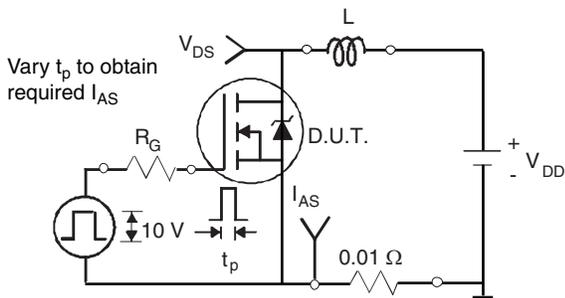


Fig. 12a - Unclamped Inductive Test Circuit

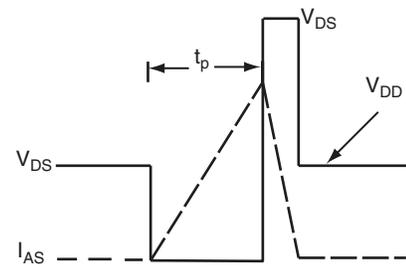


Fig. 12b - Unclamped Inductive Waveforms

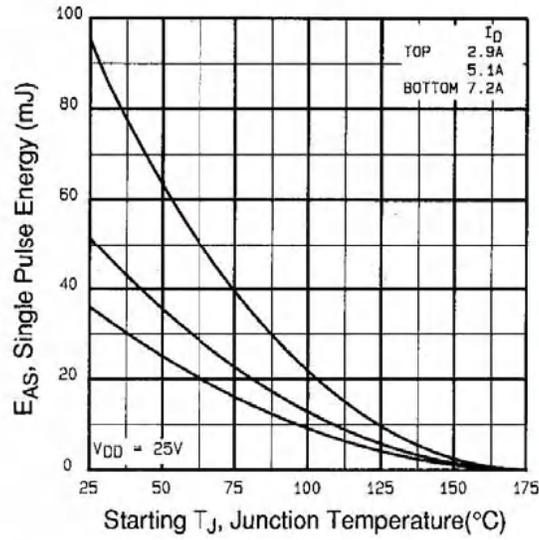


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

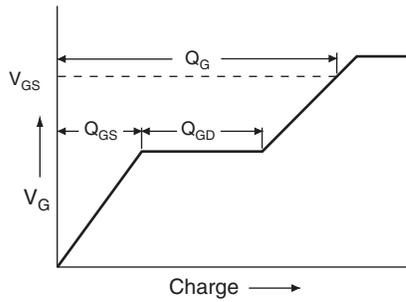


Fig. 13a - Basic Gate Charge Waveform

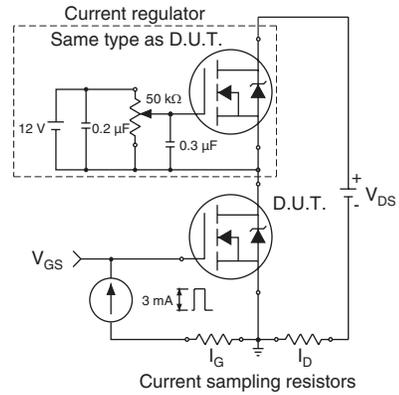


Fig. 13b - Gate Charge Test Circuit

### Peak Diode Recovery dV/dt Test Circuit

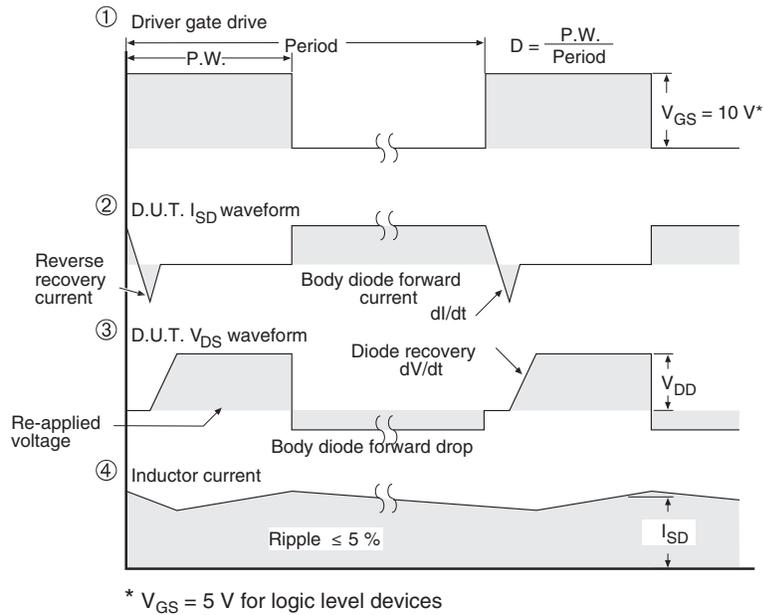
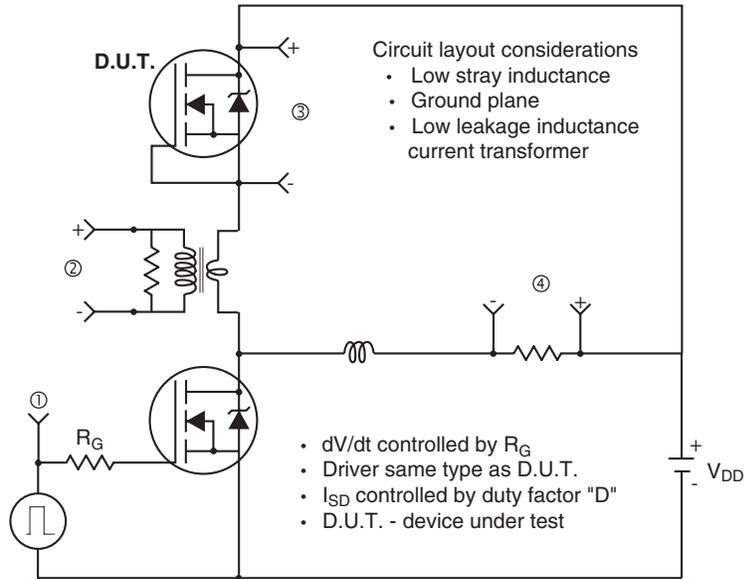


Fig. 14 - For N-Channel

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