ft2928

2X6.8W Class-G Stereo Audio Power Amplifier with Automatic Level Control & Battery Tracking AGC

GENERAL DESCRIPTION

The ft2928 is a fully integrated, highly efficient, 2X6.8W filterless Class-G stereo audio power amplifier with automatic level control (ALC) and battery tracking AGC. It integrates dual filterless Class-D audio amplifiers with an adaptive Class-G synchronous boost regulator and operates with a wide range of supply voltages from 2.7V to 5.5V. With a supply voltage at 3.6V, the ft2928 can deliver an output power of 6.8W per channel with 10% THD+N, or 5.5W per channel with 1% THD+N, into a pair of 4Ω speaker loads.

In ft2928, the power supply rails of the audio amplifiers' output stages are internally boosted and regulated by a synchronous PWM switching regulator with two integrated power switches. The boost regulator employs current-mode PWM control with proprietary multi-level Class-G topology to regulate the boosted output voltage dynamically in response to the voltage level of the audio outputs. The higher output power and greater power efficiency resulted from the adaptive Class-G boost regulator make ft2928 an ideal audio solution for battery-powered electronic devices.

To facilitate various applications, the boost regulator in ft2928 is independently controlled with three operating modes: Adaptive Boost, Continual Boost, and Bypass.

The ft2928 features ALC function to constantly monitor and safeguard the audio outputs against the boosted supply voltage, preventing output clipping distortion, excessive power dissipation, and speaker over-load. Once an over-level condition is detected in either channel, the ALC lowers the voltage gain of both audio amplifiers together to limit the peak audio outputs.

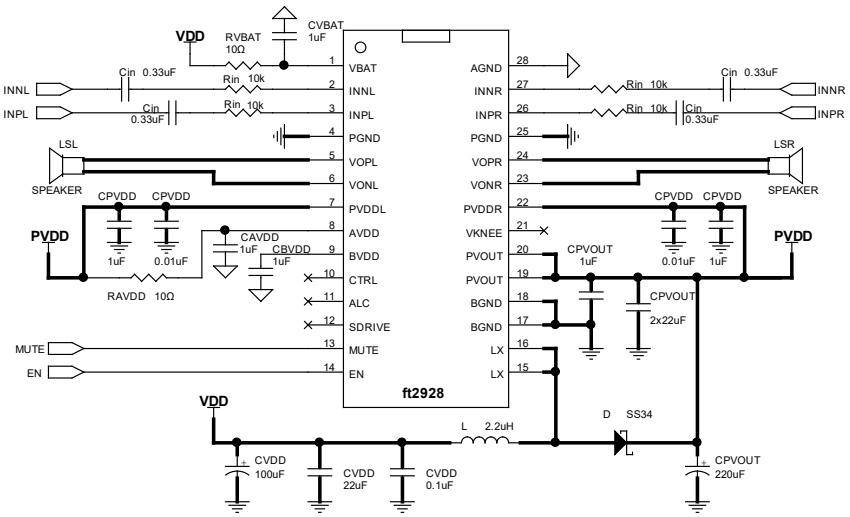
FEATURES

- Maximum output power in Non-ALC Mode
  (VDD=3.6V, THD+N=10%, Dual channels driven)
  2 X 6.8W into a pair of 4Ω speaker loads
  (VDD=3.6V, THD+N=1%, Dual channels driven)
  2 X 5.5W into a pair of 4Ω speaker loads
- ALC output power in ALC Mode
  (VDD=3.6V, THD+N≤0.6%, Dual channels driven)
  2 X 5W into a pair of 4Ω speaker loads
- Wide range of supply voltages from 2.7V to 5.5V
- Dual filterless Class-D audio amplifiers integrated with an adaptive Class-G boost regulator
- Automatic level control to eliminate output clipping
- Battery tracking AGC to prevent battery voltage collapse
- Optional soft-drive for low-EMI operation
- Independent control of boost regulator
- Mute control for fast turn-off / turn-on of audio outputs
- Low THD+N: 0.02%
  (VDD=3.6V, 4Ω+33μH, Po=2W/Ch, Dual channels driven)
- Wide ALC dynamic range: 11dB
- Maximum voltage gain: 26dB
- High efficiency: 80%
  (VDD=3.6V, 4Ω+33μH, Po=2W/Ch, Dual channels driven)
- Comprehensive protection modes: Under-voltage lockout protection, Auto-recovering over-current protection, and Thermal over-load protection
- Available in TSSOP-28L package

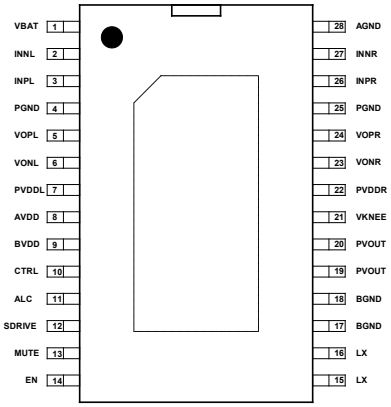
APPLICATIONS

- Blue Tooth Speakers
- Portable Audio Decks
- Consumer Audio Electronics

APPLICATION CIRCUIT



PIN DESIGNATION AND DESCRIPTION



ft2928P (TOP VIEW)

NAME	PIN #	TYPE	DESCRIPTION
VBAT	1	P	Supply input voltage. Connect to the system power supply through a small decoupling resistor of (10Ω ~ 20Ω). Also, add a 1μF ceramic capacitor to the pin for decoupling.
INNL	2	AI	Left-channel inverting audio input terminal.
INPL	3	AI	Left-channel non-inverting audio input terminal.
PGND	4, 25	G	Power grounds for the audio amplifiers. Connect to the system ground GND.
VOPL	5	AO	Left-channel non-inverting audio output terminal.
VONL	6	AO	Left-channel inverting audio output terminal.
PVDDL/R	7, 22	P	Power supply inputs for the output stages of the left-channel and right-channel audio amplifiers. Connect directly to PVOUT. Add 0.01μF//1μF ceramic capacitors to each pin for decoupling.
AVDD	8	P	Boosted supply input voltage. Connect to PVOUT through a small decoupling resistor of 10Ω. Also, add a 1μF ceramic capacitor to the pin for decoupling.
BVDD	9	AO	Internally generated voltage reference. Add a 1μF ceramic capacitor for decoupling.
CTRL	10	DI	**Boost Regulator Control** with an on-chip 300kΩ pullup resistor to VBAT and an on-chip 300kΩ pulldown resistor to ground. When pulled low, the boost regulator is de-biased and the device operates in Bypass mode. Conversely, the boost regulator is enabled adaptively or continually.
ALC	11	DI	**ALC Mode Control** with an on-chip 300kΩ pullup resistor to VBAT and an on-chip 300kΩ pulldown resistor to ground. When asserted high, the ALC is disabled. Conversely, the ALC is enabled with one of two ALC dynamic characteristics.
SDRIVE	12	DI	**Soft-Drive Enable** (Active High) with an on-chip 300kΩ pulldown resistor to ground.
MUTE	13	DI	**Mute Enable** (Active High) with an on-chip 300kΩ pulldown resistor to ground.
EN	14	DI	**Chip Enable** (Active High) with an on-chip 300kΩ pulldown resistor to ground.
LX	15, 16	AO	Switch node of the boost regulator.
BGND	17, 18	G	Power ground for the boost regulator. Connect to the system ground GND.
PVOUT	19, 20	P	Boosted voltage output.
VKNEE	21	DI	**Battery Tracking AGC Control** with an on-chip 300kΩ pullup resistor to VBAT. When pulled to ground, the battery tracking AGC is disabled. Conversely, the battery tracking AGC is enabled with one of two knee voltages.
VONR	23	AO	Right-channel inverting audio output terminal.
VOPR	24	AO	Right-channel non-inverting audio output terminal.
INPR	26	AI	Right-channel non-inverting audio input terminal.
INNR	27	AI	Right-channel inverting audio input terminal.
AGND	28	G	Analog ground. Connect to the system ground GND.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKING OPTION	PACKAGE
ft2928P	-40°C to +85°C	Tape and Reel, 4000	TSSOP-28L

REVISION HISTORY

Initial Release (October 2018)

Changed from Initial 1.0 (October 2018) to Revision 1.1 (February 2019)

1. Changed the boost regulator's PWM frequency from 800kHz to 900kHz (in High-Efficiency Drive mode) and from 640kHz to 720kHz (in Soft Drive mode).
2. Changed the Class-D audio amplifier's PWM frequency from 400kHz to 450kHz (in High-Efficiency Drive mode) and from 320kHz to 360kHz (in Soft Drive mode).
3. Changed the boost regulator's inductance from 3.3μH to 2.2μH.
4. Updated Application Circuit Diagram on the top page and Figure 43 & 44 on Page 28.

Changed from Initial 1.1 (February 2019) to Revision 1.1 (April 2019)

1. Revised Idle Channel Noise & SNR specifications.

Changed from Revision 1.1 (April 2019) to Revision 1.2 (September 2022)

1. Added PACKING OPTION.

ABSOLUTE MAXIMUM RATINGS (Note1)

PARAMETER	VALUE
Supply voltage, VDD	-0.3V to 6V
LX, PVOUT, PVDDL/R, AVDD, VOPL/R, VONL/R	-0.3V to 8.5V
PGND, BGND	-0.3V to 0.3V
All other Pins	-0.3V to VDD+0.3V
PVDD to AVDD	-0.3V to 0.3V
Operating Junction Temperature	-40°C to +150°C
Storage Temperature	-40°C to +125°C
ESD Ratings-Human Body Model (HBM)	1000V
Maximum Soldering Temperature (@10 second duration)	260°C

Note 1: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may also affect device reliability.

POWER DISSIPATION RATINGS (Note 2, 3)

PACKAGE	$T_A \leq +25°C$	$T_A = +70°C$	$T_A = +85°C$	Θ_{JA}
TSSOP-28L	4.5W	2.8W	2.3W	28°C/W

Note 2: The thermal pad of the package must be directly soldered onto a grounded metal island as a thermal sink on the system board.
Note 3: The power dissipation ratings are for a two-side, two-plane printed circuit board (PCB).

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	VDD		2.7		5.5	V
Operating Ambient Temperature	T_A		-40		85	°C
Minimum Load Impedance	R_L	Across VOPL/R and VONL/R	3.2	4		Ω
Audio Input Resistor	R_{IN}	@ INPL/R, INNL/R	0	10	39	kΩ
Audio Input Capacitor	C_{IN}	@ INPL/R, INNL/R		0.33	1.0	μF
Boost Regulator Inductor	L			2.2	3.3	μH
Boost Regulator Input Capacitor	C_{VDD}	Ceramic		22		μF
		Electrolytic Bulk		100	220	μF
Boost Regulator Output Capacitor	C_{PVOUT}	Ceramic		2 X 22	3 X 22	μF
		Electrolytic Bulk (Note 4)		220	330	μF
Operating Mode Control	CTRL	Boost Regulator Activated Continually	Short to VBAT			
		Boost Regulator Activated Adaptively	Unconnected			
		Boost Regulator De-biased	Short to GND			
ALC Mode Control	ALC	Non-ALC	Short to VBAT			
		ALC-2	Unconnected			
		ALC-1	Short to GND			
Battery Tracking AGC Control	VKNEE	VKNEE=3.5V	Unconnected			
		VKNEE=3..2V	300kΩ Resistor to GND			
		Battery Tracking AGC Disabled	Short to GND			
Gate Drive Control	SDRIVE	Soft Drive (Low-EMI)	Short to VBAT			
		High-Efficiency Drive	Unconnected or Short to GND			

Note 4: A bulk electrolytic capacitor can be added to facilitate higher voltage margin for higher audio power at low frequencies. However, pay attention to any bulk output capacitance higher than 330μF as it might adversely slow the boost regulator's response to load transients to some extent affecting audio dynamics when playing music.

IMPORTANT APPLICATION NOTES

1. Place the ft2928 in close proximity to the inductor, Schottky diode, and input/output capacitors of the boost regulator on the system board, minimizing parasitic impedances of high-current traces. Also, these passive components must be placed on the top layer with ft2928 and connected with wide and short metal lines without vias. Failure to do a proper layout on the system board can result in severe degradation of maximum output power, efficiency, THD, and electromagnetic interference (EMI) performance. It might even induce excessive ringing at the switch node LX and damage the device permanently.
2. Use wide open areas around the device on the top and bottom layers of the system board as the ground plane (GND). Place lots of solid vias connecting the top and bottom layers of GND. Furthermore, for proper thermal dissipation, reserve wide and uninterrupted GND areas along the thermal flow on the top layer, i.e., no wires cutting through the GND layer and obstructing the thermal flow in the proximity of the device.
3. The ft2928 is packaged with an exposed thermal pad on the underside of the device. Solder the thermal pad directly onto a large grounded metal island, as a thermal sink, underneath the package for proper thermal dissipation. On the grounded metal island, place several rows of solid, equally-spaced vias connecting to the bottom layer of GND. Failure to do so can severely limit its thermal dissipation capability. It might cause the device going into over-temperature shutdown occasionally.
4. All the ground pins (AGND, BGND, and PGND) are directly connected to the ground plane (GND). The boosted power supply inputs (PVDDL/R) for the audio amplifiers' output stages are directly connected to the output capacitors of the boost regulator with wide and short metal traces.
5. Use direct and low-impedance traces for the audio outputs (VOPL/R and VONL/R) to the speakers.
6. As a high-performance Class-G stereo audio amplifier, the ft2928 requires adequate power supply decoupling to ensure its high-efficiency, low distortion, and low EMI. Place each decoupling capacitor individually close to VBAT, AVDD, BVDD, and PVDDL/R pins respectively.
7. For best noise performance, use differential inputs from the audio source for ft2928. In single-ended input applications, the unused input of ft2928 should be AC-grounded at the audio source.
8. With an on-chip rectification power switch, the ft2928 requires no external Schottky diode for applications where speaker load resistances are 8Ω. However, for applications where speaker load resistances are 4Ω or less, it is necessary to add one or two auxiliary Schottky diodes across LX and PVOUT pins to improve maximum output power and overall power efficiency. The added Schottky diode must be rated for a current no less than 3A and a reverse breakdown voltage no less than 20V, such as SS34 or SS32.
9. The EMI of the Class-D amplifier's outputs can be suppressed using a ferrite bead filter constructed from a ferrite bead and a capacitor, as shown in Figure 39. Choose a ferrite bead with a rated current no less than 2A for an 8Ω speaker load and 3A for a 4Ω speaker load. Also, place the ferrite beard filter tightly together and individually close to VOPL/R and VONL/R pins respectively.
10. It is recommended to add an RC snubber circuit across two audio outputs, VOPL/R and VONL/R, for each channel, as shown in Figure 40, to prevent the device from accelerated deterioration or abrupt destruction due to excessive inductive flybacks that are induced on fast output switching or by an over-current or short-circuit condition.
11. The operation of the battery tracking AGC can be highly influenced by the electrical characteristics of the battery. Place a small decoupling resistor of (1Ω ~ 10Ω) between the battery supply and the VBAT pin, coupled with a decoupling capacitor of 1μF, mitigating the detrimental effect of high battery current ripples on the detection of battery voltage.
12. Place a small decoupling resistor of 10Ω between AVDD and PVOUT pins, coupled with a decoupling capacitor of 1μF, preventing high frequency transients from interfering with the on-chip linear circuitry.
13. Do not connect any audio outputs (VOPL/R or VONL/R) directly to GND, AVDD, PVOUT, or PVDDL/R as this might damage the device permanently.
14. Do not alter the logic state of the CTRL pin while the device is in operation. To change the operating mode, the device must be first placed in shutdown mode for a minimum of 10 milliseconds.

FUNCTIONAL BLOCK DIAGRAM

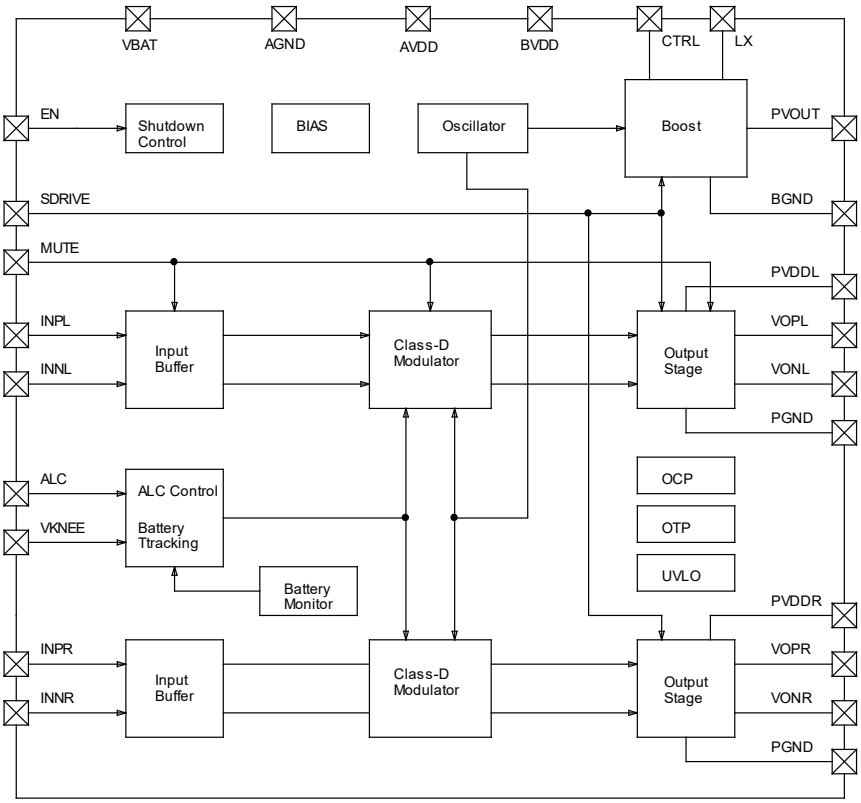


Figure 1: Simplified Functional Block Diagram of ft2928

TEST SETUP FOR ELECTRICAL & PERFORMANCE CHARACTERISTICS

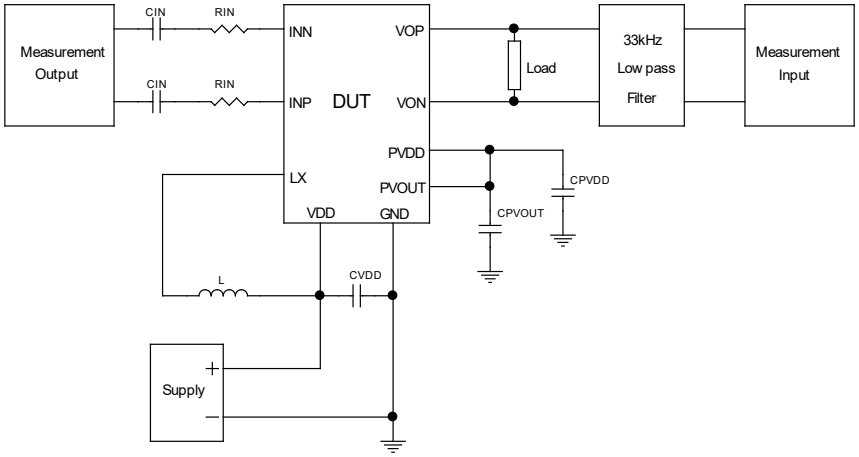


Figure 2: Test Setup Diagram for ft2928

All parameters specified in Electrical and Typical Performance Characteristics sections are measured according to the following conditions:

1. The two differential inputs are shorted for common-mode input voltage measurement. All other parameters are taken with input resistors R_{IN}=10kΩ and audio input capacitors C_{IN}=0.33μF, unless otherwise specified.
2. The boost regulator's supply decoupling capacitors C_{VDD}=22μF//0.1μF//100μF are placed close to the inductor.
3. The boost regulator's inductor L=2.2μH and Schottky diode (SS34) are placed close to the LX pins.
4. The boost regulator's output capacitors C_{PVOUT}=2X22μF//1μF//220μF is placed close to the PVOUT pins.
5. The audio amplifiers' decoupling capacitors $C_{PVDDL/R}$=1μF//0.01μF are placed close to individual PVDDL/R pins.
6. An output inductor of 33μH is placed in series with the load resistor to emulate a speaker load for all AC and dynamic parameters.
7. A 33kHz lowpass filter is added even if the analyzer has an internal lowpass filter. An RC lowpass filter (1000Ω, 4.7nF) is used on each output for the data sheet graphs.

ELECTRICAL CHARACTERISTICS

VDD=3.6V, f=1kHz, Load=4Ω+33μH, L=2.2μH, C_{IN}=0.33μF, R_{IN}=10kΩ (A_V=23dB), CTRL=NC, ALC=NC, SDRIVE=NC, VKNEE=GND, C_{VDD}=22μF//0.1μF//100μF, C_{PVOUT}=2X22μF//1μF//220μF, $C_{PVDDL/R}$=1μF//0.01μF, R_{VBAT}=R_{AVDD}=10Ω, C_{VBAT}=C_{AVDD}=C_{BVDD}=1μF, dual channels driven, T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
VDD	Supply Input Voltage			2.7		5.5	V
V_{UVLOUP}	Power-on Threshold Voltage	VDD from Low to High			2.2		V
V_{UVLODN}	Power-off Threshold Voltage	VDD from High to Low			2.0		V
I_{VBAT}	VBAT Input Quiescent Current	Inputs AC-Grounded, No Load		2.0	3.0	4.5	mA
I_{AVDD}	AVDD Input Current	Inputs AC-Grounded, No Load		2.7	3.8	5.4	mA
		V_{IN}=0.15V_{RMS}, No Load		4.8	6.5	8.8	mA
		V_{IN}=0.25V_{RMS}, No Load		5.0	7.0	10	mA
I_{VBAT_MUTE}	VBAT Mute Current	MUTE=High Inputs AC-Grounded, No Load		2.0	3.0	4.5	mA
I_{AVDD_MUTE}	AVDD Mute Current	MUTE=High Inputs AC-Grounded No Load	CTRL=Low	2.7	3.8	5.4	mA
			CTRL=NC	2.7	3.8	5.4	mA
			CTRL=High	5.0	7.0	10	mA
I_{SD}	Shutdown Current	EN=Low				1	μA
BVDD	Voltage Reference	Inputs AC-Grounded, No Load		3.1	3.3	3.5	V
		V_{IN}=0.15V_{RMS}, No Load		4.7	5.0	5.3	V
V_{IH}	Digital High Level Input Voltage	EN, MUTE, SDRIVE		1.2			V
		ALC, CTRL, VKNEE		VBAT-0.5		VBAT	V
V_{IL}	Digital Low Level Input Voltage	EN, MUTE, SDRIVE, ALC, CTRL, VKNEE				0.4	V
R_{UP}	Pullup Resistor to VBAT	ALC, CTRL, VKNEE			300		kΩ
R_{DN}	Pulldown Resistor to Ground	EN, MUTE, SDRIVE, ALC, CTRL			300		kΩ
T_{OTSD}	Over-Temperature Threshold				160		°C
T_{HYS}	Over-Temperature Hysteresis				20		°C
CLASS-G BOOST REGULATOR							
PVOUT	Boosted Voltage	CTRL=High, No Load		7.4	7.6	7.8	V
f_{SW}	Boost PWM Frequency	SDRIVE=Low			900		kHz
		SDRIVE=High			720		kHz
CLASS-D AUDIO AMPLIFIER WITH BOOST REGULATOR (CTRL=NC or High)							
$P_{O, MAX}$	Maximum Output Power (Dual channels driven)	R_L=4Ω+33μH	THD+N=10%		6.8		W/Ch
			THD+N=1%		5.5		W/Ch
		R_L=8Ω+33μH	THD+N=10%		3.9		W/Ch
			THD+N=1%		3.2		W/Ch
$P_{O, ALC}$	ALC Output Power (Dual channels driven)	ALC Mode V_{IN}=0.50V_{RMS}	R_L=4Ω+33μH		5.0		W/Ch
			R_L=8Ω+33μH		2.8		W/Ch
THD+N	Non-ALC Mode (Dual channels driven)	R_L=4Ω+33μH, Po=2W/Ch			0.02		%
		R_L=8Ω+33μH, Po=1W/Ch			0.01		%
	ALC Mode (Dual channels driven)	R_L=4Ω+33μH, V_{IN}=0.50V_{RMS}			0.6		%
		R_L=8Ω+33μH, V_{IN}=0.50V_{RMS}			0.6		%

ELECTRICAL CHARACTERISTICS

VDD=3.6V, f=1kHz, Load=4Ω+33μH, L=2.2μH, C_{IN}=0.33μF, R_{IN}=10kΩ (A_V=23dB), CTRL=NC, ALC=NC, SDRIVE=NC, VKNEE=GND, C_{VDD}=22μF//0.1μF//100μF, C_{PVOUT}=2X22μF//1μF//220μF, $C_{PVDDL/R}$=1μF//0.01μF, R_{VBAT}=R_{AVDD}=10Ω, C_{VBAT}=C_{AVDD}=C_{BVDD}=1μF, dual channels driven, T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
CLASS-D AUDIO AMPLIFIER WITH BOOST REGULATOR (CTRL=NC or High)							
η	Overall Power Efficiency (Dual channels driven, including power dissipated by external Schottky diode)	Po=2W/Ch	SDRIVE=Low		80		%
			SDRIVE=High		76		%
		ALC Mode V_{IN}=0.50V_{RMS}	SDRIVE=Low		70		%
			SDRIVE=High		67		%
A_V	Overall Voltage Gain	R_{IN}=0kΩ			26		dB
		R_{IN}=10kΩ			23		dB
A_{ALC}	ALC Maximum Attenuation				11		dB
R_{IN}	Input Resistance	@ INPL/R, INNL/R			22.5		kΩ
R_{OUT-SD}	Output Resistance in Shutdown	@ VOPL/R, VONL/R			3		kΩ
V_{COMM}	Input Common-Mode Bias	@ INPL/R, INNL/R			1.65		V
V_{OS}	Output Offset Voltage	Inputs AC-Grounded			±10		mV
V_N	Idle-Channel Noise	Inputs AC-Grounded, R_L=4Ω+33μH A-weighted, A_V=20dB			105		μV_{RMS}
SNR	Signal-to-Noise Ratio	R_L=4Ω+33μH A-weighted, A_V=20dB	Po=4W		92		dB
			Po=1W		86		dB
PSRR	Power Supply Rejection Ratio	±0.2V Supply Ripple Inputs AC-Grounded	f=217Hz		75		dB
			f=1kHz		70		dB
CMRR	Common Mode Rejection Ratio	f=1kHz, V_{IN}=0.20V_{RMS}			60		dB
X_{TALK}	Crosstalk	Po=2W/Ch			100		dB
T_{START}	Startup Time				80		ms
T_{SD}	Shutdown Settling Time				5		ms
f_{SW}	PWM Output Carrier Frequency	SDRIVE=Low			450		kHz
		SDRIVE=High			360		kHz
$I_{LIMIT, APA}$	Over-Current Limit	CTRL=High or NC			2.8		A/Ch
		CTRL=Low			1.5		A/Ch
VOLUME FADE-IN & FADE-OUT							
T_{FDIN}	Fade-In Time				25		ms
T_{FDOUT}	Fade-Out Time				3		ms
BATTERY TRACKING AGC							
V_{KNEE}	Knee Voltage	VKNEE=NC, No Load			3.5		V
		300kΩ from VKNEE to GND No Load			3.2		V
S_{ATT}	Output Attenuation Slope	No Load			3		V/V

ELECTRICAL CHARACTERISTICS

VDD=3.6V, f=1kHz, Load=4Ω+33μH, L=2.2μH, C_{IN}=0.33μF, R_{IN}=10kΩ (A_V=23dB), CTRL=NC, ALC=NC, SDRIVE=NC, VKNEE=GND, C_{VDD}=22μF//0.1μF//100μF, C_{PVOUT}=2X22μF//1μF//220μF, $C_{PVDDL/R}$=1μF//0.01μF, R_{VBAT}=R_{AVDD}=10Ω, C_{VBAT}=C_{AVDD}=C_{BVDD}=1μF, dual channels driven, T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
CLASS-D AUDIO AMPLIFIER W/O BOOST REGULATOR (CTRL=Low)							
$P_{O, MAX}$	Maximum Output Power (Dual channels driven)	R_L=4Ω+33μH	THD+N=10%		1.5		W/Ch
			THD+N=1%		1.2		W/Ch
		R_L=8Ω+33μH	THD+N=10%		0.90		W/Ch
			THD+N=1%		0.70		W/Ch
$P_{O, ALC}$	ALC Output Power (Dual channels driven)	ALC Mode V_{IN}=0.30V_{RMS}	R_L=4Ω+33μH		1.0		W/Ch
			R_L=8Ω+33μH		0.60		W/Ch
THD+N	Non-ALC Mode (Dual channels driven)	R_L=4Ω+33μH, Po=1W/Ch			0.02		%
		R_L=8Ω+33μH, Po=0.5W/Ch			0.02		%
	ALC Mode (Dual channels driven)	ALC Mode V_{IN}=0.30V_{RMS}	R_L=4Ω+33μH		0.6		%
			R_L=8Ω+33μH		0.5		%
η	Overall Power Efficiency (Dual channels driven, including power dissipated by external Schottky diode)	Po=0.5W/Ch	SDRIVE=Low		82		%
			SDRIVE=High		78		%
		ALC Mode V_{IN}=0.30V_{RMS}	SDRIVE=Low		83		%
			SDRIVE=High		81		%
V_N	Idle-Channel Noise	Inputs AC-Grounded, R_L=4Ω+33μH A-weighted, A_V=20dB			105		μV_{RMS}
SNR	Signal-to-Noise Ratio	R_L=4Ω+33μH A-weighted, A_V=20dB	Po=1W		86		dB
			Po=0.5W		83		dB

TYPICAL PERFORMANCE CHARACTERISTICS

VDD=3.6V, f=1kHz, Load=4Ω+33μH, L=2.2μH, C_{IN}=0.33μF, R_{IN}=10kΩ (A_V=23dB), CTRL=NC, ALC=NC, SDRIVE=NC, VKNEE=NC, C_{VDD}=22μF//0.1μF//100μF, C_{PVOUT}=2X22μF//1μF//220μF, $C_{PVDDL/R}$=1μF//0.01μF, R_{VBAT}=R_{AVDD}=10Ω, C_{VBAT}=C_{AVDD}=C_{BVDD}=1μF, dual channels driven, T_A=25°C, unless otherwise specified.

List of Typical Performance Characteristics

DESCRIPTION	CONDITIONS		FIGURE #
Max. Output Power vs. VDD (Dual channels driven)	Non-ALC Mode, CTRL=NC THD+N=10%, 1%	R_L=4Ω+33μH	3
		R_L=8Ω+33μH	4
	Non-ALC Mode, CTRL=Low THD+N=10%, 1%	R_L=4Ω+33μH	5
		R_L=8Ω+33μH	6
ALC Output Power vs. VDD (Dual channels driven)	V_{IN}=0.50V_{RMS}, ALC Mode, CTRL=NC VKNEE=NC/300kΩ to GND/GND	R_L=4Ω+33μH	7
		R_L=8Ω+33μH	8
	V_{IN}=0.30V_{RMS}, ALC Mode, CTRL=Low	R_L=4Ω+33μH	9
		R_L=8Ω+33μH	10
Output Power vs. Input Voltage (Dual channels driven)	ALC & Non-ALC Modes	R_L=4Ω+33μH	11
		R_L=8Ω+33μH	12
	ALC Mode, CTRL=NC/Low	R_L=4Ω+33μH	13
		R_L=8Ω+33μH	14
Overall Efficiency vs. Output Power (Dual channels driven, including power dissipated by external Schottky diode)	Non-ALC Mode, CTRL=NC SDRIVE=Low, VDD=3.6V/4.2V	R_L=4Ω+33μH	15
		R_L=8Ω+33μH	16
	Non-ALC Mode, CTRL=NC SDRIVE=Low/High	R_L=4Ω+33μH	17
		R_L=8Ω+33μH	18
	Non-ALC Mode, CTRL=Low SDRIVE=Low/High	R_L=4Ω+33μH	19
		R_L=8Ω+33μH	20
THD+N vs. Output Power	Non-ALC Mode, CTRL=NC/Low		21
THD+N vs. Input Voltage	ALC Mode, CTRL=NC/Low		22
THD+N vs. Input Frequency	ALC Mode, Po=1W/3W		23
PSRR vs. Input Frequency	Inputs AC-Grounded		24
Supply Quiescent Current vs. VDD	Input AC-Grounded, R_L= 4Ω+33μH, CTRL=Low/NC/High		25
Mode Transitions of Boost Regulator	Non-ALC Mode		26
Output Waveforms during Startup	V_{IN}=0.10V_{RMS}		27
Output Waveforms during Shutdown	V_{IN}=0.10V_{RMS}		28
Output Waveforms during ALC Release	ALC-1 Mode		29
	ALC-2 Mode		30
Broadband Output Spectrum	R_L=4Ω+33μH, V_{IN}=0.20V_{RMS}	SDRIVE=Low	31
		SDRIVE=High	32

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

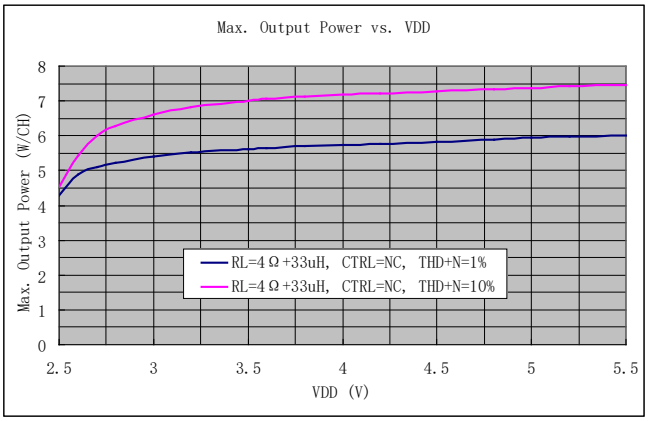


Figure 3: Max. Output Power vs. VDD (CTRL=NC)

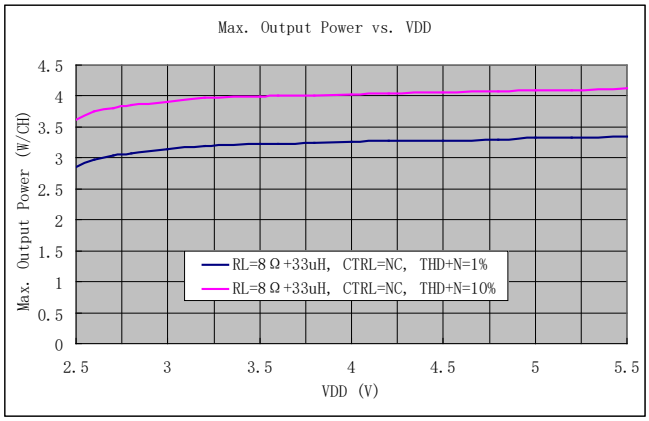


Figure 4: Max. Output Power vs. VDD (CTRL=NC)

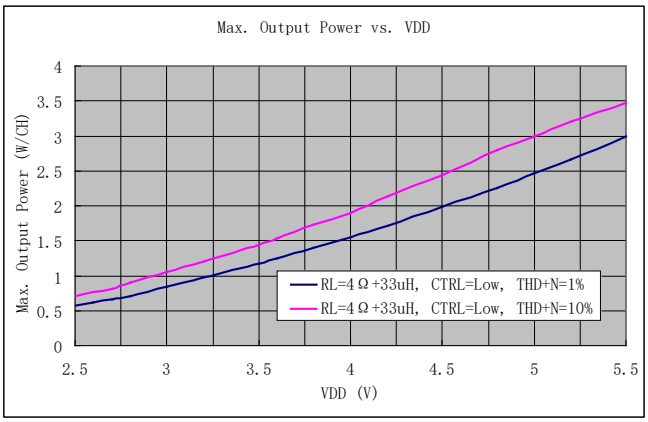


Figure 5: Max. Output Power vs. VDD (CTRL=Low)

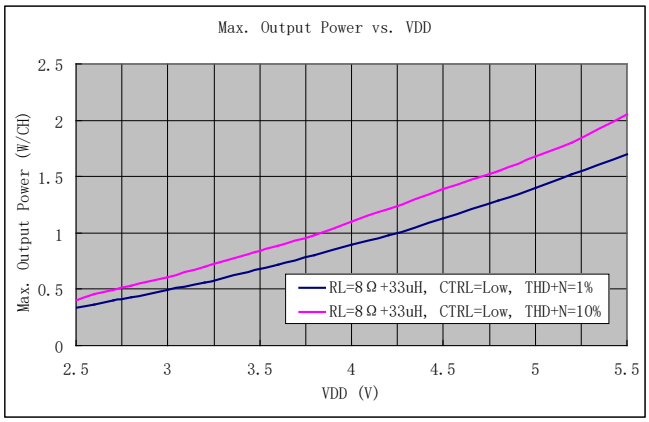


Figure 6: Max. Output Power vs. VDD (CTRL=Low)

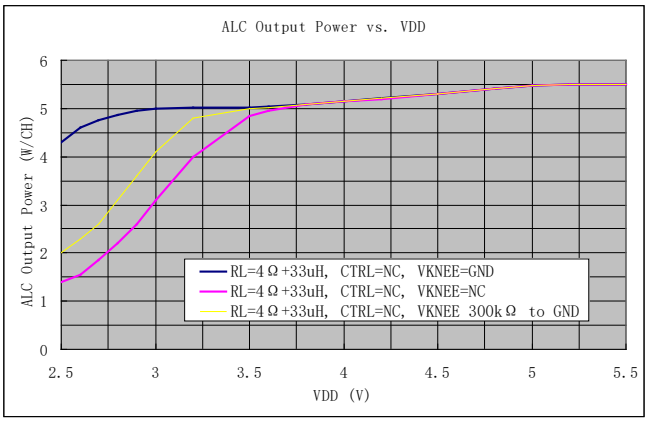


Figure 7: ALC Output Power vs. VDD (CTRL=NC)

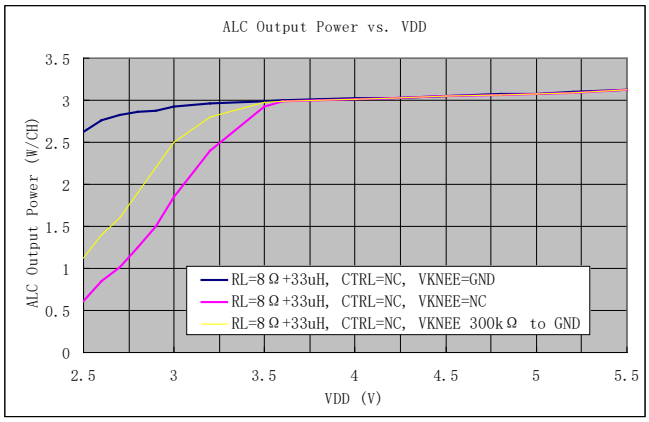


Figure 8: ALC Output Power vs. VDD (CTRL=NC)

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

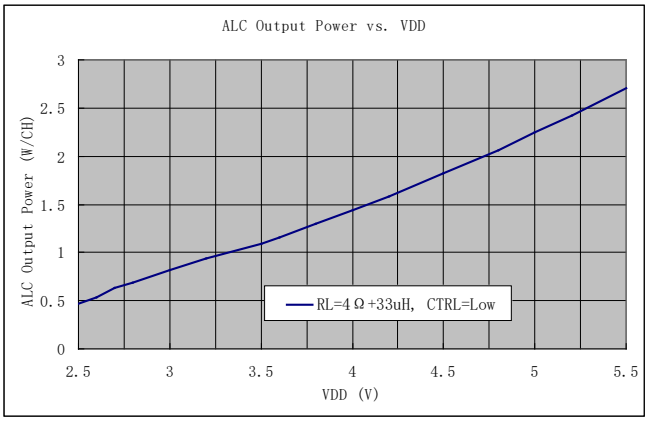


Figure 9: ALC Output Power vs. VDD (CTRL=Low)

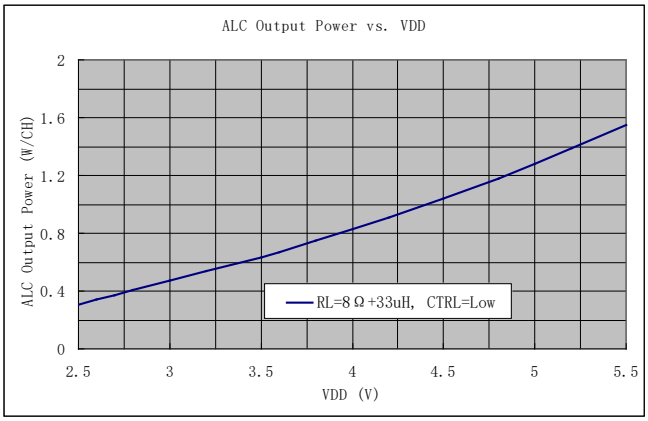


Figure 10: ALC Output Power vs. VDD (CTRL=Low)

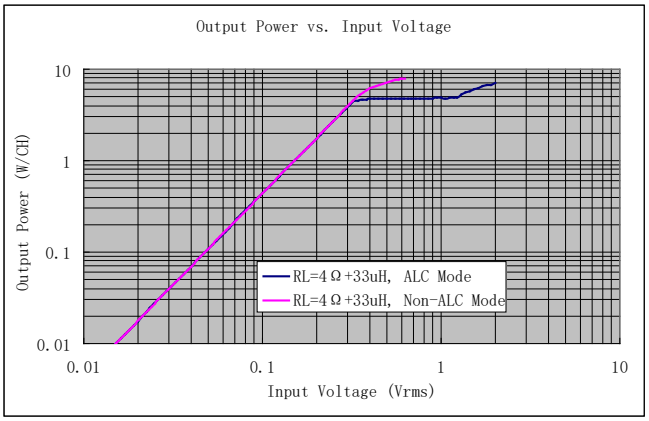


Figure 11: Output Power vs. Input Voltage

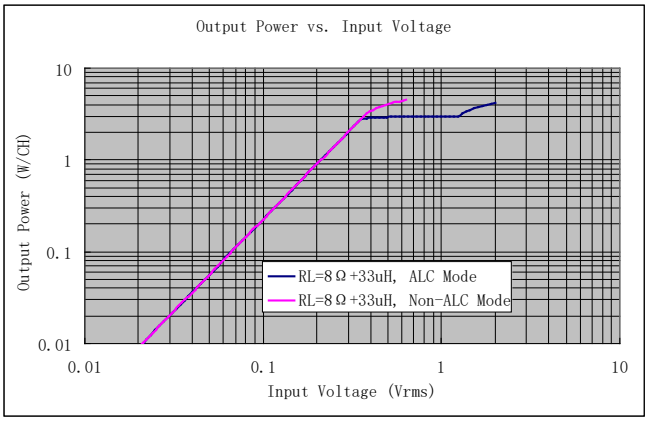


Figure 12: Output Power vs. Input Voltage

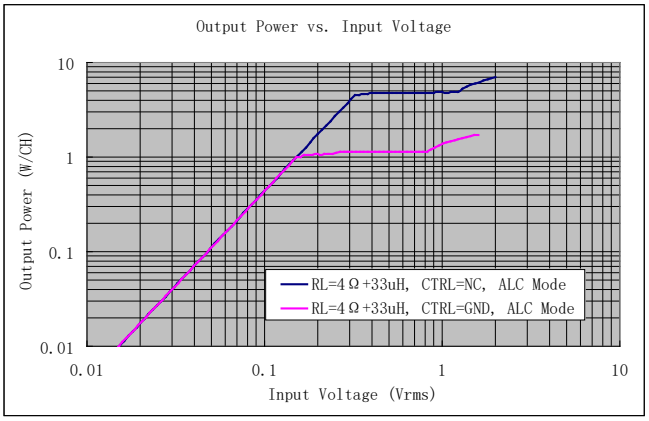


Figure 13: Output Power vs. Input Voltage

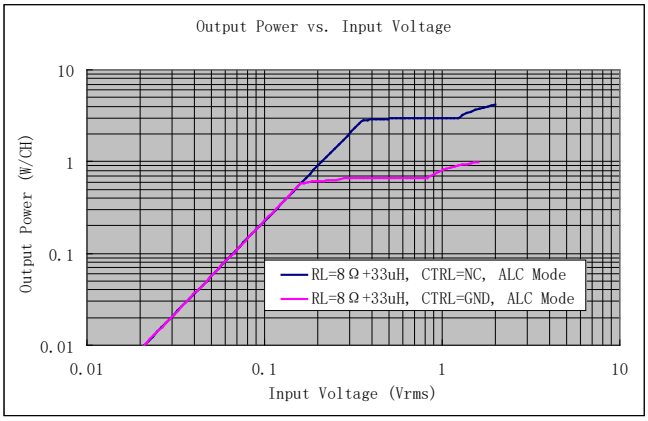


Figure 14: Output Power vs. Input Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

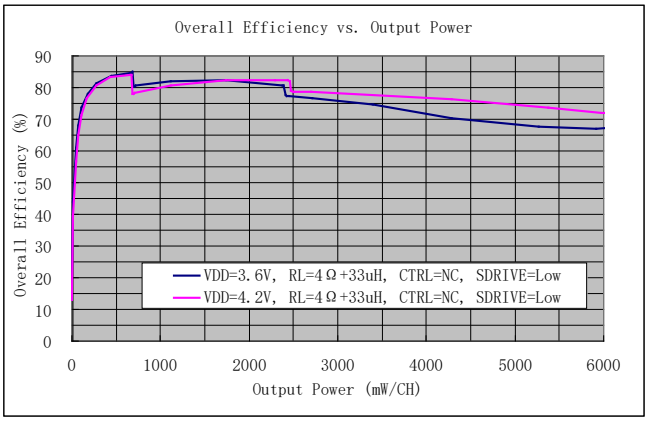


Figure 15: Overall Efficiency vs. Output Power
(Dual channels driven, including power dissipated by external Schottky diode)

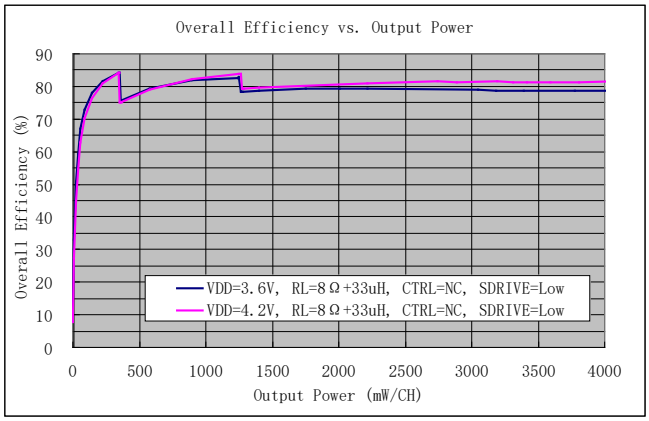


Figure 16: Overall Efficiency vs. Output Power
(Dual channels driven, including power dissipated by external Schottky diode)

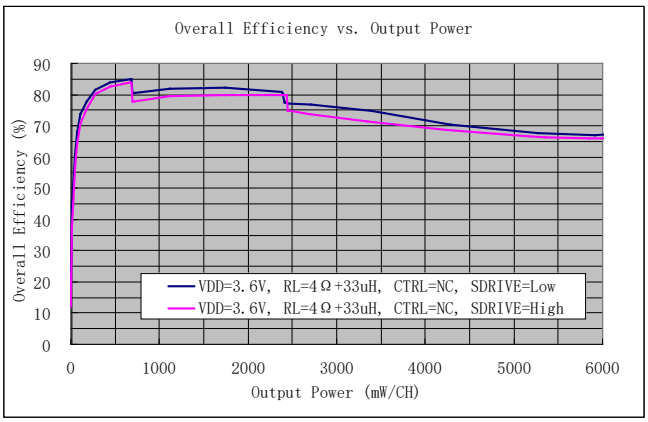


Figure 17: Overall Efficiency vs. Output Power
(Dual channels driven, including power dissipated by external Schottky diode)

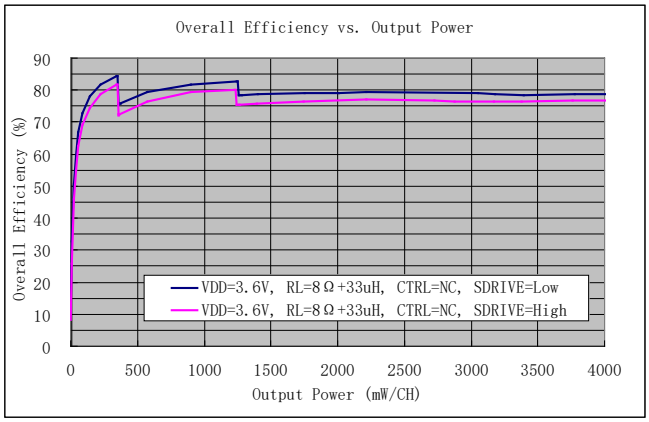


Figure 18: Overall Efficiency vs. Output Power
(Dual channels driven, including power dissipated by external Schottky diode)

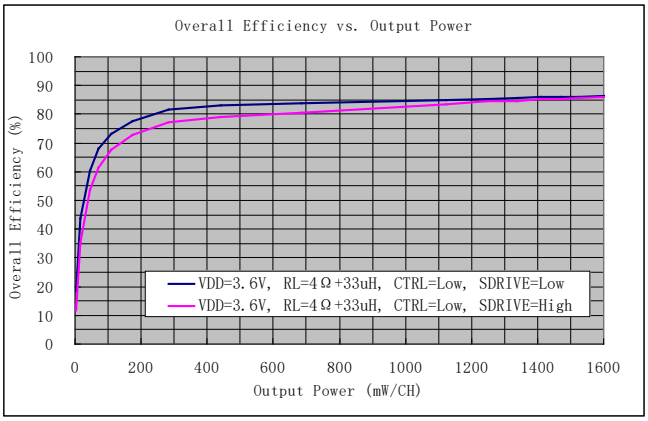


Figure 19: Overall Efficiency vs. Output Power
(Dual channels driven, including power dissipated by external Schottky diode)

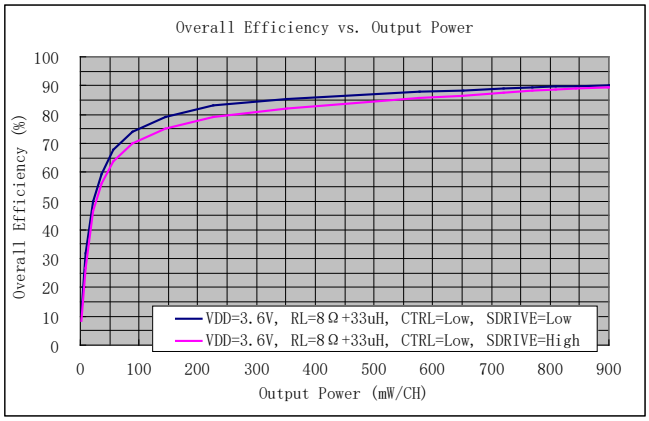


Figure 20: Overall Efficiency vs. Output Power
(Dual channels driven, including power dissipated by external Schottky diode)

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

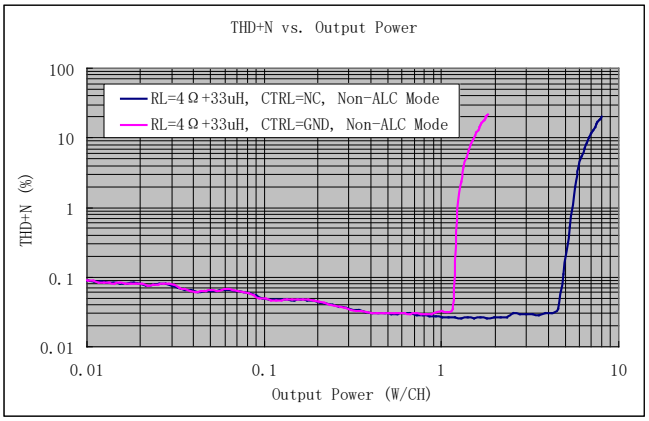


Figure 21: THD+N vs. Output Power

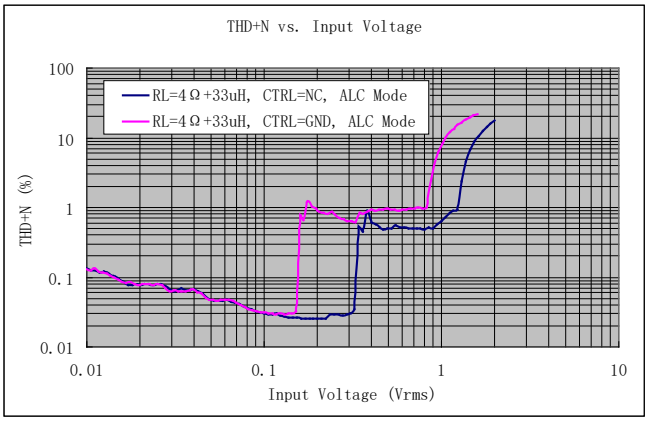


Figure 22: THD+N vs. Input Voltage

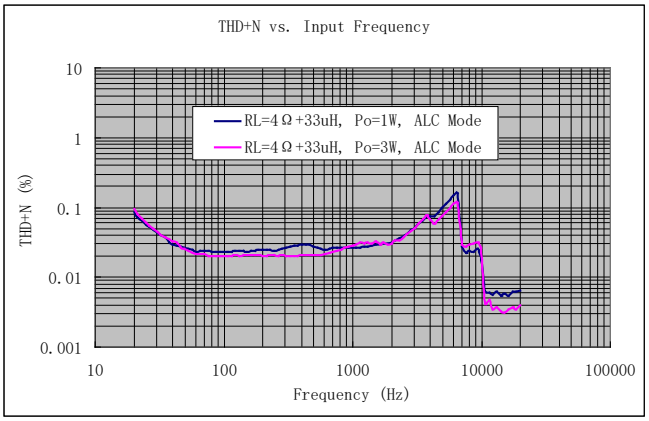


Figure 23: THD+N vs. Frequency

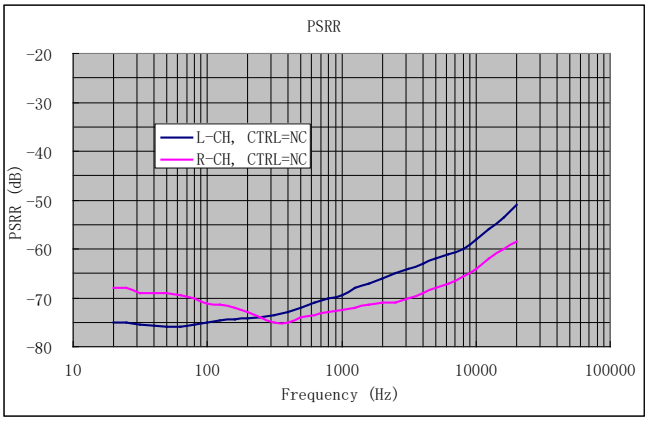


Figure 24: PSRR vs. Frequency

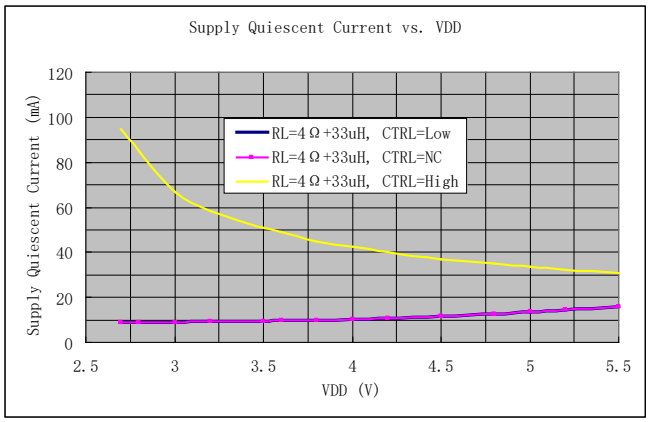


Figure 25: Supply Quiescent Current vs. VDD

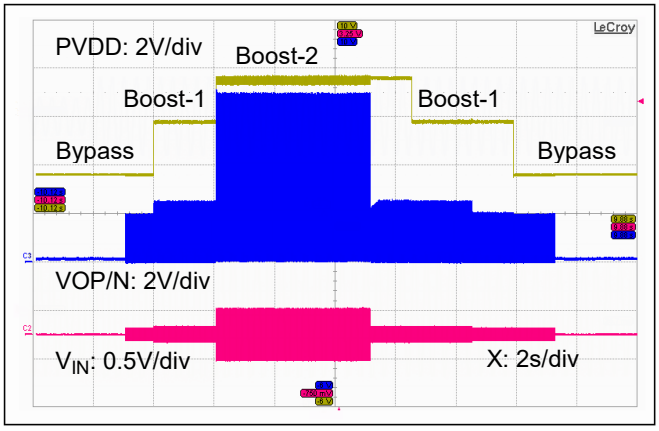


Figure 26: Mode Transitions of Boost Regulator

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

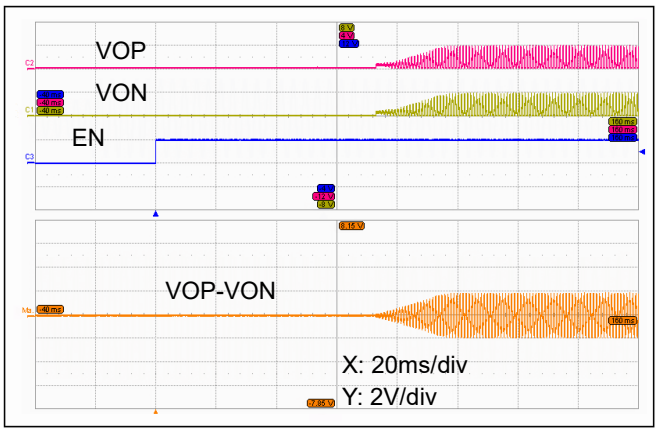


Figure 27: Output Waveforms on Startup

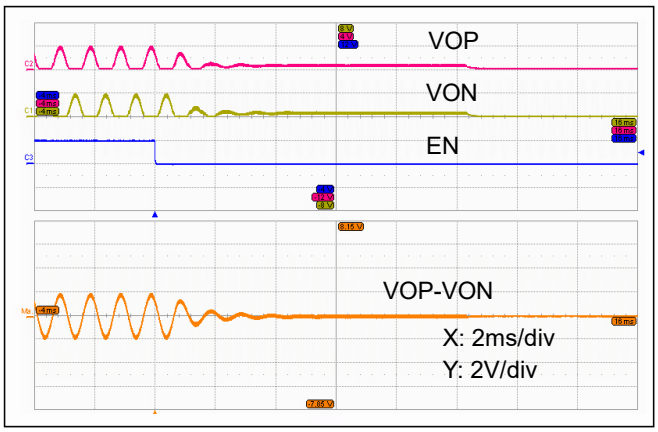


Figure 28: Output Waveforms on Shutdown

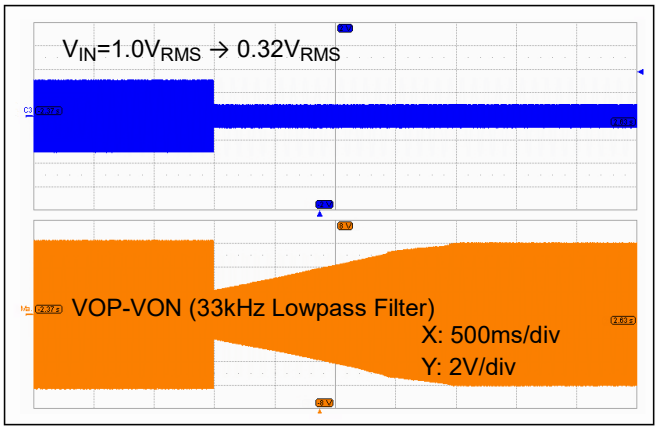


Figure 29: Output Waveforms on ALC-1 Release

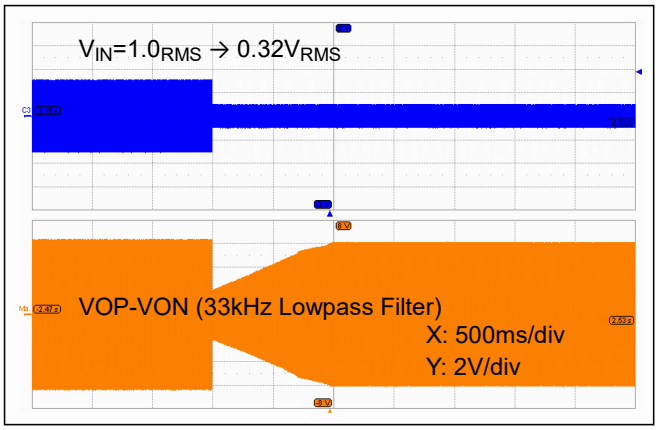


Figure 30: Output Waveforms on ALC-2 Release

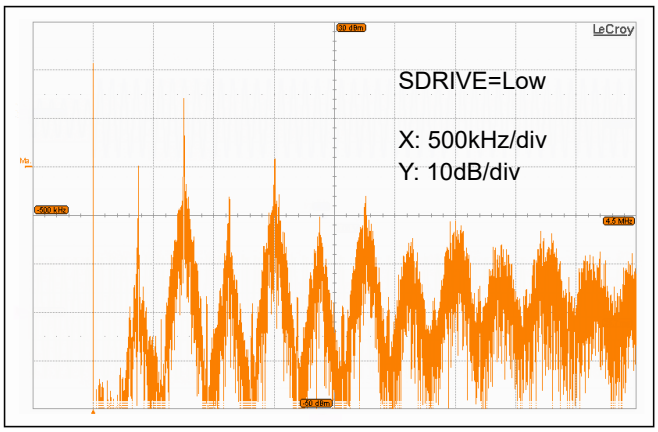


Figure 31: Broadband Output Spectrum

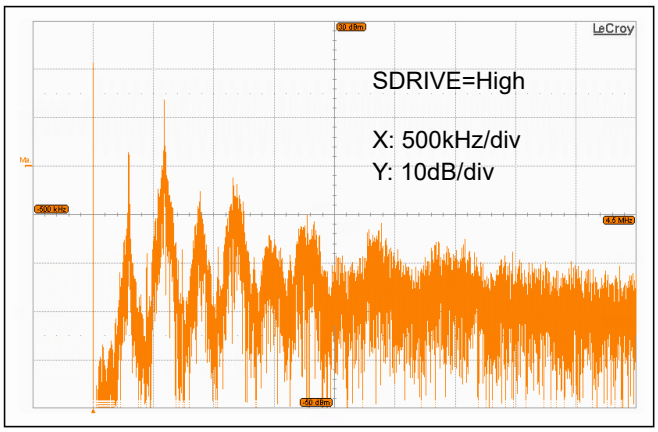


Figure 32: Broadband Output Spectrum

APPLICATION INFORMATION

The ft2928 is a fully integrated, highly efficient, 2X6.8W filterless Class-G stereo audio power amplifier with automatic level control (ALC) and battery tracking AGC. It integrates dual filterless Class-D audio amplifiers with an adaptive Class-G synchronous boost regulator and operates with a wide range of supply voltages from 2.7V to 5.5V. With a 3.6V supply voltage, the ft2928 can deliver an output power of 6.8W per channel with 10% THD+N, or 5.5W per channel with 1% THD+N, into a pair of 4Ω speaker loads.

In ft2928, the power supply rails of the audio amplifiers' output stages are internally boosted and regulated by a synchronous PWM switching regulator with two integrated power switches. The boost regulator employs current-mode PWM control with proprietary multi-level Class-G topology to regulate the boosted output voltage. The adaptive nature of the Class-G boost regulator, whose output voltage varies dynamically in response to the voltage level of the audio outputs, improves overall power efficiency and extends battery life when playing music. The higher output power and greater power efficiency resulted from the adaptive Class-G boost regulator make ft2928 an ideal audio solution for battery-powered electronic devices.

To facilitate various applications, the boost regulator in ft2928 is independently controlled with three operating modes: Adaptive Boost, Continual Boost, and Bypass.

The ft2928 features two modes of operation, i.e., ALC and Non-ALC, which can be selected via the ALC pin. When the ALC pin is shorted to VBAT, the ft2928 operates in Non-ALC mode, where the audio amplifiers are configured as conventional Class-D amplifiers without ALC. Conversely, when the ALC pin is unconnected or shorted to GND, the ft2928 operates in ALC mode, where the audio outputs of both channels are constantly monitored and safeguarded against the boosted supply voltage, preventing output clipping distortion, excessive power dissipation, and speaker over-load. Once an over-level condition is detected, the ALC lowers the voltage gain of both audio amplifiers together to eliminate output clipping while allowing for a maximally-allowed dynamic range of the audio outputs. The ft2928 offers two ALC dynamic characteristics for two distinctive sound effects, which are also selected via the ALC pin. In ALC-2 mode, with a supply voltage at 3.6V, the ft2928 can deliver an ALC output power of 5W per channel with 0.6% THD+N, into a pair of 4Ω speakers.

In conjunction with ALC, as the battery supply voltage drops below a prescribed value, the battery tracking AGC lowers the voltage gain of both audio amplifiers to limit peak audio outputs, preventing the collapse of battery voltage.

Furthermore, the Class-D audio amplifiers in ft2928 feature filterless PWM modulators that substantially lower or completely eliminate the requirement for external LC filters, reducing the number of external components, the system board space, and the system cost. With filterless PWM modulators, the efficiency of the audio amplifiers is also improved.

The ft2928 incorporates shutdown mode to minimize power consumption by holding the EN pin to ground. It also includes comprehensive protection features against various operating faults such as over-current, short-circuit, over-temperature, or under-voltage for safe and reliable operation.

ADAPTIVE BOOST REGULATOR

To allow for higher audio loudness, a Class-G boost regulator is integrated in ft2928 to boost the power supply rails (PVDDL/R) of the audio amplifiers' output stages from VDD to a higher voltage in response to the voltage level of the audio outputs. For proper operation, the power supply rails (PVDDL/R) must be externally shorted to PVOUT, the voltage output of the boost regulator, via sufficiently wide metal lines on the system board.

The integrated boost regulator employs fixed-frequency, peak-current PWM scheme with current-mode control. The PWM switching frequency is internally set at either 900kHz (High-Efficiency Drive mode) or 720kHz (Soft Drive mode), which allows using smaller inductance and output capacitance for stability and results in a higher PWM control loop bandwidth. Furthermore, the Class-G boost regulator in ft2928 features proprietary multi-level operation. As either one of the audio outputs is higher than the first prescribed value for an extended period, the ft2928 enters into Boost-1 mode, where the boost regulator is activated to boost and regulate PVOUT at an intermediate value. As either one of the audio outputs grows higher than the second prescribed value for an

extended period, the ft2928 enters into Boost-2 mode, where PVOUT is further boosted and regulated at its final value at 7.6V, typically.

Conversely, when both audio outputs are reduced to be lower than the second prescribed value for an extended period, the boost regulator returns back to Boost-1 mode. If both audio outputs are further reduced to be lower than the first prescribed value for an extended period, the ft2928 returns back to Bypass mode, where the boost regulator is de-biased. In Bypass mode, the audio amplifiers' output stages are powered directly from the supply input voltage, through the inductor and on-chip rectification power switch. Thus, in Bypass mode, PVOUT is equal to the supply input voltage minus the voltage drop across the rectification power switch.

The adaptive nature of the Class-G boost regulator in ft2928, where PVOUT varies dynamically in response to the voltage level of the audio outputs, can greatly improve overall power efficiency and extend battery life when playing music. The higher output power and greater efficiency resulted from the multi-level Class-G boost regulator make the ft2928 an ideal audio solution for battery-powered electronic devices.

DESIGN GUIDELINES OF BOOST REGULATOR

Selection of Boost Regulator Inductor

The selection of the inductor is the most important consideration in the design of power switching regulators since it affects the boost regulator's steady-state operation as well as dynamic response and loop stability. Three important inductor specifications are to be considered: Inductor value, DC resistance (DCR), and Saturation current. Note that inductor values may have tolerance up to ±20% with zero-current bias. Also, when the inductor current approaches its saturation limit, the effective inductance can fall to a fraction of its zero-current value. For typical applications, the recommended inductor peak (saturation) current ratings for speak loads of 4Ω and 8Ω are higher than 7A and 5A, respectively.

In general, a larger inductance value produces less inductor current ripple, which in turn results in lower inductor peak current, higher output current, lower EMI, and higher efficiency. On the other hand, a smaller inductance value, with a physically small size, results in an improved transient response with higher inductor peak current and potentially worse EMI and lower efficiency. An inductor in the range from 1.5μH to 3.3μH suffices for most applications of ft2928. Do not use any inductance higher than 3.3μH as it requires a larger output capacitance for stability of the PWM control loop, which in turn slows the boost regulator's response to load transients to a large extent with little improvements on the output current capability or efficiency. Select an inductor with DCR less than 10mΩ for higher overall power efficiency (from the power supply to the speaker load).

Selection of Boost Regulator Schottky Diode

A rectification power switch is integrated in the synchronous boost regulator of ft2928, thus no external Schottky diode is necessary for applications with speaker load impedances of 8Ω. However, for applications where speaker load resistances are 4Ω or less, it is necessary to add one or two Schottky diodes across LX and PVOUT pins to enhance maximum output power and overall power efficiency. The added Schottky diode must be rated for a current no less than 3A and a reverse breakdown voltage no less than 20V, such as SS34 or SS32. For best power efficiency, use a pair of SS34 diodes instead of a single SS54 diode for applications with heavy speaker loads.

Selection of Boost Regulator Output Capacitor (C_{PVOUT})

The output capacitor of the boost regulator is required to keep the output voltage ripple small and ensure the stability of the PWM control loop. The output capacitor must have low equivalent-series-resistance (ESR) at the PWM switching frequency, so ceramic capacitors are the best choice. Make sure that the output capacitors maintain their capacitances over the specified range of DC bias and operating temperature. A 22μF low-ESR ceramic capacitor suffices for most applications with speaker load impedances of 8Ω. For applications where the speaker load impedances are 4Ω or less, use two 22μF low-ESR ceramic capacitors in tandem.

Though unwarranted for loop stability, a bulk electrolytic capacitor can be added, as a part of the boost

regulator's output capacitors, to facilitate higher voltage margin for higher audio power at low frequencies. However, pay attention to any bulk output capacitance higher than 330μF as it might adversely slow the boost regulator's response to load transients to some extent affecting audio dynamics when playing music.

Also, add a small, good quality, low-ESR ceramic capacitor of 1μF in close proximity to the PVOUT pins for high-frequency filtering.

The boost regulator's output, PVOUT, must be externally connected to the power supply rails of the audio amplifiers' output stages, PVDDL/R, on the system board with wide and short metal traces.

Selection of Boost Regulator Input Capacitor (C_{VDD})

In practice, supply input capacitors are required for boost regulators. At least 22μF of input capacitance is required for supply decoupling for ft2928. The rated voltage of the input capacitor must be higher than the supply input voltage with sufficient tolerance to limit the effects of dc bias. For most applications where the power supply is reasonably designed, a low-ESR ceramic capacitor of 22μF, 16V with 10mΩ ESR is sufficient for ft2928. Also, add a small, good quality, low-ESR ceramic capacitor of 0.1μF in close proximity to the inductor for high-frequency supply decoupling.

For applications where additional input capacitance is required to meet the requirement of the input current ripple or transient response, place a bulk electrolytic capacitor between 100μF and 220μF in close proximity to ft2928. The bulk capacitor acts as a charge reservoir for the inductor current, providing energy faster than the system power supply, mitigating current surges or voltage droops of the supply voltage.

Boost Regulator Snubber Circuit

It is not uncommon for boost regulators to observe voltage oscillations in a frequency range of 100MHz ~ 200MHz at the switch node LX due to parasitic inductances and capacitances on its high-current path. If the amplitude of the voltage ringing is above the absolute maximum rating of the LX pin, the on-chip power switches can be damaged permanently.

For applications where excessive voltage spikes or oscillations are observed due to severe restrictions on the board layout, it may become necessary to add a snubber circuit from the switch node LX to the power ground BGND to lower voltage spikes and eliminate voltage oscillations at the switch node. A snubber circuit, a small resistor in series with a small capacitor, is an energy-absorbing circuit to provide an alternative path to ground for the current flowing through the parasitic inductances. In practice, the snubber circuit is added to lower EMI emissions as well as enhance the operational reliability of the boost regulator.

Figure 33 shows an RC snubber circuit with suggested values of R_{LX}=1Ω and C_{LX}=4.7nF ~ 10nF. Note that the design of the RC snubber circuit is specific to each design and board layout, of which the parasitic inductances and capacitances must be taken into consideration to reach proper values of R_{LX} and C_{LX}. Evaluate and ensure that the voltage spikes at LX are within the absolute maximum rating of LX on the actual system board. Pay close attention to the layout of the snubber circuit to be tight and in close proximity to LX and BGND pins. Note that the RC snubber circuit will adversely affect the overall efficiency of the boost regulator by a few percent, which is a function of the C_{LX} value.

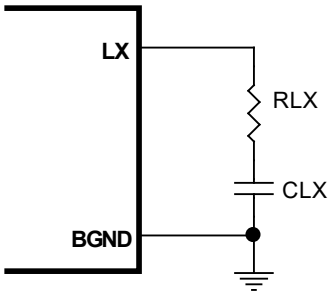


Figure 33: RC Snubber Circuit at LX Pin

BOOST REGULATOR CONTROL

To facilitate various applications, the operation of the boost regulator is independently controlled via the CTRL pin, which includes an on-chip pullup resistor of 300kΩ to VBAT and an on-chip pulldown resistor of 300kΩ to ground. As shown in Table 1, three operating modes (Adaptive Boost, Continual Boost, and Bypass) are available in ft2928. In typical applications, the boost regulator is activated either adaptively (in response to the voltage level of the audio outputs) or continually.

When the CTRL pin is left unconnected, the device operates in Adaptive Boost mode. In Adaptive Boost mode, the boost regulator is adaptively activated and the boosted output voltage (PVOUT) varies dynamically as a function of the voltage level of the audio outputs. The adaptive nature of the Class-G boost regulator improves overall power efficiency and extends battery life when playing music

When the CTRL pin is asserted high or shorted to VBAT, the device operates in Continual Boost mode. In Continual Boost mode, the boost regulator is activated at all times and the boosted output voltage (PVOUT) remains constant, which can be used as a regulated supply voltage for other on-board devices such as LEDs. The total RMS current drawn from PVOUT by other on-board devices should be limited to less than 200mA. An excessive load current at PVOUT may cause severe loss of maximum output power and power efficiency of ft2928.

When the CTRL pin is pulled low or shorted to GND, the device operates in Bypass mode. In Bypass mode, the boost regulator is de-biased at all times and the output voltage PVOUT is equal to the battery supply voltage minus the voltage drop across the inductor and the on-chip rectification power switch. Although it offers minimum EMI emissions, the Bypass mode delivers lower output power, which is limited by the battery supply voltage. In practice, the Bypass mode is chosen specifically for applications where minimum FM interference is required.

CTRL Pin Configuration	Mode of Operation	Description
High	Continual Boost	Boost regulator activated continually
Unconnected	Adaptive Boost	Boost regulator activated adaptively
Low	Bypass	Boost regulator de-biased

Table 1: Boost Regulator Control

AUTOMATIC LEVEL CONTROL (ALC)

The automatic level control (ALC) is to maintain the audio outputs for a maximum voltage swing without clipping when excessive inputs that may cause clipping distortion are applied. With ALC, the ft2928 lowers the voltage gain of the audio amplifiers to an appropriate value such that output clipping is substantially eliminated.

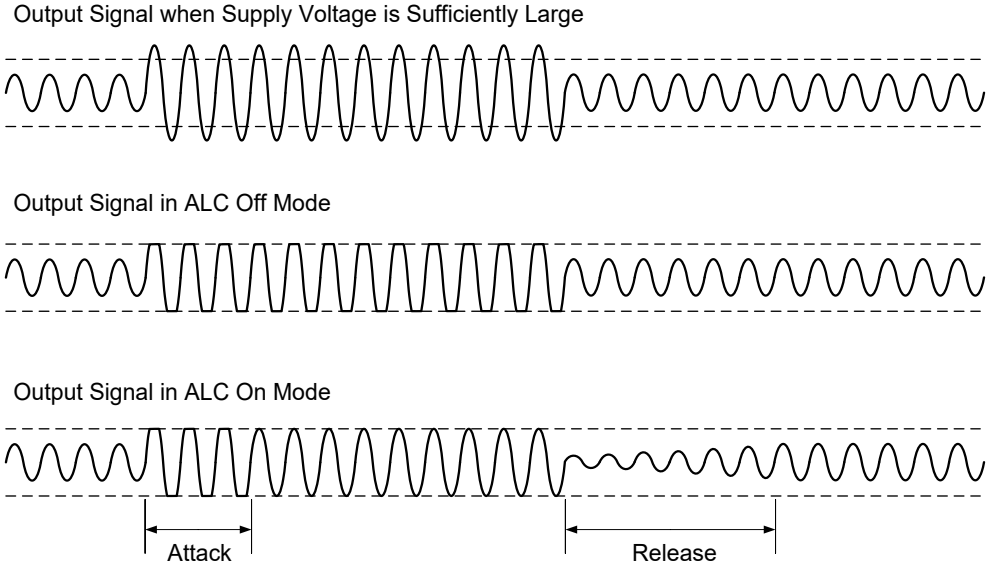


Figure 34: Automatic Level Control Diagram

Figure 34 depicts the effect of ALC on the audio outputs. In the figure, “Attack” is defined as the process where the voltage gain of the audio amplifiers decreases until output clipping is substantially eliminated. “Release” is defined as the process where the voltage gain of the audio amplifiers recovers (increases) until it reaches to a value that is maximally allowed without output clipping.

ALC MODE CONTROL

The ft2928 can be configured in ALC or Non-ALC mode via the ALC pin, which includes an on-chip pullup resistor of 300kΩ to VBAT and an on-chip pulldown resistor of 300kΩ to ground. As described in Table 2, when the ALC pin is asserted high or shorted to VBAT, the ft2928 operates in Non-ALC mode. The Non-ALC operation is typically chosen for applications where maximum audio loudness is much desired and output clipping distortion can be properly controlled and largely eliminated at the audio source. Conversely, when the ALC pin is left unconnected or shorted to GND, the ft2928 operates in ALC mode with two sets of dynamic characteristics. For most applications, the ALC mode of operation is preferred for its capability to substantially eliminate output clipping distortion, excessive power dissipation, and speaker over-load.

Two sets of ALC dynamic characteristics can be selected for specific sound effects, as described in Table 2. The ALC-1 mode, where the ALC pin is shorted to GND, tends to play music in a mellower manner with negligible amount of clipping distortion and lower average output power (loudness). On the other hand, the ALC-2 mode, where the ALC pin is left unconnected, tends to play music in a more dynamic manner with higher average output power (loudness) and some extent of clipping distortion.

ALC Pin Configuration	Mode of Operation	Sound Effects	
		Loudness	Output Clipping Distortion
High	Non-ALC	Potentially highest loudness	No control on output clipping
Unconnected	ALC-2	Higher loudness (Dynamic sound)	Acceptable output clipping
Low	ALC-1	Lower loudness (Mellow sound)	Negligible output clipping

Table 2: ALC Mode Control

VOLTAGE GAIN SETTING

In ft2928, the voltage gain of the audio amplifiers can be externally adjusted by inserting additional input resistors in series with audio input capacitors, as depicted in Figure 35 and Figure 36. In typical applications, it is required that $C_{IN}=C_{INL1}=C_{INL2}=C_{INR1}=C_{INR2}$ and $R_{IN}=R_{INL1}=R_{INL2}=R_{INR1}=R_{INR2}$.

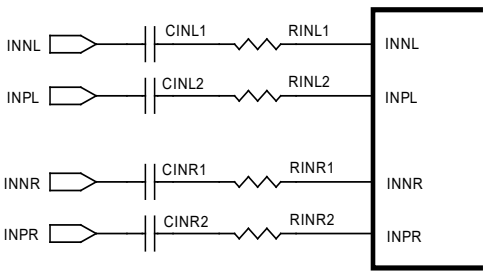


Figure 35: Gain Setting (Differential Inputs)

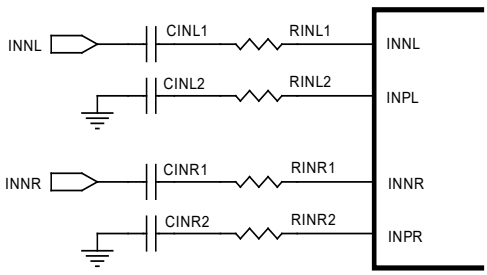


Figure 36: Gain Setting (Single-Ended Inputs)

The value of R_{IN} (in kΩ) for a given voltage gain can be calculated by Equation 1, where A_V is the voltage gain and R_{IN} is the external input resistance (in kΩ) in series with the internal input resistance of 22.5kΩ. Table 3 shows proper resistor values of R_{IN} that can be used for various voltage gains.

$$A_V = \frac{450}{R_{IN} + 22.5} \qquad (1)$$

R_{IN} (kΩ)	0	2.7	3.9	5.6	7.5	10	14	18	22	27	33	39
A_V (V/V)	20	18	17	16	15	14	12.3	11	10	9	8	7.3
A_V (dB)	26	25	24.6	24	23.5	23	22	21	20	19	18	17

Table 3: External Input Resistors Required for Various Voltage Gains

The choice of the voltage gain strongly influences the loudness and quality of audio sounds. In general, the higher the voltage gain is, the louder the sound is perceived. However an excessive voltage gain may cause the audio outputs to be severely compressed or clipped for high-level (loud) audio sounds. On the other hand, an unusually low gain may cause relatively low-level (quiet) sounds soft or inaudible. Thus it is crucial to choose a proper voltage gain for high audio quality.

The voltage gain is chosen based upon various system-level considerations including the boosted supply voltage, maximum input level of the audio source, output power rating, and desired sound effect. As an example, Table 4 and 5 show the voltage gains for various audio input levels in ALC (with 3dB ALC dynamic range) and Non-ALC (with 1% THD+N) operation, respectively. In the table, R_{IN} is the external input resistor in series with the audio input capacitor. In ALC, the voltage gain of the audio amplifiers is typically set between 20X (26dB) and 7.3X (17dB), which corresponds to an external input resistor between 0kΩ and 39kΩ, respectively. In non-ALC, the voltage gain of the audio amplifiers is typically set between 17X (24.6dB) and 5X (17dB), which corresponds to an external input resistor between 3.9kΩ and 68kΩ, respectively.

The voltage gain can be also expressed in Equation 2. In the equation, $V_{IN,\,MAX}$ (in V_{RMS}) is the maximum input level of the audio source, PVDD (in volts) is the boosted supply voltage, and α is a design parameter that determines the ALC dynamic range (maximum attenuation) and typically ranges from 0.65 to 1.2. Higher α will result in higher ALC dynamic range and higher average output power (loudness) with some degree of compression for high-level audio sounds. Conversely, lower α will result in lower ALC dynamic range and lower average output power (loudness) with minimum or no compression for high-level audio sounds.

$$A_V = \frac{\alpha \times PVDD}{V_{IN,\,MAX}} \qquad (2)$$

$V_{IN,\,MAX}$ (V_{RMS})	A_V (V/V)	A_V (dB)	R_{IN} (kΩ)
0.3	20	26	0
0.5	14	23	10
0.7	10	20	22
1.0	7.3	17	39

Table 4: Typical Voltage Gain Settings in ALC Operation (with 3dB ALC Dynamic Range)

$V_{IN,\,MAX}$ (V_{RMS})	A_V (V/V)	A_V (dB)	R_{IN} (kΩ)
0.3	17	24.6	3.9
0.5	10	20	22
0.7	7.3	17	39
1.0	5	14	68

Table 5: Typical Voltage Gain Settings in Non-ALC Operation (with 1% THD+N)

BATTERY TRACKING AGC CONTROL

The ft2928 features battery tracking AGC to limit peak audio outputs as the battery voltage droops. Although it affects audio output loudness on low battery voltages, the battery tracking AGC limits high battery current at the end-of-charge battery voltage and prevents the battery voltage from collapsing, which may cause a system reset.

The battery tracking AGC keeps peak audio outputs below a limiting value that is a function of the battery voltage. The peak audio outputs are maintained at a value close to PVDD for battery voltages down to the knee voltage and reduced linearly at a rate of 3V/V for lower battery voltages. The knee voltage of the battery tracking AGC can be selected via the VKNEE pin, as described in Table 5. Note that an on-chip 300kΩ pullup resistor to VBAT is included onto the VKNEE pin. Thus, the battery tracking knee voltage is set at 3.5V with the pin unconnected.

VKNEE Pin Configuration	Battery Tracking Knee Voltage (V)
Unconnected	3.5
300kΩ to GND	3.2
Short to GND	Battery Tracking AGC Disabled

Table 5: Battery Tracking AGC Control

The operation of the battery tracking AGC can be highly influenced by the electrical characteristics of the battery used with ft2928. Place a small decoupling resistor of 10Ω between the battery supply voltage and the VBAT pin, coupled with a decoupling capacitor of 1μF, mitigating the detrimental effect of high battery current ripples on the detection of battery voltage. The value of the decoupling resistor R_{VBAT} can also adjusted to fine-tune the knee voltage of the battery tracking AGC.

The battery tracking AGC can be activated only when the boost regulator and ALC function are both enabled, where the CTRL pin is asserted high or left unconnected and the ALC pin is shorted to ground or left unconnected. The battery tracking AGC is de-activated when either the CTRL pin is shorted to ground or the ALC pin is asserted high.

SOFT-DRIVE CONTROL

To minimize EMI emissions, proprietary gate drivers with edge-rate control are applied to the power stages of both Class-D audio amplifiers and the Class-G boost regulator in ft2928. For further reduction of EMI emissions and FM interferences, the ft2928 facilitates optional soft-drive operation for all the gate drivers. In the soft-drive operation, the slew rates of high-current outputs (VOPL/R, VONL/R, and LX) are largely lowered at the expense of higher power dissipations, resulting in lower efficiency. As shown in Table 6, the soft-drive operation can be enabled by asserting the SDRIVE pin high. Note that an on-chip pulldown resistor of 300kΩ to ground is included onto the SDRIVE pin. Thus, high-efficiency drive is applied when the pin is unconnected.

SDRIVE	Gate Driver	Description
Low	High-Efficiency Drive	High-Efficiency, High Power Operation
High	Soft Drive	Low-EMI, Medium Power Operation

Table 6: Soft-Drive Control

VOLUME FADE-IN & FADE-OUT

The ft2928 features volume fade-in and fade-out to reduce intermittent sound and eliminate uncomfortable hearing experience during the transitions when the device enters into or exits out of normal operation. Figure 37 and Figure 38 show the audio output waveforms during fade-in and fade-out respectively.

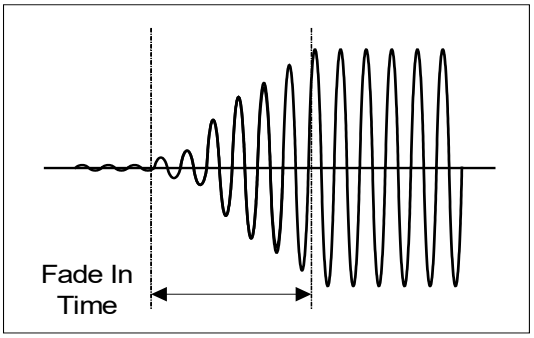


Figure 37: Fade-In Output Waveform

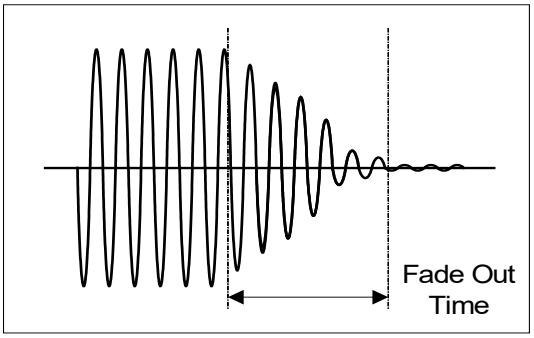


Figure 38: Fade-Out Output Waveform

MUTE CONTROL

To facilitate fast turn-off and turn-on of audio outputs, the ft2928 can be configured in mute mode via the MUTE pin. Once the MUTE pin is asserted high, the power stages of both audio amplifiers are placed in Hi-Z and the differential audio outputs (VOPL/R and VONL/R) pulled to ground through their individual on-chip pulldown resistors. Conversely, when the MUTE pin is pulled low, the device will exit out of mute mode and resume normal operation immediately. An on-chip pulldown resistor of 300kΩ to ground is included onto the MUTE pin.

SHUTDOWN AND STARTUP

The ft2928 employs the EN pin to minimize power consumption while it is not in use. When the EN pin is pulled low, the ft2928 is forced into shutdown mode, where all the analog circuitry is de-biased and the supply current is reduced to be less than 1μA, and the differential outputs are shorted to ground through their individual on-chip pulldown resistors. Once in shutdown mode, the EN pin must remains low for at least 5 milliseconds (T_{SD}), the shutdown settling time, before it can be brought high again. When the EN pin is asserted high, the device exits out of shutdown mode and enters into normal operation after a startup time (T_{STUP}) of 80 milliseconds.

Note that an on-chip pulldown resistor of 300kΩ to ground is included onto the EN pin. Thus, shutdown mode is the default state when the power supply is first applied to the device. Whenever possible, it is recommended to assert EN high to exit the device out of shutdown mode only after the device is properly started up. Also, place the amplifier in shutdown mode prior to removing the power supply voltage for the best power-off pop performance.

CLICK-AND-POP SUPPRESSION

The ft2928 features comprehensive click-and-pop suppression. During startup, the click-and-pop suppression circuitry reduces any audible transients internal to the device. When entering into shutdown, the differential audio outputs ramp down to ground simultaneously.

PSRR ENHANCEMENT

Without a dedicated pin for the common-mode voltage bias, the ft2928 achieves a PSRR, 70dB at 1kHz.

PROTECTION MODES

Against various operating faults for safe and reliable operation, the ft2928 includes comprehensive protection modes including Under-Voltage Lockout (UVLO), Over-Current Protection (OCP), and Over-Temperature Shutdown (OTSD).

Under-Voltage Lockout (UVLO)

The ft2928 incorporates a circuitry to detect a low supply voltage. When the supply voltage is first applied, the ft2928 will remain inactive until the supply voltage exceeds 2.3V (V_{UVLU}). When the supply voltage is removed and drops below 2.1V (V_{UVLD}), the ft2928 enters into shutdown mode immediately.

Over-Temperature Shutdown (OTSD)

When the die temperature exceeds a prescribed threshold (160°C), the device enters into over-temperature shutdown mode, where the audio outputs are pulled to ground through their individual on-chip resistors. The device will resume normal operation once the die temperature returns to a lower temperature, which is about 20°C lower than the threshold.

Over-Current Protection (OCP)

During operation, the Class-D amplifier outputs are constantly monitored for any over-current or short-circuit conditions. When an over-current condition between two differential outputs, differential output to PVDDL/R or PGND is detected, the output stage of the amplifier is immediately forced into high impedance state. If the fault condition persists over a prescribed period, the ft2928 then enters into shutdown mode and remains in shutdown mode for about 40 milliseconds, the over-current recovery time. When shutdown mode times out, the ft2928 will initiate a startup sequence and then check if the over-current condition has been removed. If the fault condition is still present, the ft2928 will repeat itself for the process of a startup followed by detection, qualification, and shutdown. It is the so-called hiccup mode of operation. Once the fault condition is removed,

the ft2928 automatically resumes to its normal mode of operation.

Although the output stages of the Class-D audio amplifiers can withstand a short between VOPL/R and VONL/R, do not connect any audio outputs directly to GND, AVDD, PVOUT, or PVDDL/R as this might damage the device permanently.

CLASS-D AUDIO AMPLIFIER

The Class-D audio amplifiers in the ft2928 operate in much the same way as traditional Class-D amplifiers and similarly offer much higher power efficiency than Class-AB amplifiers. The high efficiency of Class-D operation is achieved by the switching operation of the output stages of the amplifiers. The power loss associated with the output stage is limited to the conduction and switching loss of the power switches, which are much less than the power loss associated with a linear output stage in Class-AB amplifiers.

Fully Differential Amplifier

The ft2928 includes a pair of fully differential amplifiers with differential inputs and outputs. The fully differential amplifiers ensure that the differential output voltages are equal to the differential input voltages times the amplifier gain. Although the ft2928 supports for a single-ended input, differential inputs are much preferred for applications where the environment can be noisy in order to ensure maximum SNR.

Low-EMI Filterless Output Stage

Traditional Class-D audio amplifiers require external LC filters or shielding to meet EN55022B EMI regulation standards. The ft2928 applies an edge-rate control circuitry to reduce EMI emissions, while maintaining high power efficiency.

Filterless Design

Traditional Class D amplifiers require an output filter to recover the audio signal from the amplifier's output. The filter adds cost, increases the solution size of the amplifier, and can adversely affect efficiency and THD performance. The traditional PWM scheme uses large differential output swings (twice of the supply voltage) and causes large ripple currents. Any parasitic resistance in the filter components results in loss of power and lowers the efficiency.

The ft2928 does not require an output filter. The device relies on the inherent inductance of the speaker coil and the natural filtering of both the speaker and the human ear to recover the audio component of the square-wave output. By eliminating the output filter, a smaller, less costly, and more efficient solution can be accomplished.

Because the frequency of the audio outputs is well beyond the bandwidth of most speakers, voice coil movement due to the square-wave frequency is very small. Although this movement is small, a speaker not designed to handle the additional power can be damaged. For optimum performance, use speakers with series inductances greater than 10uH. Typical 4Ω speakers exhibit series inductances in the range from 10μH to 47uH.

EMI Reduction

The ft2928 does not require an LC output filter for the connections from the amplifier to the speaker. However, additional EMI suppression can be made by use of a ferrite bead filter comprising a ferrite bead and a capacitor, as shown in Figure 39. Choose a ferrite bead with low DC resistance (DCR) and high impedance (100Ω ~ 330Ω) at high frequencies (>100MHz). The current flowing through the ferrite bead must be also taken into consideration. The effectiveness of ferrites can be greatly aggravated at much lower than the rated current values. Choose a ferrite bead with a rated current no less than 2A for an 8Ω load and 3A for a 4Ω load. The capacitor value varies based on the ferrite bead chosen and the actual speaker lead length. Choose a capacitor less than 1nF based on EMI performance. Place each ferrite bead filter tightly together and individually close to VOPL/R and VONL/R pins respectively.

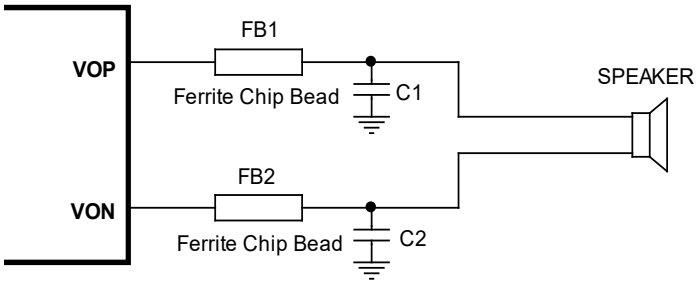


Figure 39: Ferrite Bead Filter to Reduce EMI

Class-D Output Snubber Circuit

For applications where speaker load resistances are 4Ω or less, it may become necessary to add a snubber circuit across the two output pins, VOPL/R and VONL/R, to prevent the device from accelerated deterioration or abrupt destruction due to excessive inductive flybacks that are induced on fast output switching or by an over-current or short-circuit condition. The snubber circuit can further lower EMI emissions of Class-D outputs.

Figure 40 shows a simple RC snubber circuit with suggested values of R_3=4.7Ω in series with C_3=4.7nF. Note that the design of the RC snubber circuit is specific to each design and must take into account the parasitic reactance of the system board to reach proper values of R and C. Evaluate and ensure that the voltage spikes (overshoots and undershoots) at VOPL/R and VONL/R on the actual system board are within their absolute maximum ratings. Pay close attention to the layout of the RC snubber circuit to be tight and individually close to VOPL/R and VONL/R pins, respectively.

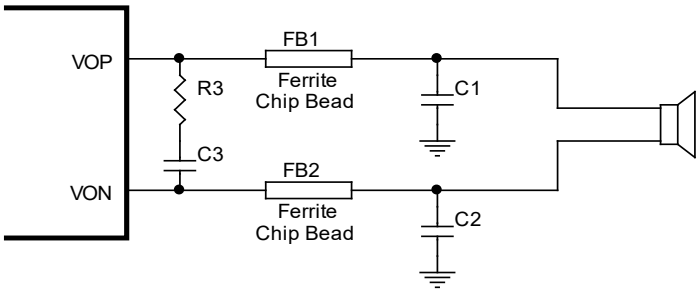


Figure 40: RC Snubber Circuit of Class-D Outputs

Audio Input Capacitor (C_{IN})

DC decoupling capacitors for audio inputs (INPL/R and INNL/R) are recommended. The input audio DC decoupling capacitors will remove the DC bias from audio inputs. The audio input capacitor C_{IN} and the total input resistance (R_{IN} + 22.5kΩ) form a highpass filter with the corner frequency, f_C, determined by Equation 3.

$$f_C = 1 / [2 \times \pi \times (R_{IN} + 22.5k\Omega) \times C_{IN}] \quad (3)$$

where $R_{IN}=R_{INL1}=R_{INL2}=R_{INR1}=R_{INR2}$ and $C_{IN}=C_{INL1}=C_{INL2}=C_{INR1}=C_{INR2}$

R_{IN} is the external input resistance for a specific voltage gain. Note that the variation of the actual input resistance will affect the voltage gain proportionally. Choose R_{IN} with a tolerance of 2% or better.

Choose C_{IN} such that f_C is well below the lowest frequency of interest. Setting it too high affects the amplifiers' low-frequency response. Consider an example where the specification calls for A_V=23dB and a flat frequency response down to 20Hz. In this example, R_{IN}=10kΩ and C_{IN} is calculated to be about 0.25μF; thus 0.33μF, as a common choice of capacitance, can be chosen for C_{IN}.

Any mismatch in resistance and capacitance between two audio inputs will cause a mismatch in the corner frequencies. Severe mismatch may also cause turn-on pop noise and degradation of PSRR and CMRR performance. Choose R_{IN} and C_{IN} with a tolerance of ±2% or better.

Furthermore, the type of audio input capacitors is crucial to audio quality. For best audio quality, use capacitors whose dielectrics have low voltage coefficients, such as aluminum electrolytic. Capacitors with high voltage coefficients, such as ceramics, may result in increased distortion at low frequencies.

Supply Decoupling Capacitors (C_{VBAT}, C_{AVDD}, C_{BVDD}, $C_{PVDDL/R}$)

Sufficient decoupling of the power supplies is crucial for Class-D audio amplifiers to ensure high efficiency, low distortion, and low EMI.

Place a 1μF low-ESR ceramic capacitor (C_{VBAT}) in close proximity to the VBAT pin. Furthermore, add a small decoupling resistor (R_{VBAT}) of 10Ω between the system power supply and the VBAT pin, minimizing the detrimental effect of high battery current ripples on the detection of battery voltage.

Place a 1μF low-ESR ceramic capacitor (C_{AVDD}) in close proximity to the AVDD pin. This capacitor type and placement of C_{AVDD} help minimize higher frequency transients, spikes, or digital hash on the supply line. Furthermore, add a small decoupling resistor (R_{AVDD}) of 10Ω between AVDD and PVOUT pins, preventing high frequency transients of PVOUT from interfering with on-chip linear circuitry.

Place a 1μF low-ESR ceramic capacitor (C_{BVDD}) in close proximity to the BVDD pin for high-frequency filtering.

Place a 1μF low-ESR ceramic capacitor ($C_{PVDDL/R}$) individually close to each PVDDL/R pin. Also, it is highly suggested to add a small, good quality, low-ESR ceramic capacitor of 0.01μF in close proximity to PVDDL/R pins for high-frequency supply decoupling.

PRINTED CIRCUIT BOARD (PCB) LAYOUT GUIDELINES

Ground Plane - It is required to use a solid metal plane with sufficiently wide area as a central ground connection (GND) for ft2928. All ground pins (AGND, BGND, and PGND) are directly shorted to the ground plane.

Supply Decoupling capacitors – The supply decoupling capacitors (C_{VBAT}, C_{AVDD}, C_{BVDD}, and $C_{PVDDL/R}$) should be placed as individually close as possible to VBAT, AVDD, BVDD, and PVDDL/R pins.

Boost Regulator Input Capacitors - Place the supply input capacitors (C_{VDD}) in close proximity to the inductor. They should be placed on the same layer of the system board with ft2928.

Boost Regulator Inductor & Schottky Diode - Place the inductor and Schottky diode tightly together and in close proximity to the LX pins. They should be placed on the same layer of the system board with ft2928.

Boost Regulator Output Capacitors - Place the output capacitors (C_{PVOUT}) in close proximity to the PVOUT pins. They should be placed on the same layer of the system board with ft2928.

Boost Regulator Snubber Circuit - Place the RC snubber circuit tightly together and in close proximity to the LX pins. They should be placed on the same layer of the system board with ft2928.

Ferrite Bead EMI Filter - Place the ferrite bead filters of the Class-D outputs as individually close to audio output pins, VOPL/R and VONL/R, as possible for optimum EMI performance. Keep the current loop from each of the audio outputs through the ferrite bead and the capacitor and back to PGND as short and tight as possible.

Class-D Output RC Snubber – Place the RC snubber circuit tightly together and as close as possible to the audio output pins, VOPL/R and VONL/R.

Power Dissipation - The maximum output power of ft2928 can be severely limited by its thermal dissipation capability of the system board. To ensure the device operating properly and reliably at maximum output power without incurring over-temperature shutdown, the following design guidelines of the system board are given for best thermal dissipation capability:

- Fill both top and bottom layers of the system board with solid GND metal traces.
- Solder the thermal pad directly onto a grounded metal plane.
- Place lots of equally-spaced vias underneath the thermal pad connecting the top and bottom layers of GND. The vias are connected to a solid metal plane on the bottom layer of the board.
- Reserve wide and uninterrupted areas along the thermal flow on the top layer, i.e., no wires cutting through the GND layer and obstructing the thermal flow.
- Place all the passive devices (Inductor, Schottky diode, and Input/output capacitors) of the boost regulator tightly together and placed on the same layer of the board with ft2928.
- Avoid using vias for traces carrying high current.

PCB LAYOUT EXAMPLE

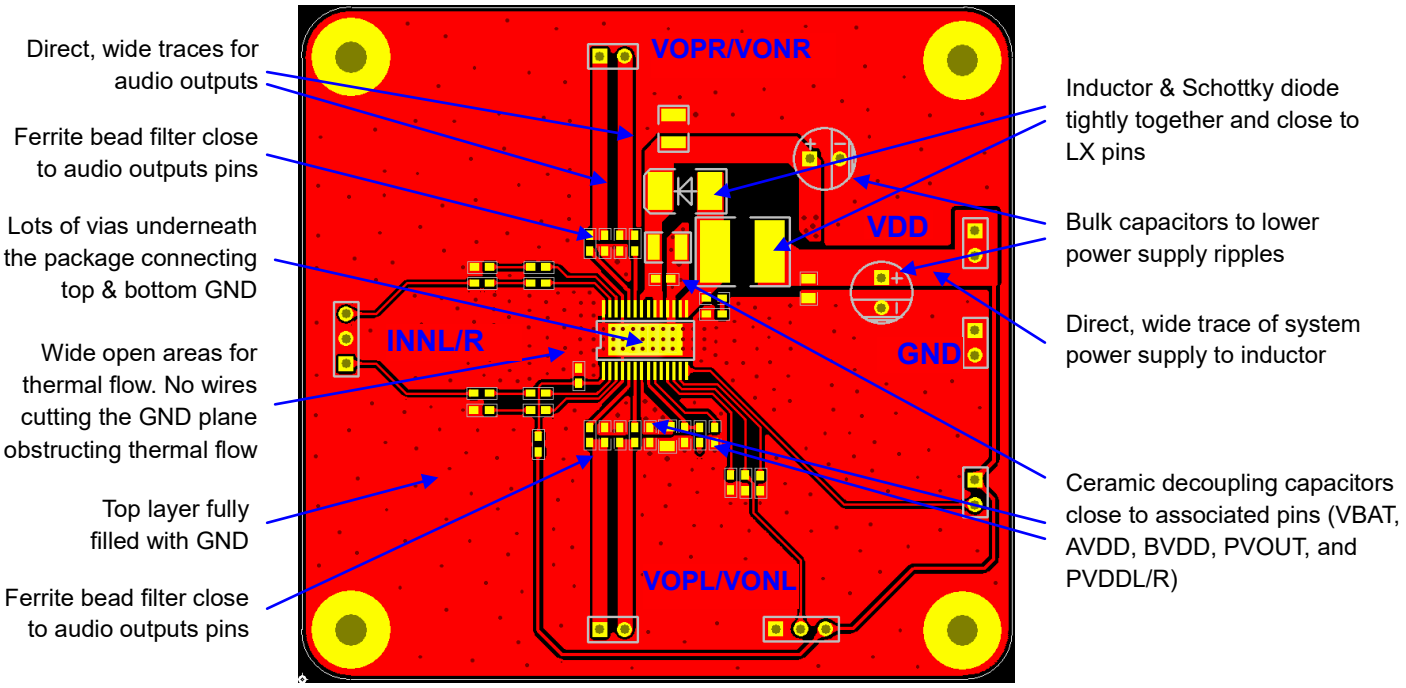


Figure 41: Top Layer of Layout Example

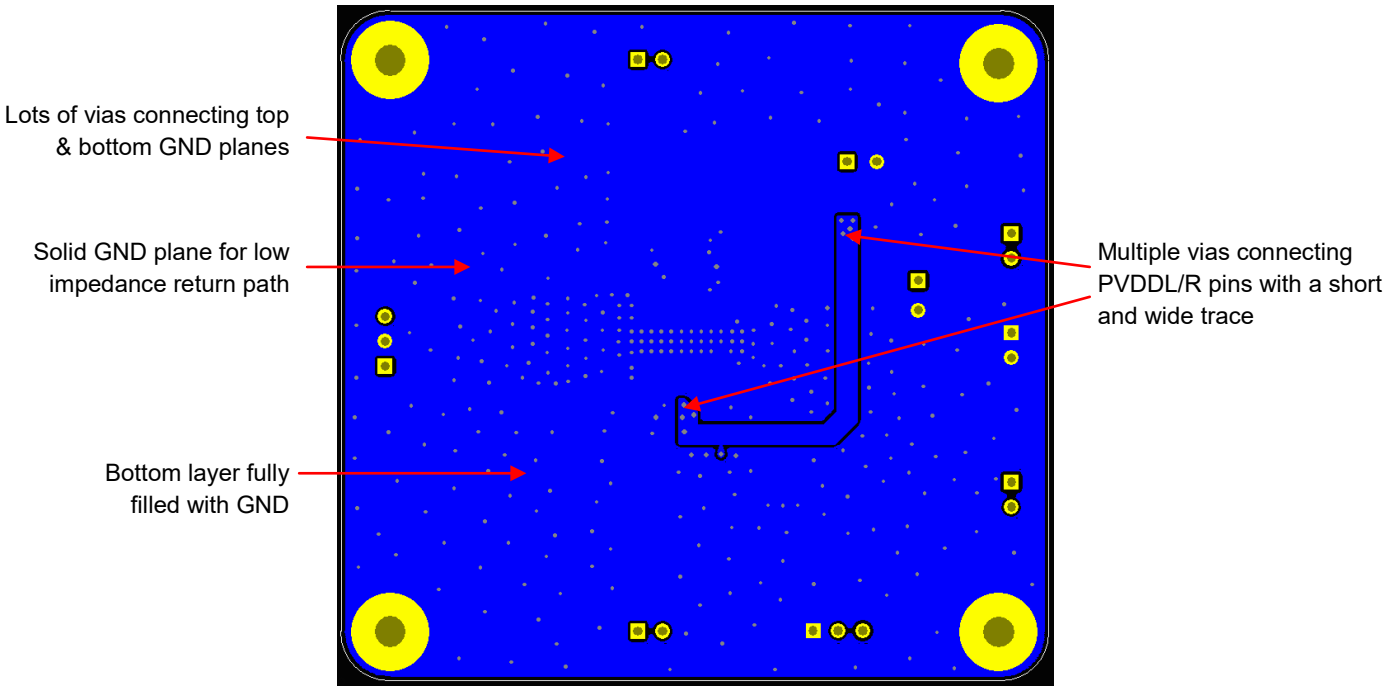


Figure 42: Bottom Layer of Layout Example

TYPICAL APPLICATION CIRCUITS

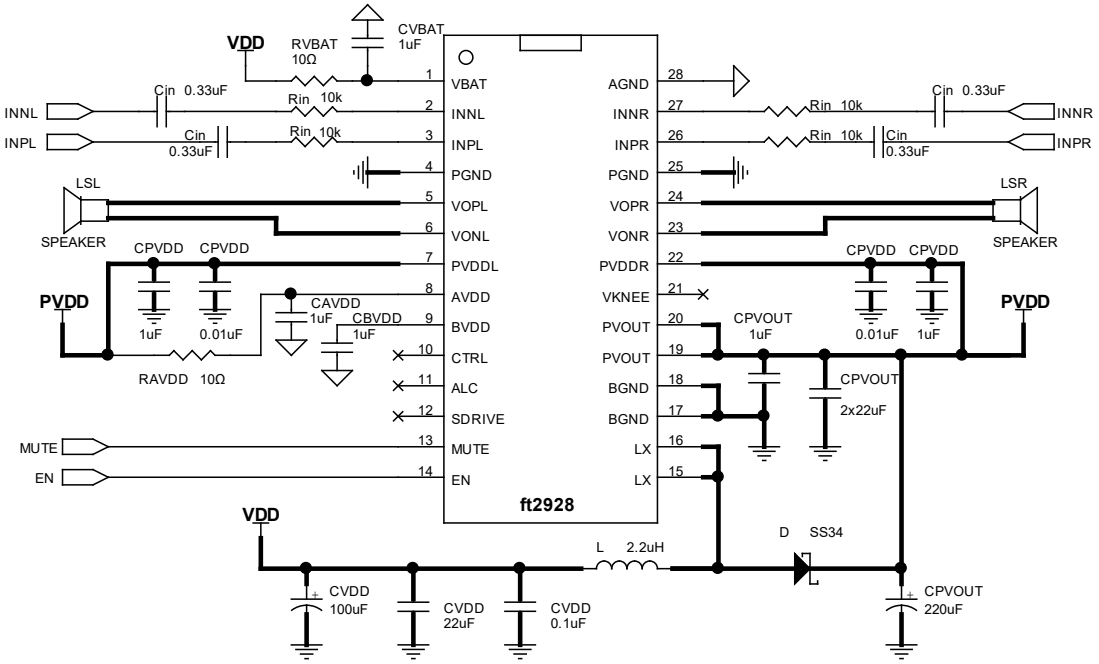


Figure 43: Differential Inputs with Adaptive Boost Regulator (CTRL=NC)

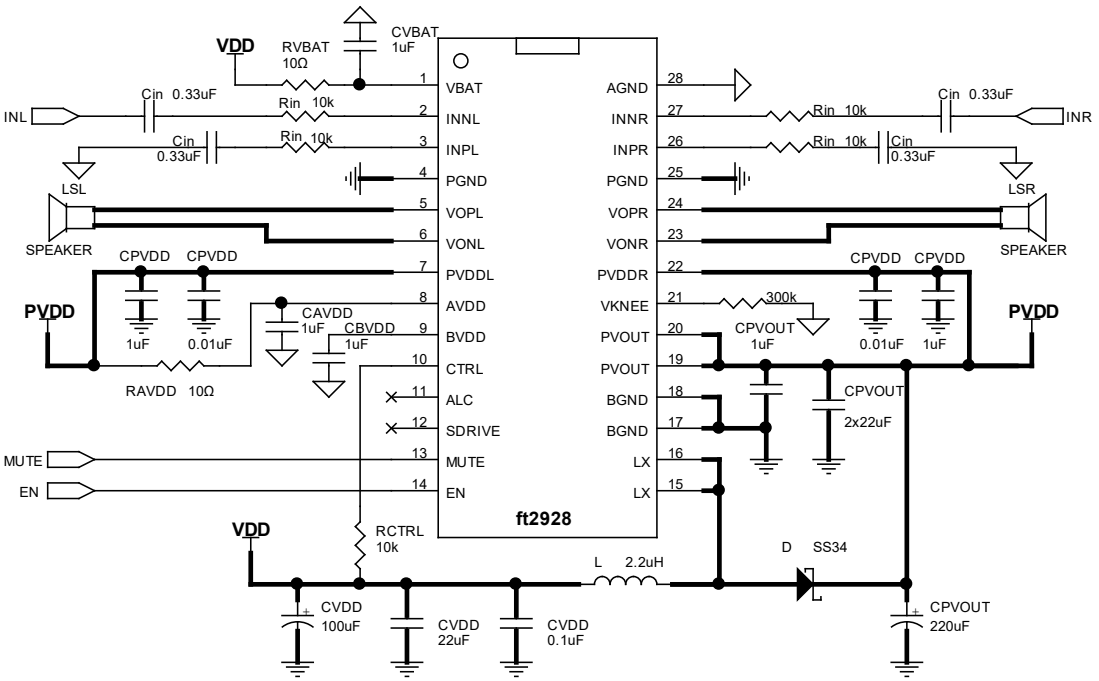
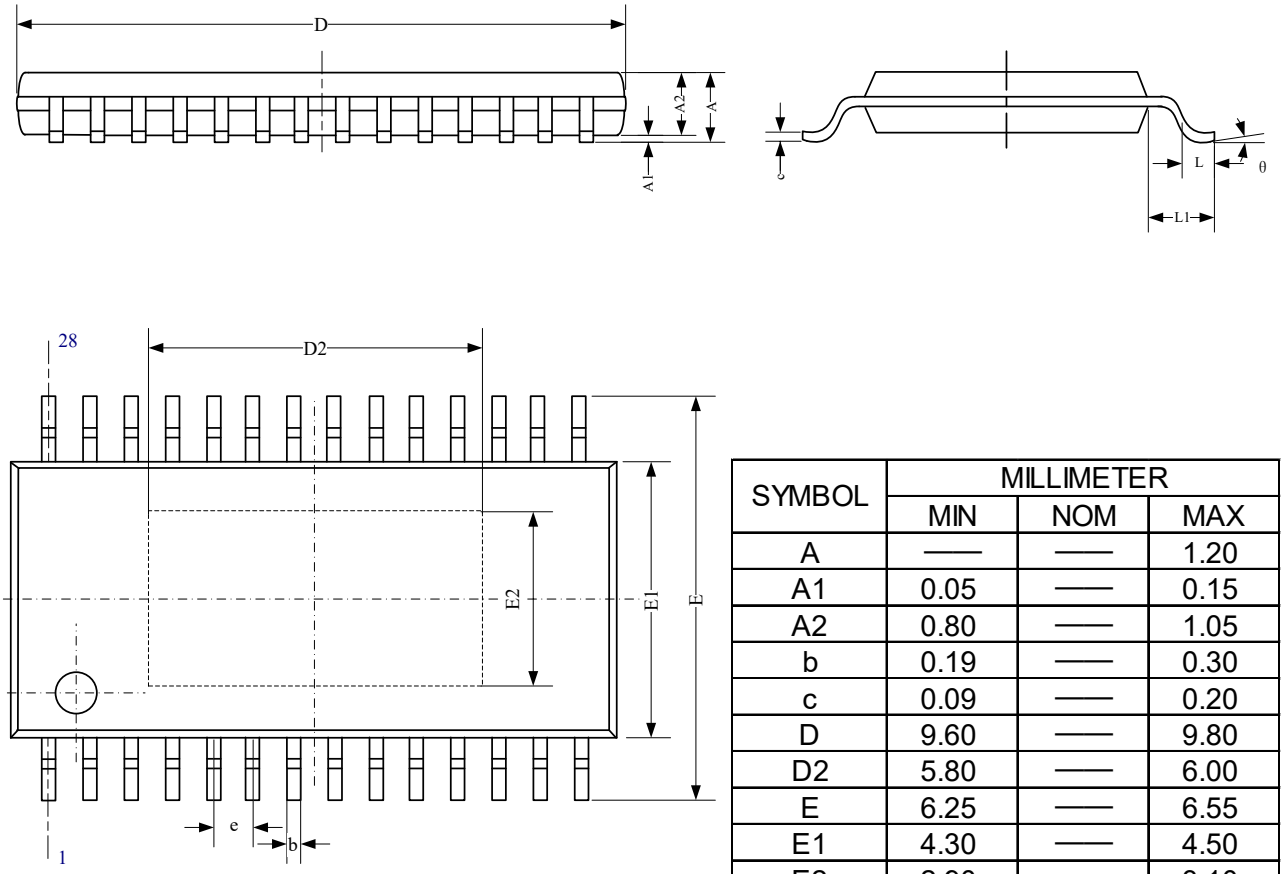


Figure 44: Single-Ended Inputs with Continual Boost Regulator (CTRL=High)

Note: The bold lines indicate high current paths and their respective traces are required to be as wide and short as possible on the system board for best performance in maximum output power, power efficiency, THD+N, and EMI emissions.

PHYSICAL DIMENSIONS

TSSOP-28L PACKAGE OUTLINE DIMENSIONS



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	——	——	1.20
A1	0.05	——	0.15
A2	0.80	——	1.05
b	0.19	——	0.30
c	0.09	——	0.20
D	9.60	——	9.80
D2	5.80	——	6.00
E	6.25	——	6.55
E1	4.30	——	4.50
E2	2.90	——	3.10
e	0.65		
L	0.45	——	0.75
L1	1.00		
θ	0°	——	8°

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