

J176, J177 P-Channel JFET

Features

- InterFET [P0099F Geometry](#)
- Low noise: 2.0 nV/VHz typical
- High gain: 10mS typical
- Low gate leakage: 2.5pA typical @10V
- Typical I_{SS}: 10mA
- Typical BV_{GSS}: 55V
- High radiation tolerance
- RoHS, REACH, CMR compliant
- Custom test and binning options available
- SMT, TH, and bare die package options
- SPICE Edge case modeling: [InterFET SPICE](#)

Industry Standard Crosses

- SST176, SST177, 2N5116, SST270, SST271

InterFET Similar Parts

- 2N5019, 2N5114, 2N5115, 2N5116
- P1086, P1087, J270, J271, VCR3P
- IFN3993, IFN3994, U304, U305, U306

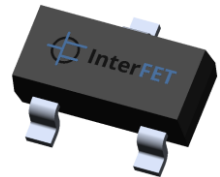
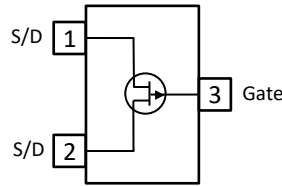
Applications

- General: Amplifiers; Switches; Voltage regulators; Oscillators; Signal mixers; Noise generators
- Military/Aero: Radar; Communications; Satellites; Missiles guidance; Hydrophone preamplifiers
- Medical: Medical imaging systems; Medical monitors and recorders; Ultrasound equipment
- Audio: Tone control circuits; Headphone amplifiers; Audio filters; Electret Microphone

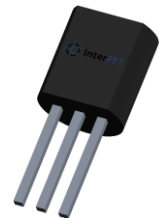
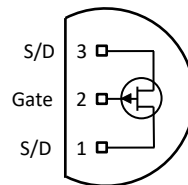
Description

The 30V InterFET J176 and J177 are very low leakage low noise P-channel JFETs targeted for high gain switching, commutator, and chopper applications. Gate leakages are typically less 3pA at room temperatures. The J177 has a cutoff voltage of less than 2.25V ideal for low-level power supplies. Proprietary InterFET processes yield exceptionally high radiation tolerance.

SOT23 Top View



TO-92 Bottom View



NOTE: S/D pins are interchangeable Source Drain connections

Ordering Information Custom Part and Binning Options Available

| Part Number | Description | Case | Packaging |
|----------------------|---|-------|---------------------------------------|
| J176; J177 | Through-Hole | TO-92 | Bulk |
| J176TB; J177TB | Ammo Pack | TO-92 | Minimum 1200 Typical 2000 |
| SMPJ176; SMPJ177 | SOT23 | SOT23 | Bulk |
| SMPJ176TR; SMPJ177TR | 7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces | SOT23 | Minimum 1,000 Pieces Tape and Reel |
| J176COT; J177COT | Chip Orientated Tray (COT Waffle Pack) | COT | 400/Waffle Pack |
| J176CFT; J177CFT | Chip Face-up Tray (CFT Waffle Pack) | CFT | 400/Waffle Pack |



NOTICE: Please refer to the end of this document for information on product materials, compliance, safety, and legal statements.

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

| Parameters | SOT-23 | TO-92 | Unit |
|---|------------|------------|-------|
| V _{RGS} Reverse Gate Source and Gate Drain Voltage | 30 | 30 | V |
| I _{FG} Continuous Forward Gate Current | 50 | 50 | mA |
| P _D Continuous Device Power Dissipation ¹ | 350 | 500 | mW |
| P Power Derating ¹ | 2.8 | 4 | mW/°C |
| T _J Operating Junction Temperature | -55 to 150 | -55 to 150 | °C |
| T _{STG} Storage Temperature | -55 to 150 | -55 to 150 | °C |

¹ Thermal power dissipation and derating values obtained with gate pin (substrate) thermally connected to pad and/or internal layer.

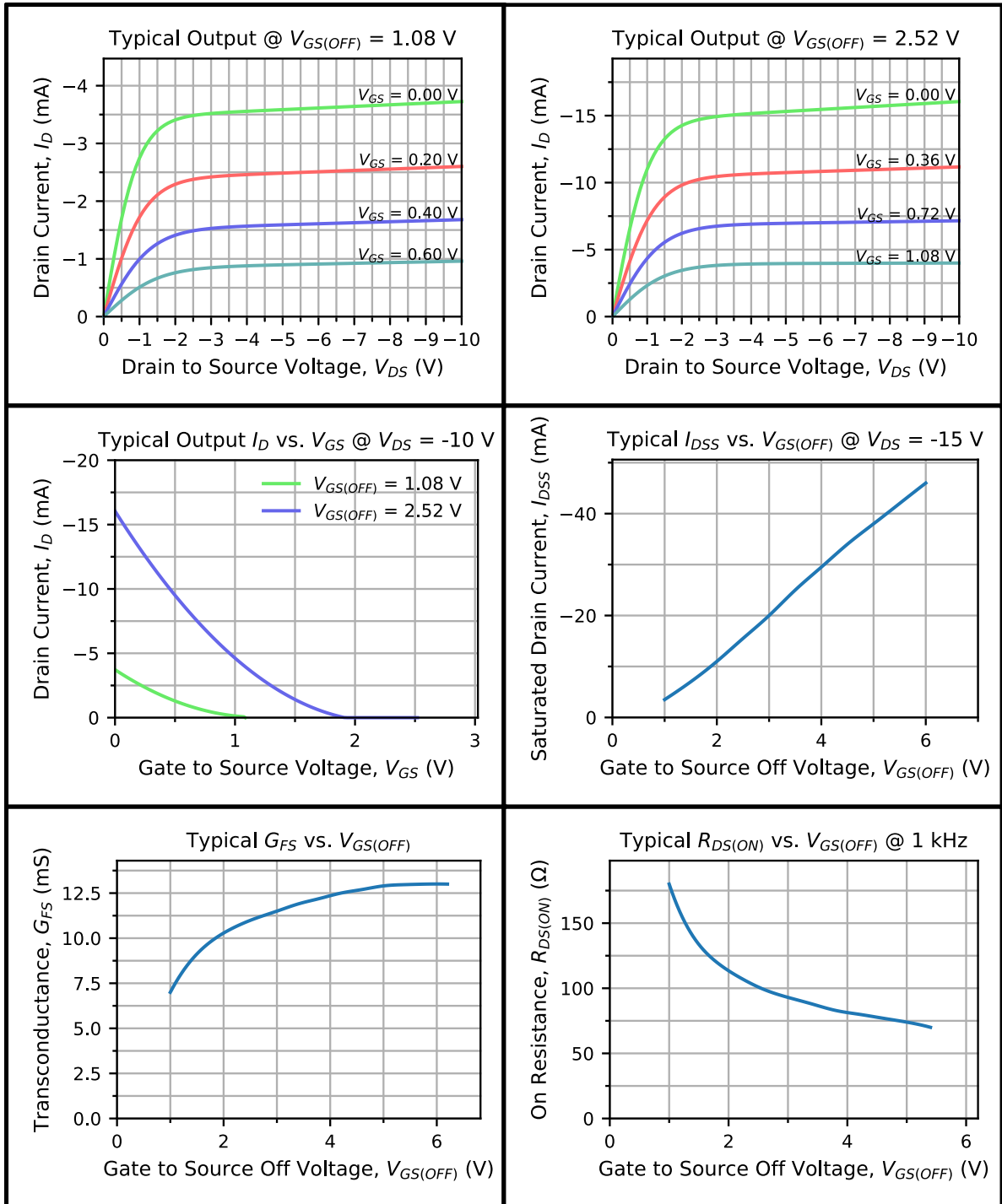
Static Characteristics (@ T_A = 25°C, Unless otherwise specified)

| Parameters | Conditions | J176 | | J177 | | Unit |
|---|---|------|-----|------|------|------|
| | | Min | Max | Min | Max | |
| V _{(BR)GSS} Gate to Source Breakdown Voltage | V _{DS} = 0V, I _G = 1μA | 30 | | 30 | | V |
| I _{GSS} Gate to Source Reverse Current | V _{GS} = 20V, V _{DS} = 0V | | 1 | | 1 | nA |
| V _{GS(OFF)} Gate to Source Cutoff Voltage | V _{DS} = -15V, I _D = -10nA | 1 | 4 | 0.8 | 2.25 | V |
| I _{DSS} Drain to Source Saturation Current | V _{GS} = 0V, V _{DS} = -15V (Pulsed) | -2 | -35 | -1.5 | -20 | mA |
| I _{D(OFF)} Drain Cutoff Current | V _{DS} = -15V, V _{GS} = 10V | | -1 | | -1 | nA |

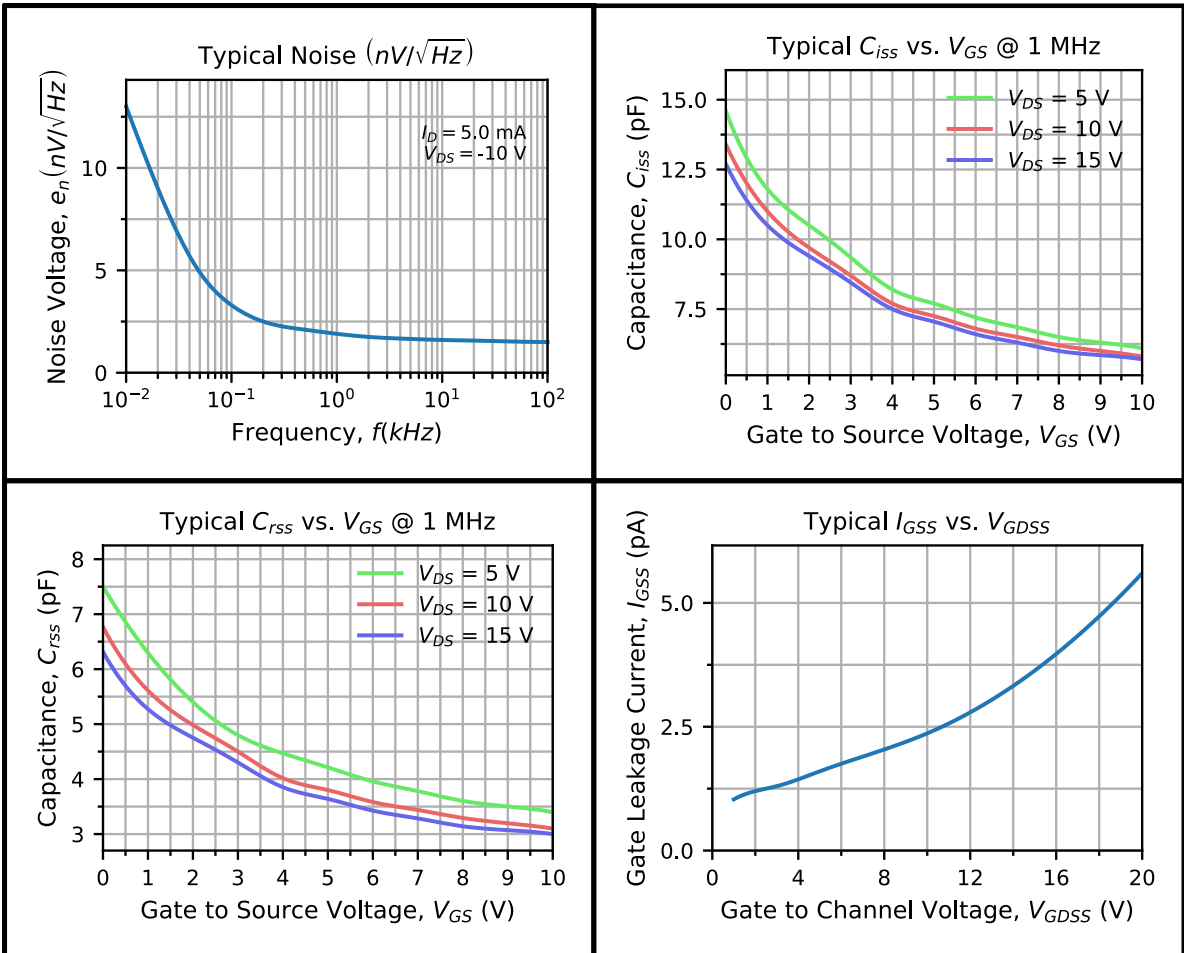
Dynamic Characteristics (@ T_A = 25°C, Unless otherwise specified)

| Parameters | Conditions | J176 | | J177 | | Unit |
|---|--|-----------|-----|-----------|-----|------|
| | | Min | Max | Min | Max | |
| R _{DS(ON)} Drain to Source ON Resistance | V _{DS} <= 0.1V, V _{GS} = 0V, f = 1kHz | | 250 | | 300 | Ω |
| C _{gd} Drain Gate Capacitance | V _{DS} = 0V, V _{GS} = 10V, f = 1MHz | 5.5 (typ) | | 5.5 (typ) | | pF |
| C _{gs} Input Capacitance | V _{DS} = 0V, V _{GS} = 10V, f = 1MHz | 5.5 (typ) | | 5.5 (typ) | | pF |
| C _{gd} + C _{gs} Drain + Source Gate Capacitance | V _{DS} = V _{GS} = 0V, f = 1MHz | 32 (typ) | | 32 (typ) | | pF |
| t _{d(ON)} Turn ON Delay Time | V _{DD} = -6V J176: V _{GS(OFF)} = 6V, R _L = 5600 Ω J177: V _{GS(OFF)} = 3V, R _L = 10000 Ω | 15 (typ) | | 20 (typ) | | ns |
| t _r Rise Time | | 20 (typ) | | 25 (typ) | | ns |
| t _{d(OFF)} Turn OFF Delay Time | | 15 (typ) | | 20 (typ) | | ns |
| t _f Fall Time | | 20 (typ) | | 25 (typ) | | ns |

Typical J176, J177 Characteristics

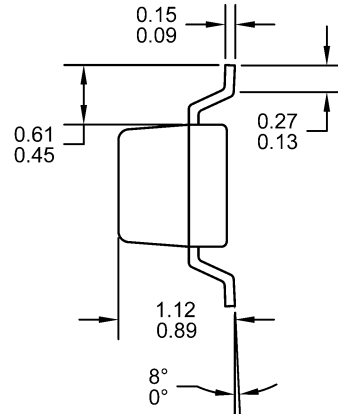
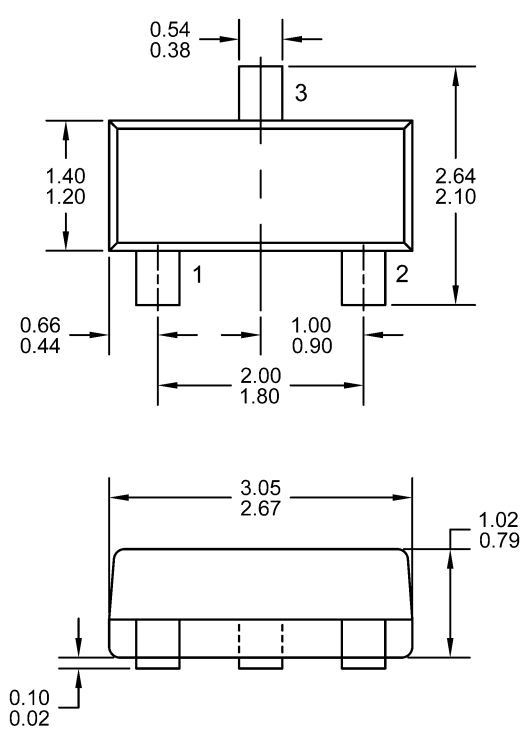


Typical J176, J177 Characteristics (Continued)



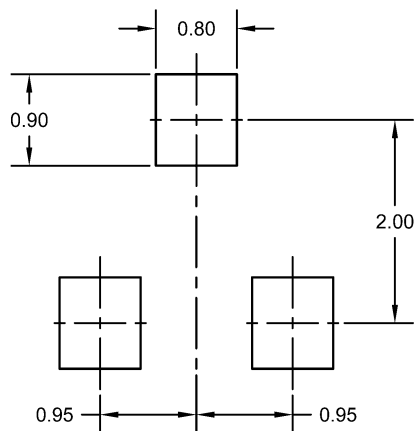
SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.12 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

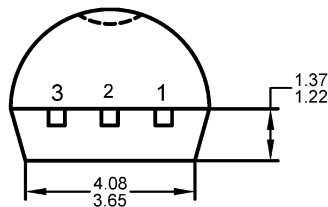
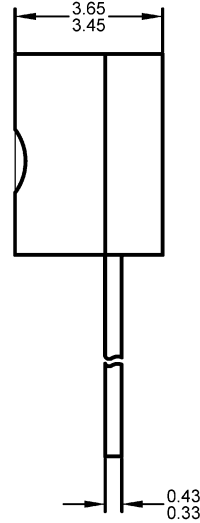
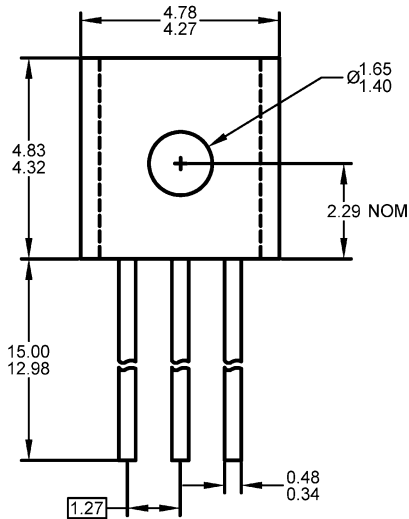
Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

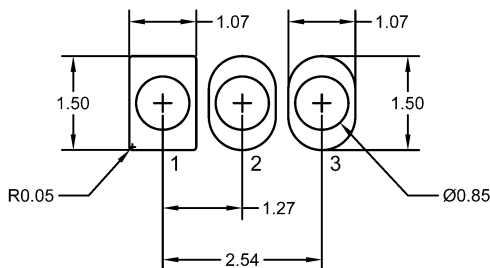
TO-92 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.19 grams
3. Molded plastic case UL 94V-0 rated
4. Bulk product is shipped in standard ESD shipping material
5. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.

Compliance and Legal

Environment

InterFET parts follow the latest RoHS Compliance, REACH Compliance, Proposition 65 Statement, TSCA Statement, and Chemical Disposal and Waste Mitigation requirement and guidelines. For more on InterFET’s Environmental Commitment please visit www.InterFET.com/environmental/.

Package materials

| Parameters | SOT23 | SOIC8 | TO-92 | Metal Case |
|------------|---------------|---------------|---------------|------------|
| Alloy | CDA194 | C194 1/2H | C194 1/2H | Kovar |
| Cu | Balance | 97% min | 97% min | |
| Fe | 2.1 – 2.6% | 2.1 – 2.6% | 2.1 – 2.6% | 53% |
| Zn | 0.05 – 0.2% | 0.05 – 0.2% | 0.05 – 0.15% | |
| P | 0.015 – 0.15% | 0.015 – 0.15% | 0.015 – 0.15% | |
| Pb | 0.03% max | 0.03% max | 0.03% max | |
| Ni | | | | 29% |
| Co | | | | 17% |
| Mn | | | | 0.3% |
| Si | | | | 0.2% |
| C | | | | <0.01% |
| Au | | | | Plating |

Package tests

| Parameters | SOT23 | SOIC8 | TO-92 | Metal Case |
|------------|--|--|--|--|
| MSL | Level 1 | TBD | N/A | N/A |
| ESD | Class M4 Machine Model Class 3B HBM | Class M4 Machine Model Class 3B HBM | Class M4 Machine Model Class 3B HBM | Class M4 Machine Model Class 3B HBM |

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