

# Smart Card Interface IC

## NCN8024R

The NCN8024R is a single smart card interface IC. It is dedicated for 3.0 V/5.0 V smart card reader/writer applications. The card  $V_{CC}$  supply is provided by a very low drop-out and low noise regulator (LDO).

The device is fully compatible with the ISO 7816-3 and EMV standards as well as with standards specifying conditional access in Set-Top-Box (STB) including NDS.

The smart card interface IC is available in SOIC-28 and TSSOP-28 packages providing the industry-standard features required by STB smart card interfaces.

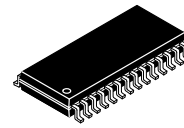
### Features

- Single IC Card Interface
- Fully Compatible with ISO 7816-3, EMV and Related Standards Including NDS and Other STB Standards (Nagravision, Irdeto, ...)
- Three Bidirectional Buffered I/O Level Shifters (C4, C7 and C8 Card Pins)
- 3.0 V or 5.0 V  $\pm 5\%$  Regulated Card Power Supply such as  $I_{CC} \leq 70$  mA with  $3.0$  V  $\leq V_{DDP} \leq 5.5$  V @ 3.0 V (Class B) and  $4.85$  V  $\leq V_{DDP} \leq 5.5$  V @ 5.0 V (Class A)
- Independent Power Supply Range on Controller Interface ( $2.7$  V  $< V_{DD} < 5.5$  V)
- Handles 5.0 V and 3.0 V Smart Cards (Class A & B)
- Thermal and Short Circuit Protection on all Card Pins
- Support up to 27 MHz Clock with Internal Division Ratio 1/1, 1/2, 1/4 and 1/8 through CLKDIV1 and CLKDIV2 Pins
- ESD Protection on Card Pins up to 8 kV+ (Human Body Model)
- Activation/Deactivation Sequences (ISO7816)
- Fault Protection Mechanisms Enabling Automatic Device Deactivation in Case of Overload, Overheating, Card Take-off or Power Supply Drop-out (OCP, OTP, UVP)
- Interrupt Signal  $\overline{INT}$  for Card Presence and Faults
- External Under-Voltage Lockout Threshold Adjustment on  $V_{DD}$  (PORADJ Pin)
- Available in Two Package Formats: SOIC-28 and TSSOP-28
- These are Pb-Free Devices

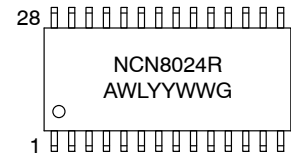
### Typical Application

- Pay TV, Set-Top-Box Decoder with Conditional Access and Pay-per-View
- Conditional Access Modules (CAM)
- POS / ATM
- Access Control, Identification

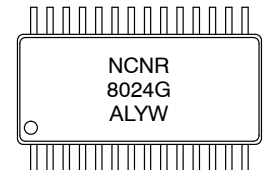
### MARKING DIAGRAMS



SOIC-28  
CASE 751F



TSSOP-28  
CASE 948AA



NCN8024R = Specific Device Code  
 A = Assembly Location  
 WL, L = Wafer Lot  
 YY, Y = Year  
 WW, W = Work Week  
 G = Pb-Free Package

### ORDERING INFORMATION

See detailed ordering and shipping information on page 13 of this data sheet.

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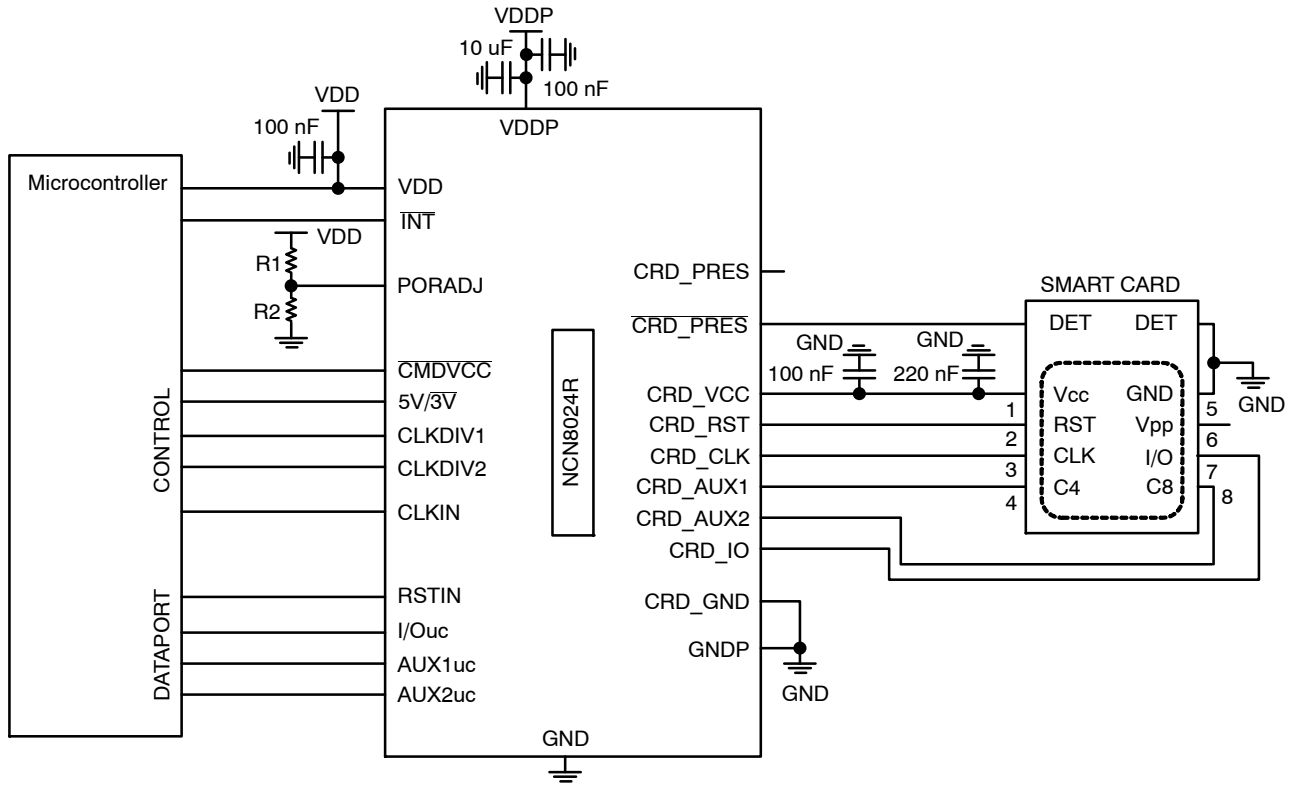


Figure 1. Typical Smart Card Interface Application

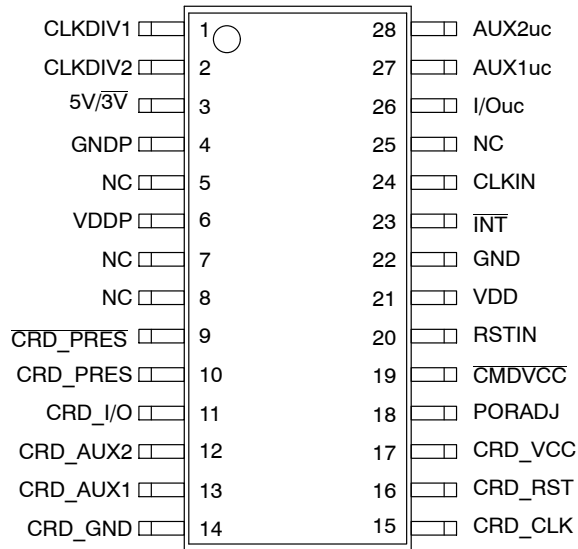
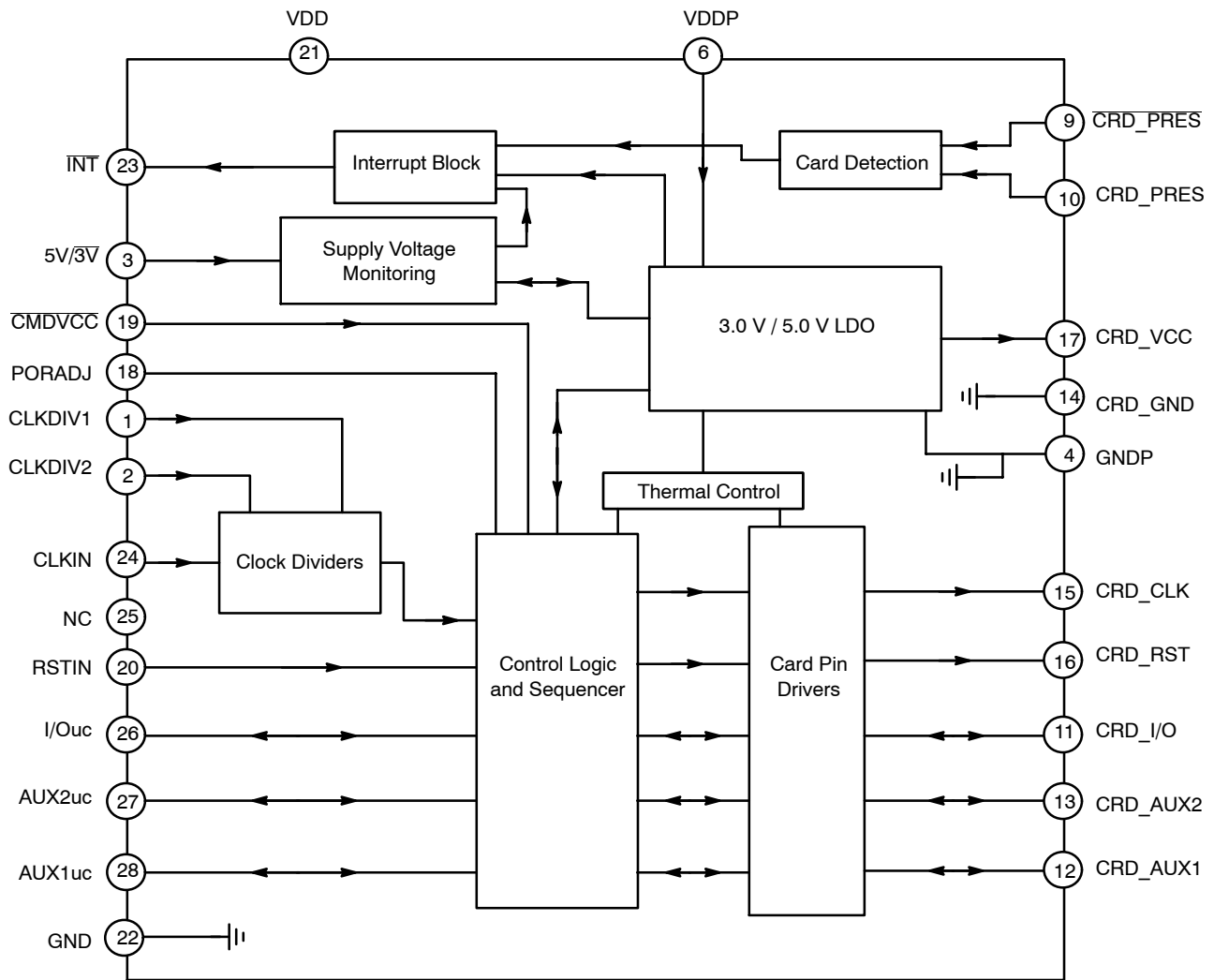


Figure 2. SOIC-28 and TSSOP-28 Pinout (Top View)

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**Figure 3. NCN8024R Block Diagram**

## PIN FUNCTION AND DESCRIPTION

Pin #	Name	Type	Description
1	CLKDIV1	Input	This pin coupled with CLKDIV2 is used to program the clock frequency division ratio (Table 1).
2	CLKDIV2	Input	This pin coupled with CLKDIV1 is used to program the clock frequency division ratio (Table 1).
3	5V/3V	Input	Allows selecting card V <sub>CC</sub> power supply voltage. CRD_V <sub>CC</sub> = 5 V when 5V/3V = HIGH or 3 V when 5V/3V = LOW
4	GNDP	GND	Regulator Power Supply Ground
5	NC	-	Not Connected
6	VDDP	Power	Regulator Power Supply
7	NC	-	Not Connected
8	NC	-	Not Connected
9	CRD_PRES	Input	Card presence pin active (card present) when $\overline{\text{CRD\_PRES}}$ = Low. A built-in debounce timer of about 8 ms is activated when a card is inserted. Convenient for Normally Open (NO) smart card connector.
10	CRD_PRES	Input	Card presence pin active (card present) when CRD_PRES = High. A built-in debounce timer of about 8 ms is activated when a card is inserted. Convenient for Normally Closed (NC) smart card connector.

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## PIN FUNCTION AND DESCRIPTION

Pin #	Name	Type	Description
11	CRD_I/O	Input/Output	This pin handles the connection to the serial I/O (C7) of the card connector. A bi-directional level translator adapts the serial I/O signal between the card and the micro controller. An 11 k $\Omega$ (typical) pullup resistor to CRD_VCC provides a High impedance state for the smart card I/O link.
12	CRD_AUX2	Input/Output	This pin handles the connection to the chip card's serial auxiliary AUX2 I/O pin (C8). A bi-directional level translator adapts the serial I/O signal between the card and the micro controller. An 11 k $\Omega$ (typical) pullup resistor to CRD_VCC provides a High impedance state for the smart card C8 pin.
13	CRD_AUX1	Input/Output	This pin handles the connection to the chip card's serial auxiliary AUX1 I/O pin (C4). A bi-directional level translator adapts the serial I/O signal between the card and the micro controller. An 11 k $\Omega$ (typical) pullup resistor to CRD_VCC provides a High impedance state for the smart card C4 pin.
14	CRD_GND	GND	Card Ground
15	CRD_CLK	Output	This pin is connected to the CLOCK card connector's pin (Chip card's pin C3). The Clock signal comes from the CLKIN input through clock dividers and level shifter.
16	CRD_RST	Output	This pin is connected to the chip card's RESET pin (C2) through the card connector. A level translator adapts the external Reset (RSTIN) signal to the smart card.
17	CRD_VCC	Power	This pin is connected to the smart card power supply pin. An internal DC/DC converter is programmable using the pin 5V/3V to supply either 5 V or 3 V output voltage. An external distributed ceramic capacitor ranging from 80 nF to 1.2 $\mu$ F recommended must be connected across CRD_VCC and CRD_GND. This set of capacitor must be low ESR (< 100 m $\Omega$ ).
18	PORADJ	Input	Power-on reset threshold adjustment input pin for changing the reset threshold with an external resistor power divider. Recommended to be connected to ground when unused.
19	$\overline{\text{CMDVCC}}$	Input	Command VCC pin. Activation sequence Enable/Disable pin (active Low). The activation sequence is enabled by toggling $\overline{\text{CMDVCC}}$ High to Low and when a card is present.
20	RSTIN	Input	This Reset input connected to the host and referred to V <sub>DD</sub> (microcontroller side), is connected to the smart card Reset pin through the internal level shifter which translates the level according to the CRD_VCC programmed value.
21	VDD	Power	This pin is connected to the system controller power supply. It configures the level shifter input stage to accept the signals coming from the controller. A 0.1 $\mu$ F capacitor shall be used to bypass the power supply voltage. When V <sub>DD</sub> is below 2.30 V typical the card pins are disabled.
22	GND	GND	Ground
23	$\overline{\text{INT}}$	Output	The interrupt request is activated LOW on this pin. This is enabled when a card is present and the card presence is detected by CRD_PRES or $\overline{\text{CRD\_PRES}}$ pins. Similarly an interrupt is generated when CRD_VCC is overloaded. 20 k $\Omega$ typical integrated pullup resistor to V <sub>DD</sub> .
24	CLKIN	Input	Clock Input for External Clock
25	NC		Not Connected
26	I/Ouc	Input/Output	This pin is connected to an external micro-controller. A bi-directional level translator adapts the serial I/O signal between the smart card and the external controller. A built-in constant 11 k $\Omega$ (typical) resistor provides a high impedance state.
27	AUX1uc	Input/Output	This pin is connected to an external micro-controller. A bi-directional level translator adapts the serial C4 signal between the smart card and the external controller. A built-in constant 11 k $\Omega$ (typical) resistor provides a high impedance state.
28	AUX2uc	Input/Output	This pin is connected to an external micro-controller. A bi-directional level translator adapts the serial C8 signal between the smart card and the external controller. A built-in constant 11 k $\Omega$ (typical) resistor provides a high impedance state.

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## ATTRIBUTES

Characteristics	Values
ESD protection Human Body Model (HBM) (Note 1) Card Pins (Card Interface Pins 9 – 17) All Other Pins Machine Model (MM) Card Pins (Card Interface Pins 9 – 17) All Other Pins	8 kV 2 kV 400 V 150 V
Moisture sensitivity (Note 2) SOIC–28 and TSSOP–28	Level 3
Flammability Rating Oxygen Index: 28 to 34	UL 94 V–0 @ 0.125 in
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latch–up Test	

- Human Body Model (HBM), R = 1500 Ω, C = 100 pF.
- For additional information, see Application Note AND8003/D.

## MAXIMUM RATINGS (Note 3)

Rating	Symbol	Value	Unit
DC/DC Converter Power Supply Voltage	V <sub>DDP</sub>	-0.3 ≤ V <sub>DDP</sub> ≤ 5.5	V
Power Supply from Microcontroller Side	V <sub>DD</sub>	-0.3 ≤ V <sub>DD</sub> ≤ 5.5	V
External Card Power Supply	CRD_V <sub>CC</sub>	-0.3 ≤ CRD_V <sub>CC</sub> ≤ 5.5	V
Charge Pump Output	V <sub>UP</sub>	-0.3 ≤ V <sub>UP</sub> ≤ 5.5	
Digital Input Pins	V <sub>in</sub>	-0.3 ≤ V <sub>in</sub> ≤ V <sub>DD</sub>	V
Digital Output Pins (I/Ouc, AUX1uc, AUX2uc, INT)	V <sub>out</sub>	-0.3 ≤ V <sub>out</sub> ≤ V <sub>DD</sub>	V
Smart Card Output Pins	V <sub>out</sub>	-0.3 ≤ V <sub>out</sub> ≤ CRD_V <sub>CC</sub>	V
Thermal Resistance Junction–to–Air SOIC–28 TSSOP–28	R <sub>θJA</sub>	75 76	°C/W
Operating Ambient Temperature Range	T <sub>A</sub>	-40 to +85	°C
Operating Junction Temperature Range	T <sub>J</sub>	-40 to +125	°C
Maximum Junction Temperature	T <sub>Jmax</sub>	+125	°C
Storage Temperature Range	T <sub>stg</sub>	-65 to + 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Maximum electrical ratings are defined as those values beyond which damage to the device may occur at T<sub>A</sub> = +25°C

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## POWER SUPPLY SECTION ( $V_{DD} = 3.3\text{ V}$ ; $V_{DDP} = 5\text{ V}$ ; $T_{amb} = 25^{\circ}\text{C}$ ; $F_{CLKIN} = 10\text{ MHz}$ )

Symbol	Rating	Min	Typ	Max	Unit
$V_{DDP}$	DC/DC Converter Power Supply, CRD_VCC = 5 V $ I_{CC}  \leq 70\text{ mA}$ (EMV Conditions) $ I_{CC}  \leq 70\text{ mA}$ (NDS Conditions) CRD_VCC = 3 V $ I_{CC}  \leq 70\text{ mA}$	4.75 4.85 3.0	5.0	5.5	V
$I_{DDP}$	Inactive Mode	–	–	1	$\mu\text{A}$
$I_{DDP}$	DC Operating Supply Current, $F_{CLKIN} = 10\text{ MHz}$ , $C_{out\_CRD\_CLK} = 33\text{ pF}$ , $ I_{CRD\_VCC}  = 0$ (CMDVCC = Low)	–	–	3.0	mA
$I_{DDP}$	DC Operating Supply Current, CRD_VCC = 5 V, $I_{CRD\_VCC} = 70\text{ mA}$ CRD_VCC = 3 V, $I_{CRD\_VCC} = 70\text{ mA}$	–	–	80 80	mA
$V_{DD}$	Operating Voltage	2.7	–	5.5	V
$I_{VDD}$	Inactive Mode 0 Standby Current	–	–	60	$\mu\text{A}$
$I_{VDD}$	Operating Current – $F_{CLK\_IN} = 10\text{ MHz}$ , $C_{out\_CRD\_CLK} = 33\text{ pF}$ , $ I_{CRD\_VCC}  = 0$ (CMDVCC = Low)	–	–	1	mA
UVLOV <sub>DD</sub>	Undervoltage Lockout (UVLO), No External Resistor at Pin PORADJ (Connected to GND), Falling $V_{DD}$ Level	2.20	2.30	2.40	V
UVLOHys	UVLO Hysteresis, No External Resistor at Pin PORADJ (Connected to GND) (Note 4)	50	100	180	mV

### PORADJ PIN

$V_{PORth+}$	External Rising Threshold Voltage on $V_{DD}$ for Power On Reset – Pin PORADJ	1.20	1.27	1.34	V
$V_{PORth-}$	External Falling Threshold voltage on $V_{DD}$ for Power On Reset – Pin PORADJ	1.15	1.20	1.28	V
$V_{PORHys}$	Hysteresis on $V_{PORth}$ (pin PORADJ) (Note 4)	30	80	100	mV
$t_{POR}$	Width of Power-On Reset Pulse (Note 4) No External Resistor on PORADJ External Resistor on PORADJ	4 4	8 8	12 12	ms
$I_{IL}$	Low Level Input Leakage Current, $V_{IL} < 0.5\text{ V}$ (Pulldown Current Source)		5		$\mu\text{A}$

### LOW DROP OUT REGULATOR

$C_{CRD\_VCC}$	Output Capacitance on card power supply CRD_VCC (Notes 4 and 5)	80	100 + 220	1200	nF
CRD_VCC	Output Card Supply Voltage (including ripple) 3.0 V CRD_VCC Mode @ $I_{CC} \leq 70\text{ mA}$ 5.0 V CRD_VCC Mode @ $I_{CC} \leq 70\text{ mA}$ with 4.85 V VDDP 5.5 V (NDS) 5.0 V CRD_VCC Mode @ $I_{CC} \leq 70\text{ mA}$ with 4.75 V VDDP 5.5 V (EMV)	2.85 4.75 4.60	3.00 5.00 5.00	3.15 5.25 5.25	V
CRD_VCC	Current Pulses 40 nAs ( $t < 400\text{ ns}$ & $ I_{CC}  \leq 200\text{ mA}$ peak) 3.0 V mode / Ripple $\leq 250\text{ mV}$ ( $2.9\text{ V} \leq V_{DDP} \leq 5.5\text{ V}$ ) Current Pulses 40 nAs ( $t < 400\text{ ns}$ & $ I_{CC}  \leq 200\text{ mA}$ peak) 5.0 V mode / Ripple $\leq 250\text{ mV}$ ( $4.85\text{ V} \leq V_{DDP} \leq 5.5\text{ V}$ )	2.70 4.60	3.00 5.00	3.20 5.25	V
$I_{CRD\_VCC}$	Card Supply Current @ CRD_VCC = 3.0 V @ CRD_VCC = 5.0 V			70 70	mA
$I_{CRD\_VCC\_SC}$	Short-Circuit Current – CRD_VCC Shorted to Ground		120	150	mA
$\Delta V_{CRD\_VCC}$	Output Card Supply Voltage Ripple Peak-to-Peak – $f_{ripple} = 100\text{ Hz}$ to 200 MHz (Load Transient with 65 mA Peak Current) (Note 4)			300	mV
CRD_VCCSR	Slew Rate on CRD_VCC Up or Down (Note 4)			0.22	V/ $\mu\text{s}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Guaranteed by design and characterization
- These values take into account the tolerance of the cms capacitor used. The allowed values are single or distributed capacitor combination not exceeding 1.2  $\mu\text{F}$  with 100 nF + 220 nF typical and recommended. It is recommended to use X5R or X7R-type capacitors with very low ESR ( $< 100\text{ m}\Omega$ ) for optimal performances.

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## HOST INTERFACE SECTION CLKIN, RSTIN, I/Ouc, AUX1uc, AUX2uc, CLKDIV1, CLKDIV2, $\overline{\text{CMDVCC}}$ , 5V/3V

( $V_{DD} = 3.3\text{ V}$ ;  $V_{DDP} = 5\text{ V}$ ;  $T_{amb} = 25^\circ\text{C}$ ;  $F_{CLKIN} = 10\text{ MHz}$ )

Symbol	Rating	Min	Typ	Max	Unit
$F_{CLKIN}$	Clock Frequency on Pin CLKIN (with Divider Ratio $\geq 2$ ) (Note 6)	-	-	27	MHz
$V_{IL}$	Input Voltage Level Low: CLKIN, RSTIN, I/Ouc, AUX1uc, AUX2uc, CLKDIV1, CLKDIV2, $\overline{\text{CMDVCC}}$ , 5V/3V	-0.3	-	$0.3 \times V_{DD}$	V
$V_{IH}$	Input Voltage Level High: CLKIN, RSTIN, I/O, AUX1, AUX2, CLKDIV1, CLKDIV2, $\overline{\text{CMDVCC}}$ , 5V/3V	$0.7 \times V_{DD}$	-	$V_{DD} + 0.3$	V
$ I_{IL} $	CLKDIV1, CLKDIV2, $\overline{\text{CMDVCC}}$ , RSTIN, CLKIN, 5V/3V Low Level Input Leakage Current, $V_{IL} = 0\text{ V}$	-	-	1.0	$\mu\text{A}$
$ I_{IH} $	CLKDIV1, CLKDIV2, $\overline{\text{CMDVCC}}$ , RSTIN, CLKIN, 5V/3V Low Level Input Leakage Current, $V_{IH} = V_{DD}$	-	-	1.0	$\mu\text{A}$
$V_{IL}$	Input Voltage Level Low: I/Ouc, AUX1uc, AUX2uc	-0.3	-	0.5	V
$V_{IH}$	Input Voltage Level High: I/Ouc, AUX1uc, AUX2uc	$0.7 \times V_{DD}$	-	$V_{DD} + 0.3$	V
$ I_{IL} $	I/Ouc, AUX1uc, AUX2uc Low Level Input Leakage Current, $V_{IL} = 0\text{ V}$	-	-	600	$\mu\text{A}$
$ I_{IH} $	I/Ouc, AUX1uc, AUX2uc High Level Input Leakage Current, $V_{IH} = V_{DD}$	-	-	10	$\mu\text{A}$
$V_{OH}$	I/Ouc, AUX1uc, AUX2uc data channels, @ $C_s \leq 30\text{ pF}$ High Level Output Voltage ( $\text{CRD\_I/O} = \text{CRD\_AUX1} = \text{CRD\_AUX2} = \text{CRD\_VCC}$ ) $I_{OH} = 0$ $I_{OH} = -40\ \mu\text{A}$ for $V_{DD} > 2\text{ V}$ ( $I_{OH} = -20\text{ mA}$ for $V_{DD} \leq 2\text{ V}$ )	$0.9 \times V_{DD}$ $0.75 \times V_{DD}$	- -	$V_{DD} + 0.1$ $V_{DD} + 0.1$	V V
$V_{OL}$	Low Level Output Voltage ( $\text{CRD\_I/O} = \text{CRD\_AUX1} = \text{CRD\_AUX2} = 0\text{ V}$ ) $I_{OL} = +1\text{ mA}$	0	-	0.3	V
$t_{Ri/Fi}$	Input Rising/Falling Times (Note 6)	-	-	1.2	$\mu\text{s}$
$t_{Ro/Fo}$	Output Rising/Falling Times (Note 6)	-	-	0.1	$\mu\text{s}$
$F_{bidi}$	Maximum Frequency through Bidirectional I/O, AUX1 and AUX2 Channels (Note 6)	-	-	1	MHz
$R_{pu}$	I/Ouc, AUX1uc, AUX2uc Pullup Resistor	8.0	11	16	$\text{k}\Omega$
$V_{OH}$	Output High Voltage INT @ $I_{OH} = -15\ \mu\text{A}$ (Source)	$0.6 \times V_{DD}$	-	-	V
$V_{OL}$	Output Low Voltage INT @ $I_{OL} = 2\text{ mA}$ (Sink)	0	-	0.30	V
$R_{INT}$	INT Pullup Resistor	40	50	60	$\text{k}\Omega$

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6. Guaranteed by design and characterization

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## SMART CARD INTERFACE SECTION, CRD\_IO, CRD\_AUX1, CRD\_AUX2, CRD\_CLK, CRD\_RST, CRD\_PRES, CRD\_PRES (V<sub>DD</sub> = 3.3 V; V<sub>DDP</sub> = 5 V; T<sub>amb</sub> = 25°C; F<sub>CLKIN</sub> = 10 MHz)

Symbol	Rating	Min	Typ	Max	Unit
V <sub>OH</sub> V <sub>OL</sub>	CRD_RST @ CRD_V <sub>CC</sub> = 3.0 V, 5.0 V Output RESET V <sub>OH</sub> @ I <sub>rst</sub> = -200 μA Output RESET V <sub>OL</sub> @ I <sub>rst</sub> = 200 μA	0.9 x CRD_V <sub>CC</sub> 0	- -	CRD_V <sub>CC</sub> 0.20	V V
V <sub>OH</sub> V <sub>OL</sub>	Output RESET V <sub>OH</sub> @ I <sub>rst</sub> = -20 mA Output RESET V <sub>OL</sub> @ I <sub>rst</sub> = 20 mA	0 CRD_V <sub>CC</sub> - 0.4	- -	0.4 CRD_V <sub>CC</sub>	V V
t <sub>R</sub> t <sub>F</sub>	Output RESET Risetime @ C <sub>out</sub> = 100 pF (Note 7) Output RESET Falltime @ C <sub>out</sub> = 100 pF (Note 7)	- -	- -	100 100	ns ns
t <sub>d</sub>	RSTIN to CRD_RST Delay - Reset Enabled (Note 7)	-	-	2	μs
F <sub>CRDCLK</sub>	CRD_CLK @ CRD_V <sub>CC</sub> = 3.0 V or 5.0 V Output Frequency (Note 7)	-	-	18	MHz
V <sub>OH</sub> V <sub>OL</sub>	Output CRD_CLK V <sub>OH</sub> @ I <sub>clk</sub> = -200 μA Output CRD_CLK V <sub>OL</sub> @ I <sub>clk</sub> = 200 μA	0.9 x CRD_V <sub>CC</sub> 0	- -	CRD_V <sub>CC</sub> +0.2	V V
V <sub>OH</sub> V <sub>OL</sub>	Output CRD_CLK V <sub>OH</sub> @ I <sub>clk</sub> = -70 mA Output CRD_CLK V <sub>OL</sub> @ I <sub>clk</sub> = 70 mA	0 CRD_V <sub>CC</sub> - 0.4	- -	0.4 CRD_V <sub>CC</sub>	V V
F <sub>DC</sub>	Output Duty Cycle (Note 7)	45	-	55	%
t <sub>ri</sub> t <sub>ulsa</sub>	Rise & Fall time (Note 5) Output CRD_CLK Risetime @ C <sub>out</sub> = 30 pF Output CRD_CLK Falltime @ C <sub>out</sub> = 30 pF	- -	- -	16 16	ns ns
SR	Slew Rate @ C <sub>out</sub> = 33 pF (Note 7)	0.2	-	-	V/ns
V <sub>IH</sub> V <sub>IH</sub> V <sub>IL</sub>	CRD_AUX1, CRD_AUX2, CRD_IO @ CRD_V <sub>CC</sub> = 3.0 V, 5.0 V Input Voltage High Level (5 V Mode) Input Voltage High Level (3 V Mode) Input Voltage Low Level	2.3 1.6 0.30	- - -	CRD_V <sub>CC</sub> +0.3 CRD_V <sub>CC</sub> +0.3 0.80	V V V
I <sub>IL</sub> I <sub>IH</sub>	Low Level Input Current V <sub>IL</sub> = 0 V High Level Input Current V <sub>IH</sub> = CRD_V <sub>CC</sub>	- -	- -	600 10	μA μA
V <sub>OH</sub>	Output V <sub>OH</sub> @ I <sub>OH</sub> = -40 μA	0.75 x CRD_V <sub>CC</sub>	-	CRD_V <sub>CC</sub> +0.1	V
V <sub>OL</sub>	Output V <sub>OL</sub> @ I <sub>OL</sub> = 1 mA, V <sub>IL</sub> = 0 V	0	-	0.30	V
t <sub>Ri</sub> /F <sub>i</sub>	Input Rising/Falling Times	-	-	1.2	μs
t <sub>Ro</sub> /F <sub>o</sub>	Output Rising/Falling Times / C <sub>out</sub> = 80 pF	-	-	0.1	μs
R <sub>PU</sub>	CRD_AUX1, CRD_AUX2, CRD_IO Pullup Resistor	8.0	11	16	kΩ
t <sub>IO</sub>	Propagation delay I <sub>Ouc</sub> -> CRD_IO and CRD_IO -> IOuc (Falling Edge) (Note 7)	-	-	200	ns
t <sub>pu</sub>	Active pull-up pulse width buffers I/O, AUX1 & AUX2 (Note 7)	-	200	-	ns
V <sub>IH</sub> V <sub>IL</sub>	CRD_PRES, $\bar{C}$ RD_PRES Card Presence Voltage High Level Card Presence Voltage Low Level	0.7 x V <sub>DD</sub> -0.3		V <sub>DD</sub> + 0.3 0.3 x V <sub>DD</sub>	V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

7. Guaranteed by design and characterization



**SMART CARD INTERFACE SECTION, CRD\_IO, CRD\_AUX1, CRD\_AUX2, CRD\_CLK, CRD\_RST, CRD\_PRES, CRD\_PRES** ( $V_{DD} = 3.3\text{ V}$ ;  $V_{DDP} = 5\text{ V}$ ;  $T_{amb} = 25^{\circ}\text{C}$ ;  $F_{CLKIN} = 10\text{ MHz}$ )

Symbol	Rating	Min	Typ	Max	Unit
$ I_{IH} $	CRD_PRES, $\overline{\text{CRD\_PRES}}$ High level input leakage current, $V_{IH} = V_{DD}$		3	10	$\mu\text{A}$
$ I_{IL} $	CRD_PRES $\overline{\text{CRD\_PRES}}$ Low level input leakage current, $V_{IL} = 0\text{ V}$		3	1	$\mu\text{A}$
$T_{\text{debounce}}$	Debounce Time CRD_PRES and $\overline{\text{CRD\_PRES}}$ (Note 7)	5	8	12	ms
$I_{\text{CRD\_IO}}$	CRD_IO, CRD_AUX1, CRD_AUX2 Current Limitation	–	–	15	mA
$I_{\text{CRD\_CLK}}$	CRD_CLK Current Limitation	–	–	70	mA
$I_{\text{CRD\_RST}}$	CRD_RST Current Limitation	–	–	20	mA
$t_{\text{act}}$	Activation Time (Note 7)	30	–	100	$\mu\text{s}$
$t_{\text{deact}}$	Deactivation Time (Note 7)	30	–	250	$\mu\text{s}$
$\text{Temp}_{\text{SD}}$	Shutdown Temperature	–	160	–	$^{\circ}\text{C}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

7. Guaranteed by design and characterization

**POWER SUPPLY**

The NCN8024R smart card interface has two power supplies:  $V_{DD}$  and  $V_{DDP}$ .

$V_{DD}$  is usually common to the system controller and the interface. The applied  $V_{DD}$  ranges from 2.7 V up to 5.5 V. If  $V_{DD}$  goes below 2.30 V typical ( $UVLO_{VDD}$ ) a power-down sequence is automatically performed. In that case the interrupt ( $\overline{\text{INT}}$ ) pin is set Low.

A Low Drop-Out (LDO) and low noise regulator is used to provide the 3 V or 5 V power supply voltage ( $CRD\_V_{CC}$ ) to the card.  $V_{DDP}$  is the LDO's input voltage.  $CRD\_V_{CC}$  is the LDO output. The typical distributed reservoir output capacitor connected to  $CRD\_V_{CC}$  is 100 nF + 220 nF. To minimize dI/dt effects the capacitor of 100 nF is connected as close as possible to the  $CRD\_V_{CC}$ 's pin and the 220 nF one as close as possible to the card connector C1 pin. Both feature very low ESR values (lower than 50 m $\Omega$ ). The decoupling capacitors on  $V_{DD}$  and  $V_{DDP}$  respectively 100 nF and 10  $\mu\text{F}$  have also to be connected close to the respective IC pins.

The  $CRD\_V_{CC}$  pin can source up to 70 mA continuously over the  $V_{DDP}$  range, the absolute maximum current being internally limited below 150 mA (Typical at 120 mA).

There's no specific sequence for applying  $V_{DD}$  or  $V_{DDP}$ . They can be applied to the interface in any sequence. After powering the device  $\overline{\text{INT}}$  pin remains Low until a card is inserted.

**SUPPLY VOLTAGE MONITORING**

The supply voltage monitoring block includes the Power On Reset (POR) circuitry and the under voltage lockout (UVLO) detection ( $V_{DD}$  voltage dropout detection). PORADJ pin allows the user, according to the considered

application, to adjust the  $V_{DD}$  UVLO threshold. If not used PORADJ pin is connected to Ground (recommended even if it may be left unconnected).

The input supply voltage is continuously monitored to prevent under voltage operation. At power up, the system initializes the internal logic during POR timing and no further signal can be provided or supported during this period.

The system is ready to operate when the input voltage has reached the minimum  $V_{DD}$ . Considering this, the NCN8024R will detect an Under-Voltage situation when the input supply voltage will drop below 2.30 V typical. When  $V_{DD}$  goes down below the UVLO falling threshold a deactivation sequence is performed.

The device is inactive during power-on and power-off of the  $V_{DD}$  supply (8 ms reset pulse).

PORADJ pin is used to modify the UVLO threshold according to the below relationship considering an external resistor divider R1 / R2 (see block diagram Figure 1):

$$UVLO = \frac{R1 + R2}{R2} V_{\text{POR}}$$

If PORADJ is connected to Ground the  $V_{DD}$  UVLO threshold ( $V_{DD}$  falling) is typically 2.30 V. In some cases it can be interesting to adjust this threshold at a higher value and by the way increase the  $V_{DD}$  supply dropout detection level which enables a deactivation sequence if the  $V_{DD}$  voltage is too low.

For example, there are microcontrollers for which the minimum supply voltage insuring a correct operating is higher than 2.70 V, increasing  $UVLO_{VDD}$  ( $V_{DD}$  falling) is consequently necessary. Considering for instance a resistor

bridge with R1 = 56 kΩ, R2 = 42 kΩ and V<sub>POR-</sub> = 1.20 V typical the V<sub>DD</sub> dropout detection level can be increased up to:

$$UVLO = \frac{59k + 42k}{42k} V_{POR-} = 2.75 V$$

The minimum dropout detection voltage should be higher than 2 V.

The maximum detection level may be up to V<sub>DD</sub>.

**CLOCK DIVIDER:**

The input clock can be divided by 1/1, 1/2, 1/4, or 1/8, depending upon the specific application, prior to be applied to the smart card driver. These division ratios are programmed using pins CLKDIV1 and CLKDIV2 (see Table 1). The input clock is provided externally to pin CLKIN.

**Table 1. Clock Frequency Programming**

CLKDIV1	CLKDIV2	F <sub>CRD_CLK</sub>
0	0	CLKIN/8
0	1	CKLKIN / 4
1	0	CLKIN
1	1	CLKIN / 2

The clock input stage (CLKIN) can handle a 27 MHz maximum frequency signal. Of course, the ratio must be defined by the user to cope with Smart Card considered in a given application

In order to avoid any duty cycle out of the 45% / 55% range specification, the divider is synchronized by the last flip flop, thus yielding a constant 50% duty cycle, whatever be the divider ratio 1/2, 1/4 or 1/8. On the other hand, the output signal Duty Cycle cannot be guaranteed 50% if the division ratio is 1 and if the input Duty Cycle signal is not within the 46 – 56% range at the CLKIN input.

When the signal applied to CLKIN is coming from the external controller, the clock will be applied to the card under the control of the microcontroller or similar device after the activation sequence has been completed.

**DATA I/O, AUX1 and AUX2 LEVEL SHIFTERS**

The three bidirectional level shifters I/O, AUX1 and AUX2 adapt the voltage difference that might exist between the micro-controller and the smart card. These three channels are identical. The first side of the bidirectional level shifter dropping Low (falling edge) becomes the driver side until the level shifter enters again in the idle state pulling High CRD\_IO and I/Ouc.

Passive 11 kΩ pull-up resistors have been internally integrated on each terminal of the bidirectional channel. In addition with these pull-up resistors, an active pull-up circuit provides a fast charge of the stray capacitance.

The current to and from the card I/O lines is limited internally to 15 mA and the maximum frequency on these lines is 1 MHz.

**STANDBY MODE**

After a Power-on reset, the circuit enters the standby mode. A minimum number of circuits are active while waiting for the microcontroller to start a session:

- All card contacts are inactive
- Pins I/Ouc, AUX1uc and AUX2uc are in the high-impedance state (11 kΩ pull-up resistor to V<sub>DD</sub>)
- Card pins are inactive and pulled Low
- Supply Voltage monitoring is active

**POWER-UP**

In the standby mode the microcontroller can check the presence of a card using the signals  $\overline{INT}$  and  $\overline{CMDVCC}$  as shown in Table 2:

**Table 2. Card Presence State**

INT	CMDVCC	State
HIGH	HIGH	Card present
LOW	HIGH	Card not present

If a card is detected present ( $\overline{CRD\_PRES}$  or CRD\_PRES active) the controller can start a card session by pulling  $\overline{CMDVCC}$  Low. Card activation is run (t0, Figure 5). This Power-Up Sequence makes sure all the card related signals are LOW during the CRD\_V<sub>CC</sub> positive going slope. These lines are validated when CRD\_V<sub>CC</sub> is stable and above the minimum voltage specified. When the CRD\_V<sub>CC</sub> voltage reaches the programmed value (3.0 V or 5.0 V), the circuit activates the card signals according to the following sequence (Figure 5):

- CRD\_V<sub>CC</sub> is powered-up at its nominal value (t1)
- I/O, AUX1 and AUX2 lines are activated (t2)
- Then Clock channel is activated and the clock signal is applied to the card (typically 500 ns after I/Os lines) (t3)
- Finally the Reset level shifter is enabled (typically 500 ns after clock channel) (t4)

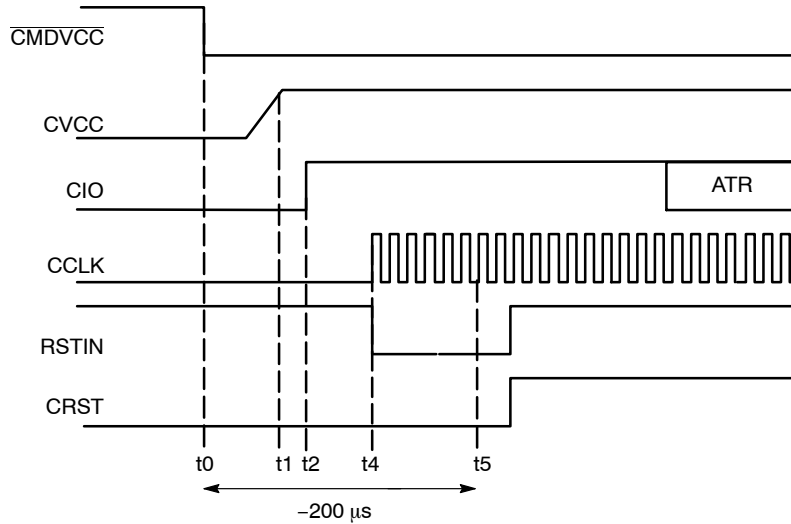
The clock can also be applied to the card using a RSTIN mode allowing controlling the clock starting by setting RSTIN Low (Figure 4). Before running the activation sequence, that is before setting Low  $\overline{CMDVCC}$  RSTIN is set High. The following sequence is applied:

- The Smart Card Interface is enable by setting  $\overline{CMDVCC}$  LOW (RSTIN is High).
- Between t2 (Figure 4) and t5 = 200 μs, RSTIN is reset to LOW and CCLK will start precisely at this moment allowing a precise count of clock cycles before toggling CRST Low to High for ATR (Answer To Reset) request.
- CRST remains LOW until 200 μs; after t5 = 200 μs CRST is enabled and is the copy of RSTIN which has no more control on the clock.

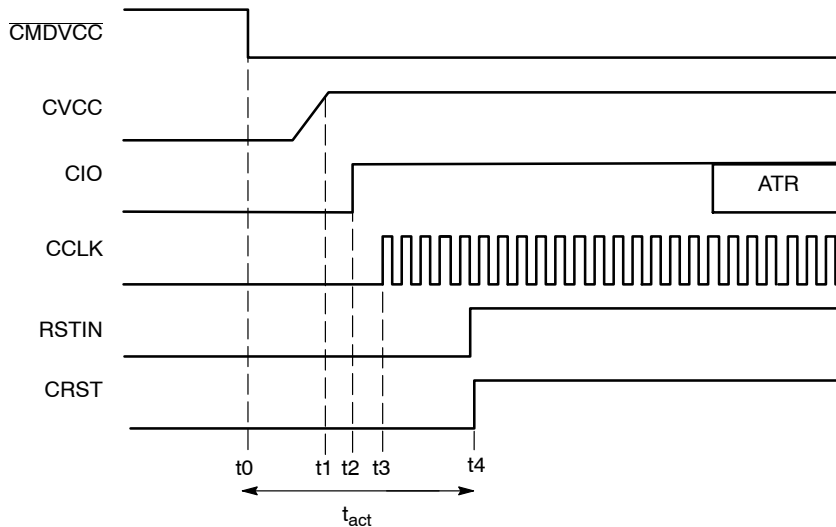
## NCN8024R

If controlling the clock with RSTIN is not necessary (**Normal Mode**), then /CMDVCC can be set LOW with RSTIN LOW. In that case, CLK will start minimum 500 ns after the transition on I/O (Figure 5), and to obtain an ATR, CRST can be set High by RSTIN also about 500 ns after the clock channel activation (tact).

The internal activation sequence activates the different channels according to a specific hardware built-in sequencing internally defined but at the end the actual activation sequencing is the responsibility of the application software and can be redefined by the micro-controller to comply with the different standards and the different ways the standards manage this activation (for example light differences exist between the EMV and the ISO7816 standards).



**Figure 4. Activation Sequence – RSTIN mode (RSTIN Starting High)**



**Figure 5. Activation Sequence – Normal Mode**

### POWER-DOWN

When the communication session is completed the NCN8024R runs a deactivation sequence by setting High CMDVCC. The below power down sequence is executed:

- CRD\_RST is forced to Low
- CRD\_CLK is set Low 12  $\mu$ s after CRD\_RST.
- CRD\_IO, CRD\_AUX1 and CRD\_AUX2 are pulled Low
- Finally CRD\_VCC supply can be shut-off.

## NCN8024R

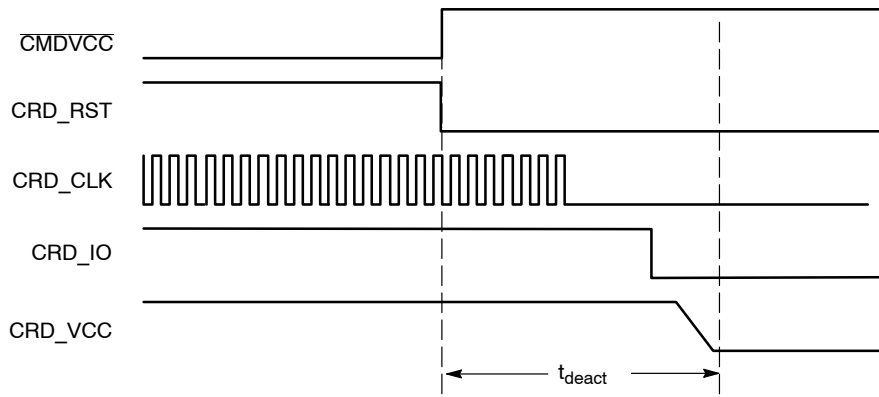


Figure 6. Deactivation Sequence

### FAULT DETECTION

In order to protect both the interface and the external smart card, the NCN8024R provides security features to prevent failures or damages as depicted here after.

- Card extraction detection
- $V_{DD}$  under voltage detection
- Short-circuit or overload on  $CRD\_VCC$
- Card pin current limitation: in the case of a short circuit to ground. No feedback is provided to the external MPU.
- LDO operation: the internal circuit continuously senses the  $CRD\_VCC$  voltage (in the case of either over or under voltage situation).
- LDO operation: under-voltage detection on  $V_{DDP}$  or overload on  $VUP$
- Overheating
- Card pin current limitation: in the case of a short circuit to ground. No feedback is provided to the external MPU

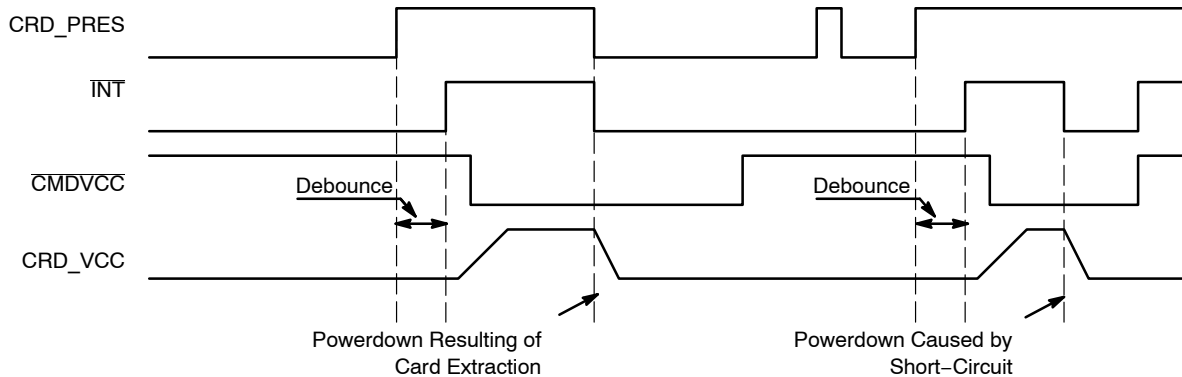


Figure 7. Fault Detection and Interrupt Management

### Interrupt Pin Management:

A card session is opened by toggling  $\overline{CMDVCC}$  High to Low.

Before a card session,  $\overline{CMDVCC}$  is supposed to be in a High position.  $\overline{INT}$  is Low if no card is present in the card connector (Normally open or normally closed type).  $\overline{INT}$  is High if a card is present. If a card is inserted ( $\overline{INT} = \text{High}$ ) and if  $V_{DD}$  drops below the UVLO threshold then  $\overline{INT}$  pin drops Low immediately. It turns back High when  $V_{DD}$  increases again over the UVLO limit (including hysteresis), a card being still present.

During a card session,  $\overline{CMDVCC}$  is Low and  $\overline{INT}$  pin goes Low when a fault is detected. In that case a deactivation is immediately and automatically performed (see Figure 6). When the microcontroller resets  $\overline{CMDVCC}$  to High it can sense the  $\overline{INT}$  level again after having got completed the deactivation.

As illustrated by Figure 7 the device has a debounce timer of 8 ms typical duration. When a card is inserted, output  $\overline{INT}$  goes High only at the end of the debounce time. When the card is removed a deactivation sequence is automatically and immediately performed and  $\overline{INT}$  goes Low.

# NCN8024R

## ESD PROTECTION

The NCN8024R includes devices to protect the pins against the ESD spikes voltages. To cope with the different ESD voltages developed across these pins, the built in structures have been designed to handle either 2 kV, when related to the micro controller side, or 8 kV when connected with the external contacts (HBM model). Practically, the

CRD\_RST, CRD\_CLK, CRD\_IO, CRD\_AUX1, CRD\_AUX2, CRD\_PRES and CRD\_PRES pins can sustain 8 kV. The CRD\_VCC pin has the same ESD protection and can source up to 70 mA continuously, the absolute maximum current being internally limited with a max at 150 mA. The CRD\_VCC current limit depends on V<sub>DDP</sub> and CRD\_VCC.

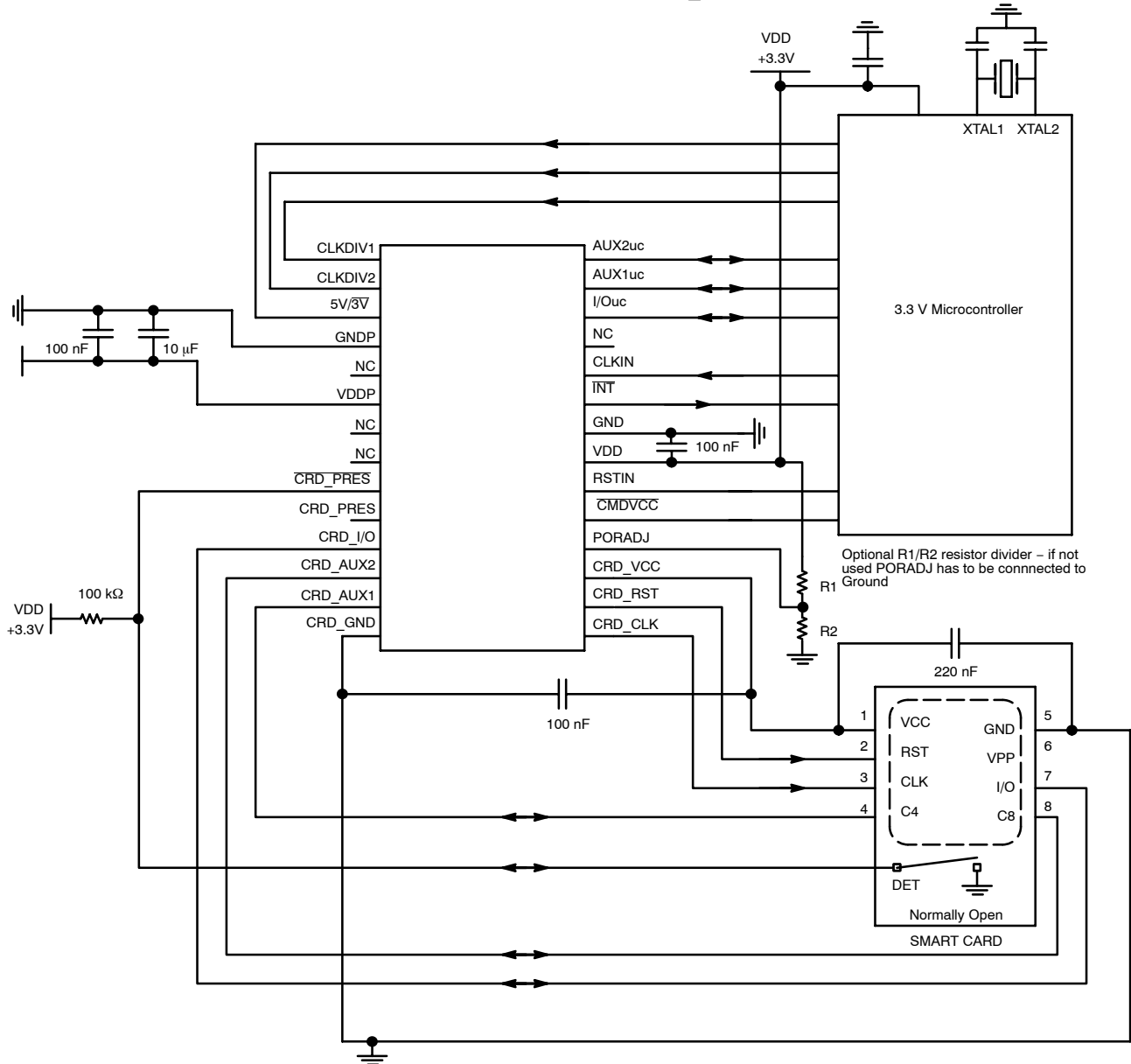


Figure 8. Application Schematic

## ORDERING INFORMATION

Device	Package	Shipping†
NCN8024RDWR2G	SOIC-28 (Pb-Free)	1000 / Tape & Reel
NCN8024RDTBR2G*	TSSOP-28 (Pb-Free)	2500 / Tape & Reel

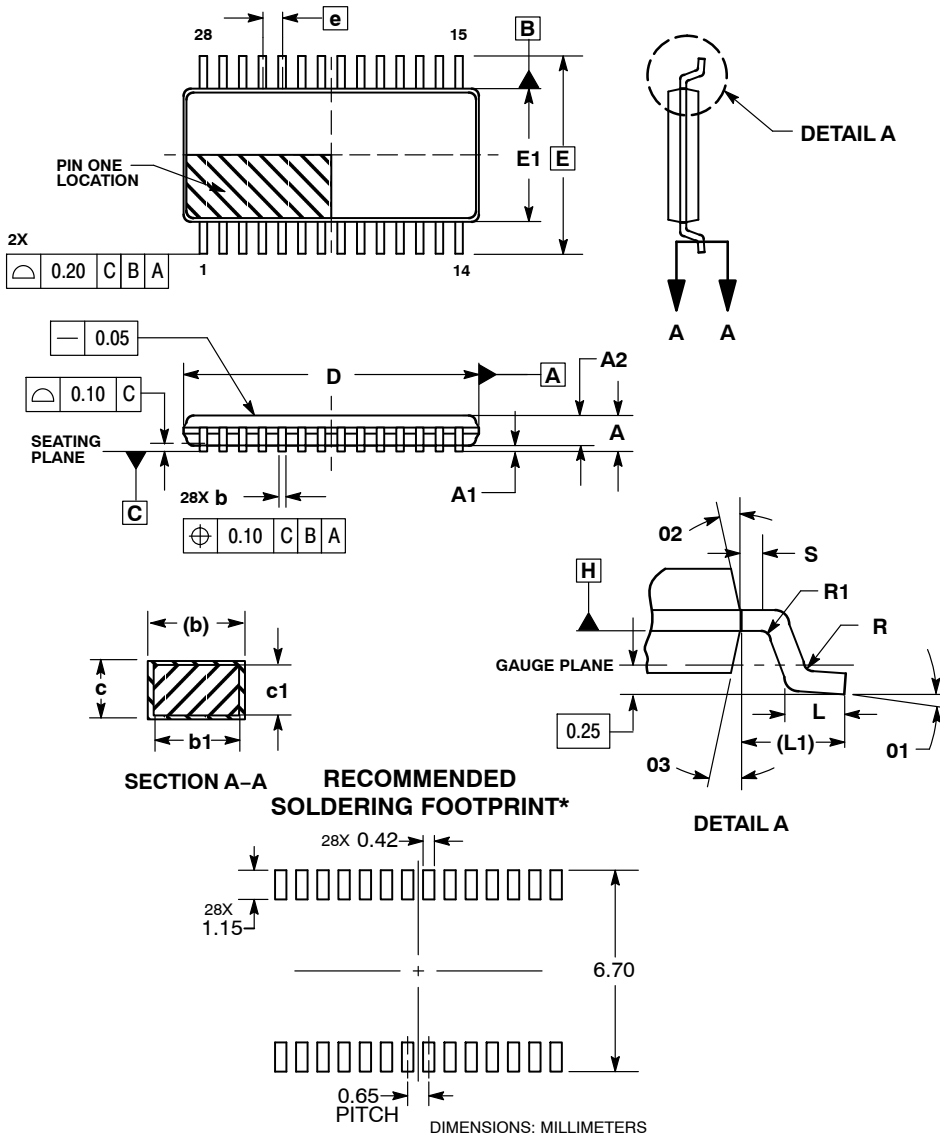
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*Consult Sales Office

# NCN8024R

## PACKAGE DIMENSIONS

### TSSOP28 CASE 948AA ISSUE A



#### NOTES:

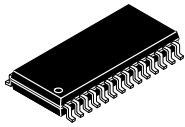
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION  $b$  DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

MILLIMETERS		
DIM	MIN	MAX
A	---	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
b1	0.19	0.25
c	0.09	0.20
c1	0.09	0.16
D	9.60	9.80
E	6.40 BSC	
E1	4.30	4.50
e	0.65 BSC	
L	0.45	0.75
L1	1.00 REF	
R	0.09	---
R1	0.09	---
S	0.20	---
01	0°	8°
02	12° REF	
03	12° REF	

\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

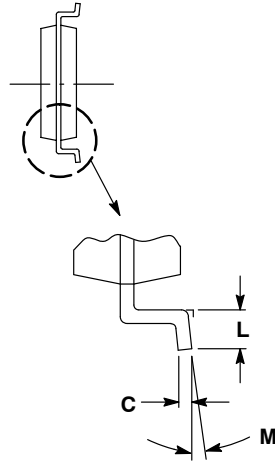
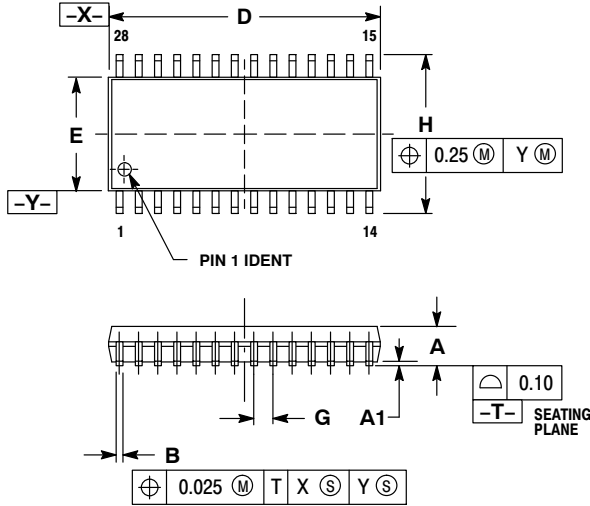
ON Semiconductor®



SCALE 1:1

SOIC-28 WB  
CASE 751F  
ISSUE J

DATE 23 SEP 2015

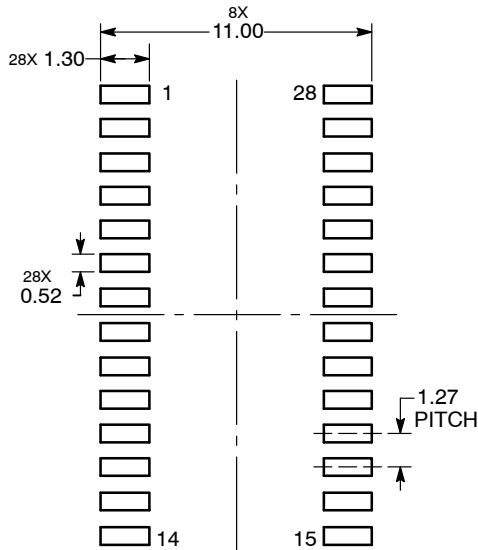


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

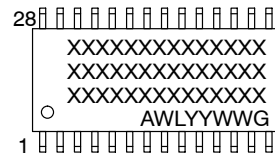
DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.13	0.29
B	0.35	0.49
C	0.23	0.32
D	17.80	18.05
E	7.40	7.60
G	1.27 BSC	
H	10.05	10.55
L	0.41	0.90
M	0°	8°

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM\*



- XXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present.

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