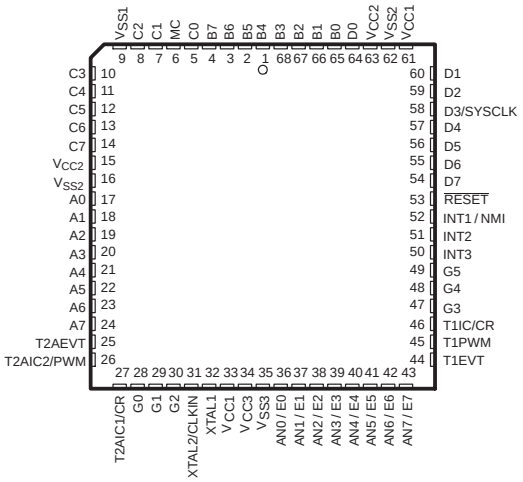
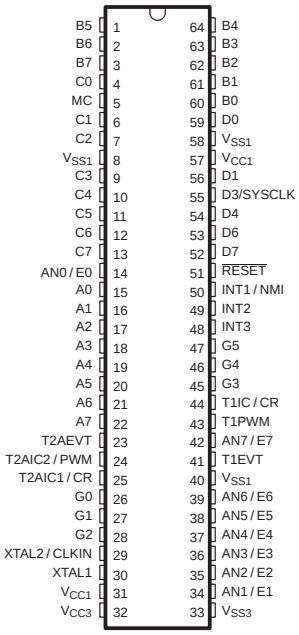
- **CMOS/EEPROM/EPROM Technologies on a Single Device**
  - **Mask-ROM Devices for High-Volume Production**
  - **One-Time-Programmable (OTP) EPROM Devices for Low-Volume Production**
  - **Reprogrammable EPROM Devices for Prototyping Purposes**
- **Internal System Memory Configurations**
  - **On-Chip Program Memory Versions**
    - **ROM: 24K Bytes**
    - **EPROM: 24K Bytes**
  - **Data EEPROM: 256 Bytes**
  - **Static RAM: 512 Bytes**
- **Flexible Operating Features**
  - **Low-Power Modes: STANDBY and HALT**
  - **Commercial, Industrial, and Automotive Temperature Ranges**
  - **Clock Options:**
    - **Divide-by-4 (0.5 MHz – 5 MHz SYSCLK)**
    - **Divide-by-1 (2 MHz – 5 MHz SYSCLK) Phase-Locked Loop (PLL)**
  - **Supply Voltage (V_{CC}): 5 V ± 10%**
- **Eight-Channel 8-Bit Analog-to-Digital Converter 1 (ADC1)**
- **TMS370 Series Compatibility**
  - **Instructions Upwardly Compatible With All TMS370 Devices**
  - **Register-to-Register Architecture**
  - **256 General-Purpose Registers**
  - **14 Powerful Addressing Modes**
- **Two 16-Bit General-Purpose Timers**
- **On-Chip 24-Bit Watchdog Timer**
- **Flexible Interrupt Handling**
- **CMOS/Package/TTL-Compatible I/O Pins**
  - **64-Pin Plastic and Ceramic Shrink Dual-In-Line Packages/44 Bidirectional, 9 Input Pins**
  - **68-Pin Plastic and Ceramic Leaded Chip Carrier Packages/46 Bidirectional, 9 Input Pins**
  - **All Peripheral Function Pins Are Software Configurable for Digital I/O**
- **Workstation/PC-Based Software Development System**
  - **C Compiler and C Source Debugger**
  - **Real-Time In-Circuit Emulation**
  - **Extensive Breakpoint/Trace Capability**
  - **Software Performance Analysis**
  - **Multi-Window User Interface**
  - **Microcontroller Programmer**

FN/FZ PACKAGE
(TOP VIEW)



JN/NM PACKAGE
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Pin Descriptions

NAME	PIN SDIP (64)	PIN LCC (68)	I/O†	DESCRIPTION
A0	15	17	I/O	Port A is a general-purpose bidirectional I/O port.
A1	16	18		
A2	17	19		
A3	18	20		
A4	19	21		
A5	20	22		
A6	21	23		
A7	22	24		
B0	60	65	I/O	Port B is a general-purpose bidirectional I/O port.
B1	61	66		
B2	62	67		
B3	63	68		
B4	64	1		
B5	1	2		
B6	2	3		
B7	3	4		
C0	4	5	I/O	Port C is a general-purpose bidirectional I/O port.
C1	6	7		
C2	7	8		
C3	9	10		
C4	10	11		
C5	11	12		
C6	12	13		
C7	13	14		
INT1/NMI	50	52	I	External (nonmaskable or maskable) interrupt/general-purpose input pin
INT2	49	51	I/O	External maskable interrupt input/general-purpose bidirectional pin
INT3	48	50	I/O	External maskable interrupt input/general-purpose bidirectional pin
AN0/E0	14	36	I	ADC1 analog input (AN0–AN7) or positive reference pins (AN1–AN7) Port E can be programmed individually as general-purpose input pins if not used as ADC1 analog input or positive reference input.
AN1/E1	34	37		
AN2/E2	35	38		
AN3/E3	36	39		
AN4/E4	37	40		
AN5/E5	38	41		
AN6/E6	39	42		
AN7/E7	42	43		
V_{CC3}	32	34		ADC1 positive-supply voltage and optional positive-reference input pin
V_{SS3}	33	35		ADC1 ground reference pin
$\overline{\text{RESET}}$	51	53	I/O	System reset bidirectional pin. As an input, $\overline{\text{RESET}}$ initializes the microcontroller; as open-drain output, $\overline{\text{RESET}}$ indicates that an internal failure was detected by the watchdog or oscillator fault circuit.
MC	5	6	I	Mode control (MC) pin. MC enables EEPROM write-protection-override (WPO) mode, also EPROM V_{PP}.
XTAL2/CLKIN	29	31	I	Internal oscillator crystal input/external clock source input
XTAL1	30	32	O	Internal oscillator output for crystal
V_{CC1}	31, 57	33, 61		Positive supply voltage
V_{CC2}	—	15,63		Positive supply voltage for digital I/O

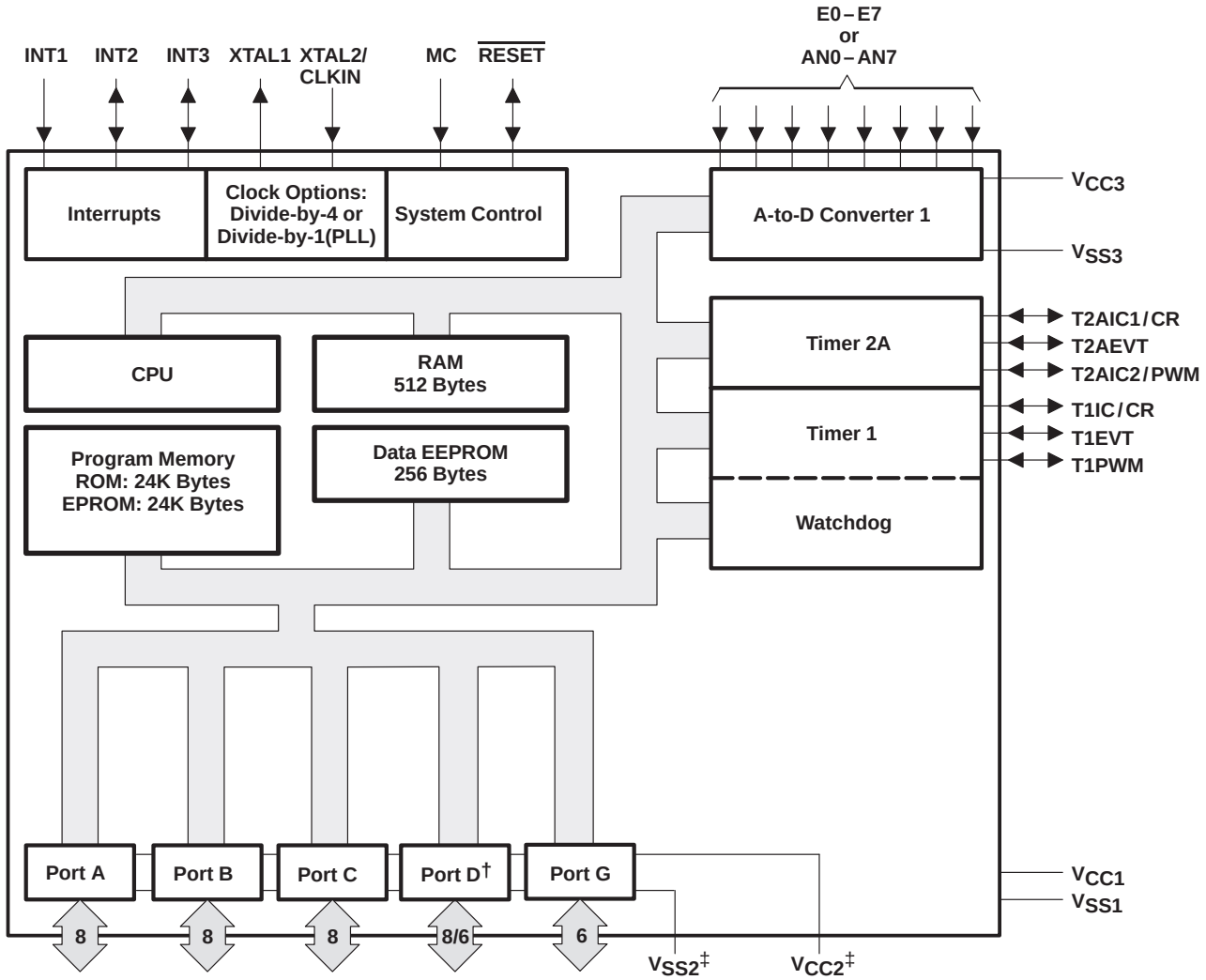
† I = input, O = output

Pin Descriptions (Continued)

PIN			I/O†	DESCRIPTION
NAME	SDIP (64)	LCC (68)		
V_{SS1}	8, 58,40	9		Ground reference for digital logic
V_{SS2}	—	16,62		Ground reference for digital I/O logic
D0 D1 D2 D3/SYSCLK D4 D5 D6 D7	59 56 — 55 54 — 53 52	64 60 59 58 57 56 55 54	I/O	Port D is a general-purpose bidirectional I/O port. D3 also can be configured as SYSCLK.
G0 G1 G2 G3 G4 G5	26 27 28 45 46 47	28 29 30 47 48 49	I/O	Port G is a general-purpose bidirectional I/O port.
T1IC/CR T1PWM T1EVT	44 43 41	46 45 44	I/O	Timer1 input capture/counter-reset input pin/general-purpose bidirectional pin Timer1 pulse-width-modulation (PWM) output pin/general-purpose bidirectional pin Timer1 external event input pin/general-purpose bidirectional pin
T2AIC1/CR T2AIC2/PWM T2AEVT	25 24 23	27 26 25	I/O	Timer2A input capture 1/counter reset input pin/general-purpose bidirectional pin Timer2A input capture 2/PWM output pin/general-purpose bidirectional pin Timer2A external event input pin/general-purpose bidirectional pin

† I = input, O = output

functional block diagram



† For the 64-pin devices, there are only six pins for port D.
‡ For the 64-pin devices, omit these power pins

description

The TMS370C077, TMS370C777, and SE370C777 devices are members of the TMS370 family of single-chip 8-bit microcontrollers. Unless otherwise noted, the term TMS370Cx7x refers to these devices. The TMS370 family provides cost-effective real-time system control through integration of advanced peripheral function modules and various on-chip memory configurations.

The TMS370Cx7x family is implemented using high-performance silicon-gate CMOS EPROM and EEPROM technologies. The low-operating power, wide-operating temperature range, and noise immunity of CMOS technology, coupled with the high performance and extensive on-chip peripheral functions make the TMS370Cx7x devices attractive in system designs for automotive electronics, industrial motor control, computer peripheral control, telecommunications, and consumer application.

All TMS370Cx7x devices contain the following on-chip peripheral modules:

- Eight-channel, 8-bit analog-to-digital converter 1 (ADC1)
- One 24-bit general-purpose watchdog timer
- Two 16-bit general-purpose timers (one with an 8-bit prescaler)

description (continued)

Table 1 provides a memory configuration overview of the TMS370Cx7x devices.

Table 1. Memory Configurations

DEVICE	PROGRAM MEMORY (BYTES)		DATA MEMORY (BYTES)		PACKAGES 68-PIN PLCC/CLCC, OR 64-PIN PSDIP/CSDIP
	ROM	EPROM	RAM	EEPROM	
TMS370C077A	24K	—	512	256	FN – PLCC / NM – PSDIP
TMS370C777A	—	24K	512	256	FN – PLCC / NM – PSDIP
SE370C777A†	—	24K	512	256	FZ – CLCC / JN – CSDIP

† System evaluators and development tools are for use only in a prototype environment, and their reliability has not been characterized.

The suffix letter A appended to the device names shown in the device column of Table 1 indicates the configuration of the device. ROM and EPROM devices have a different configuration as indicated in Table 2. ROM devices with the suffix letter A are configured through a programmable contact during manufacture.

Table 2. Suffix Letter Configuration

DEVICE‡	WATCHDOG TIMER	CLOCK	LOW-POWER MODE
EPROM A	Standard	Divide-by-4 (Standard oscillator)	Enabled
ROM A	Standard	Divide-by-4 or Divide-by-1 (PLL)	Enabled or disabled
	Hard		
	Simple		

‡ Refer to the “device numbering conventions” section for device nomenclature and the “device part numbers” section for ordering.

The 24K bytes of mask-programmable ROM in the associated TMS370C077 device are replaced with 24K bytes of EPROM in the TMS370C777 while all other available memory and on-chip peripherals are identical. A one-time-programmable device (OTP) (TMS370C777) and a reprogrammable device (SE370C777) are available.

The TMS370C777 OTP device is available in a plastic package. This microcontroller is effective for use as an immediate production update for the TMS370C077 ROM device or for low-volume production runs when the mask charge or cycle time for the low-cost mask-ROM device is not practical.

The SE370C777 has a windowed ceramic package that allows reprogramming of the program EPROM memory during the development/prototyping design phase. The SE370C777 device allows quick updates to breadboards and prototype systems while iterating initial designs.

The TMS370Cx7x family provides two low-power modes (STANDBY and HALT) for applications where low-power consumption is critical. Both modes stop all CPU activity (that is, no instructions are executed). In the STANDBY mode, the internal oscillator and the general-purpose timer remain active. In the HALT mode, all device activity is stopped. The device retains all RAM data and peripheral configuration bits throughout both low-power modes.

The TMS370Cx7x features advanced register-to-register architecture that allows direct arithmetic and logical operations without requiring an accumulator (for example, ADD R24, R47; add the contents of register 24 to the contents of register 47 and store the result in register 47). The TMS370Cx7x family is fully instruction-set-compatible, allowing easy transition between members of the TMS370 8-bit microcontroller family.

description (continued)

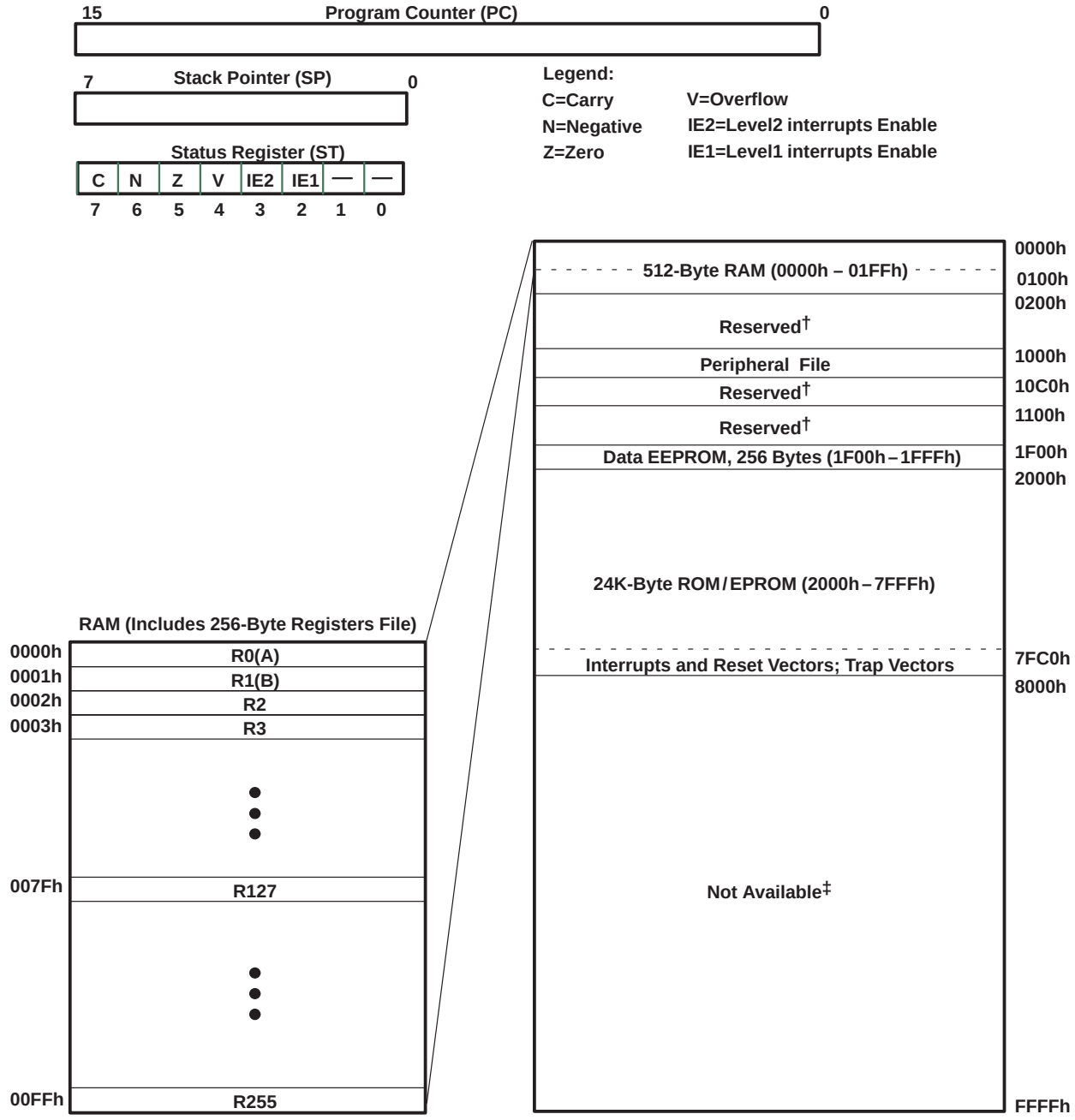
The TMS370Cx7x family provides the system designer with very economical, efficient solutions to real-time control applications. The TMS370 family compact development tool (CDT™) solves the challenge of efficiently developing the software and hardware required to design the TMS370Cx7x into an ever-increasing number of complex applications. The application source code can be written in assembly and C language, and the output code can be generated by the linker. The TMS370 family CDT development tool can communicate through a standard RS-232-C interface with an existing personal computer. This allows the use of personal-computer editors and software utilities already familiar to the designer. The TMS370 family CDT emphasizes ease-of-use through extensive use of menus and screen windowing so that a system designer with minimal training can begin developing software. Precise real-time in-circuit emulation and extensive symbolic debug and analysis tools ensure efficient software and hardware implementation as well as a reduced time-to-market cycle.

The TMS370Cx7x family, together with the TMS370 family CDT370, starter kit, software tools, the SE370C777 reprogrammable device, comprehensive product documentation, and customer support, provide a complete solution to the needs of the system designer.

CPU

The CPU used on TMS370Cx7x devices is the high-performance 8-bit TMS370 CPU module. The ’x7x implements an efficient register-to-register architecture that eliminates the conventional accumulator bottleneck. The complete ’x7x instruction set is summarized in Table 17. Figure 1 illustrates the CPU registers and memory blocks.

CPU (continued)



† Reserved means that the address space is reserved for future expansion.
‡ Not available means that the address space is not accessible.

Figure 1. Programmer's Model

CPU (continued)

The ’x7x CPU architecture provides the following components:

- CPU registers:
  - A stack pointer that points to the last entry in the memory stack
  - A status register that monitors the operation of the instructions and contains the global-interrupt-enable bits
  - A program counter (PC) that points to the memory location of the next instruction to be executed
- A memory map that includes:
  - 512 bytes of general-purpose RAM that can be data memory storage, program instructions, general-purpose register, or the stack (can be located only in the first 256 bytes)
  - A peripheral file that provides access to all internal peripheral modules, system-wide control functions, and EEPROM/EPROM programming control
  - A 256-byte EEPROM module that provides in-circuit programmability and data retention in power-off conditions
  - 24K-bytes of ROM or 24K-bytes of EPROM program memory

stack pointer (SP)

The SP is an 8-bit CPU register. Stack operates as a last-in, first-out, read/write memory. The stack is used typically to store the return address on subroutine calls as well as the status register contents during interrupt sequences.

The SP points to the last entry or to the top of the stack. The SP increments automatically before data is pushed onto the stack and decrements after data is popped from the stack. The stack can be located only in the first 256 bytes of the on-chip RAM memory.

status register (ST)

The ST monitors the operation of the instructions and contains the global-interrupt-enable bits. The ST includes four status bits (condition flags) and two interrupt-enable bits:

- The four status bits indicate the outcome of the previous instruction; conditional instructions (for example, the conditional jump instructions) use these status bits to determine program flow.
- The two interrupt-enable bits control the two interrupt levels.

The ST register and status-bit notation are shown in Table 3.

Table 3. Status Register

7	6	5	4	3	2	1	0
C	N	Z	V	IE2	IE1	Reserved	Reserved
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0		

R = read, W = write, 0 = value after reset

CPU (continued)

program counter (PC)

The contents of the PC point to the memory location of the next instruction to be executed. The PC consists of two 8-bit registers in the CPU: the program counter high (PCH) and program counter low (PCL). These registers contain the most-significant byte (MSbyte) and least-significant byte (LSbyte) of a 16-bit address.

The contents of the reset vector (7FFEh, 7FFFh) are loaded into the program counter during reset. The PCH (MSbyte of the PC) is loaded with the contents of memory location 7FFEh, and the PCL (LSbyte of the PC) is loaded with the contents of memory location 7FFFh. Figure 2 shows this operation using an example value of 2000h as the contents of memory locations 7FFEh and 7FFFh (reset vector).

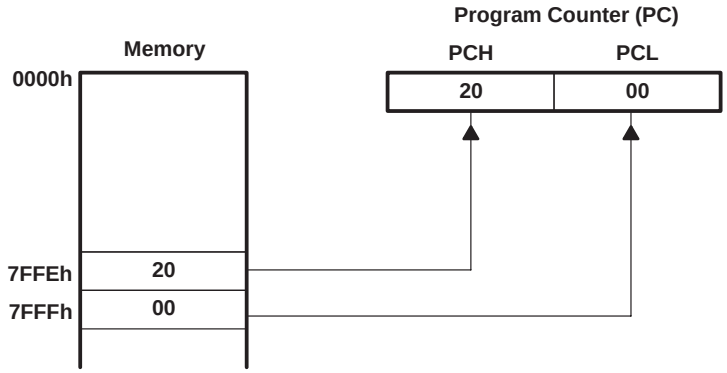


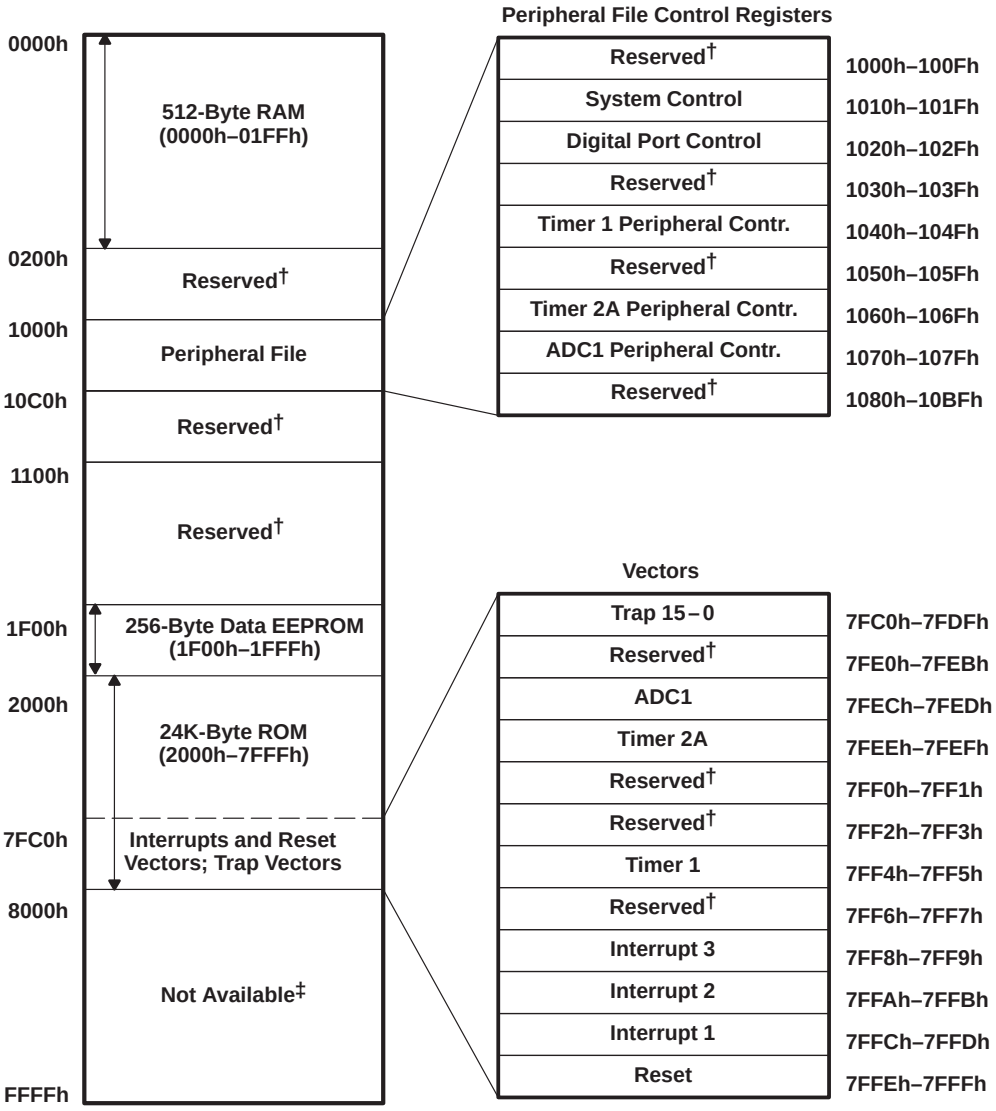
Figure 2. Program Counter After Reset

memory map

The TMS370Cx7x architecture is based on the Von Neuman architecture, where the program memory and data memory share a common address space. All peripheral input/output is memory-mapped in this same common address space. As shown in Figure 3, the TMS370Cx7x provides a memory-mapped RAM, ROM, data EEPROM, EPROM, input/output pins, peripheral functions, and system-interrupt vectors.

The peripheral file contains all input/output port control, peripheral status and control, EPROM, EEPROM programming, and system-wide control functions. The peripheral file consists of 256 contiguous addresses located from 1000h to 10FFh. The 256 contiguous addresses are divided logically into 16 peripheral file frames of 16 bytes each. Each on-chip peripheral is assigned to a separate frame through which peripheral control and data information is passed. The TMS370Cx7x has its on-chip peripherals and system control assigned to peripheral file frames 1 through 7, addresses 1010h through 107Fh.

memory map (continued)



† Reserved = the address space is reserved for future expansion.
‡ Not available = address space is unavailable in the mode illustrated.

Figure 3. TMS370Cx7x Memory Map

RAM/register file (RF)

Locations within RAM address space can serve as either register file or general-purpose read/write memory, program memory, or stack instructions. The TMS370Cx7x device contains 512 bytes of internal RAM mapped beginning at location 0000h and continuing through location 01FFh which is shown in Figure 3. The first 256 bytes of RAM (0000h – 00FFh) are the register files, R0 through R255.

The first two registers, R0 and R1, are also called registers A and B, respectively. Some instructions implicitly use register A or B; for example, the instruction LDSP (load SP) assumes that the value to be loaded into the stack pointer is contained in register B. Registers A and B are the only registers cleared on reset.

peripheral file (PF)

The TMS370Cx7x control registers contain all the registers necessary to operate the system and peripheral modules on the device. The instruction set includes some instructions that access the peripheral file (PF) directly. These instructions designate the register by the number of the PF relative to 1000h, preceded by P0 for a hexadecimal designator, or by P for a decimal designator. For example, the system control register 0 (SCCR0) is located at address 1010h; its peripheral file hexadecimal designator is P010, and its decimal designator is P16. Table 4 shows the TMS370Cx7x peripheral files.

Table 4. TMS370Cx7x Peripheral File Address Map

ADDRESS RANGE	PERIPHERAL FILE DESIGNATOR	DESCRIPTION
1000h–100Fh	P000–P00F	Reserved for factory test
1010h–101Fh	P010–P01F	System and EEPROM/EPROM control registers
1020h–103Fh	P020–P03F	Digital I/O port control registers
1040h–104Fh	P040–P04F	Timer 1 registers
1050h–105Fh	P050–P05F	Reserved
1060h–106Fh	P060–P06F	Timer 2A registers
1070h–107Fh	P070–P07F	Analog-to-digital converter 1 registers
1080h–10FFh	P080–P0FF	Reserved

data EEPROM

The TMS370Cx7x devices contain 256 bytes of data EEPROM, and have a memory map beginning at location 1F00h, and continuing through location 1FFFh. Writing to the data EEPROM module is controlled by the data EEPROM control register (DEECTL) and the write-protection register (WPR). Programming algorithm examples are available in the *TMS370 Family User's Guide* (literature number SPNU127), or the *TMS370 Family Data Manual* (SPNS014B). The data EEPROM features include the following:

- Programming:
  - Bit, byte, and block write/erase modes
  - Internal charge pump circuitry: No external EEPROM programming voltage supply is needed.
  - Control register: Data EEPROM programming is controlled by the data EEPROM control register (DEECTL) located in the PF frame beginning at location P01A.
  - In-circuit programming capability: There is no need to remove the device to program.
- Write-protection: Writes to the data EEPROM are disabled during the following conditions:
  - Reset: All programming of the data EEPROM module is halted.
  - Write protection active: There is one write-protect bit per 32-byte EEPROM block.
  - Low-power mode operation
- Write protection can be overridden by applying 12 V to MC.

Table 5 shows the memory map of the control registers.

data EEPROM (continued)

Table 5. Data EEPROM and Program EPROM Control Registers Memory Map

ADDRESS	SYMBOL	NAME†
101Ah (P01A)	DEECTL	Data EEPROM control register
101Bh (P01B)		Reserved
101Ch (P01C)	EPCTLM	Program EPROM control register – middle array
101Dh (P01D)		Reserved
101Eh (P01E)	EPCTLL	Program EPROM control register – low array

† For the 24K-byte EPROM device, the program memory is controlled by P01C and P01E.

program EPROM

The TMS370C777 contains 24K bytes of program EPROM made up of one 16K-byte array and one 8K-byte array. The 16K-byte array is located at address locations 2000h through 5FFFh, and the 8K-byte array is located at address locations 6000h through 7FFFh, as shown in Table 6.

Table 6. TMS370C777 EPROM Memory Map

PARAMETER	VALUE	
EPROM size	24K Bytes	
Memory mapped	16K Bytes at 2000h–5FFFh	8K Bytes at 6000h–7FFFh
Control registers	EPCTLL (P01E)	EPCTLM (P01C)

As shown in Table 6 for the two EPROM areas, the 16K-byte array is controlled by register EPCTLL located at 101Eh (P01E), and the 8K-byte array is controlled by register EPCTLM located at 101Ch (P01C).

Reading the program-EPROM modules is identical to reading other internal memory. During programming, the EPROM is controlled by the program EPROM control registers EPCTLL and EPCTLM. The program EPROM modules' features include:

- Programming
  - In-circuit programming capability if V_{PP} is applied to the MC pin
  - Control register: Program EPROM programming is controlled by the program EPROM control registers EPCTLL and EPCTLM, located at the addresses in PF frame 1 as shown in Table 5.
  - Programming one EPROM module while executing the other
- Write-protection: Writes to the program EPROM are disabled under the following conditions:
  - Reset: All programming to the EPROM module is halted.
  - Low-power modes
  - 13 V not applied to MC

program ROM

The program ROM consists of 24K bytes of mask-programmable ROM. The program ROM is used for permanent storage of data or instructions. Programming of the mask ROM is performed at the time of device fabrication. Memory addresses 7FE0h–7FEBh is reserved for Texas Instruments (TI™). 7FECh to 7FFFh are reserved for interrupt and reset vectors. Trap vectors, used with TRAP0 through TRAP15 instructions, are located between addresses 7FC0h and 7FDFh.

system reset

The system-reset operation ensures an orderly start-up sequence for the TMS370Cx7x CPU-based device. There are up to three different actions that can cause a system reset to the device. Two of these actions are generated internally, while one ($\overline{\text{RESET}}$) is controlled externally. These actions are as follows:

- External $\overline{\text{RESET}}$ pin. A low-level signal can trigger an external reset. To ensure a reset, the external signal should be held low for one SYSCLK cycle (it is possible, however, that a signal of less than one SYSCLK could cause a reset). See the *TMS370 Family User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (SPNS014B) for more information.
- Watchdog (WD) timer. A watchdog-generated reset occurs when an improper value is written to the WD key register or when the re-initialization does not occur before the watchdog timer timeout. See the *TMS370 Family User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (SPNS014B) for more information.
- Oscillator reset. Reset occurs when the oscillator operates outside the recommended operating range. See the *TMS370 Family User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (SPNS014B) for more information.

Once a reset source is activated, the external $\overline{\text{RESET}}$ pin is driven (active) low for a minimum of eight SYSCLK cycles. This allows the 'x7x device to reset external system components. Additionally, if a cold-start condition (e.g., V_{CC} is off for several hundred milliseconds) exists, an oscillator failure occurs, or the $\overline{\text{RESET}}$ pin is held low, then the reset logic holds the device in a reset state for as long as these actions are active.

After a reset, the program can check the oscillator fault flag (OSC FLT FLAG, SCCR0.4), the cold start flag (COLD START, SCCR0.7), and the watchdog reset (WD OVRFL INT FLAG, T1CTL2.5) to determine the source of the reset. A reset does not clear these flags. Table 7 lists the reset sources.

Table 7. Reset Sources

REGISTER	ADDRESS	PF	BIT NO.	CONTROL BIT NAME	SOURCE OF RESET
SCCR0	1010h	P010	7	COLD START	Cold (power-up)
SCCR0	1010h	P010	4	OSC FLT FLAG	Oscillator out of range
T1CTL2	104Ah	P04A	5	WD OVRFL INT FLAG	Watchdog timer timeout

Once a reset is activated, the following sequence of events occurs:

1. The CPU registers initialize: ST = 00h, SP = 01h (reset state).
2. Registers A and B initialize to 00h (no other RAM is changed).
3. The contents of the LSbyte of the reset vector (07FFh) are read and stored in the PCL.
4. The contents of the MSbyte of the reset vector (07FEh) are read and stored in the PCH.
5. Program execution begins with an opcode fetch from the address pointed to by the PC.

The reset sequence takes 20 SYSCLK cycles from the time the reset pulse is released until the first opcode fetch. During a reset, RAM contents (except for registers A and B) remain unchanged, and the module control register bits are initialized to their reset state.

interrupts

The TMS370 family software programmable interrupt structure permits flexible on-chip and external-interrupt configurations to meet real-time interrupt-driven application requirements. The hardware-interrupt structure incorporates two priority levels as shown in Figure 4. Interrupt level 1 has a higher priority than interrupt level 2. The two priority levels can be masked independently by the global-interrupt mask bits (IE1 and IE2) of the status register.

Each system interrupt is configured independently to either the high- or low-priority chain by the application program during system initialization. Within each interrupt chain, the interrupt priority is fixed by the position of the system interrupt. However, since each system interrupt is configured selectively on either the high- or low-priority interrupt chain, the application program can elevate any system interrupt to the highest priority. Arbitration between the two priority levels is performed within the CPU. Arbitration within each of the priority chains is performed within the peripheral modules to support interrupt expansion for future modules. Pending interrupts are serviced upon completion of current instruction execution, depending on their interrupt mask and priority conditions.

The TMS370Cx7x has six hardware-system interrupts (plus $\overline{\text{RESET}}$) as shown in Table 8. Each system interrupt has a dedicated vector located in program memory through which control is passed to the interrupt service routines. All of the interrupt sources are maskable individually by local interrupt-enable control bits in the associated peripheral file (PF). Each interrupt source FLAG bit is readable individually for software polling or for determining which interrupt source generated the associated system interrupt. The interrupt-control block diagram is illustrated in Figure 4.

interrupts (continued)

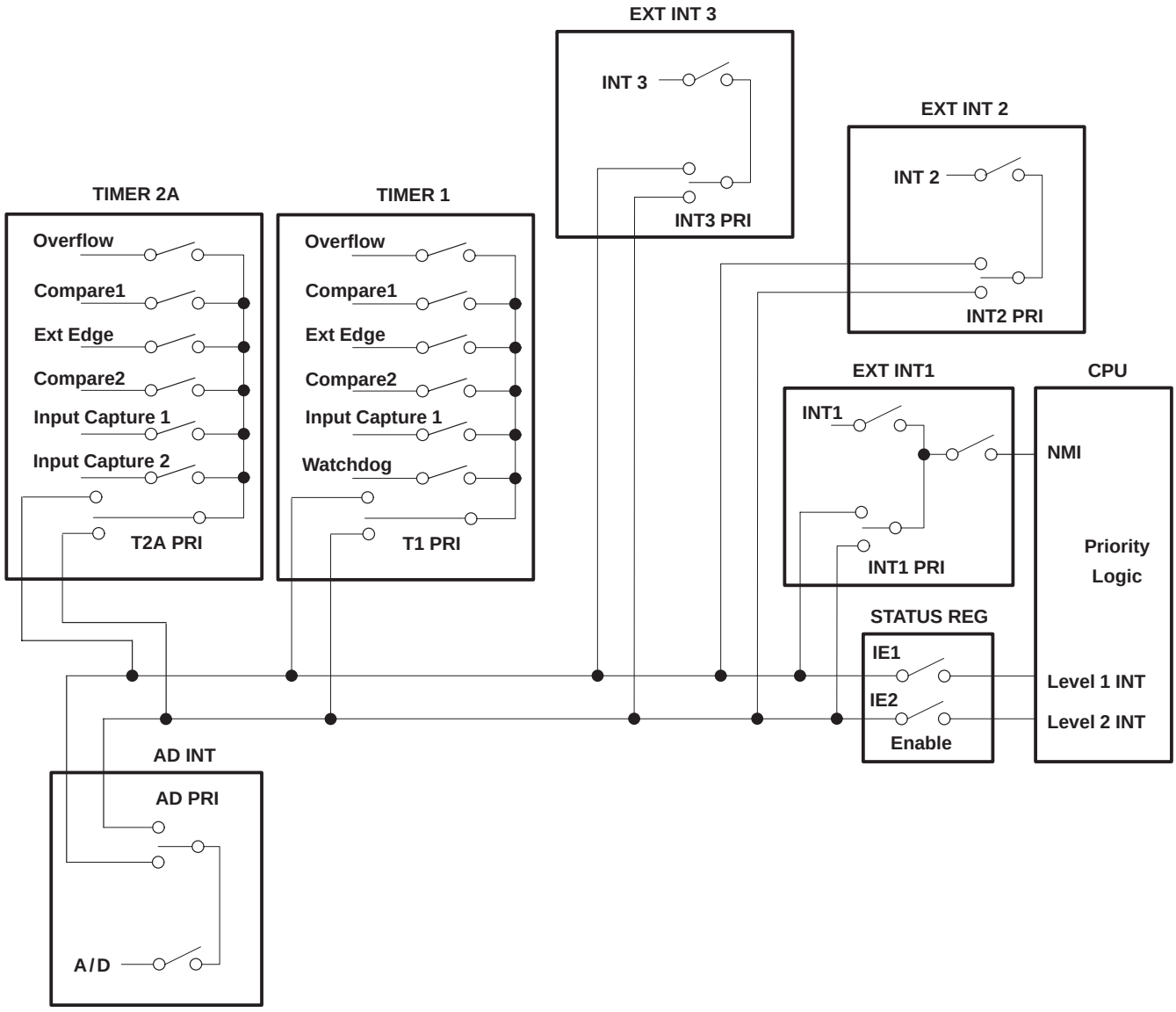


Figure 4. Interrupt Control

Of the six system interrupts, three are generated by on-chip peripherals (T1INT, T2AINT, and ADINT) and three are external interrupts (INT1 – INT3). Software configuration of the external interrupts is performed through the INT1, INT2, and INT3 control registers in PF frame 1.

Each external interrupt is individually software configurable for input polarity (rising or falling edge) for ease of system interface. External interrupt INT1 is software configurable as either a maskable or non-maskable interrupt. When INT1 is configured as nonmaskable, it cannot be masked by the individual- or global-enable mask bits. The INT1 NMI bit is protected during non-privileged operation and therefore should be configured during the initialization sequence following reset. To maximize pin flexibility, external interrupts INT2 and INT3 can be software configured as general-purpose input/output pins if the interrupt function is not required (INT1 can be configured similarly as an input pin). Table 8 lists the interrupt vector sources, corresponding addresses, and hardware priorities.

interrupts (continued)

Table 8. Hardware System Interrupts

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	VECTOR ADDRESS	PRIORITY†
External $\overline{\text{RESET}}$ Watchdog overflow Oscillator fault detect	COLD START WD OVRFL INT FLAG OSC FLT FLAG	$\overline{\text{RESET}}$‡	7FFEh, 7FFFh	1
External INT1	INT1 FLAG	INT1‡	7FFCh, 7FFDh	2
External INT2	INT2 FLAG	INT2‡	7FFAh, 7FFBh	3
External INT3	INT3 FLAG	INT3‡	7FF8h, 7FF9h	4
Timer 1 overflow Timer 1 compare 1 Timer 1 compare 2 Timer 1 external edge Timer 1 input capture 1 Watchdog overflow	T1 OVRFL INT FLAG T1C1 INT FLAG T1C2 INT FLAG T1EDGE INT FLAG T1IC1 INT FLAG WD OVRFL INT FLAG	T1INT§	7FF4h, 7FF5h	5
Timer 2A overflow Timer 2A compare 1 Timer 2A compare 2 Timer 2A external edge Timer 2A input capture 1 Timer 2A input capture 2	T2A OVRFL INT FLAG T2AC1 INT FLAG T2AC2 INT FLAG T2AEDGE INT FLAG T2AIC1 INT FLAG T2AIC2 INT FLAG	T2AINT	7FEEh, 7FEFh	6
ADC1 conversion complete	AD INT FLAG	ADINT	7FECh, 7FEDh	7

† Relative priority within an interrupt level
‡ Releases microcontroller from STANDBY and HALT low-power modes
§ Releases microcontroller from STANDBY low-power mode

privileged operation and EEPROM write-protection override

The TMS370Cx7x family has significant flexibility to enable the designer to software-configure the system and peripherals to meet the requirements of a broad variety of applications. The nonprivileged mode of operation ensures the integrity of the system configuration, once it is defined for an application. Following a hardware reset, the TMS370Cx7x operates in the privileged mode, where all peripheral file registers have unrestricted read/write access, and the application program configures the system during the initialization sequence following reset. As the last step of system initialization, the PRIVILEGE DISABLE bit (SCCR2.0) should be set to 1 to enter the nonprivileged mode, thereby disabling write operations to specific configuration control bits within the peripheral file. Table 9 lists the system configuration bits that are write-protected during the nonprivileged mode and must be configured by software prior to exiting the privileged mode.

privileged operation and EEPROM write-protection override (continued)

Table 9. Privileged Bits

REGISTER†		CONTROL BIT
NAME	LOCATION	
SCCRO	P010.5 P010.6	PF AUTOWAIT OSC POWER
SCCR1	P011.2 P011.4	MEMORY DISABLE AUTOWAIT DISABLE
SCCR2	P012.0 P012.1 P012.3 P012.4 P012.6 P012.7	PRIVILEGE DISABLE INT1 NMI CPU STEST BUS STEST PWRDWN/IDLE HALT/STANDBY
T1PRI	P04F.6 P04F.7	T1 PRIORITY T1 STEST
T2APRI	P06F.6 P06F.7	T2A PRIORITY T2A STEST
ADPRI	P07F.5 P07F.6 P07F.7	AD ESPEN AD PRIORITY AD STEST

† The privileged bits are shown in a bold typeface in the peripheral file frame 1 section.

The write-protect-override (WPO) mode provides an external hardware method of overriding the write-protection registers of the data EEPROM on the TMS370Cx7x. To enter the WPO mode apply a 12-V input to the MC pin after the $\overline{\text{RESET}}$ input goes high (logic 1). The high voltage on MC during the WPO mode is not the programming voltage for the data EEPROM or program EPROM. All EEPROM programming voltages are generated on-chip. The WPO mode provides hardware-system-level capability to modify the content of the data EEPROM while the device remains in the application but only while requiring a 12-V external input on the MC pin (normally not available in the end application except in a service or diagnostic environment).

low-power and IDLE modes

The TMS370Cx7x devices have two low-power modes (STANDBY and HALT) and an IDLE mode. For mask-ROM devices, low-power modes can be disabled permanently through a programmable contact at the time when the mask is manufactured.

The STANDBY and HALT low-power modes significantly reduce power consumption by reducing or stopping the activity of the various on-chip peripherals when processing is not required. Each of the low-power modes is entered by executing the idle instruction when the PWRDWN/IDLE bit in register SCCR2 has been set to 1. The HALT/STANDBY bit in SCCR2 controls which low-power mode is entered.

In the STANDBY mode (HALT/STANDBY = 0), all CPU activity and most peripheral module activity is stopped; however, the oscillator, internal clocks, and timer 1 remain active. System processing is suspended until a qualified interrupt (hardware $\overline{\text{RESET}}$, external interrupt on INT1, INT2, INT3, or timer 1 interrupt) is detected.

In the HALT mode (HALT/STANDBY = 1), the TMS370Cx7x is placed in its lowest power-consumption mode. The oscillator and internal clocks are stopped, causing all internal activity to be halted. System activity is suspended until a qualified interrupt (hardware $\overline{\text{RESET}}$ or an external interrupt on INT1, INT2, INT3) is detected. The low-power mode selection bits are summarized in Table 10.

low-power and IDLE modes (continued)

Table 10. Low-Power/Idle Control Bits

POWER-DOWN CONTROL BITS		MODE SELECTED
PWRDWN/IDLE (SCCR2.6)	HALT/STANDBY (SCCR2.7)	
1	0	STANDBY
1	1	HALT
0	X	IDLE

X = don't care

When low-power modes are disabled through a programmable contact in the mask-ROM devices, writing to the SCCR2.6–7 bits is ignored. In addition, if an IDLE instruction is executed when low-power modes are disabled through a programmable contact, the device always enters the IDLE mode.

To provide a method of always exiting low-power modes for mask-ROM devices, INT1 is enabled automatically as a nonmaskable interrupt (NMI) during low-power modes when the hard watchdog is selected. This means that the NMI always is generated, regardless of the interrupt enable flags.

The following information is preserved throughout both the STANDBY and HALT modes: RAM (register file), CPU registers (stack pointer, program counter, and status register), I/O pin direction and output data, and status registers of all on-chip peripheral functions. Since all CPU instruction processing is stopped during the STANDBY and HALT modes, the clocking of the watchdog timer is inhibited.

clock modules

The '370Cx7x family provides two clock options which are referred to as divide-by-1 (PLL) and divide-by-4 (standard oscillator). Both the divide-by-1 and divide-by-4 options are configurable during the manufacturing process of a TMS370 microcontroller. The '370Cx7x ROM-masked devices offer both options to meet system engineering requirements. Only one of the two clock options is allowed on the ROM device while the EPROM devices have the divide-by-4 option.

The divide-by-1 clock module option provides the capability for reduced electromagnetic interference (EMI) with no added cost.

The divide-by-1 provides a 1-to-1 match of the external resonator frequency to the internal system clock (SYSCLK) frequency. The divide-by-4 produces a SYSCLK which is one-fourth the frequency of the external resonator. Inside the divide-by-1 module, the frequency of the external resonator is multiplied by four. The clock module then divides the resulting signal by four to provide the four-phased internal system clock signals. The resulting SYSCLK is equal to the resonator frequency. The frequencies are formulated as follows:

$$\text{Divide-by-4 option : SYSCLK} = \frac{\text{external resonator frequency}}{4} = \frac{\text{CLKIN}}{4}$$

$$\text{Divide-by-1 option : SYSCLK} = \frac{\text{external resonator frequency} \times 4}{4} = \text{CLKIN}$$

The main advantage of choosing a divide-by-1 oscillator is the improved EMI performance. The harmonics of low-speed resonators extend through less of the emissions spectrum than the harmonics of faster resonators. The divide-by-1 provides the capability of reducing the resonator speed by four times, and this results in a steeper decay of emissions produced by the oscillator.

system configuration registers

Table 11 lists system configuration, control functions, and registers for controlling EEPROM programming. The privileged bits are bold typefaced and shaded.

Table 11. Peripheral File Frame 1: System Configuration Registers

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P010	COLD START	**OSC POWER**	**PF AUTO WAIT**	OSC FLT FLAG	MC PIN WPO	MC PIN DATA	—	µP/µC MODE	SCCR0
P011		—	—	**AUTOWAIT DISABLE**	—	**MEMORY DISABLE**	—	—	SCCR1
P012	**HALT/ STANDBY**	**PWRDWN/ IDLE**	—	**BUS STEST**	**CPU STEST**	—	**INT1 NMI**	**PRIVILEGE DISABLE**	SCCR2
P013 to P016	Reserved								
P017	INT1 FLAG	INT1 PIN DATA	—	—	—	INT1 POLARITY	INT1 PRIORITY	INT1 ENABLE	INT1
P018	INT2 FLAG	INT2 PIN DATA	—	INT2 DATA DIR	INT2 DATA OUT	INT2 POLARITY	INT2 PRIORITY	INT2 ENABLE	INT2
P019	INT3 FLAG	INT3 PIN DATA	—	INT3 DATA DIR	INT3 DATA OUT	INT3 POLARITY	INT3 PRIORITY	INT3 ENABLE	INT3
P01A	BUSY	—	—	—	—	AP	W1W0	EXE	DEECTL
P01B	Reserved								
P01C	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTLM
P01D	Reserved								
P01E	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTLL
P01F	Reserved								

digital port control registers

Peripheral file frame 2 contains the digital I/O pin configuration and control registers. Table 12 lists the specific addresses, registers, and control bits within this peripheral file frame. Table 13 shows the port-configuration register setup.

Table 12. Peripheral File Frame 2: Digital Port Control Registers

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P020	Reserved								APORT1
P021	Port A Control Register 2								APORT2
P022	Port A Data								ADATA
P023	Port A Direction								ADIR
P024	Reserved								BPORT1
P025	Port B Control Register 2								BPORT2
P026	Port B Data								BDATA
P027	Port B Direction								BDIR
P028	Reserved								CPORT1
P029	Port C Control Register 2								CPORT2
P02A	Port C Data								CDATA
P02B	Port C Direction								CDIR
P02C	Port D Control Register 1								DPORT1
P02D	Port D Control Register 2†								DPORT2
P02E	Port D Data								DDATA
P02F	Port D Direction								DDIR
P030 to P035	Reserved								
P036	–	–	Port G Data						GDATA
P037	–	–	Port G Direction						GDIR

† To configure pin D3 as SYSCLK, set port D control register 2 = 08h.

Table 13. Port Configuration Register Setup

PORT	PIN	abcd 00y0	abcd 00q1
A	0–7	Data In y	Data Out q
B	0–7	Data In y	Data Out q
C	0–7	Data In y	Data Out q
D	0–7	Data In y	Data Out q
G	0–5	Data In y	Data Out q
a = Port x Control Register 1‡ b = Port x Control Register 2 c = Data d = Direction			

‡ DPORT only

timer 1 (T1) module

The programmable timer 1 (T1) module of the TMS370Cx7x provides the designer with the enhanced timer resources required to perform real-time system control. The T1 module contains the general-purpose timer and the watchdog (WD) timer. The two independent 16-bit timers, T1 and WD, allow program selection of input clock sources (real-time, external event, or pulse-accumulate) with multiple 16-bit registers (input capture and compare) for special timer function control. The T1 module includes three external device pins that can be used for multiple counter functions (operation-mode dependent) or used as general-purpose I/O pins. The T1 module block diagram is shown in Figure 5.

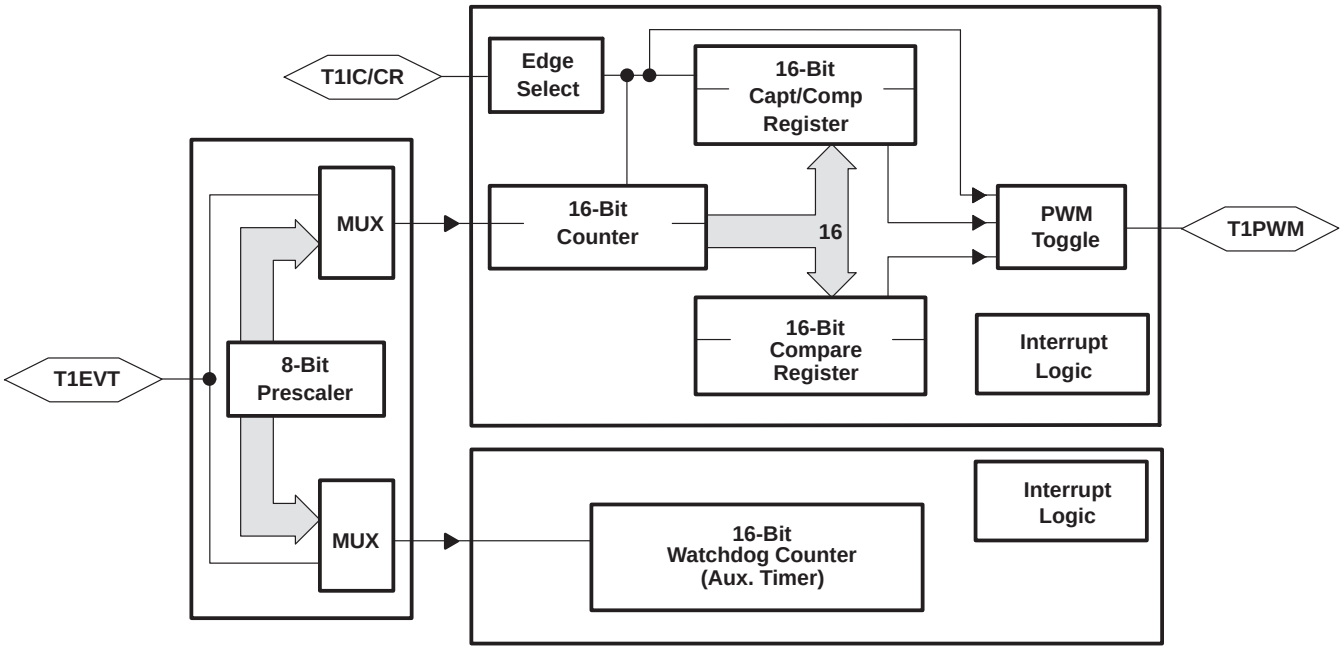


Figure 5. Timer 1 Block Diagram

- Three T1 I/O pins:
  - T1IC/CR: Timer 1 input capture / counter reset input pin, or general-purpose bidirectional I/O pin
  - T1PWM: Timer 1 pulse-width-modulation (PWM) output pin, or general-purpose bidirectional I/O pin
  - T1EVT: Timer 1 event input pin, or general-purpose bidirectional I/O pin
- Two operation modes:
  - Dual-compare mode: Provides PWM signal
  - Capture/compare mode: Provides input-capture pin
- One 16-bit general-purpose resettable counter
- One 16-bit compare register with associated compare logic
- One 16-bit capture/compare register, which, depending on the mode of operation, operates as either capture or compare register.
- One 16-bit watchdog counter can be used as an event counter, a pulse accumulator, or an interval timer if watchdog feature is not needed.
- Prescaler/clock sources that determine one of eight clock sources for general-purpose timer

timer 1 (T1) module (continued)

- Selectable edge-detection circuitry that, depending on the mode of operation, senses active transitions on the input capture pins (T1IC/CR).
- Interrupts that can be generated on the occurrence of:
  - A capture
  - A compare equal
  - A counter overflow
  - An external edge detection
- Sixteen T1 module control registers: Located in the PF frame beginning at address P040

Table 14 lists the T1 module control register.

timer 1 (T1) module (continued)

Table 14. Timer 1 Module Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
	Modes: Capture / Compare and Dual-Compare								
P040	Bit 15			T1 Counter MSbyte				Bit 8	T1CNTR
P041	Bit 7			T1 Counter LSbyte				Bit 0	
P042	Bit 15			Compare Register MSbyte				Bit 8	T1C
P043	Bit 7			Compare Register LSbyte				Bit 0	
P044	Bit 15			Capture/Compare Register MSbyte				Bit 8	T1CC
P045	Bit 7			Capture/Compare Register LSbyte				Bit 0	
P046	Bit 15			Watchdog Counter MSbyte				Bit 8	WDCNTR
P047	Bit 7			Watchdog Counter LSbyte				Bit 0	
P048	Bit 7			Watchdog Reset Key				Bit 0	WDRST
P049	WD OVRFL TAP SEL†	WD INPUT SELECT2†	WD INPUT SELECT1†	WD INPUT SELECT0†	—	T1 INPUT SELECT2	T1 INPUT SELECT1	T1 INPUT SELECT0	T1CTL1
P04A	WD OVRFL RST ENA†	WD OVRFL INT ENA	WD OVRFL INT FLAG	T1 OVRFL INT ENA	T1 OVRFL INT FLAG	—	—	T1 SW RESET	T1CTL2
	Mode: Dual-Compare								
P04B	T1EDGE INT FLAG	T1C2 INT FLAG	T1C1 INT FLAG	—	—	T1EDGE INT ENA	T1C2 INT ENA	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 0	T1C1 OUT ENA	T1C2 OUT ENA	T1C1 RST ENA	T1CR OUT ENA	T1EDGE POLARITY	T1CR RST ENA	T1EDGE DET ENA	T1CTL4
	Mode: Capture/Compare								
P04B	T1EDGE INT FLAG	—	T1C1 INT FLAG	—	—	T1EDGE INT ENA	—	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 1	T1C1 OUT ENA	—	T1C1 RST ENA	—	T1EDGE POLARITY	—	T1EDGE DET ENA	T1CTL4
	Modes: Capture / Compare and Dual-Compare								
P04D	—	—	—	—	T1EVT DATA IN	T1EVT DATA OUT	T1EVT FUNCTION	T1EVT DATA DIR	T1PC1
P04E	T1PWM DATA IN	T1PWM DATA OUT	T1PWM FUNCTION	T1PWM DATA DIR	T1IC/CR DATA IN	T1IC/CR DATA OUT	T1IC/CR FUNCTION	T1IC/CR DATA DIR	T1PC2
P04F	**T1 STEST**	**T1 PRIORITY**	—	—	—	—	—	—	T1PRI

† Once the WD OVRFL RST ENA bit is set, these bits cannot be changed until a reset; this applies only to the standard watchdog and to simple counter. In the hard watchdog, these bits can be modified at any time; the WD INPUT SELECT2 bits are ignored.

timer 1 (T1) module (continued)

The T1 capture/compare-mode block diagram is illustrated in Figure 6. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T1CTL2.0 is 104Ah, bit 0, in the T1CTL2 register.

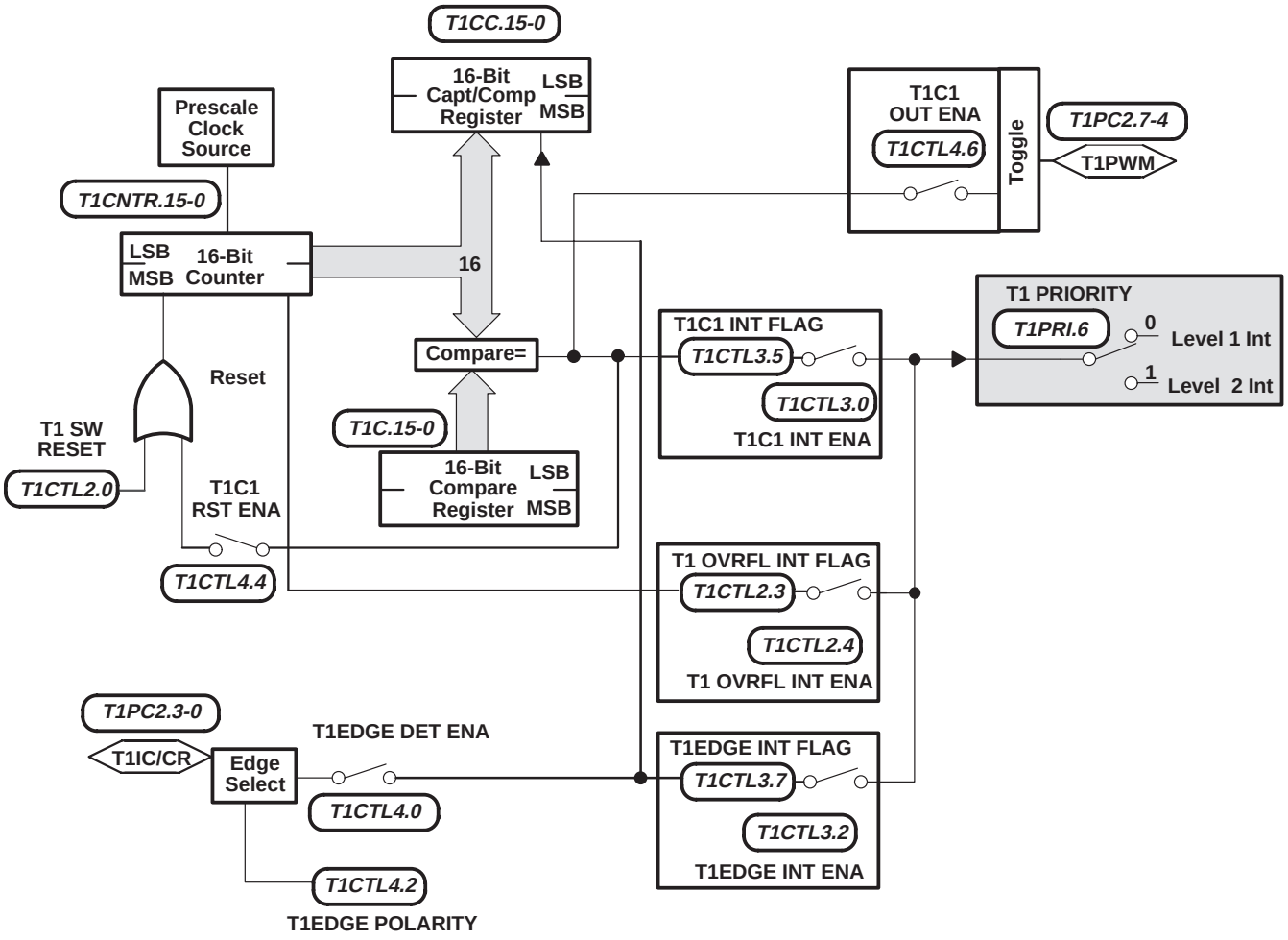


Figure 6. Capture/Compare Mode

timer 1 (T1) module (continued)

The T1 dual-compare mode block diagram is illustrated in Figure 7. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T1CTL2.0 is 104Ah, bit 0, in the T1CTL2 register.

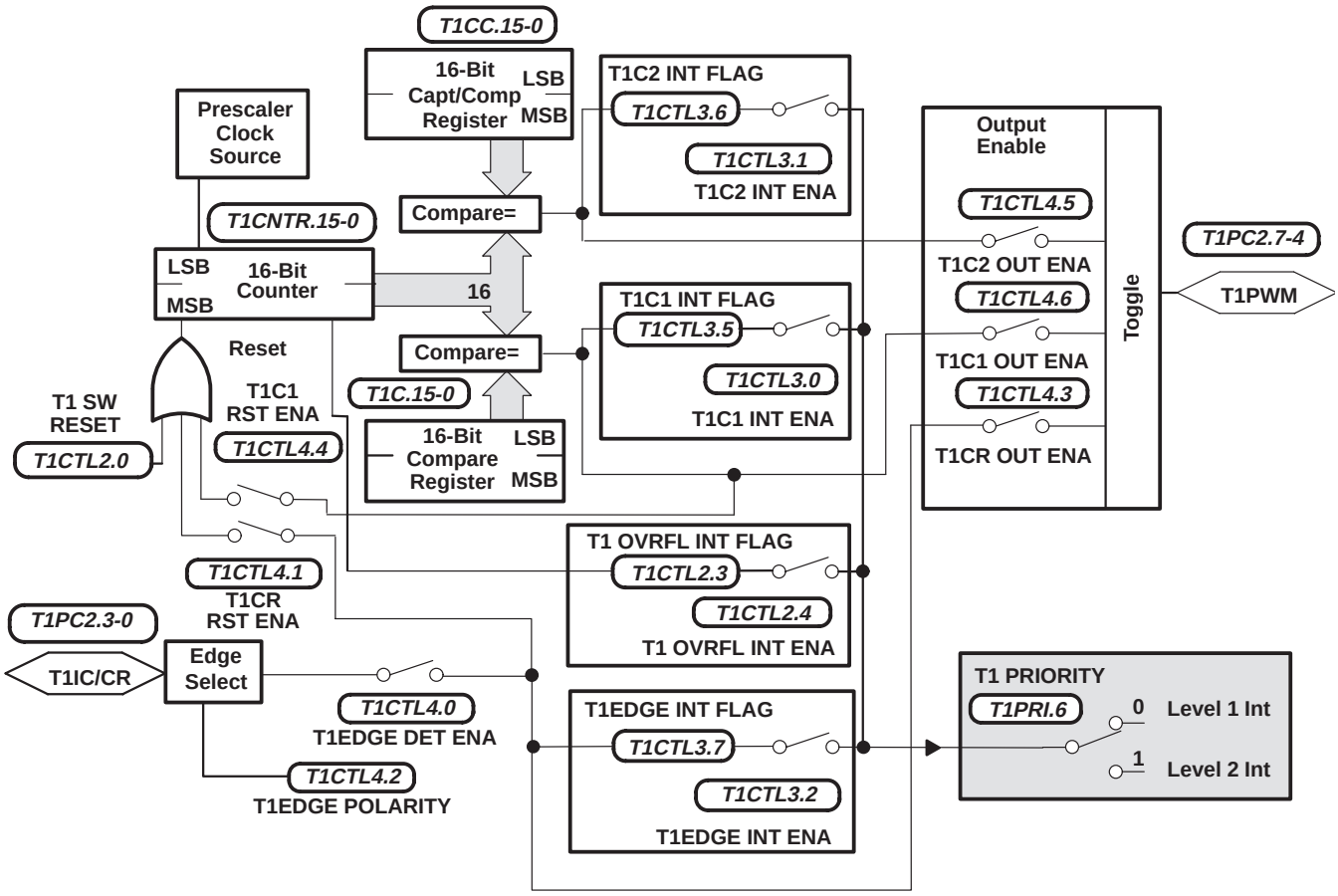


Figure 7. Dual-Compare Mode

timer 1 (T1) module (continued)

The TMS370Cx7x device includes a 24-bit watchdog (WD) timer, contained in the T1 module, which can be software programmed as an event counter, pulse accumulator, or interval timer if the WD function is not used. The WD function is to monitor software and hardware operation, and it implements a system reset when the WD counter is not serviced properly (WD counter overflow or WD counter is reinitialized by an incorrect value). The WD can be configured as one of the three mask options: standard WD, hard WD, or simple counter.

- Standard watchdog configuration for EPROM and mask-ROM devices (see Figure 8)
  - Watchdog
    - Ten different WD overflow rates ranging from 6.55 ms to 3.35 s at 5-MHz SYSCLK
    - A WD reset key (WDRST) register is used to clear the watchdog counter (WDCNTR) when a correct value is written.
    - Generates a system reset if an incorrect value is written to the WD reset key or if the counter overflows
    - A WD overflow flag (WD OVRFL INT FLAG) bit that indicates whether the WD timer initiated a system reset
  - Non-watchdog
    - Watchdog timer can be configured as an event counter, pulse accumulator, or an interval timer

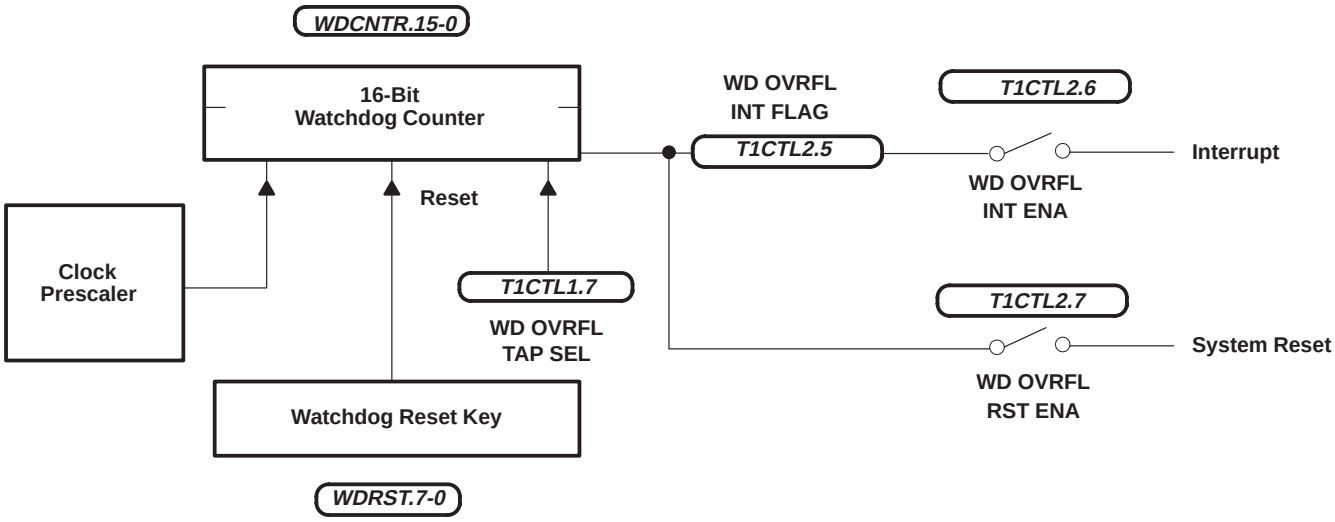


Figure 8. Standard Watchdog

timer 1 (T1) module (continued)

- Hard watchdog configuration for mask-ROM device (see Figure 9)
  - Eight different WD overflow rates ranging from 26.2 ms to 3.35 s at 5-MHz SYSCLK
  - A WD reset key (WDRST) register is used to clear the watchdog counter (WDCNTR) when a correct value is written.
  - Generates a system reset if an incorrect value is written to the watchdog reset key or if the counter overflows
  - Automatic activation of the WD timer upon power-up reset
  - INT1 is enabled as nonmaskable interrupt during low-power modes
  - A WD overflow flag (WD OVRFL INT FLAG) bit that indicates whether the WD timer initiated a system reset

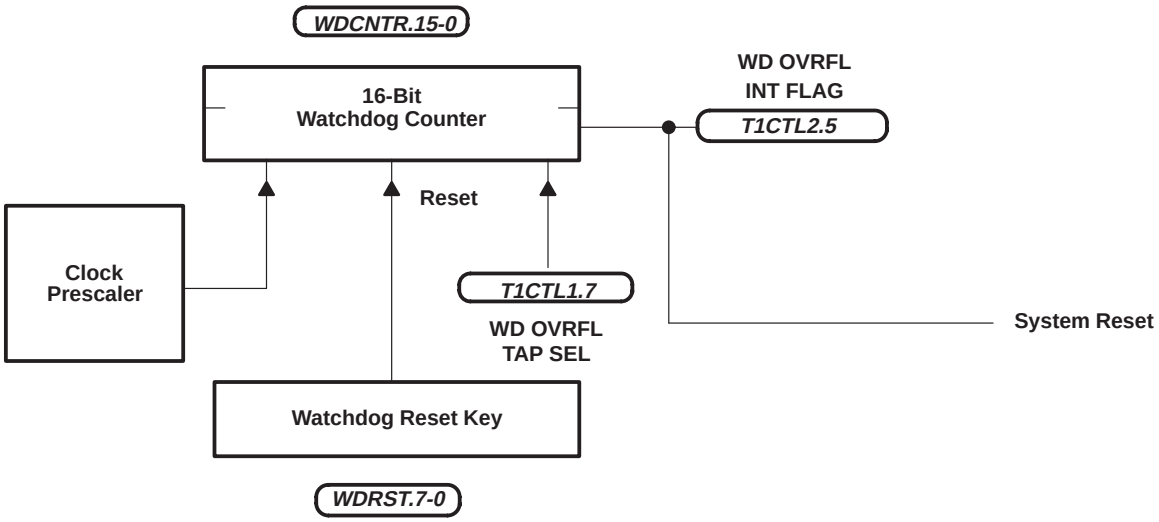


Figure 9. Hard Watchdog

timer 1 (T1) module (continued)

- Simple-counter configuration for mask-ROM devices only (see Figure 10)
  - Simple counter can be configured as an event counter, pulse accumulator, or an interval timer.

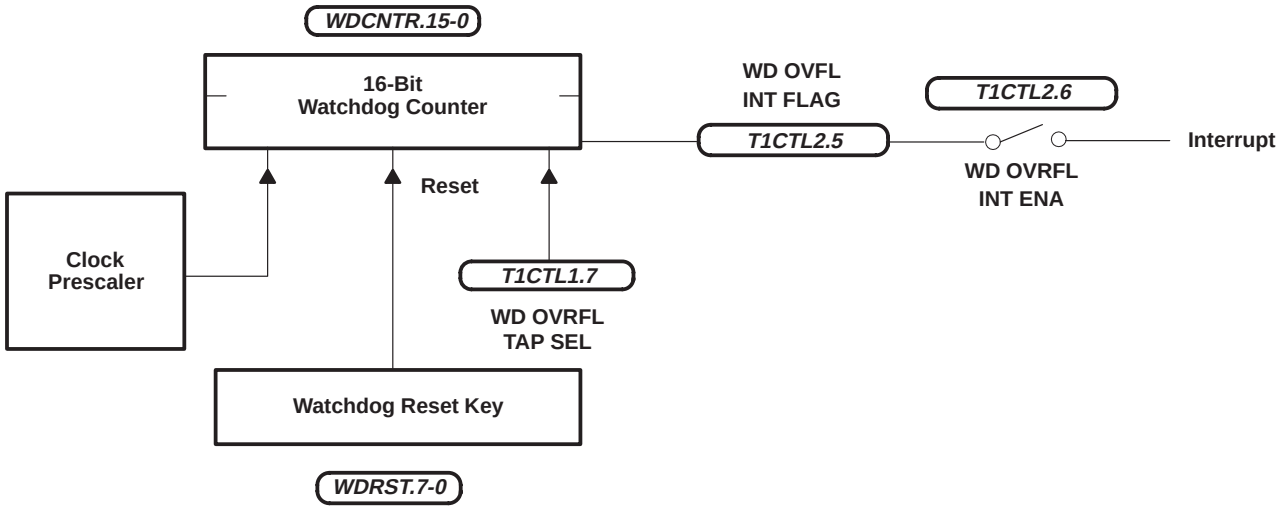


Figure 10. Simple Counter

timer 2A (T2A) module

The 16-bit general-purpose timer 2A (T2A) module is composed of a 16-bit resettable counter, 16-bit compare register with associated compare logic, 16-bit capture register, and a 16-bit register that functions as a capture register in one mode and as a compare register in the other mode. The T2A module adds an additional timer that provides event count, input capture, and compare functions. The T2A module includes three external device pins that can be dedicated as timer functions or used as general-purpose I/O pins. The T2A module block diagram is shown in Figure 11.

timer 2A (T2A) module (continued)

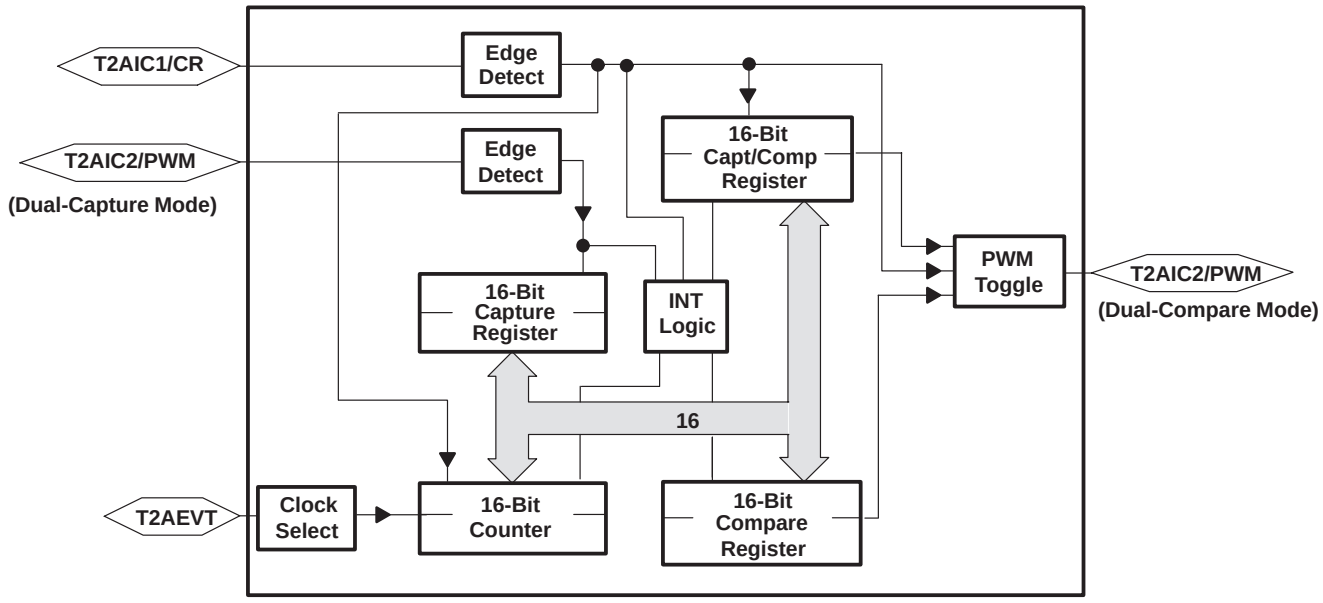


Figure 11. Timer 2A Block Diagram

The T2A module features include the following:

- Three T2A I/O pins:
  - T2AIC1/CR: T2A input capture 1/counter reset input pin, or general-purpose bidirectional I/O pin
  - T2AIC2/PWM: T2A input capture 2/pulse-width-modulation (PWM) output pin, or general-purpose bidirectional I/O pin
  - T2AEVT: T2A event input pin, or general-purpose bidirectional I/O pin
- Two operation modes:
  - Dual-compare mode: Provides PWM signal
  - Dual-capture mode: Provides input capture pin
- One 16-bit general-purpose resettable counter
- One 16-bit compare register with associated compare logic
- One 16-bit capture register with associated capture logic
- One 16-bit capture/compare register, which, depending on the mode of operation, operates as either a capture or compare register
- T2A clock sources can be any of the following:
  - System clock
  - No clock (the counter is stopped)
  - External clock synchronized to the system clock (event counter)
  - System clock while external input is high (pulse accumulation)

timer 2A (T2A) module (continued)

- Selectable edge-detection circuitry that, depending on the mode of operation, senses active transitions on the input capture pins (T2AIC1/CR)
- Interrupts that can be generated on the occurrence of:
  - A compare equal to dedicated-compare register
  - A compare equal to capture-compare register
  - A counter overflow
  - An external edge 1 detection
  - An external edge 2 detection
- Fourteen T2A module control registers located in the PF frame beginning at address P060

The T2A module control registers are listed in Table 15.

Table 15. Timer 2A Module Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
	Modes: Dual-Compare and Dual-Capture								
P060	Bit 15			T2A Counter MSbyte				Bit 8	T2ACNTR
P061	Bit 7			T2A Counter LSbyte				Bit 0	
P062	Bit 15			Compare Register MSbyte				Bit 8	T2AC
P063	Bit 7			Compare Register LSbyte				Bit 0	
P064	Bit 15			Capture/Compare Register MSbyte				Bit 8	T2ACC
P065	Bit 7			Capture/Compare Register LSbyte				Bit 0	
P066	Bit 15			Capture Register 2 MSbyte				Bit 8	T2AIC
P067	Bit 7			Capture Register 2 LSbyte				Bit 0	
P06A	—	—	—	T2A OVRFL INT ENA	T2A OVRFL INT FLAG	T2A INPUT SELECT1	T2A INPUT SELECT0	T2A SW RESET	T2ACTL1
	Mode: Dual-Compare								
P06B	T2AEDGE1 INT FLAG	T2AC2 INT FLAG	T2AC1 INT FLAG	—	—	T2AEDGE1 INT ENA	T2AC2 INT ENA	T2AC1 INT ENA	T2ACTL2
P06C	T2A MODE = 0	T2AC1 OUT ENA	T2AC2 OUT ENA	T2AC1 RST ENA	T2AEDGE1 OUT ENA	T2AEDGE1 POLARITY	T2AEDGE1 RST ENA	T2AEDGE1 DET ENA	T2ACTL3
	Mode: Dual-Capture								
P06B	T2AEDGE1 INT FLAG	T2AEDGE2 INT FLAG	T2AC1 INT FLAG	—	—	T2AEDGE1 INT ENA	T2AEDGE2 INT ENA	T2AC1 INT ENA	T2ACTL2
P06C	T2A MODE = 1	—	—	T2AC1 RST ENA	T2AEDGE2 POLARITY	T2AEDGE1 POLARITY	T2AEDGE2 DET ENA	T2AEDGE1 DET ENA	T2ACTL3
	Modes: Dual-Compare and Dual-Capture								
P06D	—	—	—	—	T2AEVT DATA IN	T2AEVT DATA OUT	T2AEVT FUNCTION	T2AEVT DATA DIR	T2APC1
P06E	T2AIC2/PWM DATA IN	T2AIC2/PWM DATA OUT	T2AIC2/PWM FUNCTION	T2AIC2/PWM DATA DIR	T2AIC1/CR DATA IN	T2AIC1/CR DATA OUT	T2AIC1/CR FUNCTION	T2AIC/CR DATA DIR	T2APC2
P06F	**T2A STEST**	**T2A PRIORITY**	—	—	—	—	—	—	T2APRI

timer 2A (T2A) module (continued)

The timer 2A dual-compare mode block diagram is illustrated in Figure 12. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T2ACTL2.0 is 106Bh, bit 0, in the T2ACTL2 register.

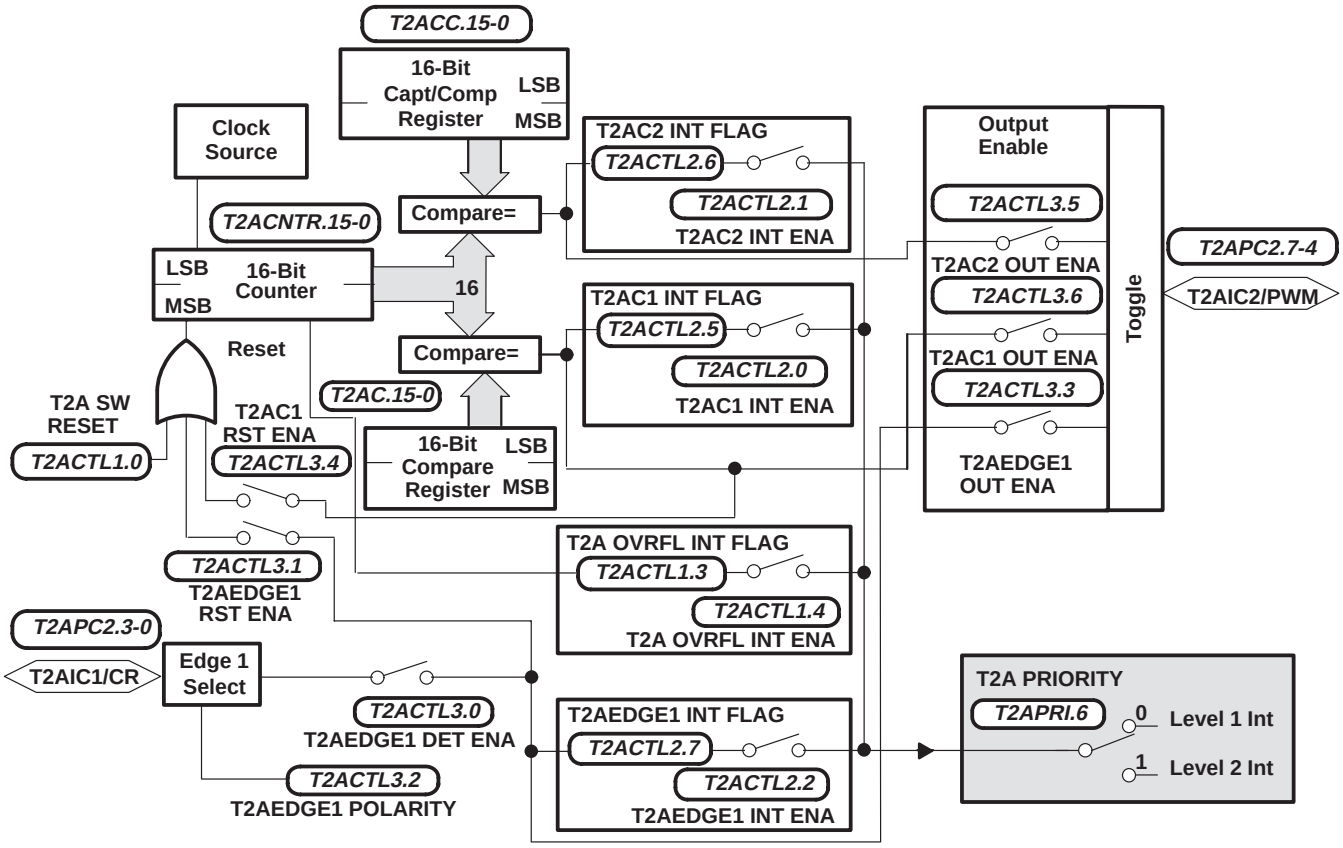


Figure 12. Dual-Compare Mode

timer 2A (T2A) module (continued)

The timer 2A dual-capture mode block diagram is illustrated in Figure 13. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T2ACTL2.0 is 106Bh, bit 0, in the T2ACTL2 register.

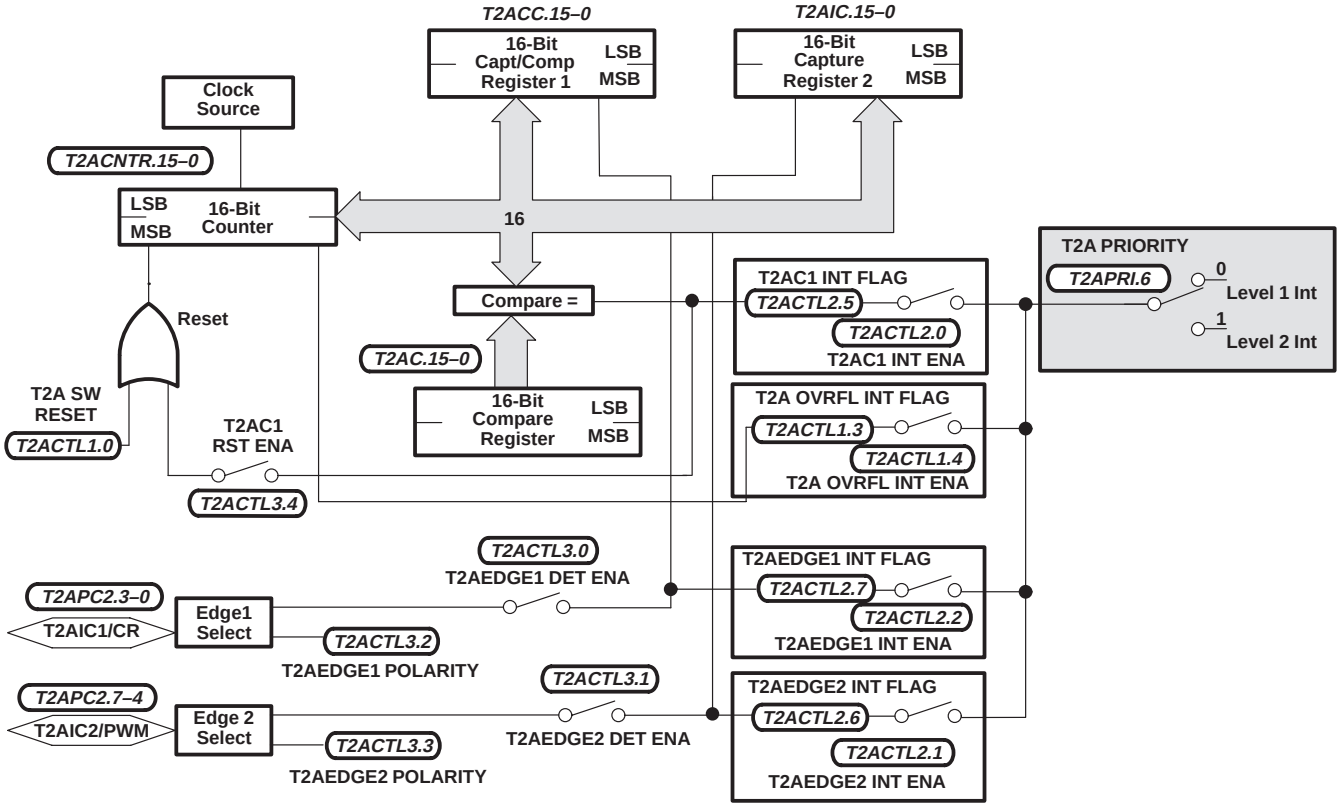


Figure 13. Dual-Capture Mode

analog-to-digital converter 1 (ADC1) module

The analog-to-digital converter 1 (ADC1) module is an 8-bit, successive approximation converter with internal sample-and-hold circuitry. The module has eight multiplexed analog input channels that allow the processor to convert the voltage levels from up to eight different sources. The ADC1 module features include the following:

- Minimum conversion time: 32.8 μs at 5-MHz SYSCLK
- Ten external pins:
  - Eight analog input channels (AN0–AN7), any of which can be software configured as digital inputs (E0–E7) if not needed as analog channels. AN1–AN7 also can be configured as positive input voltage reference.
  - V_{CC3}: ADC1 module high-voltage reference input
  - V_{SS3}: ADC1 module low-voltage reference input
- The ADDATA register which contains the digital result of the last ADC1 conversion
- ADC1 operations can be accomplished through either interrupt driven or polled algorithms
- Six ADC1 module control registers are located in the control register frame beginning at address 1070h.

The ADC1 module control registers are listed in Table 16.

Table 16. ADC1 Module Control Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P070	CONVERT START	SAMPLE START	REF VOLT SELECT2	REF VOLT SELECT1	REF VOLT SELECT0	AD INPUT SELECT2	AD INPUT SELECT1	AD INPUT SELECT0	ADCTL
P071	—	—	—	—	—	AD READY	AD INT FLAG	AD INT ENA	ADSTAT
P072	A/D Conversion Data Register								ADDATA
P073 to P07C	Reserved								
P07D	Port E Data Input Register								ADIN
P07E	Port E Input Enable Register								ADENA
P07F	**AD STEST**	**AD PRIORITY**	**AD ESPEN**	—	—	—	—	—	ADPRI

analog-to-digital converter 1 (ADC1) module (continued)

The ADC1 module block diagram is illustrated in Figure 14.

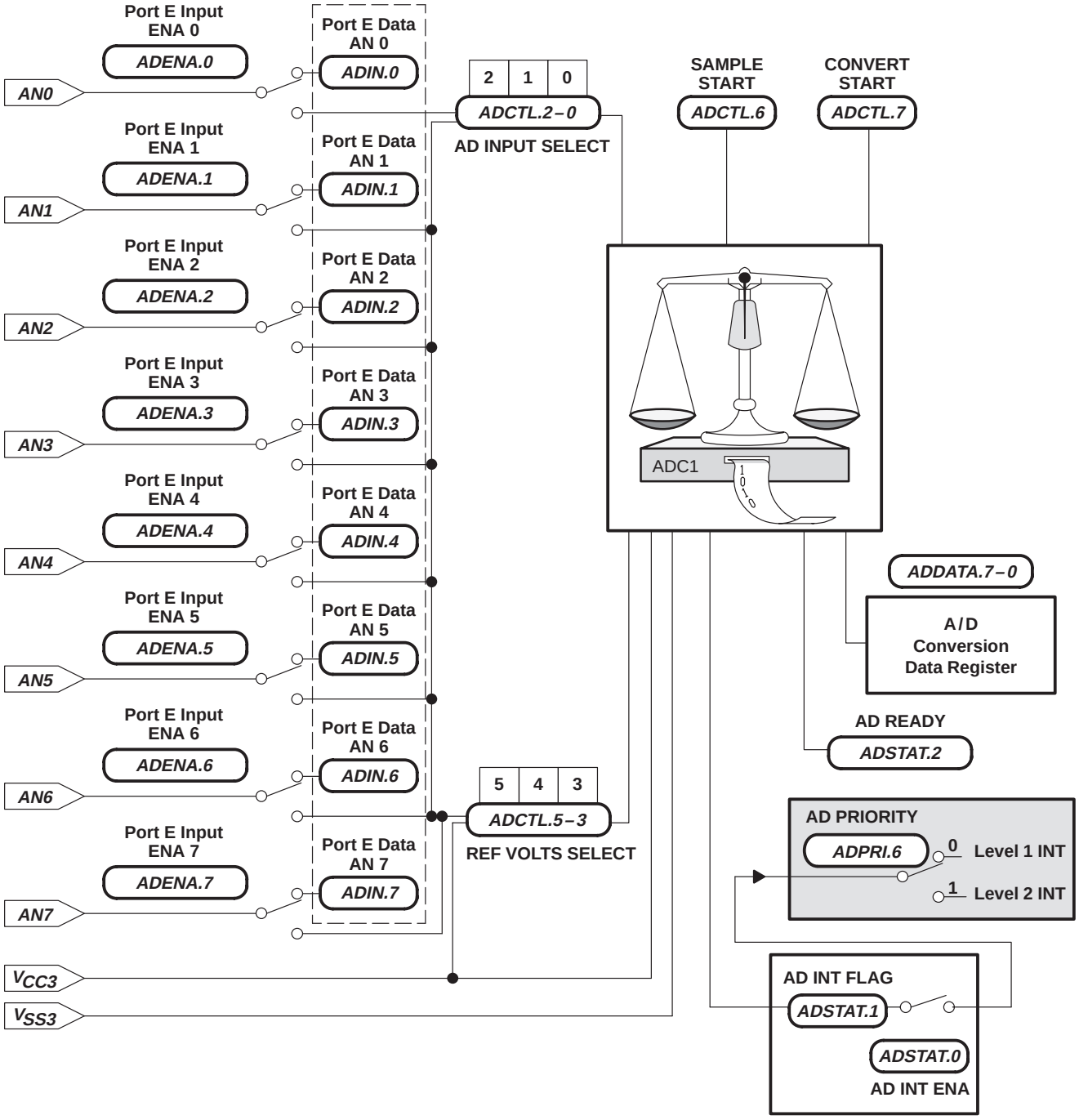


Figure 14. ADC1 Block Diagram

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instruction set overview

Table 17 provides an opcode-to-instruction cross reference of all 73 instructions and 274 opcodes of the ‘370Cx7x instruction set. The numbers at the top of this table represent the most significant nibble of the opcode while the numbers at the left side of the table represent the least significant nibble. The instruction of these two opcode nibbles contains the mnemonic, operands, and byte/cycle particular to that opcode.

For example, the opcode B5h points to the CLR A instruction. This instruction contains one byte and executes in eight SYSCLK cycles.

Table 17. TMS370 Family Opcode/Instruction Map†

LSN \ MSN	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	JMP #ra 2/7							INCW #ra,Rd 3/11	MOV Ps,A 2/8			CLRC / TST A 1/9	MOV A,B 1/9	MOV A,Rd 2/7	TRAP 15 1/14	LDST n 2/6
1	JN ra 2/5		MOV A,Pd 2/8			MOV B,Pd 2/8		MOV Rs,Pd 3/10		MOV Ps,B 2/7				MOV B,Rd 2/7	TRAP 14 1/14	MOV #ra[SP],A 2/7
2	JZ ra 2/5	MOV Rs,A 2/7	MOV #n,A 2/6	MOV Rs,B 2/7	MOV Rs,Rd 3/9	MOV #n,B 2/6	MOV B,A 1/8	MOV #n,Rd 3/8			MOV Ps,Rd 3/10	DEC A 1/8	DEC B 1/8	DEC Rd 2/6	TRAP 13 1/14	MOV A,*ra[SP] 2/7
3	JC ra 2/5	AND Rs,A 2/7	AND #n,A 2/6	AND Rs,B 2/7	AND Rs,Rd 3/9	AND #n,B 2/6	AND B,A 1/8	AND #n,Rd 3/8	AND A,Pd 2/9	AND B,Pd 2/9	AND #n,Pd 3/10	INC A 1/8	INC B 1/8	INC Rd 2/6	TRAP 12 1/14	CMP *n[SP],A 2/8
4	JP ra 2/5	OR Rs,A 2/7	OR #n,A 2/6	OR Rs,B 2/7	OR Rs,Rd 3/9	OR #n,B 2/6	OR B,A 1/8	OR #n,Rd 3/8	OR A,Pd 2/9	OR B,Pd 2/9	OR #n,Pd 3/10	INV A 1/8	INV B 1/8	INV Rd 2/6	TRAP 11 1/14	extend inst,2 opcodes
5	JPZ ra 2/5	XOR Rs,A 2/7	XOR #n,A 2/6	XOR Rs,B 2/7	XOR Rs,Rd 3/9	XOR #n,B 2/6	XOR B,A 1/8	XOR #n,Rd 3/8	XOR A,Pd 2/9	XOR B,Pd 2/9	XOR #n,Pd 3/10	CLR A 1/8	CLR B 1/8	CLR Rn 2/6	TRAP 10 1/14	
6	JNZ ra 2/5	BTJO Rs,A,ra 3/9	BTJO #n,A,ra 3/8	BTJO Rs,B,ra 3/9	BTJO Rs,Rd,ra 4/11	BTJO #n,B,ra 3/8	BTJO B,A,ra 2/10	BTJO #n,Rd,ra 4/10	BTJO A,Pd,ra 3/11	BTJO B,Pd,ra 3/10	BTJO #n,Pd,ra 4/11	XCHB A 1/10	XCHB A / TST B 1/10	XCHB Rn 2/8	TRAP 9 1/14	IDLE 1/6
7	JNC ra 2/5	BTJZ Rs.,A,ra 3/9	BTJZ #n,A,ra 3/8	BTJZ Rs,B,ra 3/9	BTJZ Rs,Rd,ra 4/11	BTJZ #n,B,ra 3/8	BTJZ B,A,ra 2/10	BTJZ #n,Rd,ra 4/10	BTJZ A,Pd,ra 3/10	BTJZ B,Pd,ra 3/10	BTJZ #n,Pd,ra 4/11	SWAP A 1/11	SWAP B 1/11	SWAP Rn 2/9	TRAP 8 1/14	MOV #n,Pd 3/10
8	JV ra 2/5	ADD Rs,A 2/7	ADD #n,A 2/6	ADD Rs,B 2/7	ADD Rs,Rd 3/9	ADD #n,B 2/6	ADD B,A 1/8	ADD #n,Rd 3/8	MOVW #16,Rd 4/13	MOVW Rs,Rd 3/12	MOVW #16[B],Rpd 4/15	PUSH A 1/9	PUSH B 1/9	PUSH Rd 2/7	TRAP 7 1/14	SETC 1/7
9	JL ra 2/5	ADC Rs,A 2/7	ADC #n,A 2/6	ADC Rs,B 2/7	ADC Rs,Rd 3/9	ADC #n,B 2/6	ADC B,A 1/8	ADC #n,Rd 3/8	JMPL lab 3/9	JMPL *Rp 2/8	JMPL *lab[B] 3/11	POP A 1/9	POP B 1/9	POP Rd 2/7	TRAP 6 1/14	RTS 1/9
A	JLE ra 2/5	SUB Rs,A 2/7	SUB #n,A 2/6	SUB Rs,B 2/7	SUB Rs,Rd 3/9	SUB #n,B 2/6	SUB B,A 1/8	SUB #n,Rd 3/8	MOV & lab,A 3/10	MOV *Rp,A 2/9	MOV *lab[B],A 3/12	DJNZ A,#ra 2/10	DJNZ B,#ra 2/10	DJNZ Rd,#ra 3/8	TRAP 5 1/14	RTI 1/12
B	JHS ra 2/5	SBB Rs,A 2/7	SBB #n,A 2/6	SBB Rs,B 2/7	SBB Rs,Rd 3/9	SBB #n,B 2/6	SBB B,A 1/8	SBB #n,Rd 3/8	MOV A, & lab 3/10	MOV A, *Rp 2/9	MOV A,*lab[B] 3/12	COMPL A 1/8	COMPL B 1/8	COMPL Rd 2/6	TRAP 4 1/14	PUSH ST 1/8

† All conditional jumps (opcodes 01–0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

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Table 17. TMS370 Family Opcode/Instruction Map† (Continued)

LSN \ MSN	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
C	JNV ra 2/5	MPY Rs,A 2/46	MPY #n,A 2/45	MPY Rs,B 2/46	MPY Rs,Rd 3/48	MPY #n,B 2/45	MPY B,A 1/47	MPY #n,Rs 3/47	BR lab 3/9	BR *Rp 2/8	BR *lab[B] 3/11	RR A 1/8	RR B 1/8	RR Rd 2/6	TRAP 3 1/14	POP ST 1/8
D	JGE ra 2/5	CMP Rs,A 2/7	CMP #n,A 2/6	CMP Rs,B 2/7	CMP Rs,Rd 3/9	CMP #n,B 2/6	CMP B,A 1/8	CMP #n,Rd 3/8	CMP & lab,A 3/11	CMP *Rp,A 2/10	CMP *lab[B],A 3/13	RRC A 1/8	RRC B 1/8	RRC Rd 2/6	TRAP 2 1/14	LDSP 1/7
E	JG ra 2/5	DAC Rs,A 2/9	DAC #n,A 2/8	DAC Rs,B 2/9	DAC Rs,Rd 3/11	DAC #n,B 2/8	DAC B,A 1/10	DAC #n,Rd 3/10	CALL lab 3/13	CALL *Rp 2/12	CALL *lab[B] 3/15	RL A 1/8	RL B 1/8	RL Rd 2/6	TRAP 1 1/14	STSP 1/8
F	JLO ra 2/5	DSB Rs,A 2/9	DSB #n,A 2/8	DSB Rs,B 2/9	DSB Rs,Rd 3/11	DSB #n,B 2/8	DSB B,A 1/10	DSB #n,Rd 3/10	CALLR lab 3/15	CALLR *Rp 2/14	CALLR *lab[B] 3/17	RLC A 1/8	RLC B 1/8	RLC Rd 2/6	TRAP 0 1/14	NOP 1/7

Second byte of two-byte instructions (F4xx):			
F4	8	MOVW *n[Rn] 4/15	DIV Rn.A 3/14-63
F4	9	JMPL *n[Rn] 4/16	
F4	A	MOV *n[Rn],A 4/17	
F4	B	MOV A,*n[Rn] 4/16	
F4	C	BR *n[Rn] 4/16	
F4	D	CMP *n[Rn],A 4/18	
F4	E	CALL *n[Rn] 4/20	
F4	F	CALLR *n[Rn] 4/22	

Legend:

*	=	Indirect addressing operand prefix
&	=	Direct addressing operand prefix
#	=	immediate operand
#16	=	immediate 16-bit number
lab	=	16-label
n	=	immediate 8-bit number
Pd	=	Peripheral register containing destination type
Pn	=	Peripheral register
Ps	=	Peripheral register containing source byte
ra	=	Relative address
Rd	=	Register containing destination type
Rn	=	Register file
Rp	=	Register pair
Rpd	=	Destination register pair
Rps	=	Source Register pair
Rs	=	Register containing source byte

† All conditional jumps (opcodes 01–0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

development system support

The TMS370 family development support tools include an assembler, a C compiler, a linker, compact development tool, and an EEPROM/UVEPROM programmer.

- Assembler/linker (Part No. TMDS3740850–02 for PC)
  - Includes extensive macro capability
  - Provides high-speed operation
  - Provides format conversion utilities for popular formats
- ANSI C compiler (Part No. TMDS3740855–02 for PC, Part No. TMDS3740555–09 for HP700™, Sun-3™, or Sun-4™)
  - Generates assembly code for the TMS370 that can be easily inspected
  - Improves code execution speed and reduces code size with optional optimizer pass
  - Enables direct referencing of the TMS370's port registers by using a naming convention
  - Provides flexibility in specifying the storage for data objects
  - Interfaces C functions and assembly functions easily
  - Includes assembler and linker
- CDT370 (compact development tool) Timer real-time in-circuit emulation
  - Base (Part Number EDSCDT37T – for PC, requires cable)
    - Cable for 68-pin PLCC (Part No. EDSTRG68PLCC)
    - Cable for 64-pin SDIP (Part No. EDSTRG64SDIL)
  - Includes EEPROM and EPROM programming support
  - Allows inspection and modification of memory locations
  - Uploads/downloads program and data memory
  - Executes programs and software routines
  - Includes 1024 samples trace buffer
  - Includes single-step executable instructions
  - Uses software breakpoints to halt program execution at selected address
- Microcontroller programmer
  - Base (Part No. TMDS3760500A — for PC, requires programmer head)
    - Single unit head for 68-pin PLCC (Part No. TMDS3780510A)
    - Single unit head for 64-pin SDIP (Part No. TMDS3780511A)
  - Includes PC-based, window/function-key oriented user interface for ease of use and rapid learning environment

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Sun-3 and Sun-4 are trademarks of Sun Microsystems, Inc.

development system support (continued)

- Starter Kit (Part No. TMDS37000 — for PC)
  - Includes TMS370 assembler diskette and documentation
  - Includes TMS370 simulator
  - Includes programming adapter board and programming software
  - Not included (to be supplied by the user):
    - + 5 V power supply
    - ZIF sockets
    - 9-pin RS232 cable

device numbering conventions

Figure 15 illustrates the numbering and symbol nomenclature for the TMS370Cx7x family.

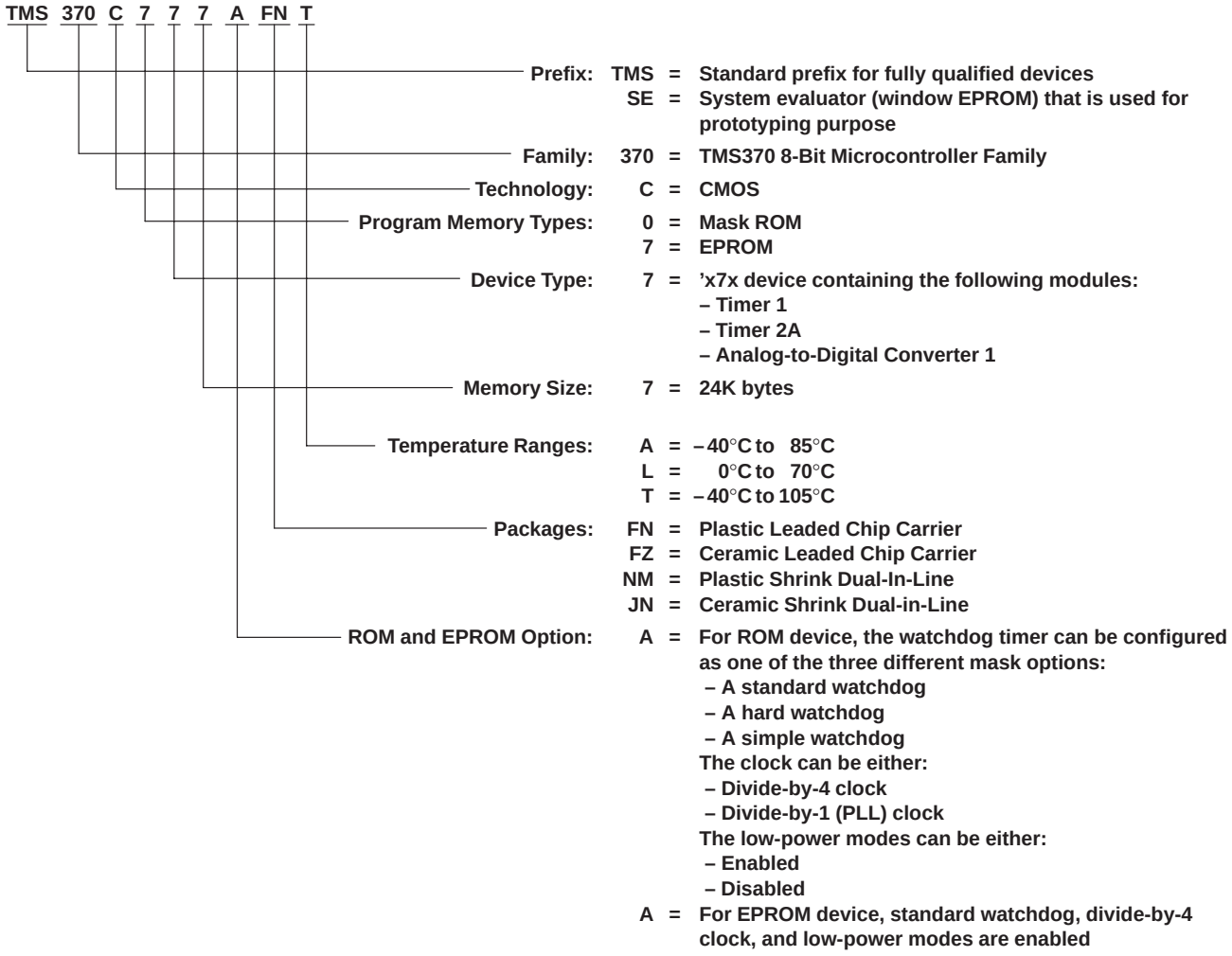


Figure 15. TMS370Cx7x Family Nomenclature

device part numbers

Table 18 lists all the TMS370Cx7x devices available. The device part-number nomenclature is designed to assist ordering. Upon ordering, the customer must specify not only the device part number, but also the clock and watchdog-timer options desired. Each device can have only one of the three possible watchdog-timer options and one of the two clock options. The options to be specified pertain solely to orders involving ROM devices.

Table 18. Device Part Numbers

DEVICE PART NUMBERS FOR 68 PINS (LCC)	DEVICE PART NUMBERS FOR 64 PINS (DIP)
TMS370C077AFNA TMS370C077AFNL TMS370C077AFNT	TMS370C077ANMA TMS370C077ANML TMS370C077ANMT
TMS370C777AFNT	TMS370C777ANMT
SE370C777AFZT†	SE370C777AJNT†

† System evaluators are for use only in prototype environment, and their reliability has not been characterized.

new code release form

Figure 16 shows a sample of the new code release form.

NEW CODE RELEASE FORM
TEXAS INSTRUMENTS
TMS370 MICROCONTROLLER PRODUCTS

DATE: _____

To release a new customer algorithm to TI incorporated into a TMS370 family microcontroller, complete this form and submit with the following information:

1. A ROM description in object form on Floppy Disk, Modem XFR, or EPROM (Verification file will be returned via same media)
2. An attached specification if not using TI standard specification as incorporated in TI's applicable device data book.

Company Name: _____
Street Address: _____
Street Address: _____
City: _____ State _____ Zip _____

Customer Part Number: _____
Customer Application: _____

TMS370 Device: _____

TI Customer ROM Number: _____
(provided by Texas Instruments)

OSCILLATOR FREQUENCY

	MIN	TYP	MAX
[] External Drive (CLKIN)	_____	_____	_____
[] Crystal	_____	_____	_____
[] Ceramic Resonator	_____	_____	_____

[] Supply Voltage MIN: _____ MAX: _____
(std range: 4.5V to 5.5V)

TEMPERATURE RANGE
[] 'L': 0° to 70°C (standard)
[] 'A': –40° to 85°C
[] 'T': –40° to 105°C

SYMBOLIZATION
[] TI standard symbolization
[] TI standard w/customer part number
[] Customer symbolization
(per attached spec, subject to approval)

Contact Mr./Ms.: _____
Phone: (_____)_____ Ext.: _____

Customer Purchase Order Number: _____

Customer Print Number *Yes:____ # _____
No: ___ (Std. spec to be followed)
*If Yes: Customer must provide "print" to TI w/NCRF for approval before ROM code processing starts.

CONTACT OPTIONS FOR THE 'A' VERSION TMS370 MICROCONTROLLERS

Low Power Modes	Watchdog counter	Clock Type
[] Enabled	[] Standard	[] Standard (/4)
[] Disabled	[] Hard Enabled	[] PLL (/1)
	[] Simple Counter	

NOTE:
Non 'A' version ROM devices of the TMS370 microcontrollers will have the "Low-power modes Enabled", "Divide-by-4" Clock, and "Standard" Watchdog options. See the *TMS370 Family User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (literature number SPNS014B).

PACKAGE TYPE
[] 'N' 28-pin PDIP
[] "FN" 28-pin PLCC
[] "N" 40-pin PDIP
[] "NJ" 40-pin PSDIP (formerly known as N2)
[] "FN" 44-pin PLCC
[] "FN" 68-pin PLCC
[] "NM" 64-pin PSDIP

BUS EXPANSION
[] YES [] NO

NON-STANDARD SPECIFICATIONS:
ALL NON-STANDARDS SPECIFICATIONS MUST BE APPROVED BY THE TI ENGINEERING STAFF: If the customer requires expedited production material (i.e., product which must be started in process prior to prototype approval and full production release) and non-standard spec issues are not resolved to the satisfaction of both the customer and TI in time for a scheduled shipment, the specification parameters in question will be processed/tested to the standard TI spec. Any such devices which are shipped without conformance to a mutually approved spec, will be identified by a 'P' in the symbolization preceding the TI part number.

RELEASE AUTHORIZATION:
This document, including any referenced attachments, is and will be the controlling document for all orders placed for this TI custom device. Any changes must be in writing and mutually agreed to by both the customer and TI. The prototype cycletime commences when this document is signed off and the verification code is approved by the customer.

1. Customer: _____ Date: _____

2. TI: Field Sales: _____
Marketing: _____
Prod. Eng.: _____
Proto. Release: _____

Figure 16. Sample New Code Release Form

Table 19 is a collection of all the peripheral file frames using the 'Cx7x (provided for a quick reference).

Table 19. Peripheral File Frame Compilation

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
	System Configuration Registers								
P010	COLD START	**OSC POWER**	**PF AUTO WAIT**	OSC FLT FLAG	MC PIN WPO	MC PIN DATA	—	µP/µC MODE	SCCR0
P011		—	—	**AUTOWAIT DISABLE**	—	**MEMORY DISABLE**	—	—	SCCR1
P012	**HALT/ STANDBY**	**PWRDWN/ IDLE**	—	**BUS STEST**	**CPU STEST**	—	**INT1 NMI**	**PRIVILEGE DISABLE**	SCCR2
P013 to P016	Reserved								
P017	INT1 FLAG	INT1 PIN DATA	—	—	—	INT1 POLARITY	INT1 PRIORITY	INT1 ENABLE	INT1
P018	INT2 FLAG	INT2 PIN DATA	—	INT2 DATA DIR	INT2 DATA OUT	INT2 POLARITY	INT2 PRIORITY	INT2 ENABLE	INT2
P019	INT3 FLAG	INT3 PIN DATA	—	INT3 DATA DIR	INT3 DATA OUT	INT3 POLARITY	INT3 PRIORITY	INT3 ENABLE	INT3
P01A	BUSY	—	—	—	—	AP	W1W0	EXE	DEECTL
P01B	Reserved								
P01C	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTLM
P01D	Reserved								
P01E	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTLL
P01F	Reserved								
	Digital Port Control Registers								
P020	Reserved								APORT1
P021	Port A Control Register 2								APORT2
P022	Port A Data								ADATA
P023	Port A Direction								ADIR
P024	Reserved								BPORT1
P025	Port B Control Register 2								BPORT2
P026	Port B Data								BDATA
P027	Port B Direction								BDIR
P028	Reserved								CPORT1
P029	Port C Control Register 2								CPORT2
P02A	Port C Data								CDATA
P02B	Port C Direction								CDIR
P02C	Port D Control Register 1								DPORT1
P02D	Port D Control Register 2†								DPORT2
P02E	Port D Data								DDATA
P02F	Port D Direction								DDIR
P030 to P035	Reserved								
P036	—	—	Port G Data						GDATA
P037	—	—	Port G Direction						GDIR

† To configure pin D3 as SYSCLK, set port D control register 2 = 08h.

Table 19. Peripheral File Frame Compilation (Continued)

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
	Timer 1 Module Register								
	Modes: Capture / Compare and Dual-Compare								
P040	Bit 15	T1 Counter MSbyte						Bit 8	T1CNTR
P041	Bit 7	T1 Counter LSbyte						Bit 0	
P042	Bit 15	Compare Register MSbyte						Bit 8	T1C
P043	Bit 7	Compare Register LSbyte						Bit 0	
P044	Bit 15	Capture/Compare Register MSbyte						Bit 8	T1CC
P045	Bit 7	Capture/Compare Register LSbyte						Bit 0	
P046	Bit 15	Watchdog Counter MSbyte						Bit 8	WDCNTR
P047	Bit 7	Watchdog Counter LSbyte						Bit 0	
P048	Bit 15	Watchdog Reset Key						Bit 0	WDRST
P049	WD OVRFL TAP SEL†	WD INPUT SELECT2†	WD INPUT SELECT1†	WD INPUT SELECT0†	—	T1 INPUT SELECT2	T1 INPUT SELECT1	T1 INPUT SELECT0	T1CTL1
P04A	WD OVRFL RST ENA†	WD OVRFL INT ENA	WD OVRFL INT FLAG	T1 OVRFL INT ENA	T1 OVRFL INT FLAG	—	—	T1 SW RESET	T1CTL2
	Mode: Dual-Compare								
P04B	T1EDGE INT FLAG	T1C2 INT FLAG	T1C1 INT FLAG	—	—	T1EDGE INT ENA	T1C2 INT ENA	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 0	T1C1 OUT ENA	T1C2 OUT ENA	T1C1 RST ENA	T1CR OUT ENA	T1EDGE POLARITY	T1CR RST ENA	T1EDGE DET ENA	T1CTL4
	Mode: Capture/Compare								
P04B	T1EDGE INT FLAG	—	T1C1 INT FLAG	—	—	T1EDGE INT ENA	—	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 1	T1C1 OUT ENA	—	T1C1 RST ENA	—	T1EDGE POLARITY	—	T1EDGE DET ENA	T1CTL4
	Modes: Capture / Compare and Dual-Compare								
P04D	—	—	—	—	T1EVT DATA IN	T1EVT DATA OUT	T1EVT FUNCTION	T1EVT DATA DIR	T1PC1
P04E	T1PWM DATA IN	T1PWM DATA OUT	T1PWM FUNCTION	T1PWM DATA DIR	T1IC/CR DATA IN	T1IC/CR DATA OUT	T1IC/CR FUNCTION	T1IC/CR DATA DIR	T1PC2
P04F	**T1 STEST**	**T1 PRIORITY**	—	—	—	—	—	—	T1PRI
	T2A Module Register								
	Modes: Dual-Compare and Dual-Capture								
P060	Bit 15	T2A Counter MSbyte						Bit 8	T2ACNTR
P061	Bit 7	T2A Counter LSbyte						Bit 0	
P062	Bit 15	Compare Register MSbyte						Bit 8	T2AC
P063	Bit 7	Compare Register LSbyte						Bit 0	
P064	Bit 15	Capture/Compare Register MSbyte						Bit 8	T2ACC
P065	Bit 7	Capture/Compare Register LSbyte						Bit 0	
P066	Bit 15	Capture Register 2 MSbyte						Bit 8	T2AIC
P067	Bit 7	Capture Register 2 LSbyte						Bit 0	

† Once the WD OVRFL RST ENA bit is set, these bits cannot be changed until a reset; this applies only to the standard WD and to simple counter. The WD input select 2 bits are ignored.

Table 19. Peripheral File Frame Compilation (Continued)

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
	T2A Module Register (Continued)								
P06A	—	—	—	T2A OVRFL INT ENA	T2A OVRFL INT FLAG	T2A INPUT SELECT1	T2A INPUT SELECT0	T2A SW RESET	T2ACTL1
	Mode: Dual-Compare								
P06B	T2AEDGE1 INT FLAG	T2AC2 INT FLAG	T2AC1 INT FLAG	—	—	T2AEDGE1 INT ENA	T2AC2 INT ENA	T2AC1 INT ENA	T2ACTL2
P06C	T2A MODE = 0	T2AC1 OUT ENA	T2AC2 OUT ENA	T2AC1 RST ENA	T2AEDGE1 OUT ENA	T2AEDGE1 POLARITY	T2AEDGE1 RST ENA	T2AEDGE1 DET ENA	T2ACTL3
	Mode: Dual-Capture								
P06B	T2AEDGE1 INT FLAG	T2AEDGE2 INT FLAG	T2AC1 INT FLAG	—	—	T2AEDGE1 INT ENA	T2AEDGE2 INT ENA	T2AC1 INT ENA	T2ACTL2
P06C	T2A MODE = 1	—	—	T2AC1 RST ENA	T2AEDGE2 POLARITY	T2AEDGE1 POLARITY	T2AEDGE2 DET ENA	T2AEDGE1 DET ENA	T2ACTL3
	Modes: Dual- Compare and Dual-Capture								
P06D	—	—	—	—	T2AEVT DATA IN	T2AEVT DATA OUT	T2AEVT FUNCTION	T2AEVT DATA DIR	T2APC1
P06E	T2AIC2 / PWM DATA IN	T2AIC2 / PWM DATA OUT	T2AIC2 / PWM FUNCTION	T2AIC2 / PWM DATA DIR	T2AIC1/CR DATA IN	T2AIC1/CR DATA OUT	T2AIC1/CR FUNCTION	T2AIC1/CR DATA DIR	T2APC2
P06F	**T2A STEST**	**T2A PRIORITY**	—	—	—	—	—	—	T2APRI
	ADC1 Module Control Register								
P070	CONVERT START	SAMPLE START	REF VOLT SELECT2	REF VOLT SELECT1	REF VOLT SELECT0	AD INPUT SELECT2	AD INPUT SELECT1	AD INPUT SELECT0	ADCTL
P071	—	—	—	—	—	AD READY	AD INT FLAG	AD INT ENA	ADSTAT
P072	A/D Conversion Data Register								ADDATA
P073 to P07C	Reserved								
P07D	Port E Data Input Register								ADIN
P07E	Port E Input Enable Register								ADENA
P07F	**AD STEST**	**AD PRIORITY**	**AD ESPEN**	—	—	—	—	—	ADPRI

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range‡ V_{CC1}, V_{CC2}, V_{CC3} (see Note 1) . . . . . –0.6 V to 7 V
Input voltage range, All pins except MC . . . . . –0.6 V to 7 V
MC . . . . . –0.6 V to 14 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC1}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC1}$) . . . . . ±20 mA
Continuous output current per buffer, I_O (V_O = 0 to V_{CC1})§ . . . . . ±10 mA
Maximum I_{CC} current . . . . . 170 mA
Maximum I_{SS} current . . . . . – 170 mA
Continuous power dissipation . . . . . 1 W
Operating free-air temperature range, T_A: L version . . . . . 0°C to 70°C
A version . . . . . – 40°C to 85°C
T version . . . . . – 40°C to 105°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ $V_{CC1} = V_{CC}$

§ Electrical characteristics are specified with all output buffers loaded with specified I_O current. Exceeding the specified I_O current in any buffer can affect the levels on other buffers.

NOTE 1: Unless otherwise noted, all voltage values are with respect to V_{SS1}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC1}	Supply voltage (see Note 1)		4.5	5	5.5	V
	RAM data-retention supply voltage (see Note 2)		3		5.5	
V_{CC2}	Digital I/O supply voltage (see Note 1)		4.5	5	5.5	V
V_{CC3}	Analog supply voltage (see Note 1)		4.5	5	5.5	
V_{SS2}	Digital I/O supply ground		– 0.3	0	0.3	V
V_{SS3}	Analog supply ground		– 0.3	0	0.3	V
V_{IL}	Low-level input voltage	All pins except MC	V_{SS1}		0.8	V
		MC, normal operation	V_{SS1}		0.3	V
V_{IH}	High-level input voltage	All pins except MC, XTAL2/CLKIN, and $\overline{\text{RESET}}$	2		V_{CC}	V
		MC (non-WPO mode)	$V_{CC1}-0.3$		$V_{CC1}+0.3$	
		XTAL2/CLKIN	0.8 V_{CC1}		V_{CC1}	
		$\overline{\text{RESET}}$	0.7 V_{CC1}		V_{CC1}	
V_{MC}	MC (mode control) voltage (see Note 3)	EEPROM write protect override (WPO)	11.7	12	13	V
		EPROM programming voltage (V_{PP})	13	13.2	13.5	
		Microprocessor	$V_{CC1}-0.3$		$V_{CC1}+0.3$	
		Microcomputer	V_{SS1}		0.3	
T_A	Operating free-air temperature	L version	0		70	°C
		A version	– 40		85	
		T version	– 40		105	

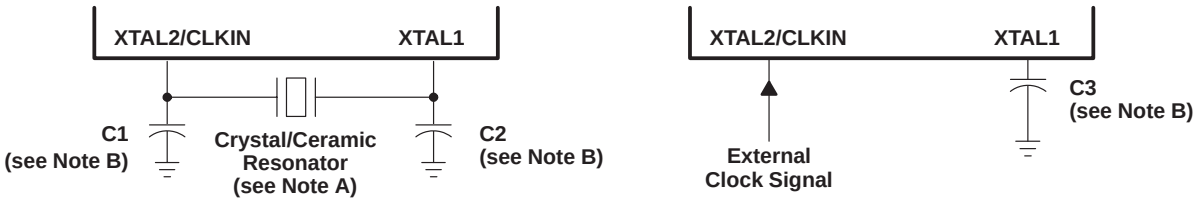
NOTES: 1. Unless otherwise noted, all voltage values are with respect to V_{SS1}.
2. $\overline{\text{RESET}}$ must be activated externally when V_{CC1} or SYSCLK is out of the recommended operating range.
3. The basic microcomputer and microprocessor operating modes are selected by the voltage level applied to the dedicated MC pin two system clock cycles (t_c) before $\overline{\text{RESET}}$ goes inactive (high). The WPO mode can be selected anytime a sufficient voltage is present on MC.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage		I_{OL} = 1.4 mA			0.4	V
V_{OH}	High-level output voltage		I_{OH} = –50 µA	0.9 V_{CC1}			V
			I_{OH} = –2 mA	2.4			
I_I	Input current	MC	0 V < V_I ≤ 0.3 V			10	µA
			0.3 V < V_I < V_{CC1}–0.3 V			50	
			V_{CC1}–0.3 V ≤ V_I ≤ V_{CC1}+0.3 V			10	
			V_{CC1} + 0.3 V < V_I ≤ 13 V			650	
			12 V ≤ V_I ≤ 13 V See Note 4			50	mA
		I/O pins	0 V ≤ V_I ≤ V_{CC1}			± 10	µA
I_{OL}	Low-level output current		V_{OL} = 0.4 V	1.4			mA
I_{OH}	High-level output current		V_{OH} = 0.9 V_{CC1}	– 50			µA
			V_{OH} = 2.4 V	– 2			mA
I_{CC}	Supply current (operating mode) OSC POWER bit = 0 (see Note 7)		SYSCLK = 5 MHz See Notes 5 and 6		35	56	mA
			SYSCLK = 3 MHz See Notes 5 and 6		25	36	
			SYSCLK = 0.5 MHz See Notes 5 and 6		13	18	
	Supply current (STANDBY mode) OSC POWER bit = 0 (see Note 8)		SYSCLK = 5 MHz See Notes 5 and 6		12	17	mA
			SYSCLK = 3 MHz See Notes 5 and 6		8	11	
			SYSCLK = 0.5 MHz See Notes 5 and 6		2.5	3.5	
	Supply current (STANDBY mode) OSC POWER bit = 1 (see Note 9)		SYSCLK = 3 MHz See Notes 5 and 6		6	8.6	mA
			SYSCLK = 0.5 MHz See Notes 5 and 6		2	3	
	Supply current (HALT mode)		XTAL2/CLKIN < 0.2 V See Note 5		2	30	µA

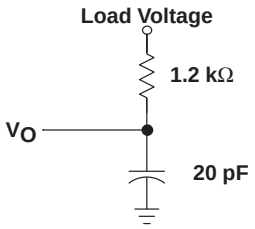
NOTES: 4. Input current I_{PP} is a maximum of 50 mA only when programming EPROM.
5. In single chip mode, ports are configured as inputs or outputs with no load. All inputs ≤ 0.2 V or ≥ V_{CC1} – 0.2V.
6. XTAL2/CLKIN is driven with an external square wave signal with 50% duty cycle and rise and fall times less than 10 ns. Current can be higher with a crystal oscillator. At 5 MHz SYSCLK, this extra current = 0.01 mA x (total load capacitance + crystal capacitance in pF).
7. Maximum operating current for TMS370Cx7x = 10 (SYSCLK) + 5.8 mA.
8. Maximum standby current for TMS370Cx7x = 3 (SYSCLK) + 2 mA. (OSC POWER bit = 0).
9. Maximum standby current for TMS370Cx7x = 2.24 (SYSCLK) + 1.9 mA. (OSC POWER bit =1, only valid up to 3 MHz SYSCLK).

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The crystal/ceramic resonator frequency is four times the reciprocal of the system clock period.
B. The values of C1 and C2 are typically 15 pF and C3 is typically 50 pF. See the manufacturer's recommendations for ceramic resonators.

Figure 17. Recommended Crystal/Clock Connections



Case 1: $V_O = V_{OH}$ = 2.4 V; Load Voltage = 0 V
Case 2: $V_O = V_{OL}$ = 0.4 V; Load Voltage = 2.1 V

NOTE A: All measurements are made with the pin loading as shown unless otherwise noted. All measurements are made with XTAL2/CLKIN driven by an external square wave signal with a 50% duty cycle and rise and fall times less than 10 ns unless otherwise stated.

Figure 18. Typical Output Load Circuit (see Note A)

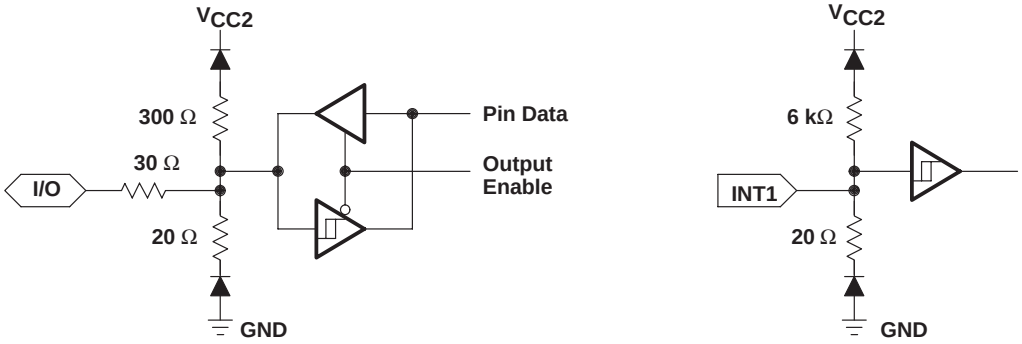


Figure 19. Typlcal Buffer Circuitry

PARAMETER MEASUREMENT INFORMATION

timing parameter symbology

Timing parameter symbols have been created in accordance with JEDEC Standard 100. In order to shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

A	Address	PGM	Program
AR	Array	R	Read
B	Byte	SC	SYSCLK
CI	XTAL2/CLKIN	W	Write
D	Data		

Lowercase subscripts and their meanings are:

c	cycle time (period)	r	rise time
d	delay time	su	setup time
f	fall time	v	valid time
h	hold time	w	pulse duration (width)

The following additional letters are used with these meanings:

H	High
L	Low
V	Valid
Z	High impedance

All timings are measured between high and low measurement points as indicated in Figure 20 and Figure 21.

Figure 20. XTAL2/CLKIN Measurement Points

Figure 21. General Measurement Points

external clocking requirements for clock divided by 4† (see Figure 22)

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{w(Cl)}$	Pulse duration, XTAL2/CLKIN (see Note 10)	20		ns
2	$t_{r(Cl)}$	Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(Cl)}$	Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCL)}$	Delay time, XTAL2/CLKIN rise to SYSCLK fall		100	ns
	CLKIN	Crystal operating frequency	2	20	MHz
	SYSCLK	System clock‡	0.5	5	MHz

† For V_{IL} and V_{IH}, refer to recommended operating conditions.
‡ SYSCLK = CLKIN/4
NOTE 10: This pulse can be either a high pulse, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

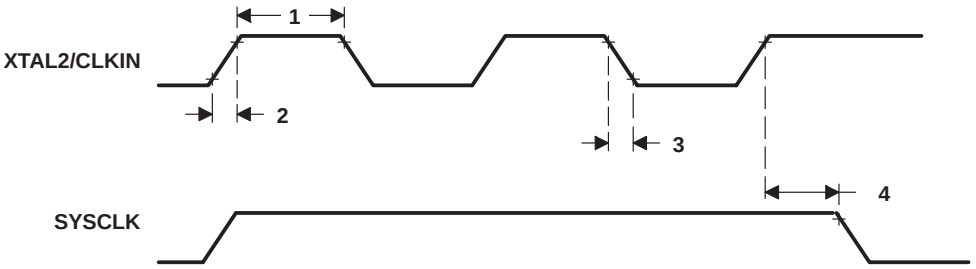


Figure 22. External Clock Timing for Divide-by-4

external clocking requirements for clock divided by 1 (PLL)† (see Figure 23)

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{w(Cl)}$	Pulse duration, XTAL2/CLKIN (see Note 10)	20		ns
2	$t_{r(Cl)}$	Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(Cl)}$	Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCH)}$	Delay time, XTAL2/CLKIN rise to SYSCLK rise		100	ns
	CLKIN	Crystal operating frequency	2	5	MHz
	SYSCLK	System clock§	2	5	MHz

† For V_{IL} and V_{IH}, refer to recommended operating conditions.
§ SYSCLK = CLKIN/1
NOTE 10: This pulse can be either a high pulse, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

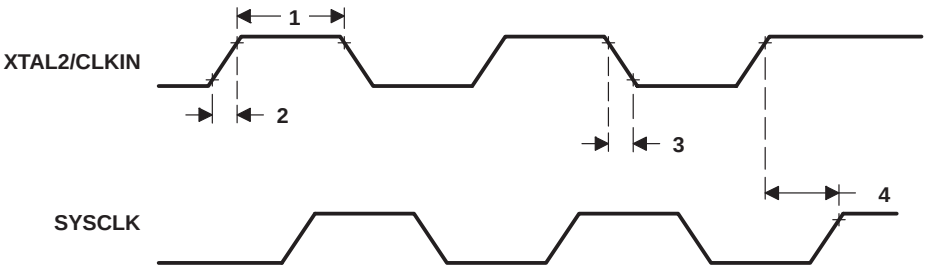


Figure 23. External Clock Timing for Divide-by-1

general-purpose output signal switching time requirements (see Figure 24)

		MIN	NOM	MAX	UNIT
t_r	Rise time		30		ns
t_f	Fall time		30		ns

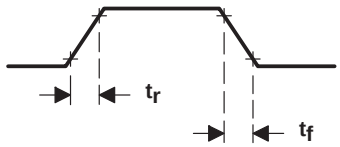


Figure 24. Signal Switching Timing

recommended EEPROM timing requirements for programming

		MIN	MAX	UNIT
$t_{w(PGM)B}$	Pulse duration, programming signal to ensure valid data is stored (byte mode)	10		ms
$t_{w(PGM)AR}$	Pulse duration, programming signal to ensure valid data is stored (array mode)	20		ms

recommended EPROM operating conditions for programming

			MIN	NOM	MAX	UNIT
V_{CC1}	Supply voltage		4.75	5.5	6	V
V_{PP}	Supply voltage at MC pin		13	13.2	13.5	V
I_{PP}	Supply current at MC pin during programming (V_{PP} = 13 V)			30	50	mA
SYSCLK	System clock	Divide-by-4	0.5		5	MHz
		Divide-by-1	2		5	

recommended EPROM timing requirements for programming

		MIN	NOM	MAX	UNIT
$t_{w(EPGM)}$	Pulse duration, programming signal (see Note 11)	0.40	0.50	3	ms

NOTE 11: Programming pulse is active when both EXE (EPCTL.0) and V_{PPS} (EPCTL.6) are set.

switching characteristics and timing requirements† (see Figure 25)

NO.	PARAMETER			MIN	MAX	UNIT
5	t_c	Cycle time, SYSCLK (system clock)	Divide-by-4 clock	200	2000	ns
			Divide-by-1-(PLL)	200	500	
6	$t_{w(SCL)}$	Pulse duration, SYSCLK low		$0.5t_c$–20	$0.5t_c$	ns
7	$t_{w(SCH)}$	Pulse duration, SYSCLK high		$0.5t_c$	$0.5t_c$+20	ns

† t_c = system-clock cycle time = 1/SYSCLK

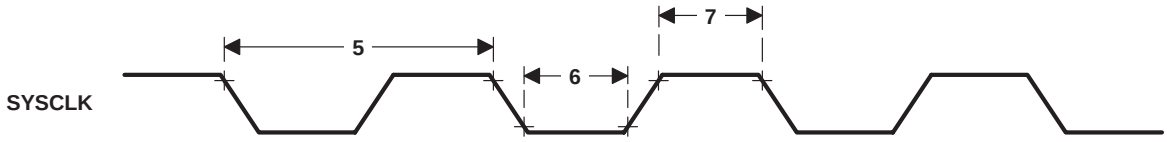


Figure 25. SYSCLK Timing

analog-to-digital converter 1 (ADC1)

The ADC1 has a separate power bus for its analog circuitry. These pins are referred to as V_{CC3} and V_{SS3}. The purpose is to enhance ADC1 performance by preventing digital switching noise in the logic circuitry that can be present on V_{SS1} and V_{CC1} when coupling into the A/D analog stage. All ADC1 specifications are given with respect to V_{SS3} unless otherwise noted.

Resolution . . . . . 8-bits (256 values)
Monotonic . . . . . Yes
Output conversion mode . . . . . 00h to FFh (00 for $V_I \le V_{SS3} \le$; FF for $V_I \le V_{ref}$)
Conversion time (excluding sample time) . . . . . 164 t_c

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC3}	Analog supply voltage	4.5	5	5.5	V
		V_{CC1}–0.3		V_{CC1}+0.3	
V_{SS3}	Analog ground	V_{SS1}–0.3		V_{SS1}+0.3	V
V_{ref}	Non-V_{CC3} reference†	2.5	V_{CC3}	V_{CC3} + 0.1	V
	Analog input for conversion	V_{SS3}		V_{ref}	V

† V_{ref} must be stable, within ± 1/2 LSB of the required resolution, during the entire conversion time.

operating characteristics over recommended ranges of operating conditions

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
	Absolute accuracy‡	V_{CC3} = 5.5 V V_{rerf} = 5.1 V		±1.5	LSB
	Differential/integral linearity error‡§	V_{CC3} = 5.5 V V_{rerf} = 5.1 V		±0.9	LSB
I_{CC3}	Analog supply current	Converting		2	mA
		Nonconverting		5	µA
I_I	Input current, AN0–AN7	0 V ≤ V_I ≤ 5.5 V		2	µA
I_{ref}	Input charge current			1	mA
Z_{ref}	Source impedance of V_{ref}	SYSCLK ≤ 3 MHz		24	kΩ
		3 MHz < SYSCLK ≤ 5 MHz		10	kΩ

‡ Absolute resolution = 20 mV. At V_{ref} = 5 V, this is one LSB. As V_{ref} decreases, LSB size decreases; therefore, the absolute accuracy and differential/integral linearity errors in terms of LSBs increase.
§ Excluding quantization error of 1/2 LSB

analog-to-digital converter 1 (ADC1) (continued)

The ADC1 module allows complete freedom in design of the sources that supply the analog inputs. The period of the sample time is user-defined so that the high impedance can be accommodated without penalty to the low-impedance sources. The sample period begins when the SAMPLE START bit of the ADC1 control register (ADCTL.6) is set to 1. The end of the signal sample period occurs when the conversion bit (CONVERT START, ADCTL.7) is set to 1. After a hold time, the converter resets the SAMPLE START and CONVERT START bits, signaling that a conversion has started and that the analog signal can be removed.

analog timing requirements (see Figure 26)

		MIN	MAX	UNIT
$t_{su(S)}$	Setup time, analog to sample command	0		ns
$t_{h(AN)}$	Hold time, analog input from start of conversion	$18t_c$		ns
$t_{w(S)}$	Pulse duration, sample time per kilohm of source impedance†	1		µs/kΩ

† The value given is valid for a signal with a source impedance > 1 kΩ. If the source impedance is < 1 kΩ, use a minimum sampling time of 1µs.

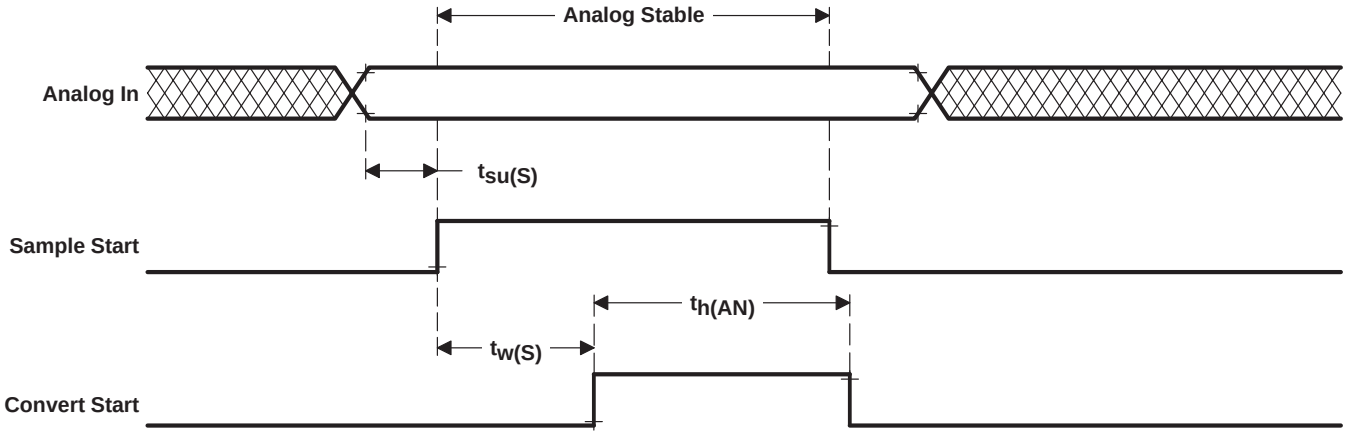


Figure 26. Analog Timing

Table 20 is designed to aid the user in referencing a device part number to a mechanical drawing. The table shows a cross-reference of the device part number to the TMS370 generic package name and the associated mechanical drawing by drawing number and name.

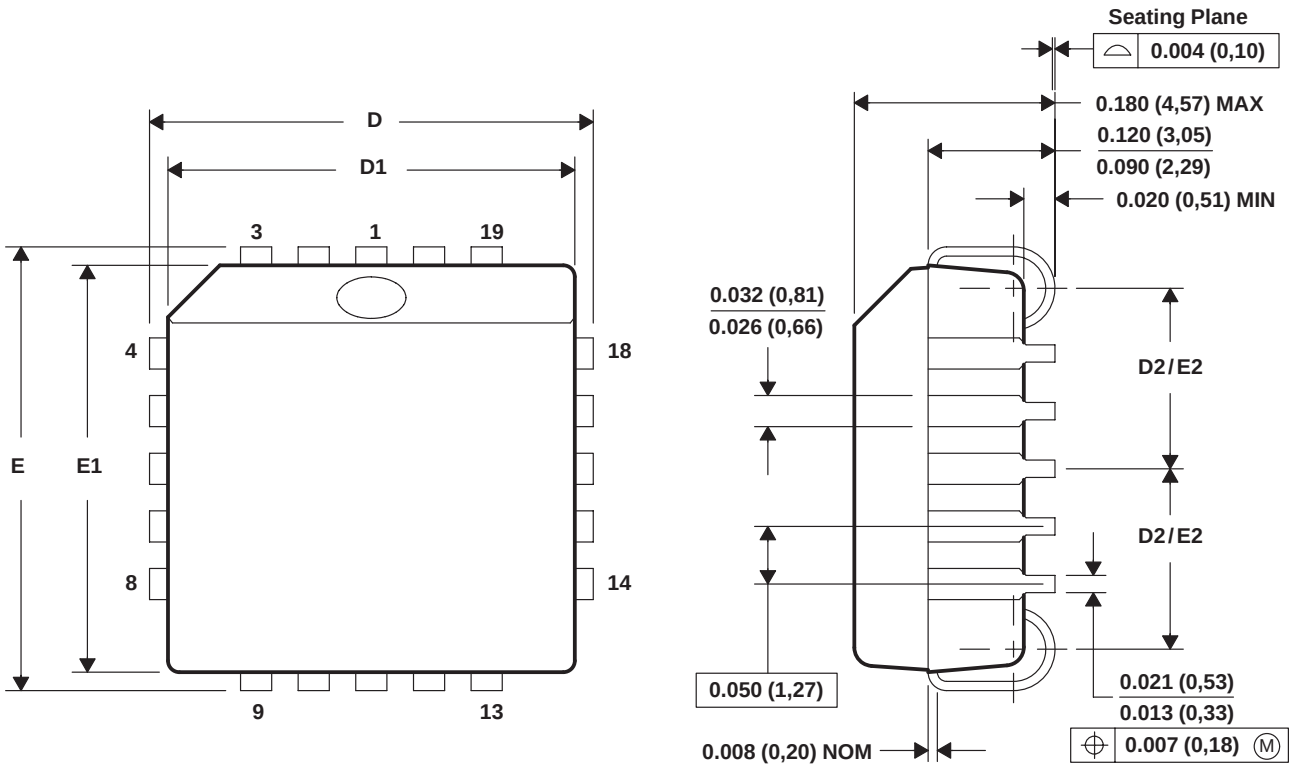
Table 20. TMS370Cx7x Family Package Type and Mechanical Cross-Reference

PKG TYPE (mil pin spacing)	TMS370 GENERIC NAME	PKG TYPE NO. AND MECHANICAL NAME	DEVICE PART NUMBERS
FN – 68 pin (50-mil pin spacing)	PLASTIC LEADED CHIP CARRIER (PLCC)	FN(S-PQCC-J**) PLASTIC J-LEADED CHIP CARRIER	TMS370C077AFNA TMS370C077AFNL TMS370C077AFNT TMS370C777AFNT
FZ – 68 pin (50-mil pin spacing)	CERAMIC LEADED CHIP CARRIER (CLCC)	FZ(S-CQCC-J**) J-LEADED CERAMIC CHIP CARRIER	SE370C777AFZT
JN – 64 pin (70-mil pin spacing)	CERAMIC SHRINK DUAL-IN-LINE PACKAGE (CSDIP)	JN(R-CDIP-T64) CERAMIC DUAL-IN-LINE PACKAGE	SE370C777AJNT
NM – 64 pin (70-mil pin spacing)	PLASTIC SHRINK DUAL-IN-LINE PACKAGE (PSDIP)	NM(R-PDIP-T64) PLASTIC SHRINK DUAL-IN-LINE PACKAGE	TMS370C077ANMA TMS370C077ANML TMS370C077ANMT TMS370C777ANMT

MECHANICAL DATA

FN (S-PQCC-J)** **PLASTIC J-LEADED CHIP CARRIER**

20 PIN SHOWN



NO. OF PINS **	D/E		D1/E1		D2/E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

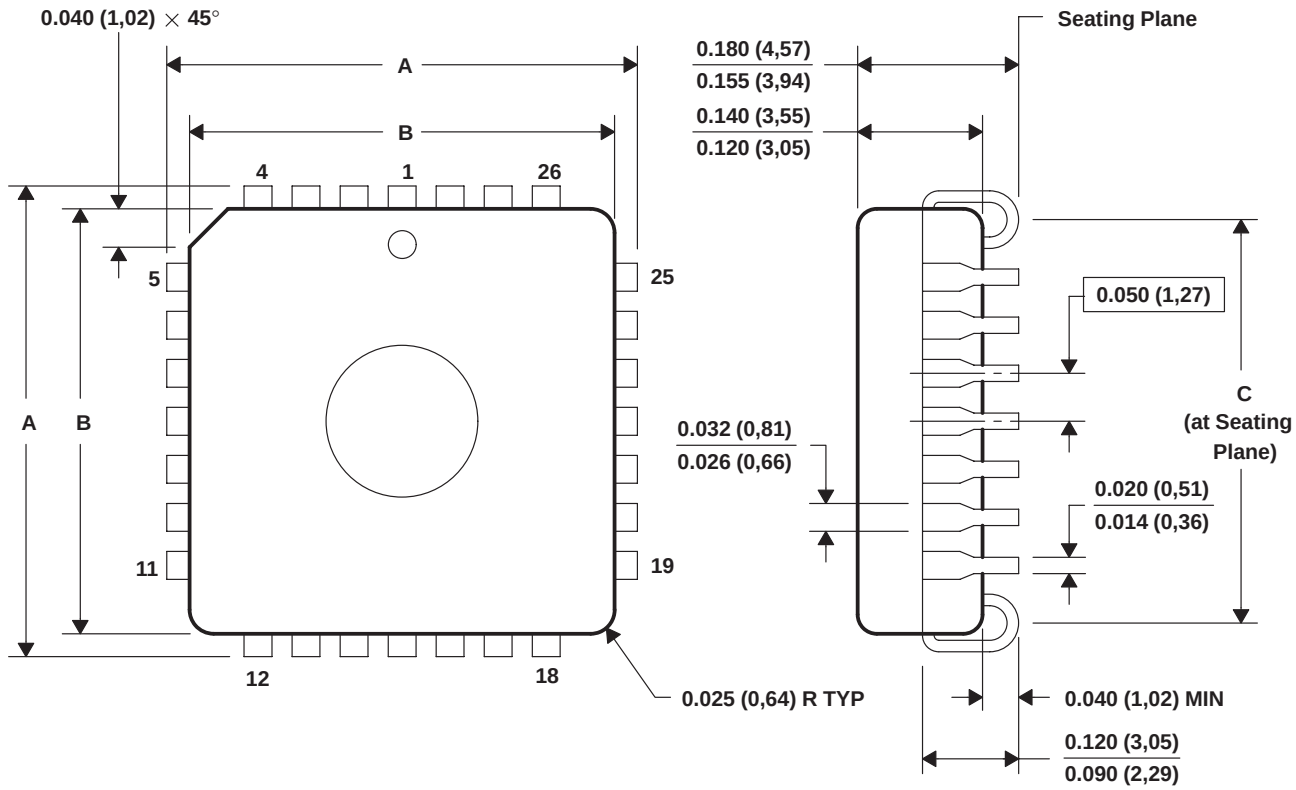
4040005/B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

MECHANICAL DATA

FZ (S-CQCC-J)** **J-LEADED CERAMIC CHIP CARRIER**

28 LEAD SHOWN



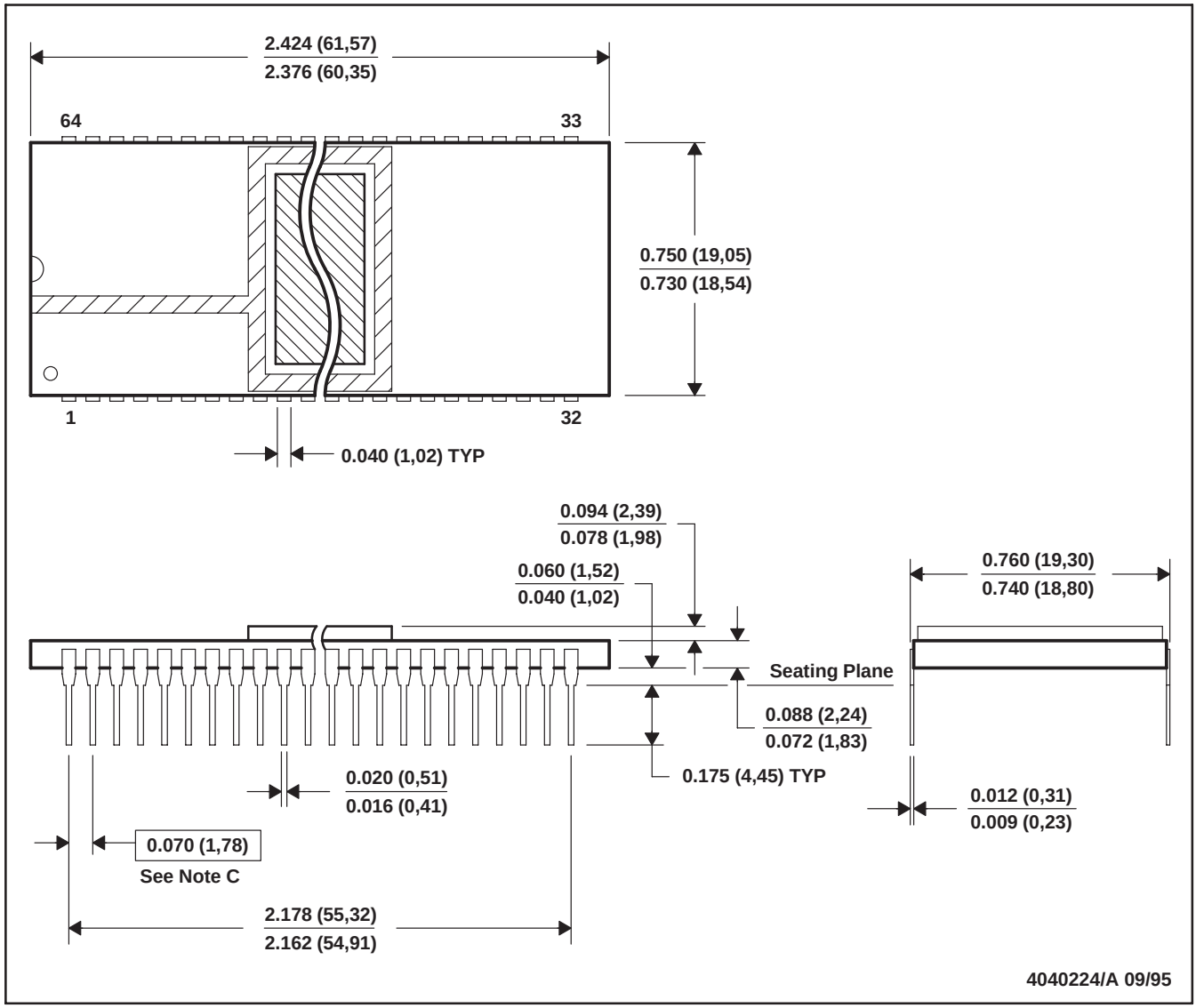
JEDEC OUTLINE	NO. OF PINS**	A		B		C	
		MIN	MAX	MIN	MAX	MIN	MAX
MO-087AA	28	0.485 (12,32)	0.495 (12,57)	0.430 (10,92)	0.455 (11,56)	0.410 (10,41)	0.430 (10,92)
MO-087AB	44	0.685 (17,40)	0.695 (17,65)	0.630 (16,00)	0.655 (16,64)	0.610 (15,49)	0.630 (16,00)
MO-087AC	52	0.785 (19,94)	0.795 (20,19)	0.730 (18,54)	0.765 (19,43)	0.680 (17,28)	0.740 (18,79)
MO-087AD	68	0.985 (25,02)	0.995 (25,27)	0.930 (23,62)	0.955 (24,26)	0.910 (23,11)	0.930 (23,62)

4040219/B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.

MECHANICAL DATA

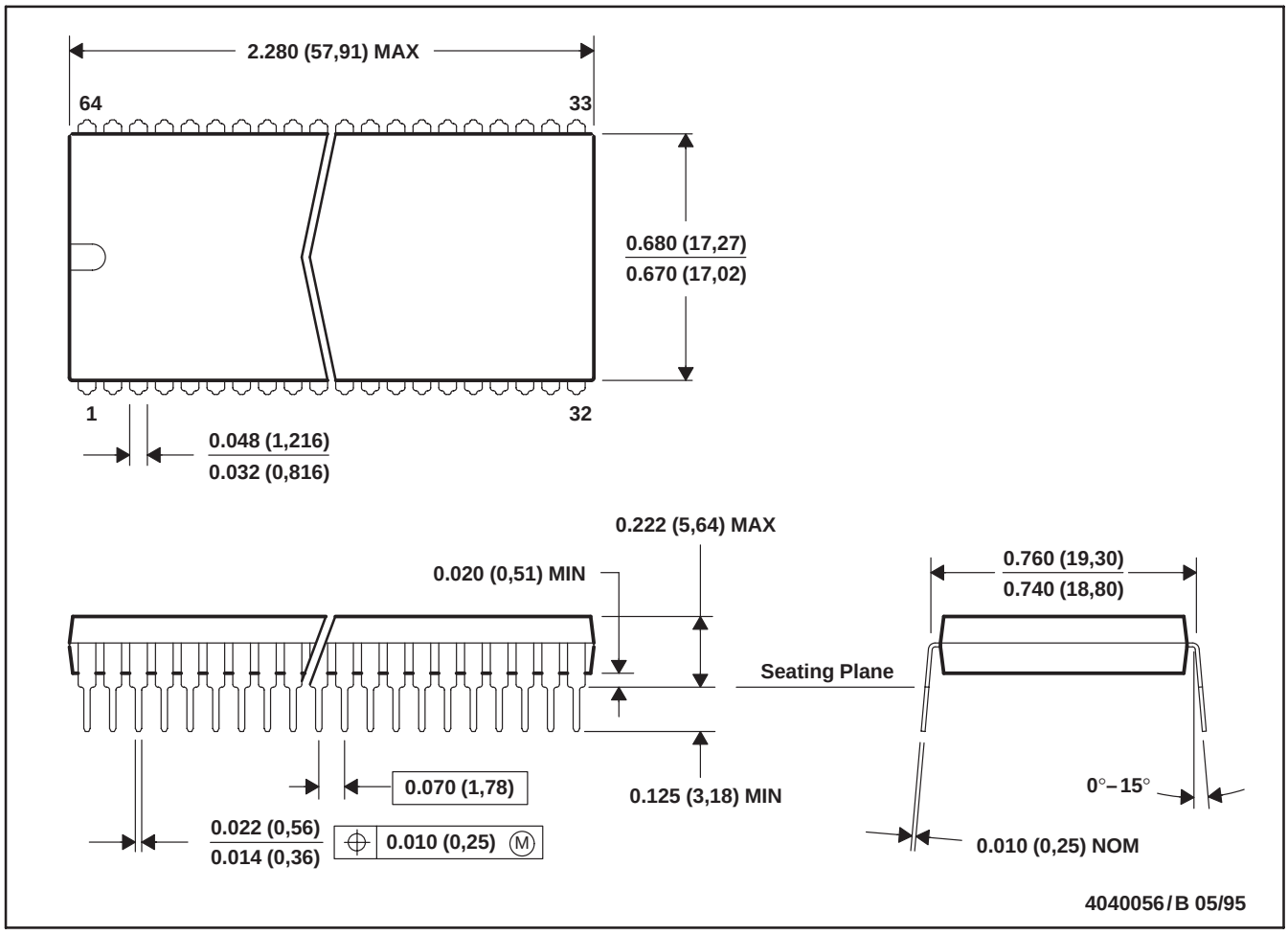
JN (R-CDIP-T64) **CERAMIC DUAL-IN-LINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Each pin centerline located within 0.010 (0,26) of it true longitudinal position.

MECHANICAL DATA

NM (R-PDIP-T64) **PLASTIC SHRINK DUAL-IN-LINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SE370C777AFZT	OBSOLETE	JLCC	FZ	68		TBD	Call TI	Call TI
SE370C777AJNT	OBSOLETE	CDIP	JN	64		TBD	Call TI	Call TI
TMS370C777AFNT	OBSOLETE	PLCC	FN	68		TBD	Call TI	Call TI
TMS370C777ANMT	OBSOLETE	SDIP	NM	64		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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