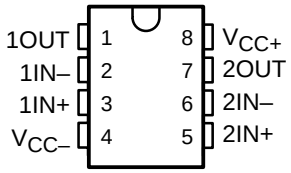
SLVS457A – JANUARY 2003 – REVISED MARCH 2003

- **Equivalent Input Noise Voltage 5 nV/$\sqrt{\text{Hz}}$ Typ at 1 kHz**
- **Unity-Gain Bandwidth . . . 10 MHz Typ**
- **High Slew Rate . . . 9 V/μs Typ**
- **Peak-to-Peak Output Voltage Swing 32 V Typ, With $V_{CC\pm}$ = ±18 V and R_L = 600 Ω**
- **Wide Supply-Voltage Range . . . ±3 V to ±20 V**
- **Common-Mode Rejection Ratio . . . 100 dB Typ**
- **High dc Voltage Gain . . . 100 V/mV Typ**
- **Applications: Audio PreAmps, Active Filters, Headphone Amps**
- **End Equipment: DVD/CD/CDRW Players; Set-Top Boxes**

D, P, OR PS PACKAGE
(TOP VIEW)



description/ordering information

The TL4581 is a dual operational amplifier that has been designed optimally for audio applications, such as improving tone control. It offers low noise, high-gain bandwidth, good slew, and high output current drive for driving capacitive loads. These features make the TL4581 ideally suited for audio applications, such as audio preamps and active filters. When high output current is required, the TL4581 also can be used as a headphone amplifier.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – P	Tube of 50	TL4581P	TL4581P
	SOIC – D	Tube of 75	TL4581D	T4581
		Reel of 2500	TL4581DR	
	SOP – PS	Reel of 2000	TL4581PSR	T4581

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (see Note 1): V_{CC+} . . . . . 22 V
$V_{CC–}$ . . . . . –22 V
Input voltage, either input (see Notes 1 and 2) . . . . . $V_{CC±}$
Input current (see Note 3) . . . . . ±10 mA
Duration of output short circuit (see Note 4) . . . . . Unlimited
Operating virtual junction temperature, T_J . . . . . 150°C
Package thermal impedance, θ_{JA} (see Notes 5 and 6): D package . . . . . 97°C/W
P package . . . . . 85°C/W
PS package . . . . . 95°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and $V_{CC–}$.
2. The magnitude of the input voltage must never exceed the magnitude of the supply voltage.
3. Excessive input current will flow if a differential input voltage in excess of approximately 0.6 V is applied between the inputs, unless some limiting resistance is used.
4. The output may be shorted to ground or either power supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.
5. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
6. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC+}	Supply voltage	5	15	V
$V_{CC–}$	Supply voltage	–5	–15	V
T_A	Operating free-air temperature range	0	70	°C

electrical characteristics, $V_{CC\pm}$ = +15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0	T_A = 25°C			0.5	4	mV
			T_A = 0°C to 70°C				5	
I_{IO}	Input offset current	T_A = 25°C				10	150	nA
		T_A = 0°C to 70°C					200	
I_{IB}	Input bias current	T_A = 25°C				200	800	nA
		T_A = 0°C to 70°C					1000	
V_{ICR}	Common-mode input-voltage range				±12	±13		V
V_{OPP}	Maximum peak-to-peak output-voltage swing	$R_L \geq 600\ \Omega$	$V_{CC\pm}$ = ±15 V		24	26		V
			$V_{CC\pm}$ = ±18 V		30	32		
A_{VD}	Large-signal differential-voltage amplification	$R_L \geq 600\ \Omega$, V_O = ±10 V	T_A = 25°C		15	50		V/mV
			T_A = 0°C to 70°C		10			
		$R_L \geq 2\ k\Omega$, V_O = ±10 V	T_A = 25°C		25	100		
			T_A = 0°C to 70°C		15			
A_{vd}	Small-signal differential-voltage amplification	f = 10 kHz				2.2		V/mV
B_{OM}	Maximum-output-swing bandwidth	R_L = 600 Ω	V_O = ±10 V			140		kHz
			$V_{CC\pm}$ = ±18 V,	V_O = ±14 V		100		
B_1	Unity-gain bandwidth	R_L = 600 Ω,	C_L = 100 pF			10		MHz
r_i	Input resistance				30	300		kΩ
z_o	Output impedance	A_{VD} = 30 dB,	R_L = 600 Ω,	f = 10 kHz		0.3		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min			70	100		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±9 V to ±15 V,		V_O = 0	80	100		dB
I_{OS}	Output short-circuit current				10	38	60	mA
I_{CC}	Total supply curent	V_O = 0,	No load			8	16	mA
	Crosstalk attenuation (V_{O1}/V_{O2})	V_{01} = 10 V peak,	f = 1 kHz			110		dB

† All characteristics are measured under open-loop conditions with zero common-mode input voltage, unless otherwise specified.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain					9		V/μs
	Overshoot factor	V_I = 100 mV, R_L = 600 Ω,		A_{VD} = 1, C_L = 100 pF		10		%
V_n	Equivalent input noise voltage	f = 30 Hz				8		nV/√Hz
		f = 1 kHz				5		
I_n	Equivalent input noise current	f = 30 Hz				2.7		pA/√Hz
		f = 1 kHz				0.7		

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL4581D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T4581	Samples
TL4581DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T4581	Samples
TL4581DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T4581	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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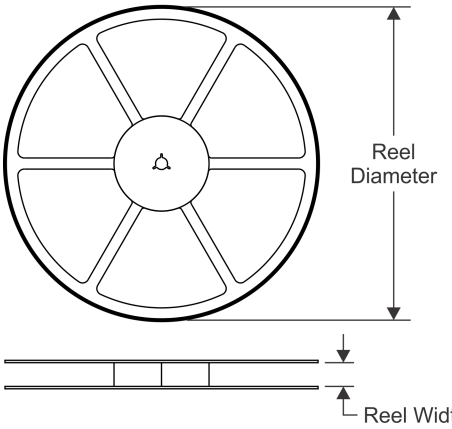
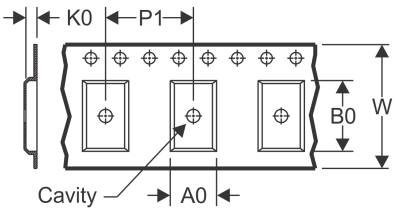
TAPE AND REEL INFORMATION

REEL DIMENSIONS

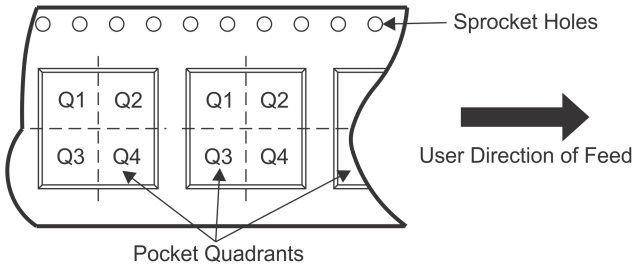


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

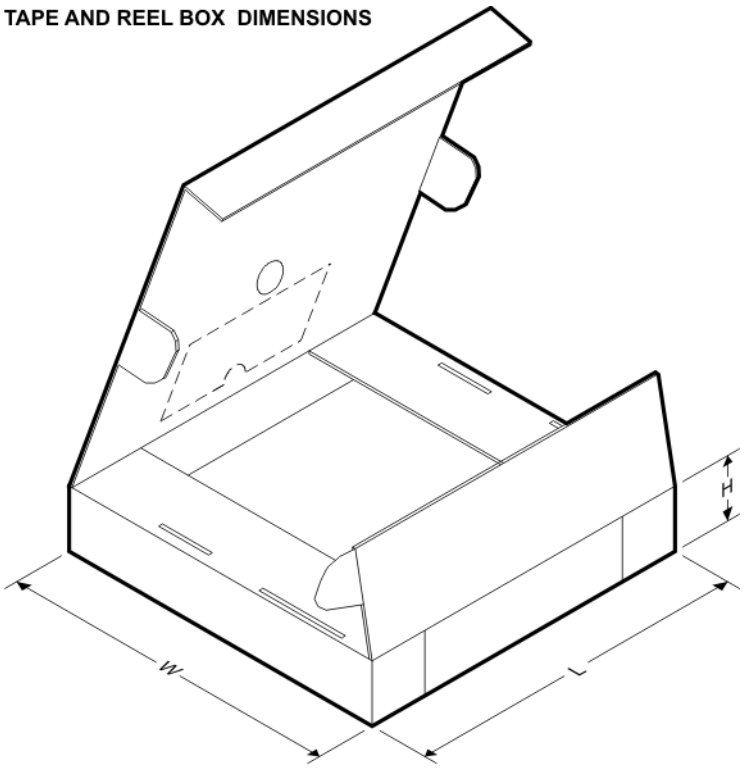
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

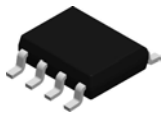
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL4581DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL4581DR	SOIC	D	8	2500	340.5	338.1	20.6

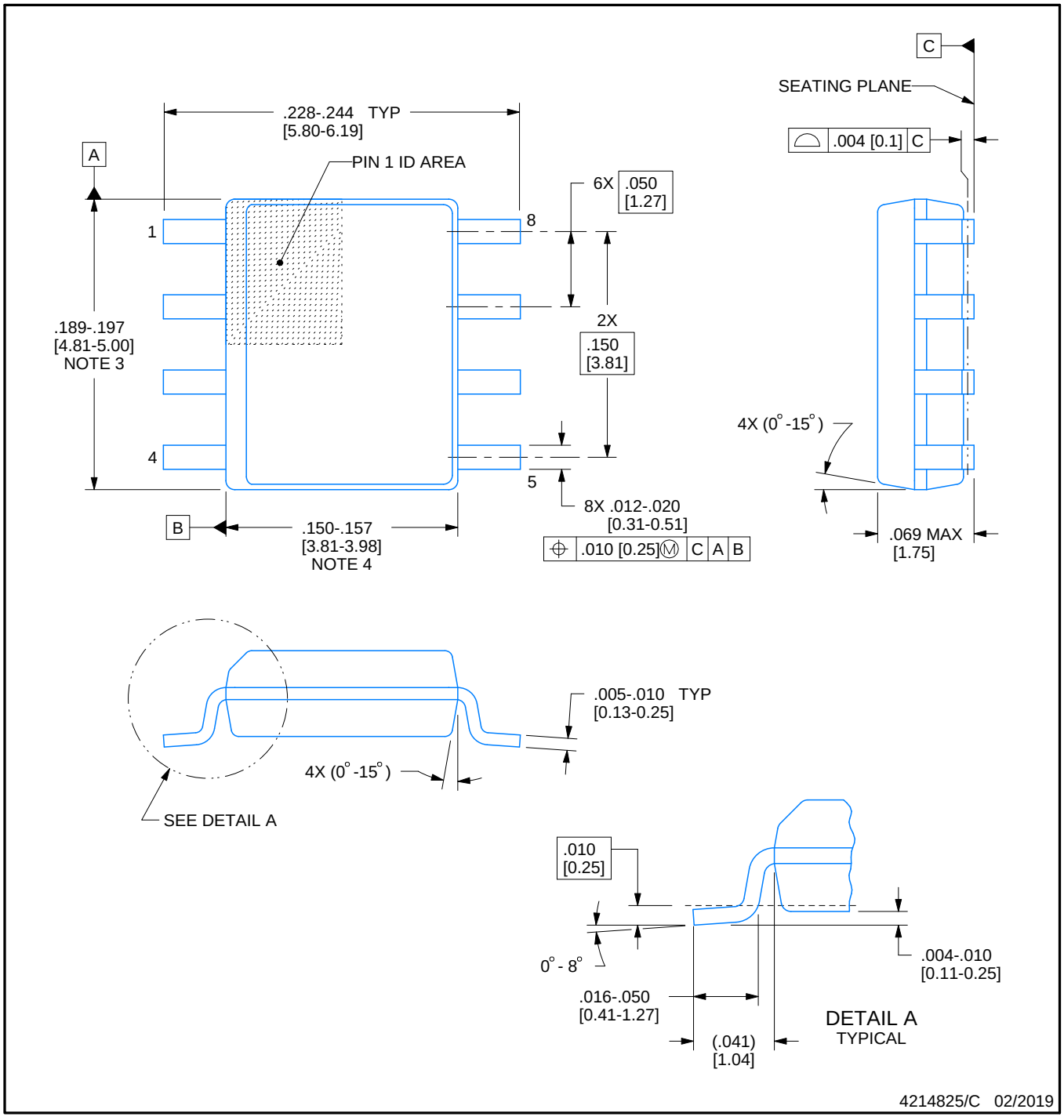


PACKAGE OUTLINE

D0008A

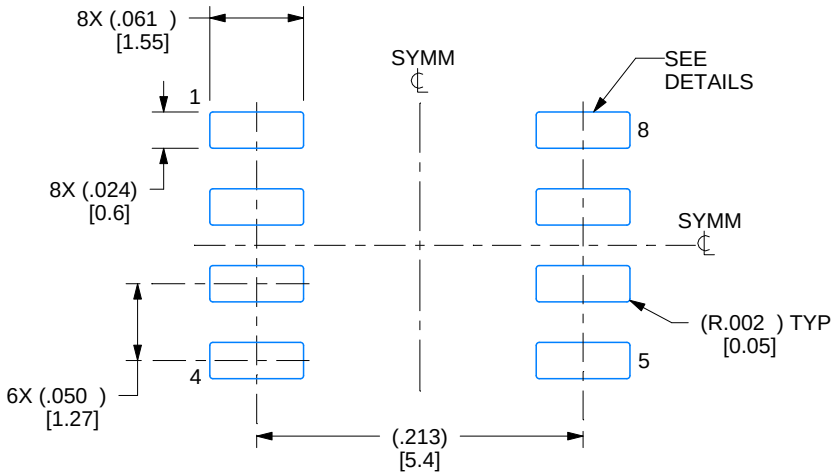
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

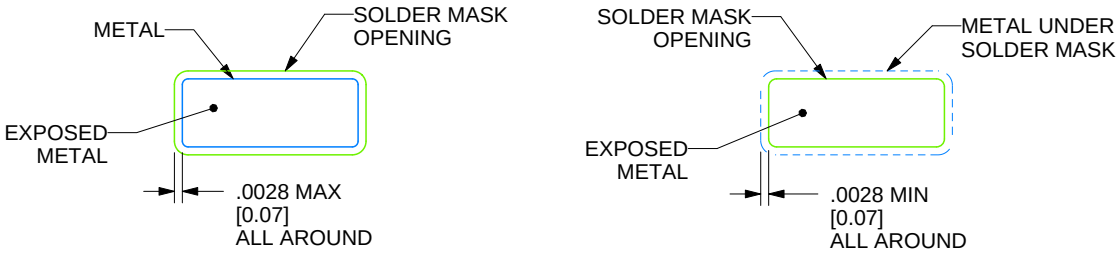


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

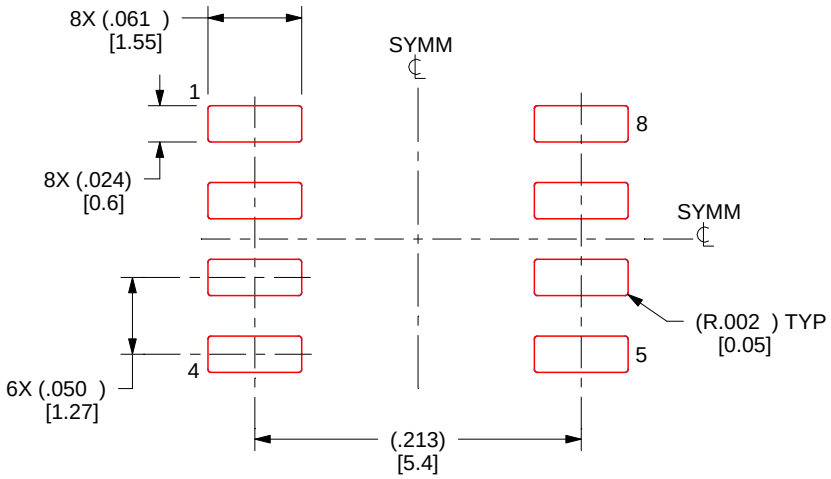
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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