

Features

- General Purpose, Low Cost
- Gain Bandwidth Product: 300KHz
- Low Quiescent Current: 21 μ A/Amplifier
- 0.01Hz-10Hz Noise: 1.5 μ V_{PP}
- Zero Drift: 0.01 μ V/°C (Typ)
- Input Bias Current: 20pA
- Unity Gain Stable
- Rail-to-Rail Input and Output
- Single or Dual Supply Operation
- Supply Voltage Range: 1.8V to 5.5V
- Operating Temperature: -50°C ~ +125°C
- Type Package: SOT23-5

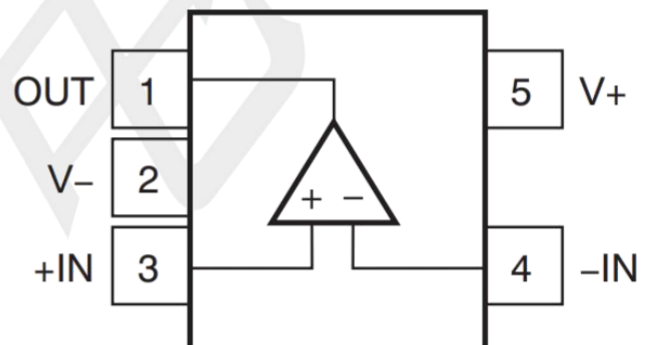
Applications

- Temperature Sensors
- Battery-Powered Instruments
- Smoke/Gas/Environment Sensors
- Medical Equipment
- Portable Instruments and Mobile Device
- Active Filters
- Piezo Electrical Transducer Amplifier
- Sensor Interface
- Handheld Test Equipment

General Description

The OPA317I of CMOS operational amplifiers use a proprietary auto-calibration technique to simultaneously provide very low offset voltage ($\pm 10\mu$ V, maximum) and near-zero drift over time and temperature. These miniature, high-precision, low quiescent current (21 μ A) amplifiers offer high impedance inputs that have a common-mode range 100 mV beyond the rails, and rail-to-rail output that swings within 50 mV of the rails. Single or dual supplies as low as 1.8 V (± 0.9 V) and up to 5.5 V (+2.75 V) can be used. These devices are optimized for low voltage, single-supply operation.

Pinout (top view)



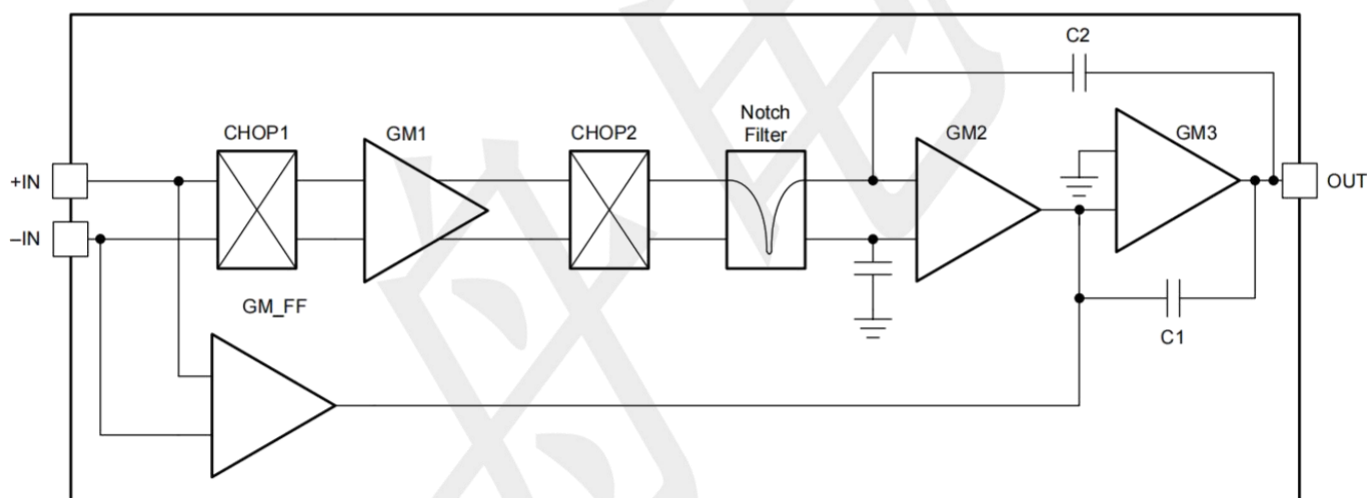
Pin Configurations

Pin Number	Pin Name	Pin Function
1	OUT	Output
2	-Vs	Chip Supply Voltage(Negative)/GND
3	+IN	In-phase input
4	-IN	Reverse input
5	+Vs	Chip Supply Voltage(Positive)/VDD

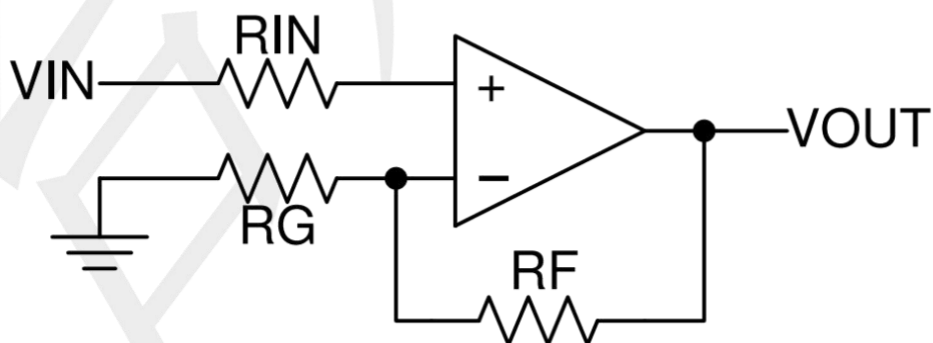
Absolute Maximum Ratings (@TA = +25°C, unless otherwise specified.)

Condition		Rating	UNIT
VDD to GND	Power Supply Voltage	7V	V
IN+ or IN-	Signal Input Terminals Voltage	GND-0.3V~VDD+0.3V	V
IN+ or IN-	Signal Input Terminals Current	-1mA ~ +1mA	mA
OUT to GND	Output Short-Circuit	Continuous	mA
TJ	Junction Temperature	150	°C
LT	Lead Temperature (Soldering, 10 sec.)	260	°C
TA	Operating Temperature Range	-55 150	°C
Tstg	Storage Temperature Range	-65 150	°C
V(ESD)	Human body model (HBM)	±4000	V
V(ESD)	Charged-device model (CDM)	±1000	V

BLOCK DIAGRAM



Power Supply Bypassing



Electrical Characteristics

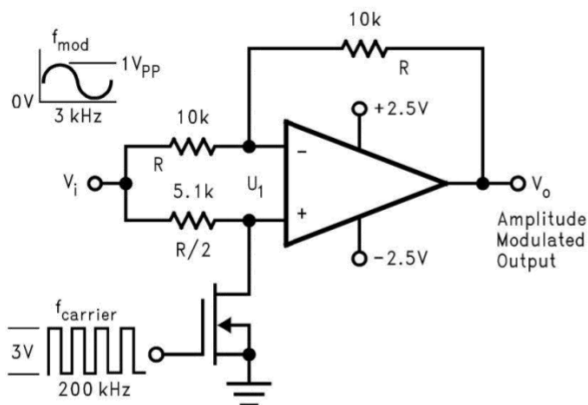
(At $T_A = +25^{\circ}\text{C}$, $V_S = +5\text{V}$, $V_{IN} = 0\text{V}$, unless otherwise noted.)

PARAMETER	SYMBOL	TEST Conditions	MIN	TYP	MAX	UNIT
Supply-Voltage Range	V_{DD}	Single-supply	1.8	--	5.5	V
		Dual-supply	± 0.9	--	± 2.75	V
Quiescent Current/Amplifier	I_Q	$V_{DD} = 5\text{V}$	--	21	35	μA
Input Offset Voltage	V_{OS}		--	± 8	± 50	μV
Input Offset Voltage Tempco	dV_{OS}/dT	$T_A = -55^{\circ}\text{C}$ to 125°C	--	0.01	--	$\mu\text{V}/^{\circ}\text{C}$
Input Bias Current	I_B	(2)	--	1	20	PA
Input Bias Current	I_B	$T_A = -55^{\circ}\text{C}$ to 125°C	--	--	180	PA
Input Offset Current	I_{OS}	(2)	--	1	20	PA
Common-Mode Voltage Range	V_{CM}		GND-0.1	--	$V_{DD}+0.1$	V
Common-Mode Rejection Ratio	CMRR	$\Delta V_{IN}=1\text{V}$	130	135	--	dB
Power-Supply Rejection Ratio	PSRR	$\Delta V_S=1\text{V}$	--	135	--	dB
Open-Loop Voltage Gain	A_V	$\Delta V_{OUT}=1\text{V}$	140	150	--	dB
Output Swing from Positive Rail	$V_{OUT - SWING}$	$R_L=10\text{k}\Omega$	--	13	--	mV
Output Swing from Negative Rail		$R_L=10\text{k}\Omega$	--	17	--	mV
Capacitive Load Drive	$C_{L(3)}$	$G = +1$, $V_{IN}=4\text{V}$ Step	--	--	1	nF
Output Short-Circuit Current	I_{SC}	Sinking or Sourcing	--	21	--	mA
Gain Bandwidth Product	GBW		--	300	--	KHz
Slew Rate	SR	$G = +1$, $V_{IN}=4\text{V}$ Step	--	0.1	--	$\text{V}/\mu\text{s}$
Input Voltage Noise	V_N	$f=0.1\text{Hz}$ to 10Hz	--	2	--	μV_{PP}
Input Voltage Noise PSD		$f=1\text{kHz}$	--	45	--	$\text{nV}/\sqrt{\text{Hz}}$
Specified temperature			-50	--	125	$^{\circ}\text{C}$

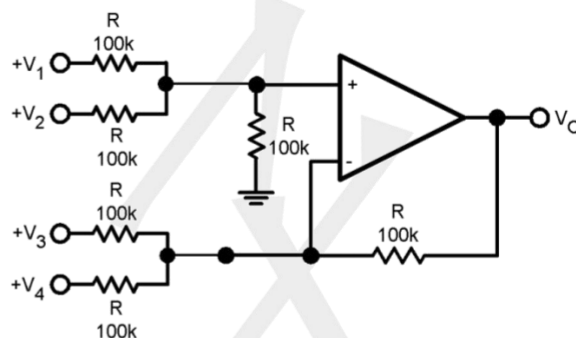
Notes:

- 1: All devices are 100% production tested at $T_A = +25^{\circ}\text{C}$; range is guaranteed by design, not production tested.
- 2: Parameter is guaranteed by design.
- 3: Capacitive load drive means that above a given maximum value, the output waveform will oscillate under the step response.

Typical Application Circuit

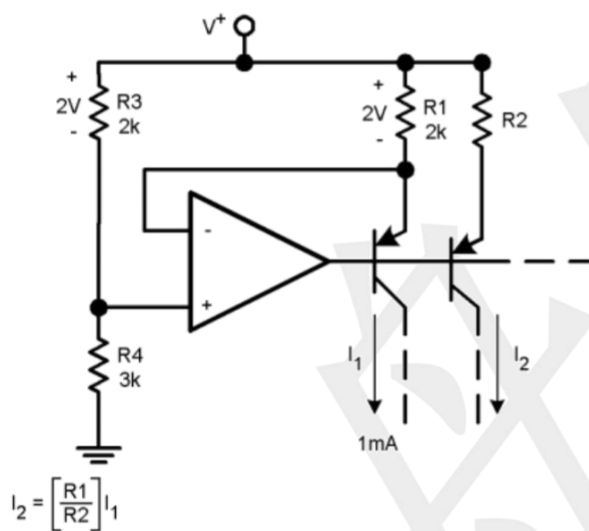


Amplitude modulator circuit

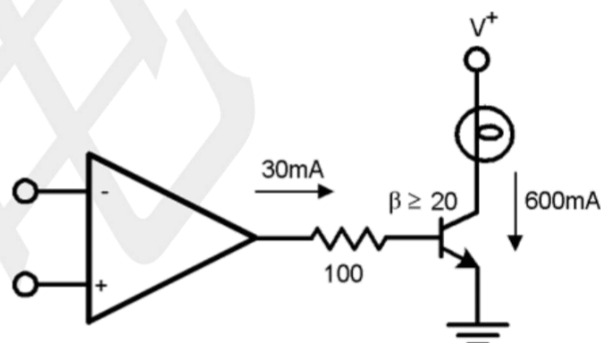


Note: $V_O = V_1 + V_2 - V_3 - V_4, (V_1 + V_2) \geq (V_3 + V_4)$ for $V_O \geq 0V_{DC}$

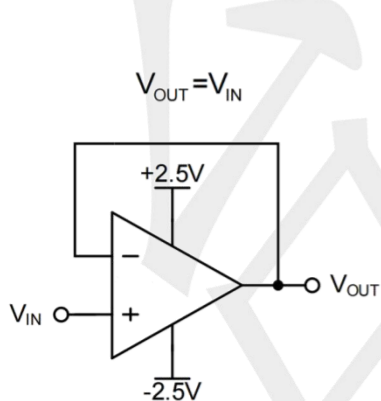
DC adder amplifier
($V_{IN'S} \geq 0V_{DC}, V_O \geq V_{DC}$)



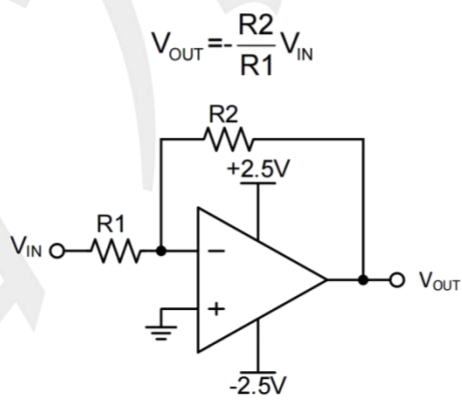
Fixed current source



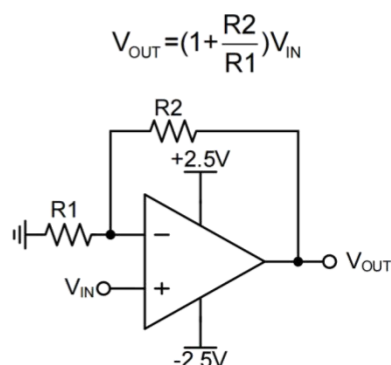
Lamp Driver



Voltage Follower

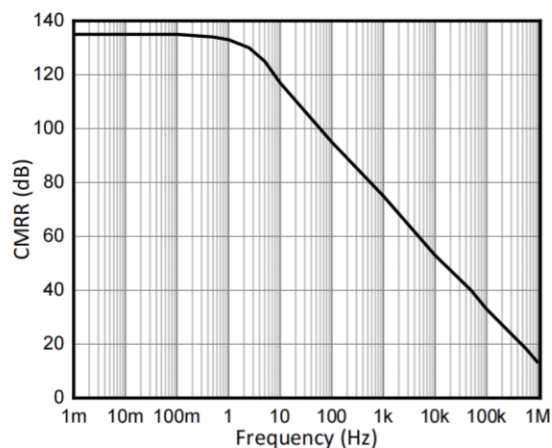


Inverting Proportional Amplifier

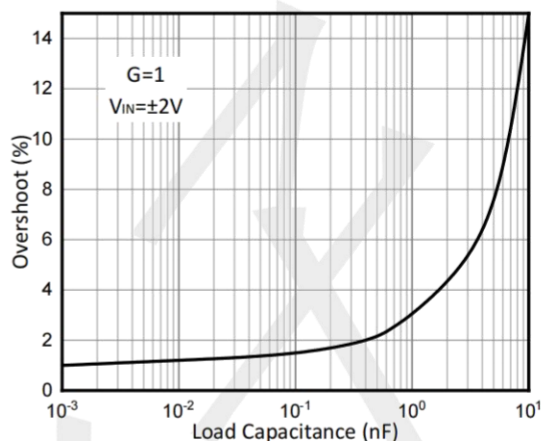


Noninverting Proportional Amplifier

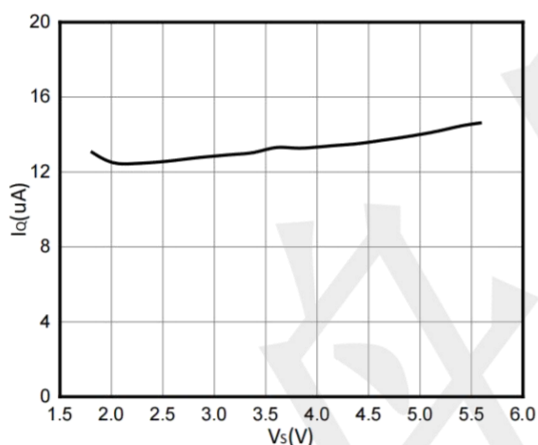
Typical Performance Characteristics (@TA = +25°C, unless otherwise specified.)



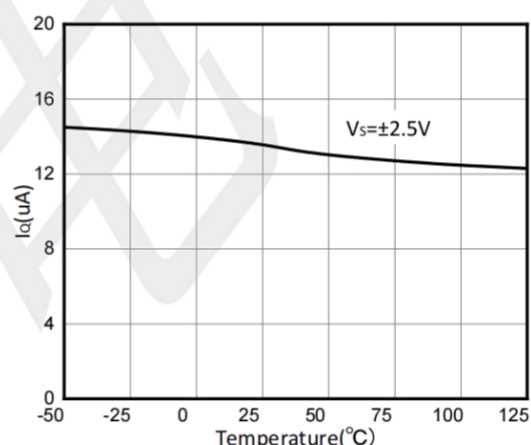
CMRR vs Frequency



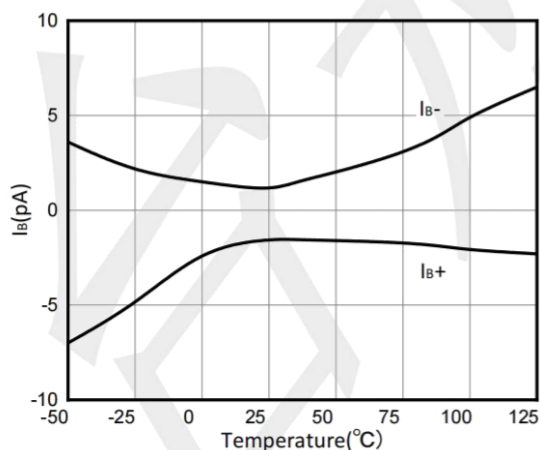
Large-Signal Overshoot vs Load Capacitance



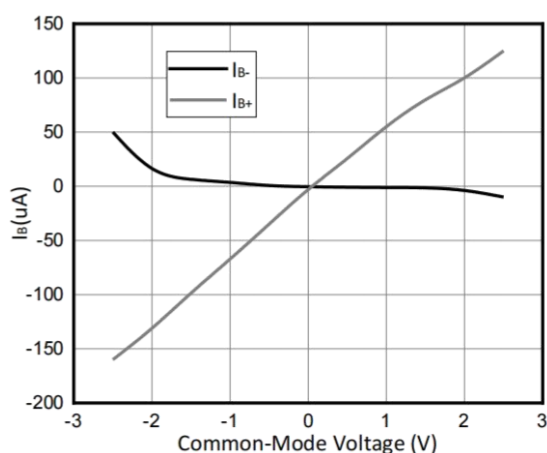
Quiescent Current vs Supply Voltage



Quiescent Current vs Temperature



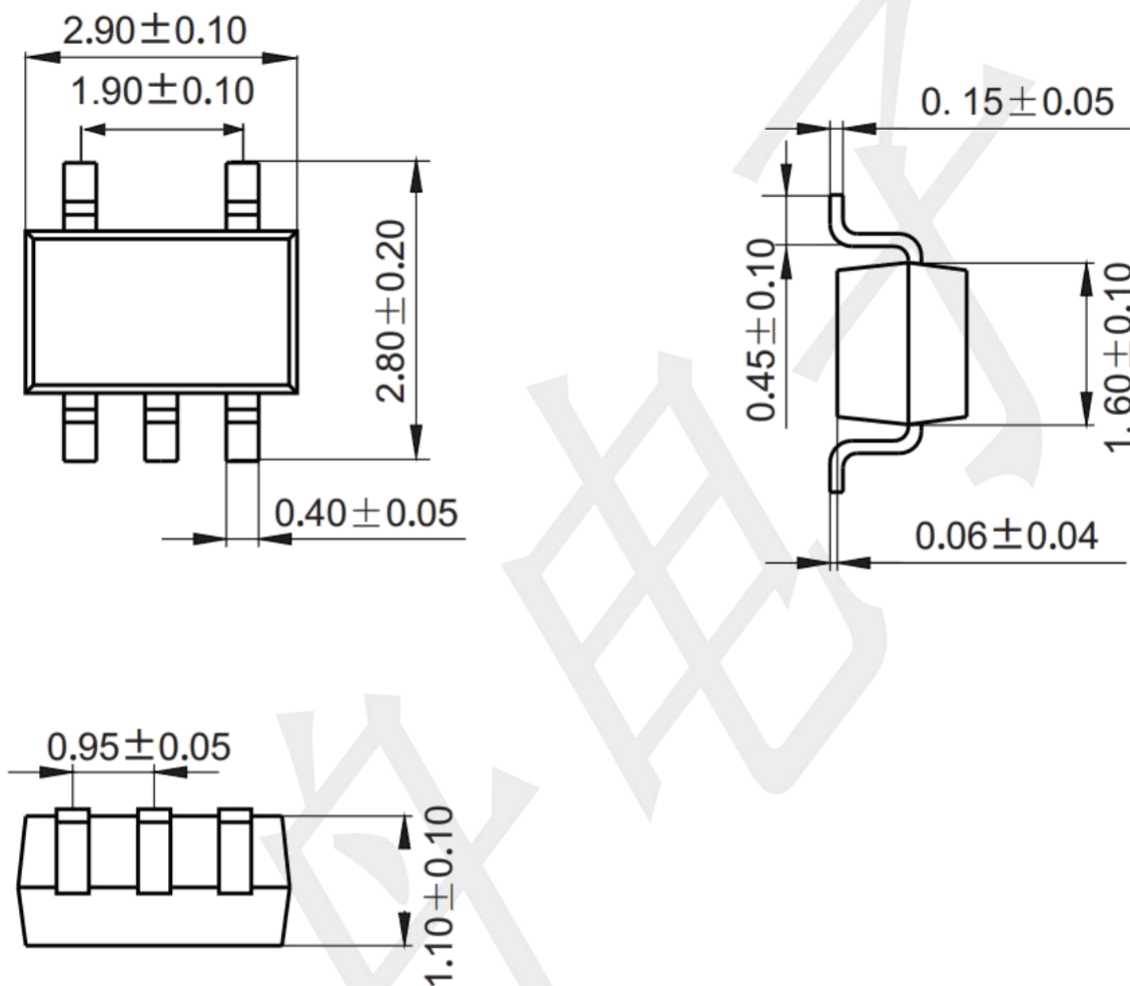
Input Bias Current vs Temperature



Input Bias Current vs Common-Mode Voltage

Package information (Unit: mm)

SOT23-5



Mounting Pad Layout (Unit: mm)

