

Silicon SPDT Switch, Nonreflective, 100 MHz to 45 GHz

**FEATURES**

- ▶ Ultra-wideband frequency range: 100 MHz to 45 GHz
- ▶ Nonreflective design
- ▶ Low insertion loss
  - ▶ 1.2 dB typical to 18 GHz
  - ▶ 1.9 dB typical to 40 GHz
  - ▶ 2.3 dB typical to 45 GHz
- ▶ High Isolation: 43 dB typical to 45 GHz
- ▶ High input linearity
  - ▶ 0.1 dB power compression (P0.1dB): 31 dBm
  - ▶ Third-order intercept (IP3): 55 dBm
- ▶ High power handling at T<sub>CASE</sub> = 85°C
  - ▶ 30 dBm through path
  - ▶ 24 dBm terminated path
  - ▶ 30 dBm hot switching (RFC port)
- ▶ RF settling time (0.1 dB final RF output): 30 ns
- ▶ No low-frequency spurious signals
- ▶ All off-state control
- ▶ Positive control interface: CMOS-/LVTTTL-compatible
- ▶ 20-terminal, 3.0 mm × 3.0 mm LGA package
- ▶ Pin-compatible with [ADRF5023](#), low-frequency cutoff version

**APPLICATIONS**

- ▶ Test and instrumentation
- ▶ Cellular infrastructure: 5G millimeter wave
- ▶ Military radios, radars, and electronic countermeasures (ECMs)
- ▶ Microwave radios and very small aperture terminals (VSATs)
- ▶ Industrial scanners

**FUNCTIONAL BLOCK DIAGRAM**

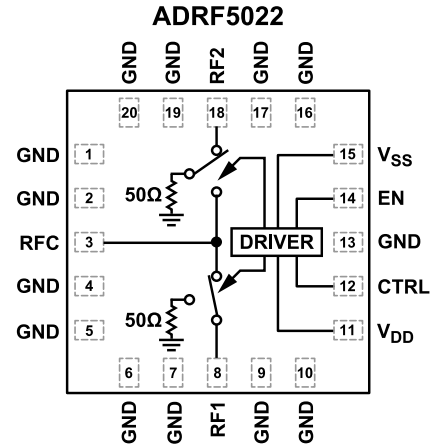


Figure 1. Functional Block Diagram

**GENERAL DESCRIPTION**

The ADRF5022 is a nonreflective, single-pole double-throw (SPDT) switch manufactured in the silicon process.

The ADRF5022 operates from 100 MHz to 45 GHz with a typical insertion loss of 2.3 dB and isolation of 43 dB. The device has an RF input-power handling capability of 30 dBm for the through path, 24 dBm for the terminated path, and 30 dBm for the hot switching at the RF common port.

The ADRF5022 requires a positive supply of +3.3 V and a negative supply of -3.3 V. The device employs complementary metal-oxide semiconductor (CMOS)/low-voltage transistor to transistor logic (LVTTTL)-compatible controls.

The ADRF5022 can also operate with a single positive supply voltage (V<sub>DD</sub>) applied while the negative supply voltage (V<sub>SS</sub>) is connected to ground. In this operating condition, the small signal performance is maintained while the switching characteristics, linearity, and power handling performance is derated. For more details, see [Table 2](#).

The ADRF5022 is pin-compatible with the [ADRF5023](#), low-frequency cutoff version, which operates from 9 kHz to 45 GHz.

The ADRF5022 comes in a 20-terminal, 3.0 mm × 3.0 mm, RoHS-compliant, land grid array (LGA) package and can operate from -40°C to +105°C.

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**REVISION HISTORY****9/2023—Revision 0: Initial Version**

## SPECIFICATIONS

$V_{DD} = 3.3\text{ V}$ ,  $V_{SS} = -3.3\text{ V}$ , CTRL voltage ( $V_{CTRL}$ )/EN voltage ( $V_{EN}$ ) = 0 V or  $V_{DD}$ , and  $T_{CASE} = 25^\circ\text{C}$ , 50  $\Omega$  system, unless otherwise noted.

Table 1. Electrical Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		100		45,000	MHz
INSERTION LOSS						
Between RFC and RF1 and RF2 (On)		100 MHz to 18 GHz		1.2		dB
		18 GHz to 26 GHz		1.4		dB
		26 GHz to 35 GHz		1.6		dB
		35 GHz to 40 GHz		1.9		dB
		40 GHz to 45 GHz		2.3		dB
RETURN LOSS						
RFC and RF1 and RF2 (On)		100 MHz to 18 GHz		20		dB
		18 GHz to 26 GHz		20		dB
		26 GHz to 35 GHz		20		dB
		35 GHz to 40 GHz		20		dB
		40 GHz to 45 GHz		20		dB
RF1 and RF2 (Off)		100 MHz to 18 GHz		19		dB
		18 GHz to 26 GHz		19		dB
		26 GHz to 35 GHz		17		dB
		35 GHz to 40 GHz		14		dB
		40 GHz to 45 GHz		13		dB
ISOLATION						
Between RFC and RF1 and RF2 (Off)		100 MHz to 18 GHz		55		dB
		18 GHz to 26 GHz		55		dB
		26 GHz to 35 GHz		55		dB
		35 GHz to 40 GHz		50		dB
		40 GHz to 45 GHz		47		dB
Between RF1 and RF2		100 MHz to 18 GHz		60		dB
		18 GHz to 26 GHz		58		dB
		26 GHz to 35 GHz		50		dB
		35 GHz to 40 GHz		47		dB
		40 GHz to 45 GHz		43		dB
SWITCHING CHARACTERISTICS						
Rise Time and Fall Time	$t_{RISE}, t_{FALL}$	10% to 90% of RF output ( $RF_{OUT}$ )		3		ns
On Time and Off Time	$t_{ON}, t_{OFF}$	50% $V_{CTRL}$ to 90% of $RF_{OUT}$		20		ns
0.1 dB RF Settling Time		50% $V_{CTRL}$ to 0.1 dB of final $RF_{OUT}$		30		ns
INPUT LINEARITY <sup>1</sup>		f = 100 MHz to 40 GHz				
0.1 dB Power Compression	P0.1dB			31		dBm
Input Third-Order Intercept	IIP3	Two-tone input power = 14 dBm each tone, $\Delta f = 1$ MHz		55		dBm
SUPPLY CURRENT		$V_{DD}$ and $V_{SS}$ pins				
Positive Supply Current	$I_{DD}$			140		$\mu\text{A}$
Negative Supply Current	$I_{SS}$			510		$\mu\text{A}$
DIGITAL CONTROL INPUTS						
Voltage						
Low	$V_{INL}$		0		0.8	V
High	$V_{INH}$		1.2		3.3	V
Current						
Low	$I_{INL}$			<1		$\mu\text{A}$
High	$I_{INH}$	CTRL		<1		$\mu\text{A}$

## SPECIFICATIONS

Table 1. Electrical Specifications (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
		EN		33		$\mu\text{A}$
RECOMMENDED OPERATING CONDITIONS						
Positive Supply Voltage	$V_{\text{DD}}$		3.15		3.45	V
Negative Supply Voltage	$V_{\text{SS}}$		-3.45		-3.15	V
Digital Control Input Voltage	$V_{\text{CTRL}}$		0		$V_{\text{DD}}$	V
RF Input Power <sup>2,3</sup>	$P_{\text{IN}}$	$f = 250 \text{ MHz to } 40 \text{ GHz}$ , $T_{\text{CASE}} = 85^\circ\text{C}$				
Through Path		RF signal is applied to the RFC or through connected RF1 and RF2			30	$\text{dBm}$
Terminated Path		RF signal is applied to terminated RF1 and RF2			24	$\text{dBm}$
Hot Switching		RF signal is applied to the RFC while switching between RF1 and RF2			30	$\text{dBm}$
Case Temperature	$T_{\text{CASE}}$		-40		+105	$^\circ\text{C}$

<sup>1</sup> For input linearity performance over frequency, see Figure 14 to Figure 17.

<sup>2</sup> For power derating over frequency, see Figure 2 and Figure 3.

<sup>3</sup> For 105°C operation, the power handling degrades from the  $T_{\text{CASE}} = 85^\circ\text{C}$  specification by 3 dB.

## SINGLE-SUPPLY OPERATION

$V_{\text{DD}} = 3.3 \text{ V}$ ,  $V_{\text{SS}} = 0 \text{ V}$ ,  $V_{\text{CTRL}}/V_{\text{EN}} = 0 \text{ V}$  or  $V_{\text{DD}}$ ,  $T_{\text{CASE}} = 25^\circ\text{C}$ , 50  $\Omega$  system, unless otherwise noted.

Table 2. Single-Supply Operation Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	$f$		100		45,000	MHz
SWITCHING CHARACTERISTICS						
Rise Time and Fall Time	$t_{\text{RISE}}$ , $t_{\text{FALL}}$	10% to 90% of $\text{RF}_{\text{OUT}}$		22		ns
On Time and Off Time	$t_{\text{ON}}$ , $t_{\text{OFF}}$	50% $V_{\text{CTRL}}$ to 90% of $\text{RF}_{\text{OUT}}$		65		ns
0.1 dB RF Settling Time		50% $V_{\text{CTRL}}$ to 0.1 dB of final $\text{RF}_{\text{OUT}}$		90		ns
INPUT LINEARITY						
0.1 dB Power Compression	P0.1dB	$f = 250 \text{ MHz to } 40 \text{ GHz}$		17		$\text{dBm}$
Input Third-Order Intercept	IIP3	Two-tone input power = 0 dBm each tone, $\Delta f = 1 \text{ MHz}$		44		$\text{dBm}$
RECOMMENDED OPERATING CONDITIONS						
RF Input Power <sup>1,2</sup>	$P_{\text{IN}}$	$f = 250 \text{ MHz to } 40 \text{ GHz}$ , $T_{\text{CASE}} = 85^\circ\text{C}$				
Through Path		RF signal is applied to the RFC or through connected RF1 and RF2			17	$\text{dBm}$
Terminated Path		RF signal is applied to terminated RF1 and RF2			12	$\text{dBm}$
Hot Switching		RF signal is applied to the RFC while switching between RF1 and RF2			17	$\text{dBm}$

<sup>1</sup> For power derating over frequency, see Figure 2 and Figure 3.

<sup>2</sup> For 105°C operation, the power handling degrades from the  $T_{\text{CASE}} = 85^\circ\text{C}$  specification by 3 dB.

## ABSOLUTE MAXIMUM RATINGS

For recommended operating conditions, see [Table 1](#) and [Table 2](#).

**Table 3. Absolute Maximum Ratings**

Parameter	Rating
Supply Voltage	
Positive	-0.3 V to +3.6 V
Negative	-3.6 V to +0.3 V
Digital Control Input Voltage	
Voltage	-0.3 V to $V_{DD} + 0.3$ V
Current	3 mA
RF Input Power, Dual Supply <sup>1</sup> ( $V_{DD} = 3.3$ V, $V_{SS} = -3.3$ V, $f = 250$ MHz to 40 GHz, $T_{CASE} = 85^{\circ}\text{C}$ )	
Through Path	31 dBm
Terminated Path	25 dBm
Hot Switching (RFC Port)	31 dBm
RF Input Power, Single Supply <sup>1</sup> ( $V_{DD} = 3.3$ V, $V_{SS} = 0$ V, $f = 250$ MHz to 40 GHz, $T_{CASE} = 85^{\circ}\text{C}$ )	
Through Path	18 dBm
Terminated Path	13 dBm
Hot Switching (RFC Port)	18 dBm
RF Power Under Unbiased Condition ( $V_{DD}$ , $V_{SS} = 0$ V)	18 dBm
Temperature	
Junction ( $T_J$ )	135°C
Storage	-65°C to +150°C
Reflow	260°C

<sup>1</sup> For power derating over frequency, see [Figure 2](#) and [Figure 3](#).

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to the printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

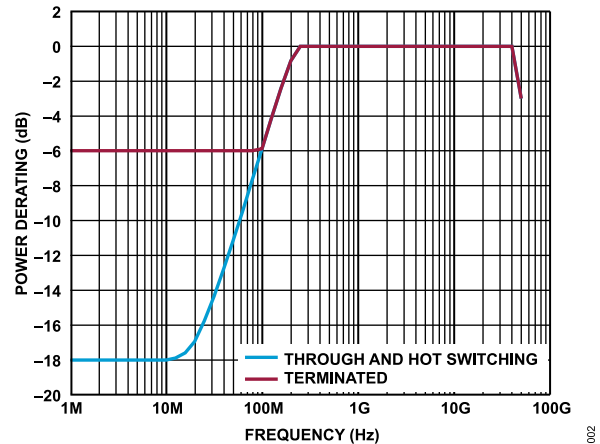
$\theta_{JC}$  is the junction-to-case bottom (channel-to-package bottom) thermal resistance.

**Table 4. Thermal Resistance**

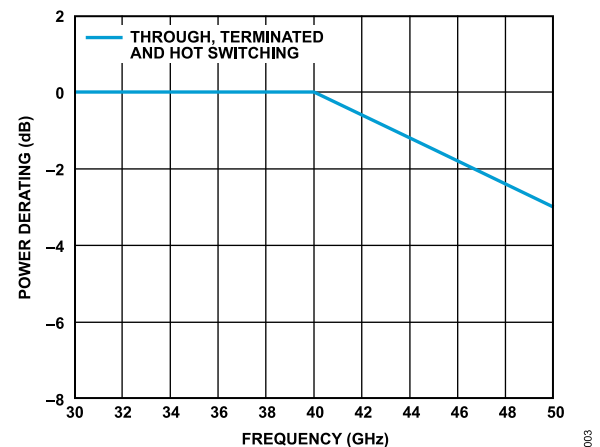
Package Type	$\theta_{JC}$ <sup>1</sup>	Unit
CC-20-19		
Through Path	120	°C/W
Terminated Path	200	°C/W

<sup>1</sup>  $\theta_{JC}$  is determined by simulation under the following conditions: the heat transfer is due solely to the thermal conduction from the channel through the ground pad to the PCB, and the ground pad is held constant at the operating temperature of 85°C.

## POWER DERATING CURVES



**Figure 2. Power Derating vs. Frequency, Low-Frequency Detail,  $T_{CASE} = 85^{\circ}\text{C}$**



**Figure 3. Power Derating vs. Frequency, High-Frequency Detail,  $T_{CASE} = 85^{\circ}\text{C}$**

**ABSOLUTE MAXIMUM RATINGS****ELECTROSTATIC DISCHARGE (ESD) RATINGS**

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

**ESD Ratings for ADRF5022**

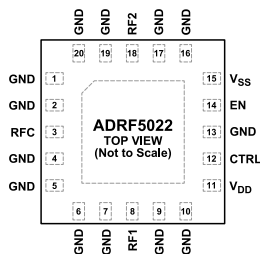
*Table 5. ADRF5022, 20-Terminal LGA*

ESD Model	Withstand Threshold (V)	Class
HBM	±1250 for RFx pins	1C
	±2000 for supply and control pins	2
CDM	±500 for all pins	C2

**ESD CAUTION**

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES  
 1. EXPOSED PAD. THE EXPOSED PAD MUST BE CONNECTED TO THE RF/DC GROUND OF THE PCB.

Figure 4. Pin Configuration (Top View)

Table 6. Pin Function Descriptions

Pin Number	Mnemonic	Description
1, 2, 4 to 7, 9, 10, 13, 16, 17, 19, 20	GND	Ground. The GND pins must be connected to the RF and DC ground of the PCB.
3	RFC	RF Common Port. The RFC pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC. For the interface schematic, see Figure 5.
8	RF1	RF Throw Port 1. The RF1 pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC. for the interface schematic, see Figure 5.
11	V <sub>DD</sub>	Positive Supply Voltage. For the interface schematic, see Figure 6.
12	CTRL	Control Input Voltage. For the interface schematic, see Figure 8.
14	EN	Enable Input Voltage. For the interface schematic, see Figure 9.
15	V <sub>SS</sub>	Negative Supply Voltage. For the interface schematic, see Figure 7.
18	RF2	RF Throw Port 2. The RF2 pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC. For the interface schematic, see Figure 5.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF/DC ground of the PCB.

INTERFACE SCHEMATICS

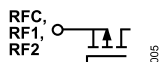


Figure 5. RFx Pins (RFC, RF1, RF2) Interface Schematic

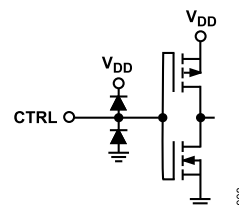


Figure 8. CTRL Pin Interface Schematic

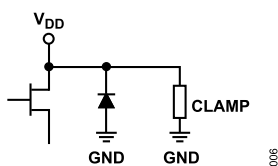


Figure 6. V<sub>DD</sub> Pin Interface Schematic

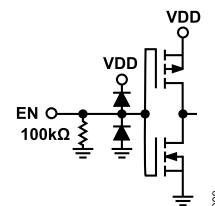


Figure 9. EN Pin Interface Schematic

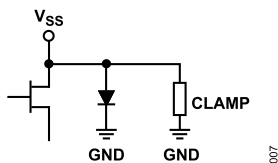


Figure 7. V<sub>SS</sub> Pin Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

$V_{DD} = 3.3\text{ V}$ ,  $V_{SS} = -3.3\text{ V}$  or  $0\text{ V}$ ,  $V_{CTRL}/V_{EN} = 0\text{ V}$  or  $V_{DD}$ , and  $T_{CASE} = 25^\circ\text{C}$  in a  $50\ \Omega$  system, unless otherwise noted. Measured on the ADRF5022-EVALZ.

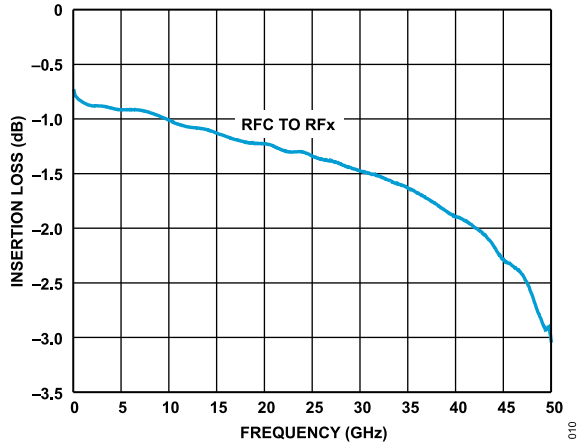


Figure 10. Insertion Loss vs. Frequency at Room Temperature for RF1 and RF2

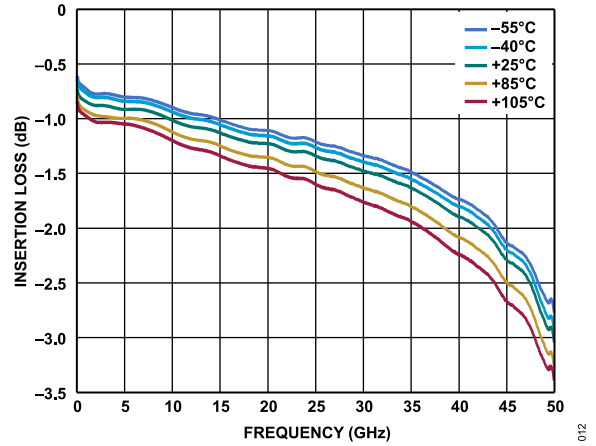


Figure 12. Insertion Loss vs. Frequency over Temperature

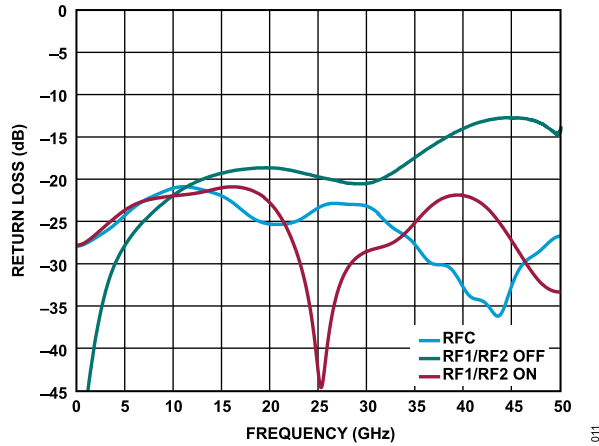


Figure 11. Return Loss vs. Frequency

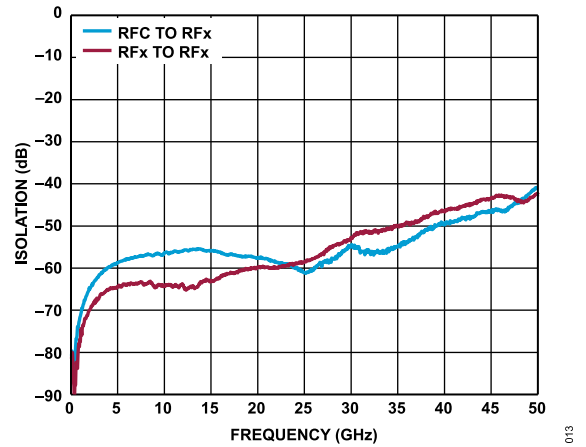


Figure 13. Isolation vs. Frequency



TYPICAL PERFORMANCE CHARACTERISTICS

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

$V_{DD} = 3.3\text{ V}$ ,  $V_{SS} = -3.3\text{ V}$ ,  $V_{CTRL}/V_{EN} = 0\text{ V}$  or  $V_{DD}$ , and  $T_{CASE} = 25^\circ\text{C}$  in a  $50\ \Omega$  system, unless otherwise noted. The large-signal performance parameters are measured on the [ADRF5022-EVALZ](#).

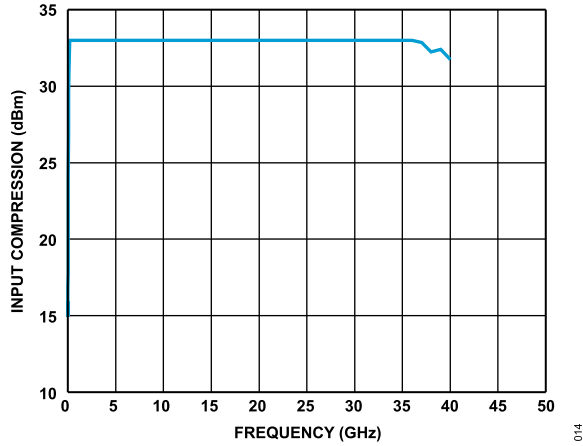


Figure 14. 0.1 dB Input Compression vs. Frequency

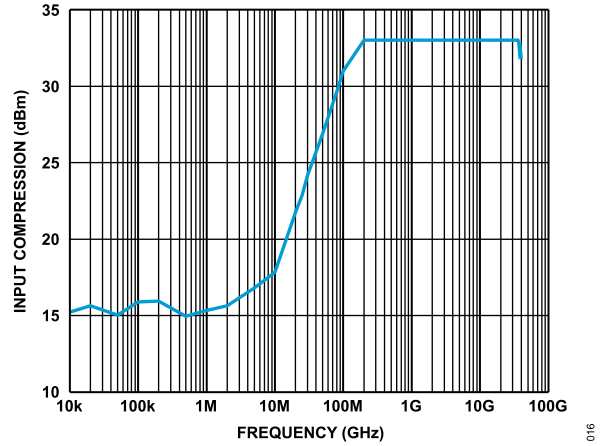


Figure 16. 0.1 dB Input Compression vs. Frequency, Low-Frequency Detail

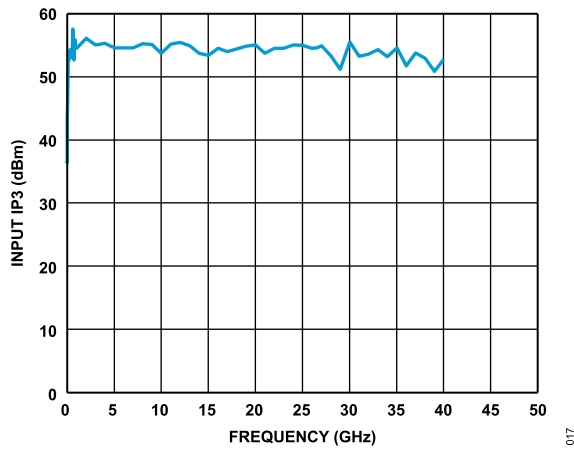


Figure 15. Input IP3 vs. Frequency

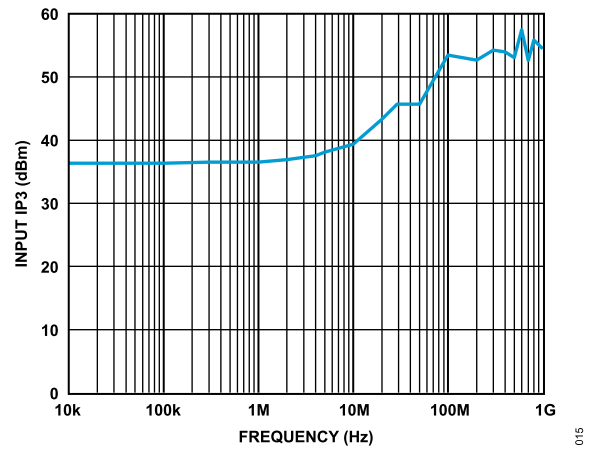


Figure 17. Input IP3 vs. Frequency, Low-Frequency Detail

## THEORY OF OPERATION

The ADRF5022 integrates a driver to perform logic function internally and to provide the advantage of a simplified control interface. The driver features two digital control input pins (CTRL and EN) that control the state of RF paths, determining which RF port is in insertion loss state and which RF port is in isolation state (see [Table 7](#)).

### POWER SUPPLY

The ADRF5022 requires a positive supply voltage applied to the  $V_{DD}$  pin and a negative supply voltage applied to the  $V_{SS}$  pin. Bypassing capacitors are recommended on the supply lines to minimize RF coupling.

The ideal power-up sequence is as follows:

1. Connect the ground.
2. Power up  $V_{DD}$  and  $V_{SS}$ . Power up  $V_{SS}$  after  $V_{DD}$  to avoid current transients on  $V_{DD}$  during ramp-up.
3. Power up the digital control inputs. Power the digital control inputs before the  $V_{DD}$  supply can inadvertently forward bias and damage the internal ESD protection structures. To avoid this damage, use a series 1 k $\Omega$  resistor to limit the current flowing into the control pin. Use pull-up or pull-down resistors if the controller output is in a high impedance state after  $V_{DD}$  is powered up and the control pins are not driven to a valid logic state.
4. Apply an RF input signal.

The ideal power-down sequence is the reverse order of the power-up sequence.

### Single-Supply Operation

The ADRF5022 can operate with a single positive supply voltage applied to the  $V_{DD}$  and  $V_{SS}$  pin connected to ground. However, some performance difference can occur in switching characteristics and large signal. For more details, see [Table 1](#).

### RF INPUT AND OUTPUT

All of the RF ports (RFC, RF1, RF2) are DC-coupled to 0 V, and no DC blocking is required at the RF ports when the RF line potential is equal to 0 V.

The RF ports are internally matched to 50  $\Omega$ . Therefore, external matching networks are not required.

When the EN pin is logic low, the logic level applied to the CTRL pin determines which RF port is in insertion loss state and which RF port is in isolation state. The insertion loss path conducts the RF signal between the selected RF throw port and the RF common port. The isolation path provides high loss between the insertion loss path and the unselected RF throw port that is terminated to an internal 50  $\Omega$  resistor.

When the EN pin is logic high, the switch is in an all-off state regardless of the logic state of the CTRL pin. Both the RF1 to RFC path and the RF2 to RFC path are in an isolation state. The RF1 and RF2 ports are terminated to internal 50  $\Omega$  resistors, and the RFC port becomes reflective open.

The switch design is bidirectional with equal power handling capabilities. The RF input signal can be applied to the RFC port or the selected RF throw port.

**Table 7. Control Voltage Truth Table**

EN	Digital Control Inputs		RF Paths	
	CTRL		RF1 to RFC	RF2 to RFC
Low	Low		Isolation (off)	Insertion loss (on)
Low	High		Insertion loss (on)	Isolation (off)
High	Low		Isolation (off)	Isolation (off)
High	High		Isolation (off)	Isolation (off)

**APPLICATIONS INFORMATION**

The ADRF5022 has two power supply pins ( $V_{DD}$  and  $V_{SS}$ ) and two control pins (CTRL and EN). Figure 18 shows the external components and connections for supply and control pins. The  $V_{DD}$  and the  $V_{SS}$  pin are decoupled with a 100 pF multilayer ceramic capacitor. The device pinout allows the placement of the decoupling capacitors close to the device. No other external components are needed for bias and operation, except DC blocking capacitors on the RF pins when the RF lines are biased at a voltage different than 0 V. For more details, see the [Pin Configuration and Function Descriptions](#) section.

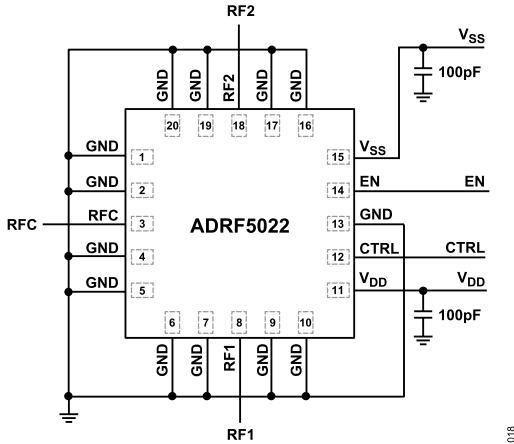


Figure 18. Recommended Schematic

**RECOMMENDATIONS FOR PCB DESIGN**

The RF ports are matched to 50  $\Omega$  internally, and the pinout is designed to mate a coplanar waveguide (CPWG) with a 50  $\Omega$  characteristic impedance on the PCB. Figure 19 shows the referenced CPWG RF trace design for an RF substrate with 8 mil thick Rogers RO4003 dielectric material. The RF trace with a 14 mil width and a 7 mil clearance is recommended for 1.5 mil finished copper thickness.

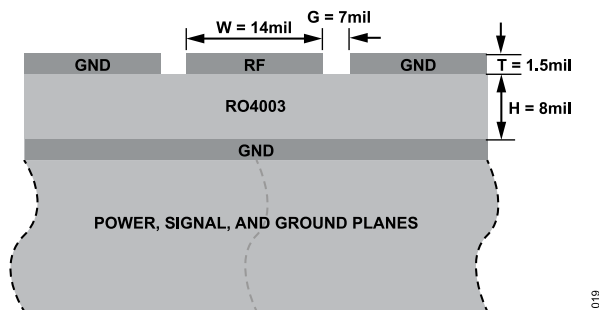


Figure 19. Example PCB Stack-Up

Figure 20 shows the routing of the RF traces, supply, and control signals from the device. The ground planes are connected with as many filled through vias as allowed for optimal RF and thermal performance. The primary thermal path for the device is the bottom side.

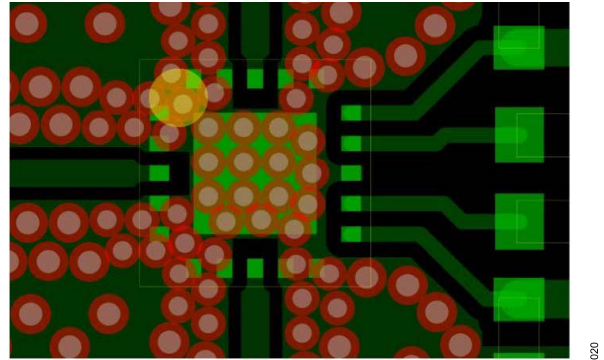


Figure 20. PCB Routings

Figure 21 shows the recommended layout from the device RF pins to the 50  $\Omega$  CPWG on the referenced stack-up. PCB pads are drawn 1:1 to device pads. The ground pads are drawn solder mask defined, and the signal pads are drawn as pad defined. The RF trace from the PCB pad is extended with the same width until the package edge and tapered to the RF trace with a 45° angle. The paste mask is also designed to match the pad without any aperture reduction and is divided into multiple openings for the paddle.

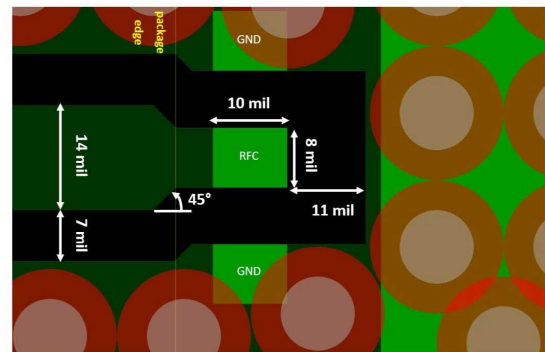
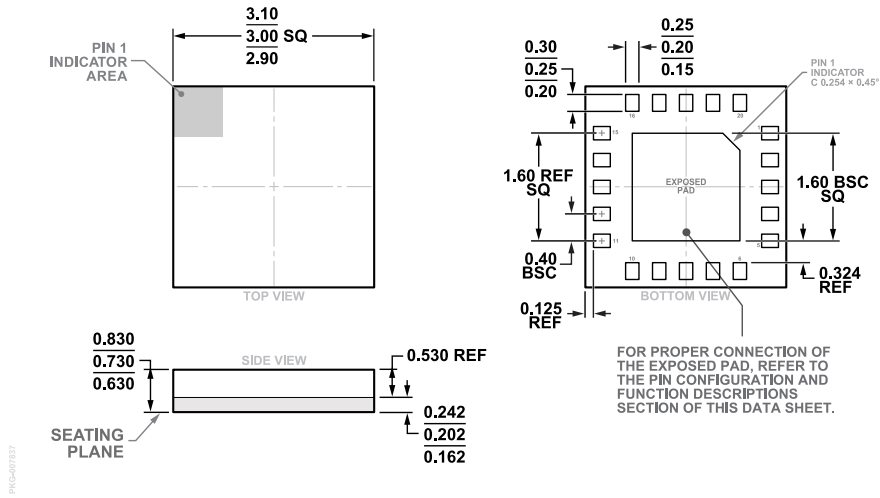


Figure 21. Recommended RF Pin Transitions

For alternate PCB stack-ups with different dielectric thickness and CPWG design and for further recommendations, contact [Technical Support](#).

OUTLINE DIMENSIONS



**Figure 22. 20-Terminal Land Grid Array [LGA]  
3.0 mm x 3.0 mm Body and 0.730 mm Package Height  
(CC-20-19)  
Dimensions Shown in millimeters**

Updated: September 15, 2023

ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Packing Quantity	Package Option
ADRF5022BCCZN	-40°C to +105°C	20-Terminal Land Grid Array [LGA]	Reel, 500	CC-20-19
ADRF5022BCCZN-R7	-40°C to +105°C	20-Terminal Land Grid Array [LGA]	Reel, 500	CC-20-19

<sup>1</sup> Z = RoHS-Compliant Part.

EVALUATION BOARDS

Model <sup>1</sup>	Description
ADRF5022-EVALZ	Evaluation Board

<sup>1</sup> Z = RoHS-Compliant Part.