

BSP19A

NPN Silicon Epitaxial Transistor

This family of NPN Silicon Epitaxial transistors is designed for use as a general purpose amplifier and in switching applications. The device is housed in the SOT-223 package which is designed for medium power surface mount applications.

Features

- High Voltage
- The SOT-223 Package Can Be Soldered Using Wave or Reflow
- SOT-223 Package Ensures Level Mounting, Resulting in Improved Thermal Conduction, and Allows Visual Inspection of Soldered Joints
- The Formed Leads Absorb Thermal Stress During Soldering, Eliminating the Possibility of Damage to the Die
- PNP Complement is BSP16T1G
- Moisture Sensitivity Level (MSL): 1
- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage (Open Base)	V_{CEO}	350	Vdc
Collector-Base Voltage (Open Emitter)	V_{CBO}	400	Vdc
Emitter-Base Voltage (Open Collector)	V_{EBO}	5.0	Vdc
Collector Current (DC)	I_C	100	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 1) Derate above 25°C	P_D	0.8 6.4	W mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	156	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
ESD - Human Body Model	HBM	3B	V
ESD - Machine Model	MM	C	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

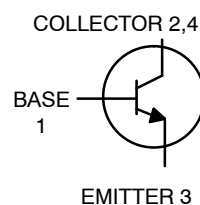
1. Device mounted on a FR-4 glass epoxy printed circuit board using minimum recommended footprint.



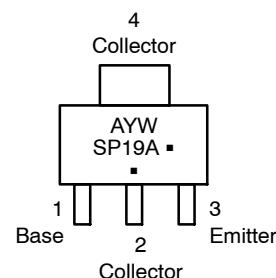
ON Semiconductor®

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SOT-223 PACKAGE NPN SILICON HIGH VOLTAGE TRANSISTOR SURFACE MOUNT



MARKING DIAGRAM



A = Assembly Location
Y = Year
W = Work Week
SP19A = Specific Device Code
▪ = Pb-Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
BSP19AT1G	SOT-223 (Pb-Free)	1000 / Tape & Reel
NSVBSP19AT1G	SOT-223 (Pb-Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

BSP19A

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristics	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage ($I_C = 1.0\text{ mA}$, $I_B = 0$)	$V_{(BR)CEO}$	350	–	Vdc
Collector-Base Cutoff Current ($V_{CB} = 400\text{ Vdc}$, $I_E = 0$)	I_{CBO}	–	20	nAdc
Emitter-Base Cutoff Current ($V_{EB} = 5.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	–	10	μAdc
ON CHARACTERISTICS (Note 2)				
DC Current Gain ($I_C = 20\text{ mA}$, $V_{CE} = 10\text{ Vdc}$)	h_{FE}	40	–	–
Current-Gain — Bandwidth Product ($I_C = 10\text{ mA}$, $V_{CE} = 10\text{ Vdc}$, $f = 5.0\text{ MHz}$)	f_T	70	–	MHz
Collector-Emitter Saturation Voltage ($I_C = 50\text{ mA}$, $I_B = 4.0\text{ mA}$)	$V_{CE(sat)}$	–	0.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 50\text{ mA}$, $I_B = 4.0\text{ mA}$)	$V_{BE(sat)}$	–	1.3	Vdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle = 2.0%

TYPICAL CHARACTERISTICS

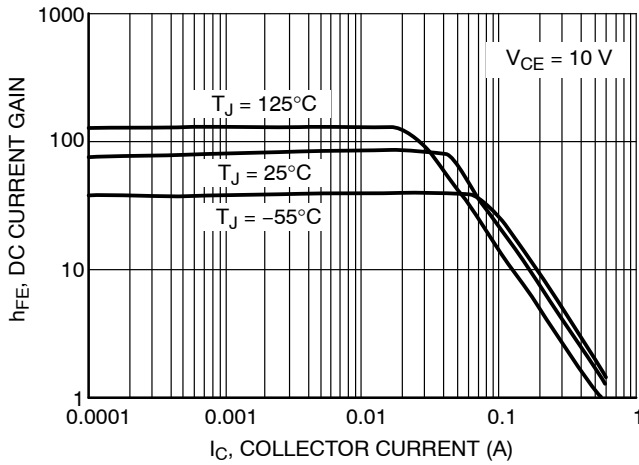


Figure 1. DC Current Gain

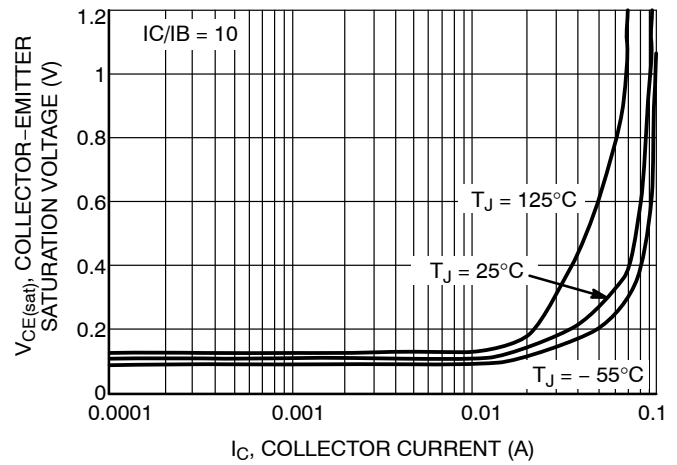


Figure 2. Collector Saturation Voltage

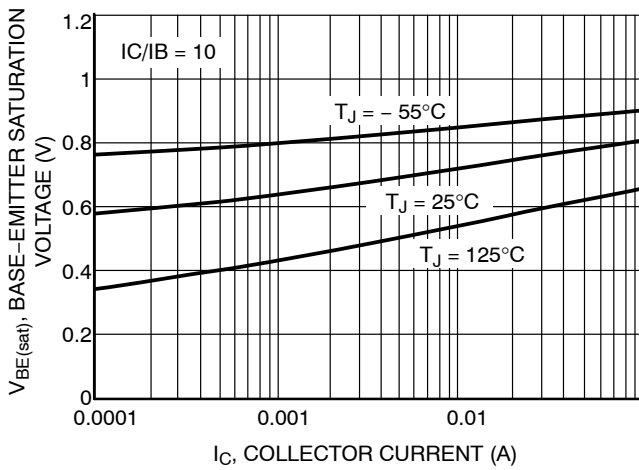


Figure 3. Base Saturation Voltage

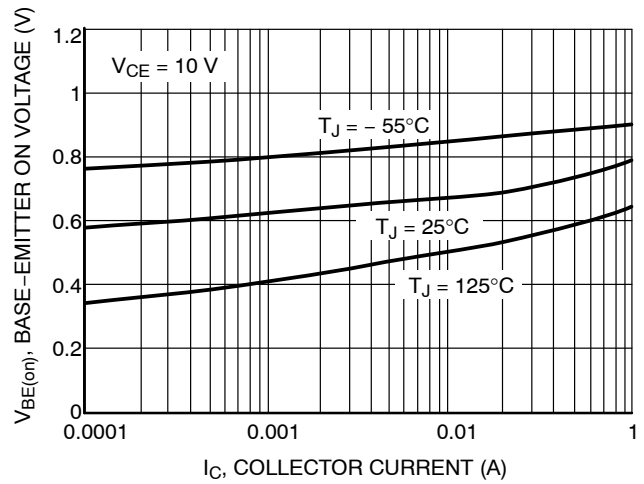


Figure 4. Base ON Voltage

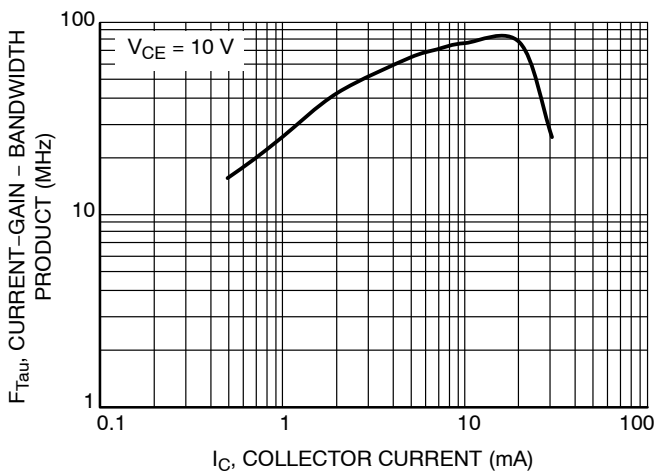


Figure 5. Current Gain - Bandwidth Product

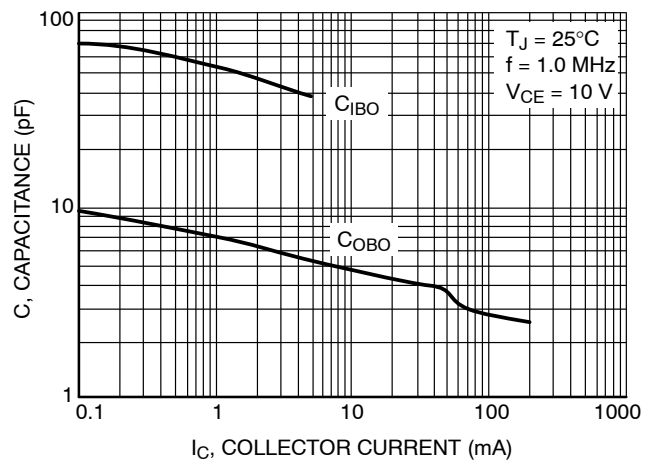


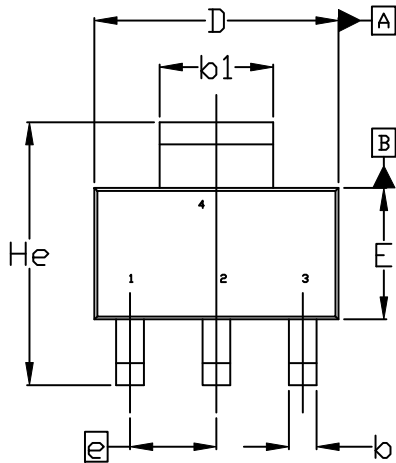
Figure 6. Capacitance



SCALE 1:1

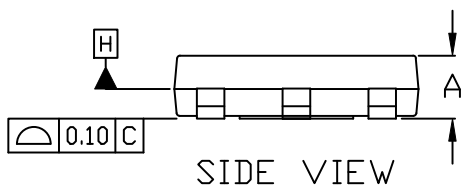
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ISSUE R

DATE 02 OCT 2018

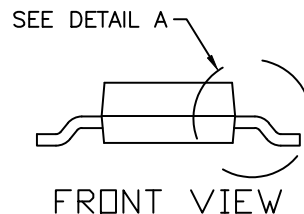


TOP VIEW

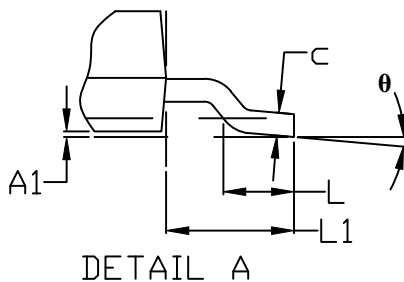
$\oplus 0.10 \text{ (M)} \text{ C A B}$
NOTE 5



SIDE VIEW



FRONT VIEW

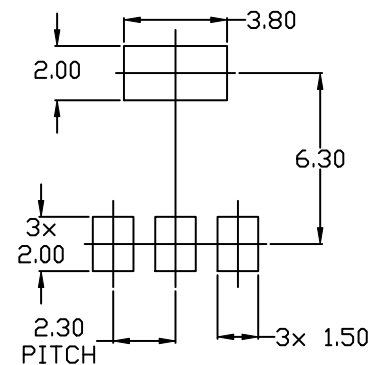


DETAIL A

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

MILLIMETERS			
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



RECOMMENDED MOUNTING
FOOTPRINT

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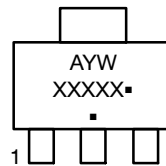
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DATE 02 OCT 2018

STYLE 1: PIN 1. BASE 2. COLLECTOR 3. EMITTER 4. COLLECTOR	STYLE 2: PIN 1. ANODE 2. CATHODE 3. NC 4. CATHODE	STYLE 3: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN	STYLE 4: PIN 1. SOURCE 2. DRAIN 3. GATE 4. DRAIN	STYLE 5: PIN 1. DRAIN 2. GATE 3. SOURCE 4. GATE
STYLE 6: PIN 1. RETURN 2. INPUT 3. OUTPUT 4. INPUT	STYLE 7: PIN 1. ANODE 1 2. CATHODE 3. ANODE 2 4. CATHODE	STYLE 8: CANCELLED	STYLE 9: PIN 1. INPUT 2. GROUND 3. LOGIC 4. GROUND	STYLE 10: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE
STYLE 11: PIN 1. MT 1 2. MT 2 3. GATE 4. MT 2	STYLE 12: PIN 1. INPUT 2. OUTPUT 3. NC 4. OUTPUT	STYLE 13: PIN 1. GATE 2. COLLECTOR 3. EMITTER 4. COLLECTOR		

**GENERIC
MARKING DIAGRAM***



A = Assembly Location
 Y = Year
 W = Work Week
 XXXXX = Specific Device Code
 ■ = Pb-Free Package

(Note: Microdot may be in either location)
 *This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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