

MOSFET – N-Channel, Shielded Gate, POWER trench®

100 V, 20 A, 24 mΩ

FDMC86102

General Description

This N-Channel MOSFET is produced using onsemi's advanced POWER trench process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance.

Features

- Shielded Gate MOSFET Technology
- Max $R_{DS(on)}$ = 24 mΩ at V_{GS} = 10 V, I_D = 7 A
- Max $R_{DS(on)}$ = 38 mΩ at V_{GS} = 6 V, I_D = 5 A
- Low Profile – 1 mm max in Power 33
- 100% UIL Tested
- This Device is Pb-Free, Halide Free and is RoHS Compliant

Applications

- DC-DC Conversion

MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

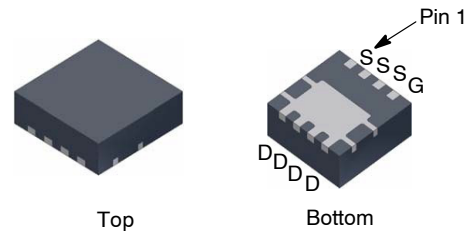
Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current – Continuous T_C = 25°C	20	A
	– Continuous T_A = 25°C (Note 1a)	7	
	– Pulsed (Note 4)	60	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	72	mJ
P_D	Power Dissipation T_C = 25°C	41	W
	Power Dissipation T_A = 25°C (Note 1a)	2.3	
T_J , T_{STG}	Operating and Storage Junction Temperature Range	–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

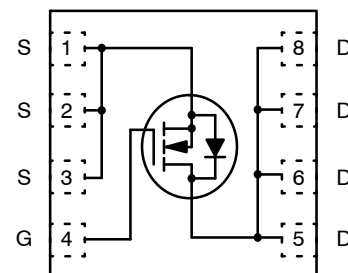
Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

V_{DS}	$R_{DS(on)}$ MAX	I_D MAX
100 V	24 mΩ @ 10 V	20 A
	38 mΩ @ 6 V	



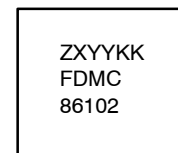
PQFN8 3.3 x 3.3, 0.65P
CASE 483AK

PIN ASSIGNMENT



N-CHANNEL MOSFET

MARKING DIAGRAM



Z = Assembly Site Code
X = Year Code
YY = Weekly Code
KK = Lot Code
FDMC86102 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
FDMC86102	PQFN8 (Pb-Free, Halide Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](http://www.onsemi.com/BRD8011/D).

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$	100	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to 25°C	–	69	–	mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80\ \text{V}$, $V_{GS} = 0\ \text{V}$	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}$, $V_{DS} = 0\ \text{V}$	–	–	± 100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\ \mu\text{A}$	2.0	3.1	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to 25°C	–	–9	–	mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}$, $I_D = 7\ \text{A}$	–	19.4	24	m Ω
		$V_{GS} = 6\ \text{V}$, $I_D = 5\ \text{A}$	–	26.8	38	
		$V_{GS} = 10\ \text{V}$, $I_D = 7\ \text{A}$, $T_J = 125^\circ\text{C}$	–	32.8	41	
g_{FS}	Forward Transconductance	$V_{DS} = 10\ \text{V}$, $I_D = 7\ \text{A}$	–	19	–	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 50\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1\ \text{MHz}$	–	725	965	pF
C_{oss}	Output Capacitance		–	175	235	pF
C_{rss}	Reverse Transfer Capacitance		–	15	25	pF
R_g	Gate Resistance		–	0.5	–	Ω

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\ \text{V}$, $I_D = 7\ \text{A}$, $V_{GS} = 10\ \text{V}$, $R_{GEN} = 6\ \Omega$	–	8	17	ns
t_r	Rise Time		–	4	10	
$t_{d(off)}$	Turn-Off Delay Time		–	14	25	
t_f	Fall Time		–	4	10	
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $10\ \text{V}$, $V_{DD} = 50\ \text{V}$, $I_D = 7\ \text{A}$	–	13	18	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $5\ \text{V}$, $V_{DD} = 50\ \text{V}$, $I_D = 7\ \text{A}$	–	8	11	
Q_{gs}	Total Gate Charge	$V_{DD} = 50\ \text{V}$, $I_D = 7\ \text{A}$	–	3.7	–	nC
Q_{gd}	Gate to Drain "Miller" Charge		–	3.6	–	

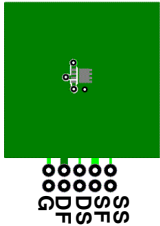
DRAIN-SOURCE DIODE CHARACTERISTICS

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}$, $I_S = 7\ \text{A}$ (Note 2)	–	0.81	1.3	V
		$V_{GS} = 0\ \text{V}$, $I_S = 2\ \text{A}$ (Note 2)	–	0.75	1.2	V
t_{rr}	Reverse Recovery Time	$I_F = 7\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$	–	44	70	ns
Q_{rr}	Reverse Recovery Charge		–	40	65	nC

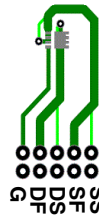
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

- $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



- 53°C/W when mounted on a 1 in² pad of 2 oz copper



- 125°C/W when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.
- Starting $T_J = 25^\circ\text{C}$; N-ch: $L = 1\ \text{mH}$, $I_{AS} = 12\ \text{A}$, $V_{DD} = 90\ \text{V}$, $V_{GS} = 10\ \text{V}$.
- Pulse I_d refers to Figure.11 Forward Bias Safe Operation Area.

TYPICAL CHARACTERISTICS

($T_J = 25^\circ\text{C}$ unless otherwise noted)

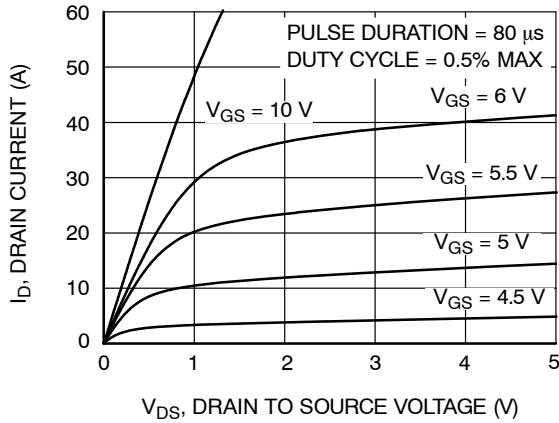


Figure 1. On-Region Characteristics

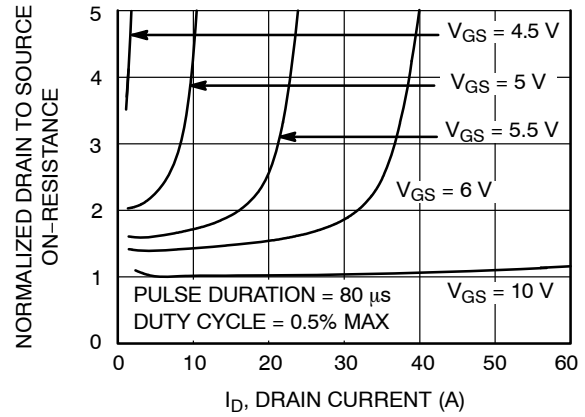


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

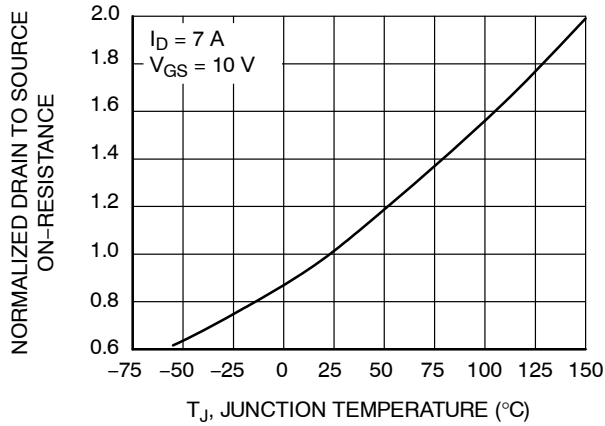


Figure 3. Normalized On Resistance vs. Junction Temperature

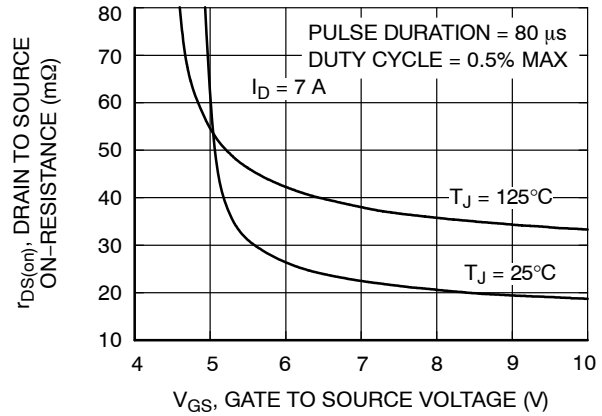


Figure 4. On-Resistance vs. Gate to Source Voltage

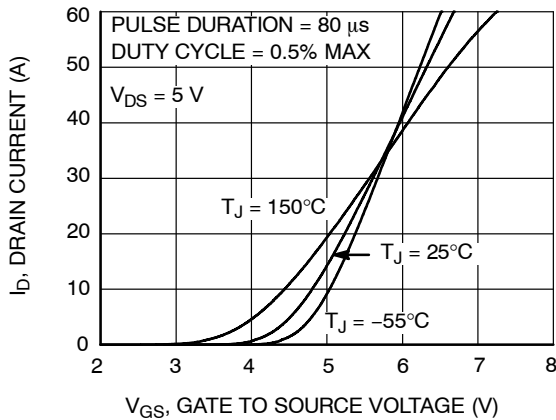


Figure 5. Transfer Characteristics

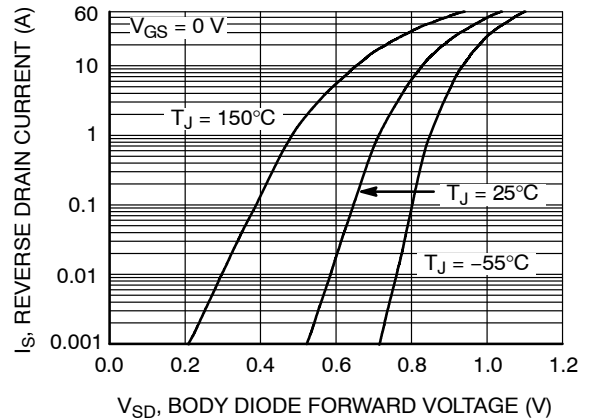


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

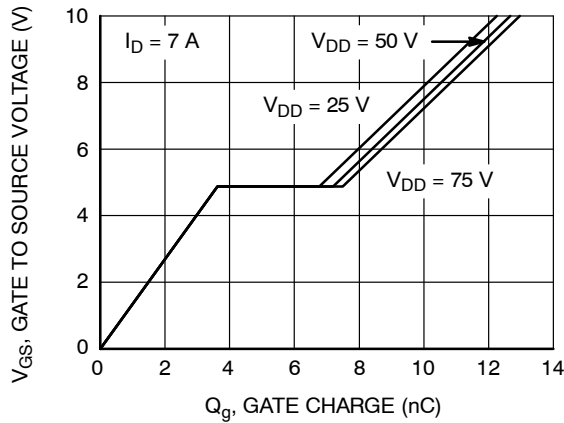


Figure 7. Gate Charge Characteristics

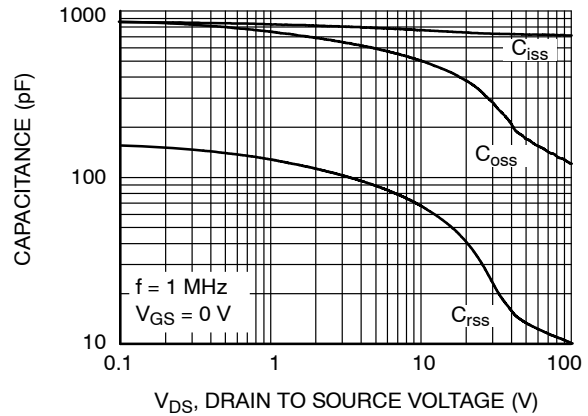


Figure 8. Capacitance vs. Drain to Source Voltage

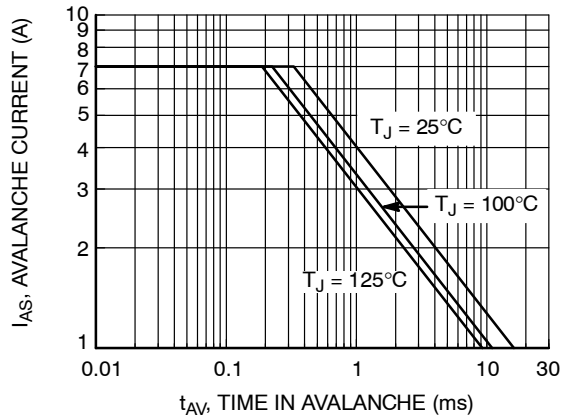


Figure 9. Unclamped Inductive Switching Capability

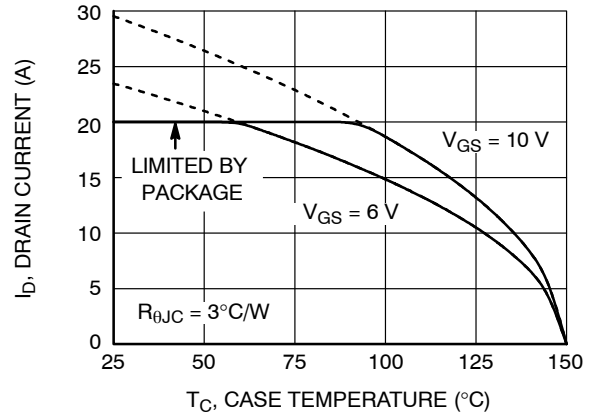


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

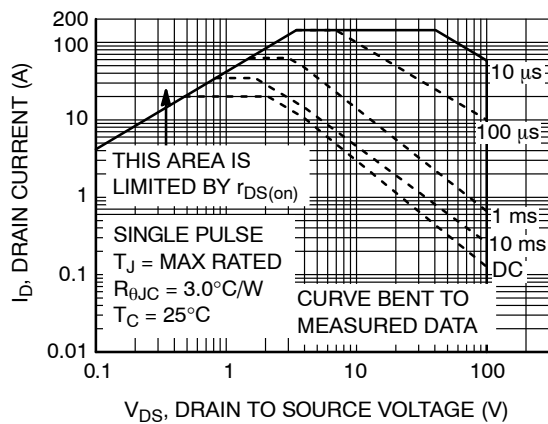


Figure 11. Forward Bias Safe Operating Area

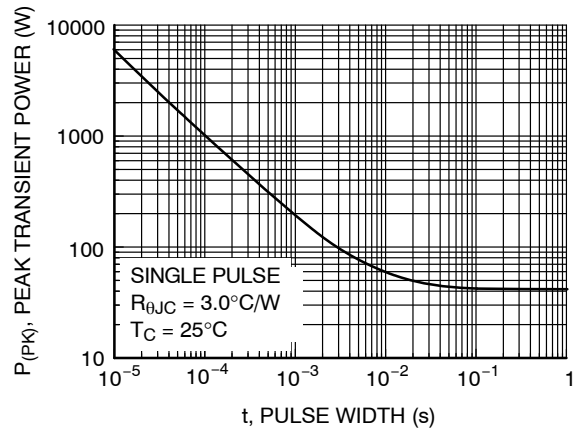


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

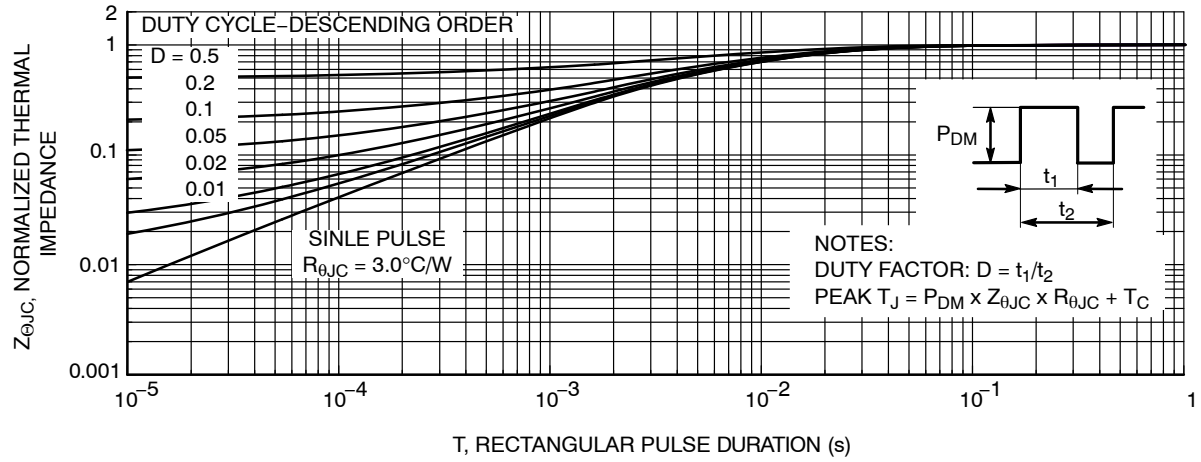
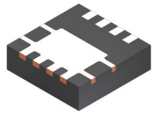


Figure 13. Transient Thermal Response Curve

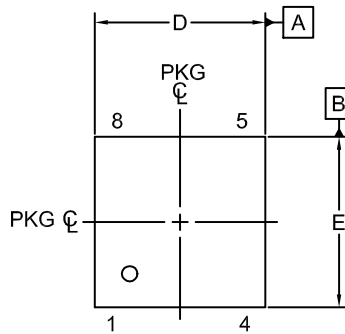
MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

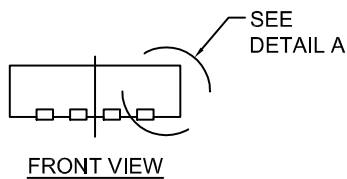


PQFN8 3.3X3.3, 0.65P
CASE 483AK
ISSUE B

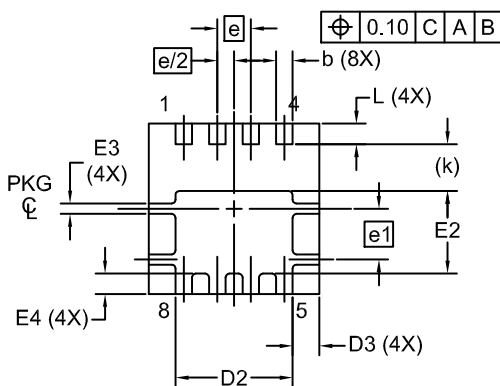
DATE 12 OCT 2021



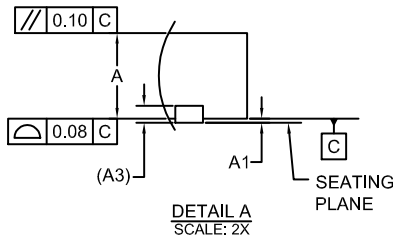
TOP VIEW



FRONT VIEW



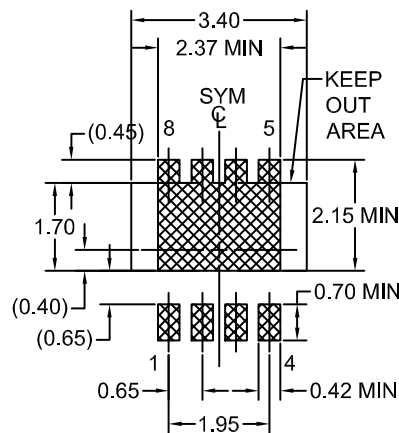
BOTTOM VIEW



DETAIL A
SCALE: 2X

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
A3	0.20 REF		
b	0.27	0.32	0.37
D	3.20	3.30	3.40
D2	2.17	2.27	2.37
D3	0.42	0.52	0.62
E	3.20	3.30	3.40
E2	1.50	1.60	1.70
E3	0.10	0.20	0.30
E4	0.29	0.39	0.49
e	0.65 BSC		
e/2	0.325 BSC		
e1	0.98 BSC		
k	0.91 REF		
L	0.30	0.40	0.50

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