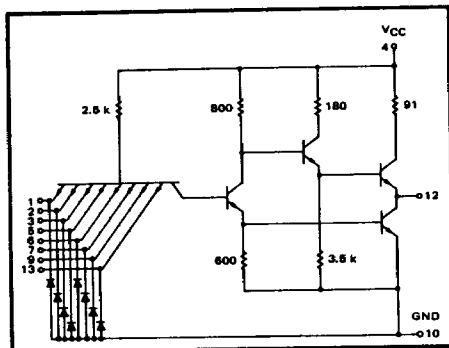


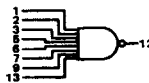
8-INPUT "NAND" GATE

MTTL II MC2100/2000 series

MC2105 • MC2155  
MC2005 • MC2055



This device is an 8-input NAND gate. It is useful when processing a large number of variables, such as in encoders or decoders.



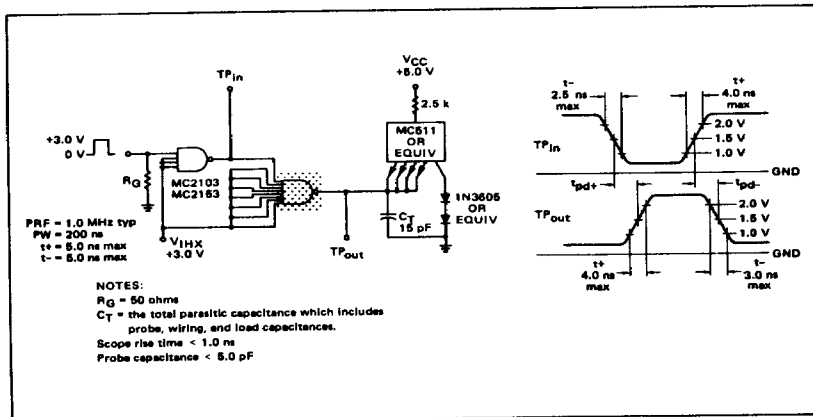
Positive Logic:  
 $12 = 1 \cdot 2 \cdot 3 \cdot 4 \cdot 5 \cdot 6 \cdot 7 \cdot 8 \cdot 13$   
 Negative Logic:  
 $12 = 1 + 2 + 3 + 4 + 5 + 6 + 7 + 8 + 13$

Total Power Dissipation = 22 mW typ/Pkg  
 Propagation Delay Time = 8.0 ns typ

TYPE NO.	INPUT LOADING FACTOR (I <sub>I</sub> )	OUTPUT DRIVE (I <sub>OL</sub> )	TEMPERATURE RANGE
MC2105 MC2155	1      -2.0 mA	11 MC2100 series Gates 22 mA 8 MC2100 series Gates 12 mA	-55°C to +125°C
MC2005 MC2055	1      -2.5 mA	9 MC2000 series Gates 22.5 mA 5 MC2000 series Gates 12.5 mA	0°C to +75°C

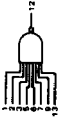
SWITCHING TIME TEST CIRCUIT

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one input of the device. To complete testing, sequence through remaining inputs in the same manner.



Characteristic	Symbol	Pin Under Test	TEST CONDITIONS												Grade			
			mA						Volts									
			$I_{CC}$	$I_{DD}$	$I_{DD}$	$I_{DD}$	$I_{DD}$	$I_{DD}$	$V_{DD}$	$V_{DD}$	$V_{DD}$	$V_{DD}$	$V_{DD}$	$V_{DD}$				
Input																		
Forward Current	$I_F$	1	-2.0	-2.0	-2.0	-2.0	-2.5	-2.5	-2.5	-2.5	-2.5	-2.5	-2.5	-2.5	-2.5	-2.5	-2.5	1,10
Leakage Current	$I_L$	1	-100	-100	-100	-100	-100	-100	-100	-100	-100	-100	-100	-100	-100	-100	-100	2,3,5,6,7,9,10,13
Increase Beta Current	$I_{\beta}$	1	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	10
Breakdown Voltage	$BV_{in}^{(1)}$	1	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	5.5	2,3,5,6,7,9,10,13
Output																		
Output Voltage	$V_{OH}^{(1)}$	12	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2,3,5,6,7,9,10,13
Leakage Current	$I_{OLK}$	12	250	250	250	250	250	250	250	250	250	250	250	250	250	250	250	2,3,5,6,7,9,10,13
Short-Circuit Current	$I_{SC}$	12	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	-25	2,3,5,6,7,9,10,13
Output Voltage	$V_{OL}$	12	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.40	2,3,5,6,7,9,10,13
Power Requirements																		
Total Device	$I_{DD}$	4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1,10
Maximum Power Supply Current	$I_{DD}$	4	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1,10
Power Supply Drain	$I_{DD}$	4	3.75	3.75	3.75	3.75	3.75	3.75	3.75	3.75	3.75	3.75	3.75	3.75	3.75	3.75	3.75	1,10
Switching Parameters																		
Turn-On Delay	$t_{pd}$	1,12	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	2,3,5,6,7,9,10,13
Turn-Off Delay	$t_{pd}$	1,12	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	2,3,5,6,7,9,10,13
Rise Time	$t_r$	1,12	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	2,3,5,6,7,9,10,13
Fall Time	$t_f$	1,12	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	2,3,5,6,7,9,10,13

\* Pulse Fan-Out.

Pin-out and Package Information

Table 3-4 DSP56001A Identification by Signal Name (Continued)

Signal Name	132 pin "FC" PQFP or "FE" CQFP Pin No.	88 pin "RC" PGA Pin No.	Signal Name	132 pin "FC" PQFP or "FE" CQFP Pin No.	88 pin "RC" PGA Pin No.
WT	45	L13	nc	103	
X/Y	48	N13	nc	107	
XTAL	126	A6	nc	110	
nc	3		nc	116	
nc	4		nc	117	
nc	7		nc	122	
nc	17		nc	125	
nc	18		nc	132	
nc	21				

Power and ground pins have special considerations for noise immunity. See the section **Design Considerations**.

Table 3-5 DSP56001A Power Supply Pins

132 pin "FC" PQFP or "FE" CQFP Pin No.	88 pin "RC" PGA Pin No.	Power Supply	Circuit Supplied
63	L8	VCCN	Address Bus Buffers
64			
55	L6	GNDN	
56	L9		
73			
74			