Microwave Wideband Synthesizer with Integrated VCO

FEATURES

- Fundamental output frequency range: 11.5 GHz to 21 GHz
- Divide by 2 output frequency range: 5.75 GHz to 10.5 GHz
- Divide by 4 output frequency range: 2.875 GHz to 5.25 GHz
- Integrated RMS jitter at 20 GHz = 20 fs (integration bandwidth: 100 Hz to 100 MHz)
- Integrated RMS jitter at 20 GHz = 31 fs (ADC SNR method)
- VCO autocalibration time < 100 µs
- Phase noise floor: −156 dBc/Hz at 20 GHz
- PLL specifications
  - −239 dBc/Hz: normalized in-band phase noise floor
  - −287 dBc/Hz: normalized 1/f phase noise floor
  - 625 MHz maximum phase/frequency detector input frequency
  - 4.5 GHz reference input frequency
  - Typical spurious f_{PFD}: −90 dBc
- Reference to output delay specifications
  - Propagation delay temperature coefficient: 0.06 ps/°C
  - Adjustment step size: <1 ps
- Multichip output phase alignment
- 3.3 V and 5 V power supplies
- ADIsimPLL™ loop filter design tool support
- 7 mm × 7 mm, 48-terminal LGA
- −40°C to +105°C operating temperature

APPLICATIONS

- High performance data converter clocking
- Wireless infrastructure (MC-GSM, 5G, 6G)
- Test and measurement

GENERAL DESCRIPTION

The ADF4382A is a high performance, ultralow jitter, fractional-N phased-locked loop (PLL) with an integrated voltage controlled oscillator (VCO) ideally suited for local oscillator (LO) generation for 5G applications or data converter clock applications. The high performance PLL has a figure of merit of −239 dBc/Hz, low 1/f noise and high PFD frequency of 625 MHz in integer mode that can achieve ultralow in-band noise and integrated jitter. The ADF4382A can generate frequencies in a fundamental octave range of 11.5 GHz to 21 GHz, thereby eliminating the need for subharmonic filters. The divide by 2 and divide by 4 output dividers on the ADF4382A allow frequencies to be generated from 5.75 GHz to 10.5 GHz and 2.875 GHz to 5.25 GHz, respectively.

For multiple data converter clock applications, the ADF4382A automatically aligns its output to the input reference edge by including the output divider in the PLL feedback loop. For applications that require deterministic delay or delay adjustment capability, a programmable reference to output delay with <1 ps resolution is provided. The reference to output delay matching across multiple devices and over temperature allows predictable and precise multichip clock and system reference (SYSREF) alignment.

The simplicity of the ADF4382A block diagram eases development time with a simplified serial peripheral interface (SPI) register map, repeatable multichip clock alignment, and limiting unwanted clock spurs by allowing off-chip SYSREF generation.

FUNCTIONAL BLOCK DIAGRAM

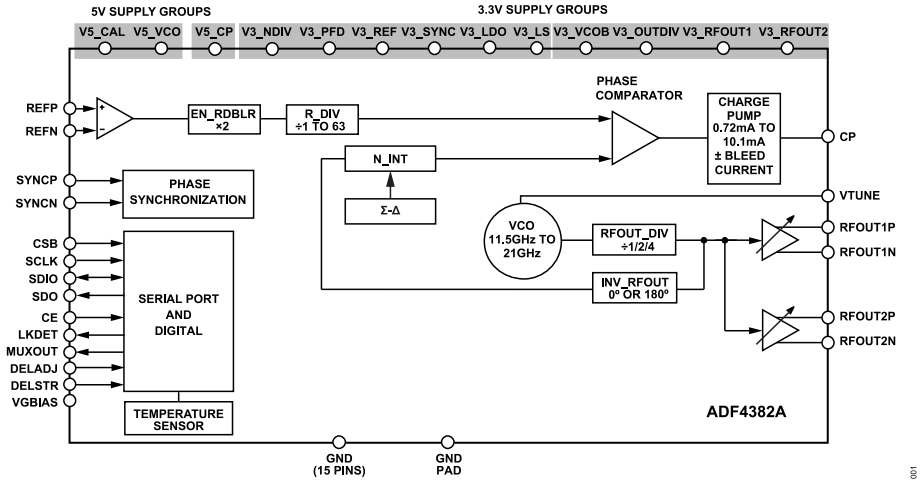

Figure 1. ADF4382A Functional Block Diagram

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REVISION HISTORY

12/2023—Revision 0: Initial Version

SPECIFICATIONS

3.3 V Supply Group 1 pins voltage ($V_{3.3V\_1}$) = 3.3 V Supply Group 2 pins voltage ($V_{3.3V\_2}$) = 3.15 V to 3.45 V, V5_VCO voltage (V_{5V_VCO}) = 5V_CP voltage (V_{5V_CP}) = 5V_CAL voltage (V_{5V_CAL}) = 4.75 V to 5.25 V, all voltages are with respect to GND, and T_A = −40°C to +105°C, operating temperature range, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE INPUTS (REFP and REFN)						
Input Frequency	f_{REF}	10		4500	MHz	
Input Signal Level	V_{REF}	0.5		2.6	V p-p	Refer to Figure 42
Minimum Input Slew Rate			100		V/µs	
Input Duty Cycle			50		%	
Self Bias Voltage			1.85		V	
Input Resistance			3		kΩ	Differential
Input Capacitance			1		pF	Differential
Input Current			2		µA	
REFERENCE PEAK DETECTOR						
Input Frequency		10		4500	MHz	
Minimum Input Signal Detected (REF_OK = 1)			200		mV p-p	f_{REF} = 100 MHz, single-ended sine wave
Maximum Input Signal Not Detected (REF_OK = 0)			160		mV p-p	f_{REF} = 100 MHz, single-ended sine wave
REFERENCE DIVIDER		1		63		All integers included
REFERENCE DOUBLER						
Input Frequency		10		2000	MHz	EN_RDBLR = 1
PHASE/FREQUENCY DETECTOR (PFD)						
Input Frequency	f_{PFD}					
Integer Mode		5.4		625	MHz	Integer mode, for all values of the N divider, excluding 15 and 28 to 31
		5.4		540	MHz	For the N divider values 15 and 28 to 31
Fractional Mode		5.4		250	MHz	EFM3_MODE = 0 and EFM3_MODE = 4
		5.4		220	MHz	EFM3_MODE = 5
SYNCHRONIZATION INPUTS (SYNCP and SYNCN)						
Input Signal Level	V_{REF}	0.4		2.6	V p-p	Low voltage differential signaling (LVDS) mode, differential
		0.5		2.6	V p-p	Current mode logic (CML) mode, differential
Self Bias Voltage			1.3		V	LVDS mode
			1.85		V	CML mode
Synchronization to Reference Setup Time		400			ps	Common-mode voltage (V_{CM}) set to self bias voltage, V_{CM} = 0.8 V p-p
Synchronization to Reference Hold Time		600			ps	V_{CM} set to self bias voltage, V_{CM} = 0.8 V p-p
Input Resistance			3		kΩ	Differential
Input Capacitance			1		pF	Differential
Input Current			3		µA	
CHARGE PUMP (CP)						
Output Current	I_{CP}					
Minimum			0.79		mA	Set by the CP_I bit fields
Maximum			11.1		mA	Set by the CP_I bit fields
Output Current Source and Sink						
Accuracy			±2		%	All setting, CP voltage (V_{CP}) = V_{CP}/2
Matching			±2		%	All setting, V_{CP} = V_{CP}/2
Output Current vs. Output Voltage Sensitivity			0.2		% V/V	V_{CP}[1]
Output Current vs. Temperature			280		ppm/C	V_{CP} = V_{CP}/2
Output High-Z Leakage Current			−0.01		µA	Minimum I_{CP}, V_{CP}[1]
			−0.3		µA	Maximum I_{CP}, V_{CP}[1]

SPECIFICATIONS

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
VCO						
Fundamental Frequency Range	f_{VCO}	11.5		21	GHz	
VCO Autocalibration Time			100		µs	
Tuning Sensitivity	K_{VCO}		50 to 150		MHz/V	K_{VCO}[2,3]
Divided Reference Clock (DIV_RCLK) VCO Calibration Frequency	f_{DIV_RCLK}			125	MHz	Must set DCLK_MODE = 1, when f_{DIV_RCLK} > 80 MHz
FEEDBACK (N) AND OUTPUT DIVIDER (O)						
N		4		4095		Integer mode
		19		4095		Fractional mode
O		1		4		1, 2, and 4
CLOCK OUTPUTS (RFOUT1P and RFOUT1N, RFOUT2P and RFOUT2N)						Differential termination = 100 Ω for all RF output (RFOUT) specifications unless otherwise noted
Output Frequency	f_{OUT}	11.5		21	GHz	
Divide by 2		5.75		10.5	GHz	
Divide by 4		2.875		5.25	GHz	
Differential RF Output Power	P_{RFOUT}		10		dBm	RFOUT1_OPWR = RFOUT2_OPWR = 11, f_{OUT} = 11.5 GHz
			9		dBm	RFOUT1_OPWR = RFOUT2_OPWR = 11, f_{OUT} =14 GHz
			5		dBm	RFOUT1_OPWR = RFOUT2_OPWR = 11, f_{OUT} = 20 GHz
Output Resistance			100		Ω	Differential
Output Common Mode			3.3 − V_{OD}[4]		V	
Output Rise Time	t_R		15		ps	20% to 80%, RFOUT1_OPWR = RFOUT2_OPWR = 1
Output Fall Time	t_F		15		ps	80% to 20%, RFOUT1_OPWR = RFOUT2_OPWR = 1
Output Duty Cycle			50		%	
Skew, RFOUT1 to RFOUT2			±3		ps	
REFERENCE INPUT TO OUTPUT DELAY						Device setup for all delay specifications unless noted as follows, measure rising reference edge at reference input to rising edge at RFOUT output
Propagation Delay	t_{PD}		190		ps	REF_SEL = 0 and REF_SEL = 1
Propagation Delay Temperature Coefficient	$t_{PD\text{-}TC}$		0.06		ps/°C	REF_SEL = 0
LOGIC INPUTS (CSB, SCLK, SDIO, DELADJ and DELSTR)						
Input High Voltage	V_{INH}	1.2			V	
Input Low Voltage	V_{INL}			0.6	V	
Input Current	I_{IH}/I_{IL}			±1	µA	
Input Capacitance	C_{IN}		3		pF	
LOGIC INPUT (CE)						
Input High Voltage	$V_{INH\text{-}3V}$	1.8			V	
Input Low Voltage	$V_{INL\text{-}3V}$			0.8	V	
Input Current	$I_{IH\text{-}3V}/I_{IL\text{-}3V}$			±1	µA	
Input Capacitance	$C_{IN\text{-}3V}$		3		pF	

SPECIFICATIONS

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC OUTPUTS (SDIO, SDO, LKDET, and MUXOUT)						
Output High Voltage (1.8 V Mode)	$V_{OH-1.8V}$	1.5	1.8	2	V	Output high current (I_{OH}) = 500 µA, 1.8 V output selected (default setting)
Output High Voltage (3.3 V Mode)	V_{OH-3V}	$V_{3.3V}$ − 0.4				I_{OH} = 500 µA, 3.3 V output selected, set by the voltage on the V3_LDO pin, and CMOS_OV can set to either 1.8 V or 3.3 V logic
Output Low Voltage	V_{OL}			0.4	V	Output low current (I_{OL}) = 500 µA
SDO High-Z Leakage	I_{ZH}/I_{ZL}			±1	µA	
POWER SUPPLIES						Device Setup is default configuration for all Supply Current specifications unless noted below.
V5_VCO Supply Range	V_{V5_VCO}	4.75	5	5.25	V	
V5_CAL Supply Range	V_{V5_CAL}	4.75	5	5.25	V	
V5_CP Supply Range	V_{V5_CP}	4.75	5	5.25	V	
$V_{3.3V\_1}$ Supply Range	$V_{3.3V\_1}$	3.15	3.3	3.45	V	Group 1: V3_LS, V3_LDO, V3_REF, V3_PFD, V3_NDIV, and V3_SYNC
$V_{3.3V\_2}$ Supply Range	$V_{3.3V\_2}$	3.15	3.3	3.45	V	Group 2: V3_RFOUT1, V3_RFOUT2, V3_VCO, and V3_OUTDIV
V5_VCO Supply Current	I_{5V_VCO}		140	195	mA	f_{OUT} = 11.5 GHz to 21GHz, RFOUT_DIV = 0, maximum charge pump current
V5_CAL Supply Current	I_{5V_CAL}		105	215	µA	
			15		mA	During VCO calibration
V5_CP Supply Current	I_{5V_CP}		60	70	mA	I_{CP} = 11.1 mA
$V_{3.3V\_1}$ Supply Current	$I_{3.3V\_1}$		200	240	mA	
$V_{3.3V\_2}$ Supply Current	$I_{3.3V\_2}$		310	340	mA	PD_RFOUT1 = 0, PD_RFOUT2 = 0, RFOUT1_OPWR = 11 and RFOUT2_OPWR = 11 (maximum power)
Typical Power Dissipation	P_{DIS}		2.2 to 2.6			PD_RFOUT1 = 1, PD_RFOUT2 = 0, RFOUT1_OPWR = 11 RFOUT2_OPWR = 11 (maximum power)
Typical Power Down Current						
3.3 V			3.1		mA	PD_ALL =1, I3.3V_1 + I3.3V_2
5 V			340		uA	PD_ALL=1, IVCO-5V + ICAL-5V + ICP-5V
Typical Disable Current						
3.3 V Supplies			710		uA	CE=LOW, $I_{3.3V\_1}$ + $I_{3.3V\_2}$
5 V Supplies			340		uA	CE=LOW, I_{VCO-5V} + I_{CAL-5V} + I_{CP-5V}
RF OUTPUT NOISE CHARACTERISTICS						
RF Output = 20 GHz						VCO noise in open-loop conditions, and offset from 20 GHz carrier
Phase Noise Floor			−156		dBc/Hz	
100 KHz Offset			−103		dBc/Hz	
1 MHz Offset			−125		dBc/Hz	
10 MHz Offset			−144		dBc/Hz	
RF Output = 14 GHz						VCO noise in open-loop conditions and offset from 14 GHz carrier
Phase Noise Floor			−156		dBc/Hz	
100 KHz Offset			−106		dBc/Hz	
1 MHz Offset			−125		dBc/Hz	
10 MHz Offset			−145		dBc/Hz	

SPECIFICATIONS

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Normalized In-Band Phase Noise Floor[5]						
Integer Mode	$L_{NORM-INT}$		−239		dBc/Hz	
Fractional Mode	$L_{NORM-FRAC}$		−237		dBc/Hz	
Normalized 1/f Phase Noise Floor[5, 6]	$L_{1/f}$		−287		dBc/Hz	Normalized to 1 Hz
Normalized 1/f Figure of Merit (FOM)[6]	L_{1/f_1G_10k}					
Integer Mode	$L_{1/f\_1G\_10k\ INT}$		−147		dBc/Hz	
Fractional Mode	$L_{1/f\_1G\_10k\ FRAC}$		−143		dBc/Hz	
Integrated RMS Jitter						
Integration Bandwidth: 100 Hz to 100 MHz			20		fs	RFOUT = 20 GHz
ADC SNR Method			31		fs	RFOUT = 20 GHz
Spurious						
f_{REF}			<−95		dBc	
f_{PFD}			−90		dBc	
TEMPERATURE SENSOR (ANALOG-TO-DIGITAL CONVERTER (ADC))						
ADC Clock Frequency	f_{ADC_CLK}			400	kHz	ADC clock divider output
ADC Clock Divider Frequency	f_{ADC_CLKDIV}			125	MHz	ADC clock divider input
Resolution				8	Bits	

[1] $0.9\ V < V_{CP} < V_{5V\_CP} - 0.9\ V$.

[2] Valid for $1.60\ V \le V_{TUNE} \le 2.85\ V$ with part calibrated after a power cycle or software power-on reset.

[3] Based on characterization.

[4] V_{OD} is the output differential voltage.

[5] These values are modeled in ADIsimPLL.

[6] Integrated ranged 1 kHz to f_{OUT}.

SPECIFICATIONS

SERIAL INTERFACE TIMING CHARACTERISTICS

$V_{3.3V\_1}$ = 3.3 V, $V_{3.3V\_2}$ = 3.15 V to 3.45 V, V_{5V_VCO} = V_{5V_CP} = V_{5V_CAL} = 4.75 V to 5.25 V, all voltages are with respect to GND, and T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1. Serial Interface Timing Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SERIAL INTERFACE (CSB, SCLK, SDIO, SDO)						See Figure 2, Figure 3, and Figure 4
SCLK Frequency	f_{SCLK}			75	MHz	
SCLK Pulse Width High	t_{HIGH}	6			ns	
SCLK Pulse Width Low	t_{LOW}	6			ns	
SDIO Setup Time	t_{DS}	4			ns	
SDIO Hold Time	t_{DH}	2			ns	
SCLK Fall Edge to SDIO Valid Prop Delay	t_{ACCESS_SDIO}	6			ns	
SCLK Fall Edge to SDO Valid Prop Delay	t_{ACCESS_SDO}	6			ns	
CSB Rising Edge to SDIO High-Z	t_Z	6			ns	
CSB Falling Edge to SCLK Rise Setup Time	t_S	2			ns	
SCLK Rising Edge to CSB Rise Hold Time	t_H	3			ns	

Serial Interface Timing Diagrams

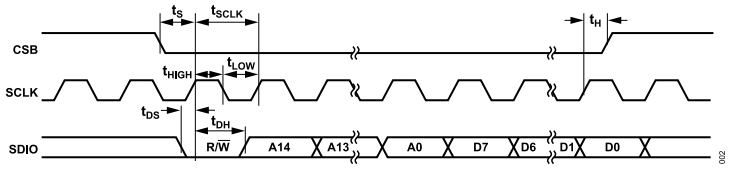


Figure 2. Write Timing Diagram

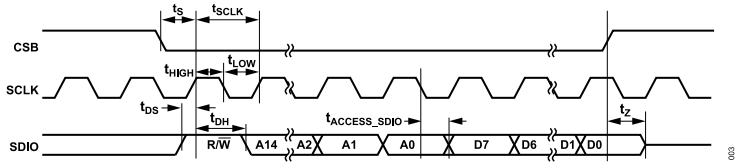


Figure 3. 3-Wire Read Timing Diagram (SDO_ACTIVE = 0)

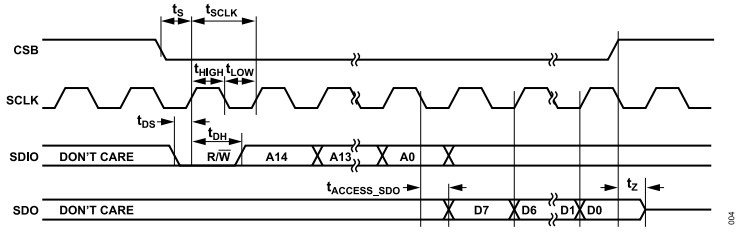


Figure 4. 4-Wire Read Timing Diagram (SDO_ACTIVE = 1)

SPECIFICATIONS

PHASE ADJUST 2-WIRE INTERFACE

Table 2. Phase Adjust 2-Wire Interface Specifications

Parameter	Symbol	Min	Typ	Max	Unit
TIME					
Setup	t_{SU}	20			ns
Hold	t_{HLD}	20			ns
STROBE WIDTH	t_{STR}	10			ns

Phase Adjust 2-Wire Interface Timing Diagram

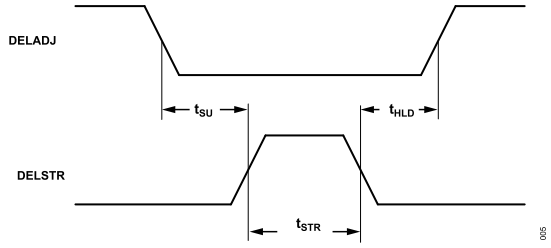


Figure 5. 2-Wire Phase Adjust Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3. Absolute Maximum Ratings

Parameter	Rating
$V_{3.3V\_1}$ (V3_LS, V3_LDO, V3_REF, V3_PFD, and V3_NDIV) to GND	−0.3 V to +3.6 V
$V_{3.3V\_2}$ (V3_VCO, V3_OUTDIV, V3_RFOUT1, and V3_FOUT2) to GND	−0.3 V to +3.6 V
V_{V5_CAL}, V_{V5_VCO}, and V_{V5_CP} to GND	−0.3 V to +5.5 V
Voltage on CP Pin	−0.3 V to V5_CP + 0.3 V
Voltage on All Other Pins	−0.3 V to $V_{3.3V\_1}$ + 0.3 V
Digital Outputs (MUXOUT, LKDET, SDO, and SDIO)	5 mA
RFOUT1P/RFOUT1N and RFOUT2P/RFOUT2N	Maximum (GND − 0.3 V, $V_{3.3V\_2}$ −1.2 V) to $V_{3.3V\_2}$ + 0.3 V
REFP and REFN	−0.65 V to $V_{3.3V\_1}$ + 0.65 V
Voltage on all Other Pins	−0.3 V to $V_{3.3V\_1}$ + 0.3 V
REFP to REFN and SYNCP to SYNCN	±1.35 V
Temperature	
Operating Junction Range	−40°C to +125°C
Storage Range	−55°C to +125°C
Maximum Junction	125°C
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	30 sec

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. $\theta_{JC\text{-}TOP}$ and $\theta_{JC\text{-}BOTTOM}$ are the junction-to-case thermal resistance top and bottom.

Table 4. Thermal Resistance

Package Type[1]	θ_{JA}	$\theta_{JC\text{-}TOP}$	$\theta_{JC\text{-}BOTTOM}$	Unit
CC-48-10	25.23	16.11	5.10	°C/W

[1] Test Condition 1: thermal impedance simulated values are based on use of a 4-layer PCB with the thermal impedance paddle soldered to a ground plane.

TRANSISTOR COUNT

The transistor count for the ADF4382A is 4700 (bipolar) and 385,400 (CMOS).

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADF4382A

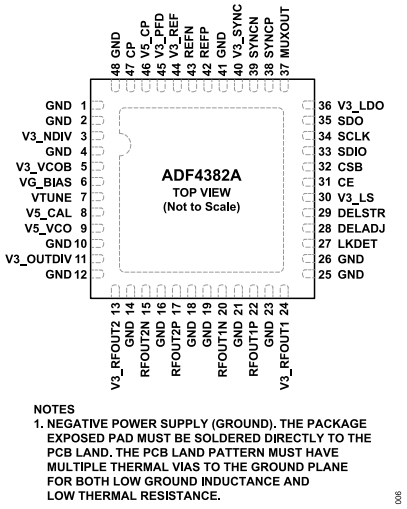
Table 5. ADF4382A, 48-Terminal LGA

ESD Model	Withstand Threshold (V)	Class
HBM	4000	3A
CDM	1000	C3

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NEGATIVE POWER SUPPLY (GROUND). THE PACKAGE EXPOSED PAD MUST BE SOLDERED DIRECTLY TO THE PCB LAND. THE PCB LAND PATTERN MUST HAVE MULTIPLE THERMAL VIAS TO THE GROUND PLANE FOR BOTH LOW GROUND INDUCTANCE AND LOW THERMAL RESISTANCE.

Figure 6. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 4, 10, 12, 14, 16, 18, 19, 21, 23, 25, 26, 41, 48	GND	Negative Power Supply (Ground). Tie the GND pins directly to the ground pad.
3	V3_NDIV	3.15 V to 3.45 V Positive Power Supply Pin for the PLL Feedback Divider Circuitry. Short the V3_NDIV pin to the other pins in the 3.3 V Power Supply Group 1.
5	V3_VCOB	3.15 V to 3.45 V Positive Power Supply Pin for the Bias Circuitry and Digital Logic Control Portion of the VCO. Short the V3_VCOB pin to the other pins in the 3.3 V Power Supply Group 2.
6	VG_BIAS	Bias Decoupling Pin. Connect uninstalled 0402, 0.1 µF capacitor footprint to GND.
7	VTUNE	VCO Tuning Input. This frequency control pin is normally connected to the external loop filter.
8	V5_CAL	4.75 V to 5.25 V Positive Power Supply Pin for VCO Calibration Circuitry. The V5_CAL pin can be shorted to the V5_VCO supply plane.
9	V5_VCO	4.75 V to 5.25 V Positive Power Supply Pin for the VCO Circuitry.
11	V3_OUTDIV	3.15 V to 3.45 V Positive Power Supply Pin for the Output Divider Circuitry. Short the V3_OUTDIV pin to the other pins in the 3.3 V Power Supply Group 2.
13	V3_RFOUT2	3.15 V to 3.45 V Positive Power Supply Pin for the RFOUT 2 Buffer Circuitry. Short the V3_RFOUT2 pin to the other pins in the 3.3 V Power Supply Group 2.
15, 17	RFOUT2N, RFOUT2P	RF Output 2 Output Signal. The VCO output divider is buffered and presented differentially on the RFOUT2N and RFOUT2P pins. The outputs have a 50 Ω (typical) output resistance per side (100 Ω differential). The far end of the transmission line is typically terminated with 100 Ω connected across the outputs. The output amplitude is programmable via the serial port.
20, 22	RFOUT1N, RFOUT1P	RF Output 1 Output Signal. The VCO output divider is buffered and presented differentially on the RFOUT1N and REFOUT1P pins. The outputs have 50 Ω (typical) output resistance per side (100 Ω differential). The far end of the transmission line is typically terminated with 100 Ω connected across the outputs. The output amplitude is programmable via the serial port.
24	V3_RFOUT1	3.15 V to 3.45 V Positive Power Supply Pin for the RFOUT 1 Buffer Circuitry. Short the V3_RFOUT1 pin to the other pins in the 3.3 V Power Supply Group 2.
27	LKDET	PLL Lock Detect. This output presents the lock status of the PLL. The PLL is locked when LKDET is a logic high.
28	DELADJ	Delay Adjust Input Signal. Logic 0 ensures that the delay of the RF output signal is reduced after DELSTR is asserted. Logic 1 ensures that the delay of the RF output signal is increased after DELSTR is asserted.
29	DELSTR	Delay Strobe Input Signal. A rising edge on this signal indicates that an adjustment is needed. The adjustment is then made on the falling edge.
30	V3_LS	3.15 V to 3.45 V Positive Power Supply Pin for the Internal Level Shift Circuitry. Short the V3_LS pin to the other pins in the 3.3 V Power Supply Group 1.
31	CE	Chip Enable. This CMOS input enables the device when driven high. A logic low disables the device, putting the device in a full power-down state causing the register to reset.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 6. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Description
32	CSB	Serial Port Chip Select. This CMOS input initiates a serial port communication burst when driven low, ending the burst when driven back high.
33	SDIO	Serial Data Input/Output. CMOS input and output. When configured as an input, the serial port uses this CMOS input for data. In 3-wire readback mode (default mode), the SDIO pin outputs data from the serial port during a read communication burst.
34	SCLK	Serial Port Clock. This CMOS input clocks serial port input data on its rising edge.
35	SDO	Optional Serial Data Output. In 3-wire mode (default mode), this three-state CMOS pin remains in a high impedance state. In 4-wire readback mode, the SDO pin presents data from the serial port during a read communication burst. When the CSB is de-asserted, SDO returns to a high impedance. Optionally, attach a resistor of >200 kΩ to prevent a floating output.
36	V3_LDO	3.15 V to 3.45 V Positive Power Supply Pin for the Internal Low Dropout (LDO) Regulator Circuitry. Short the V3_LDO pin to the other pins in the 3.3 V Power Supply Group 1.
37	MUXOUT	Internal Device Multiplexor Output. This output pin can be connected to multiple internal nodes for factory test and debug purposes.
38, 39	SYNCP, SYNCN	Synchronization Input Signals. Both RF output signals are synchronized to an input signal at these pins. SYNCP and SYNCN are used for multichip phase synchronization. This differential input can accept both high and low common-mode input signals (based on the SPI bit setting).
40	V3_SYNC	3.15 V to 3.45 V Positive Power Supply. Short the V3_SYNC pin to the other pins in the 3.3 V Power Supply Group 1.
42, 43	REFP, REFN	Reference Input Signals. These differential inputs are buffered with a low noise amplifier (LNA) ideally suited for high slew rates (default mode). For low slew rate reference input signals, an alternate LNA can be selected via the serial port. Reference inputs are self biased and must be AC-coupled with 1 µF capacitors. Reference inputs accept differential or single-ended inputs. See the Reference Input Network section for more details.
44	V3_REF	3.15 V to 3.45 V Positive Power Supply Pin for the PLL Reference Circuitry. Short the V3_REF pin to the other pins in the 3.3 V Power Supply Group 1.
45	V3_PFD	3.15 V to 3.45 V Positive Power Supply Pin for PFD Circuitry. Short the V3_PFD pin to the other pins in the 3.3 V Power Supply Group 1.
46	V5_CP	4.75 V to 5.25 V Positive Power Supply Pin for Charge Pump Circuitry. Isolate the V5_CP pin from the V5_VCO supply plane.
47	CP	Charge Pump Output. This bidirectional current output is normally connected to the external loop filter.
Exposed Pad	GND	Negative Power Supply (Ground). The package exposed pad must be soldered directly to the PCB land. The PCB land pattern must have multiple thermal vias to the ground plane for both low ground inductance and low thermal resistance.

TYPICAL PERFORMANCE CHARACTERISTICS

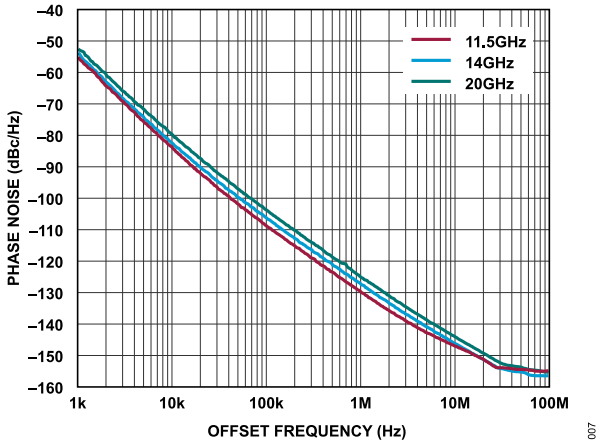


Figure 7. Open-Loop VCO Phase Noise vs. Offset Frequency at Various Frequencies

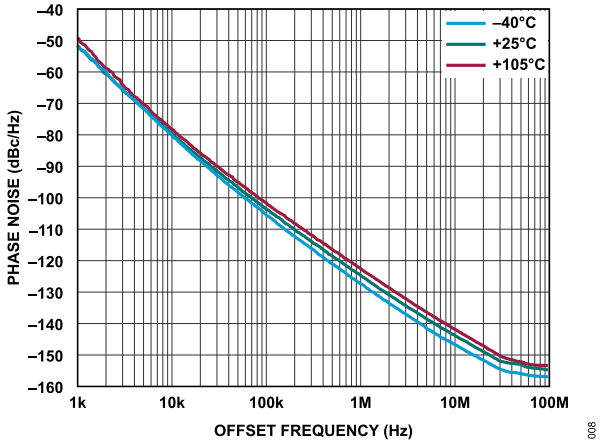


Figure 8. Open-Loop VCO Phase Noise vs. Offset Frequency at RFOUT = 20 GHz and Various Temperatures

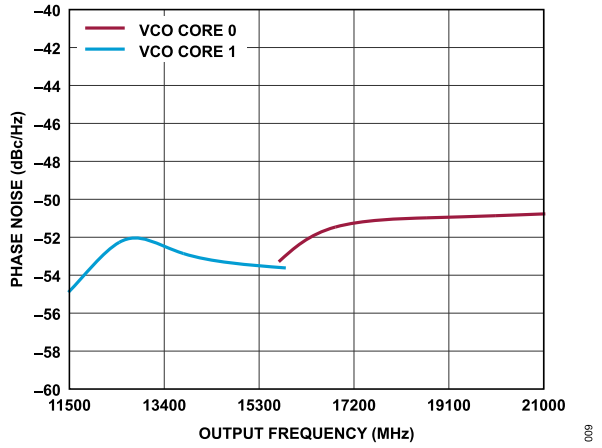


Figure 9. Open-Loop VCO Phase Noise Across Frequency at 1 kHz Offset

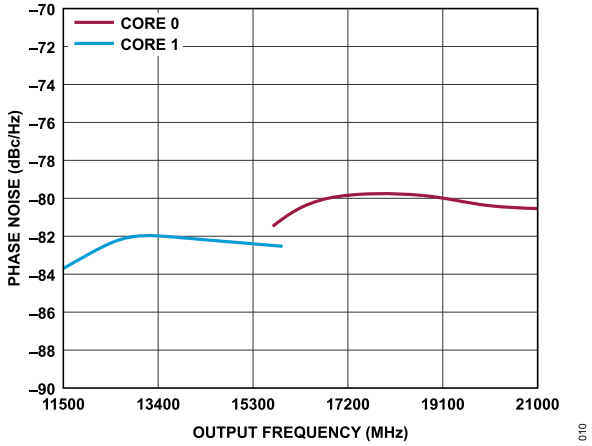


Figure 10. Open-Loop VCO Phase Noise Across Frequency at 10 kHz Offset

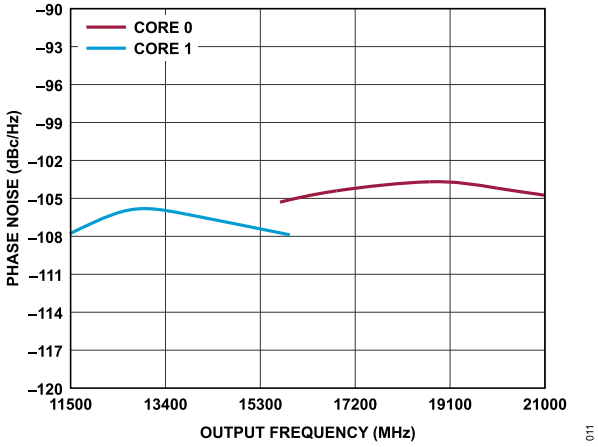


Figure 11. Open-Loop VCO Phase Noise Across Frequency at 100 kHz Offset

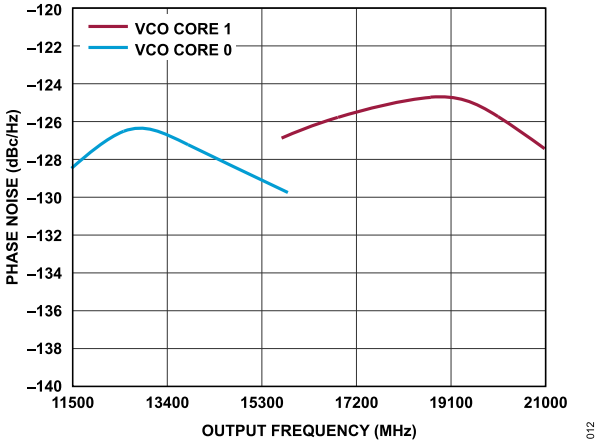


Figure 12. Open-Loop VCO Phase Noise Across Frequency at 1 MHz Offset

TYPICAL PERFORMANCE CHARACTERISTICS

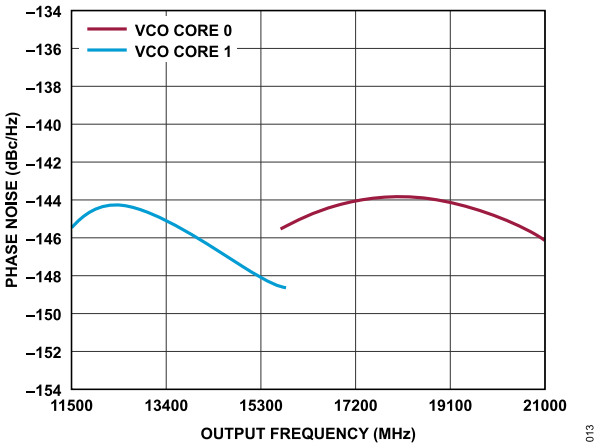


Figure 13. Open-Loop VCO Phase Noise Across Frequency at 10 MHz Offset

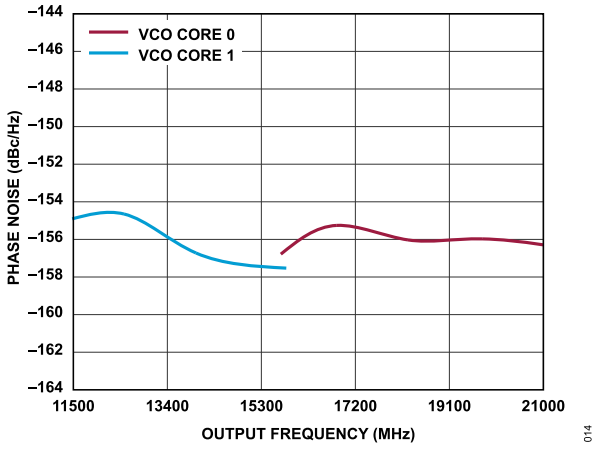


Figure 14. Open-Loop VCO Phase Noise Across Frequency at 100 MHz Offset

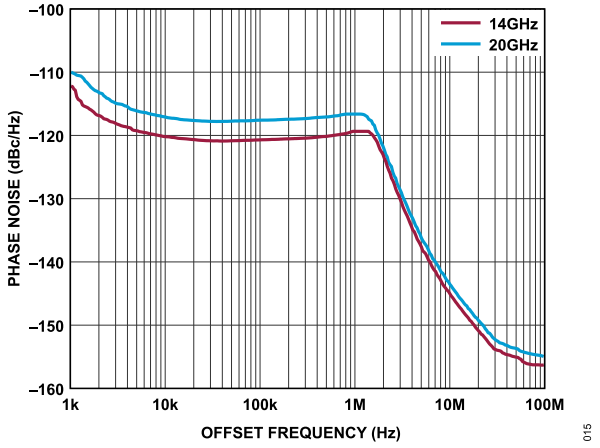


Figure 15. Closed-Loop Phase Noise vs. Offset Frequency at RFOUT = 14 GHz and 20 GHz

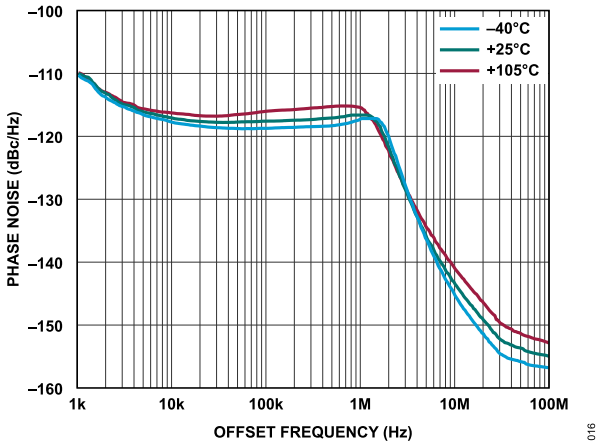


Figure 16. Closed-Loop Phase Noise vs. Offset Frequency at 20 GHz VCO Frequency Across Temperatures

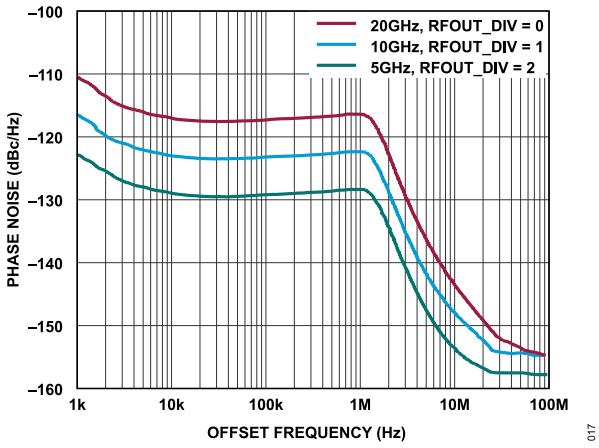


Figure 17. Closed-Loop Phase Noise vs. Offset Frequency at 20 GHz VCO Frequency and Divided Output Frequency

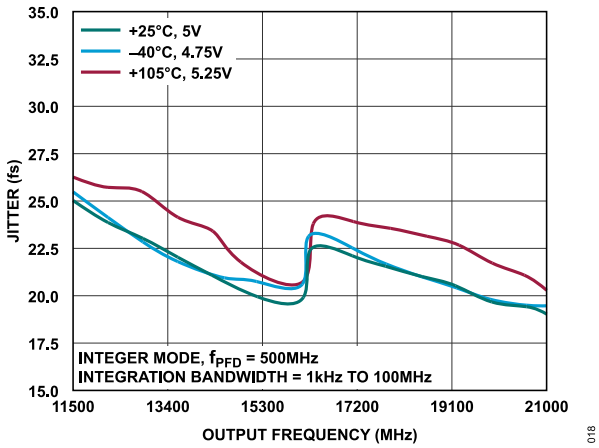


Figure 18. 1 kHz to 100 MHz Integrated Jitter in Integer Mode, f_{PFD} = 500 MHz

TYPICAL PERFORMANCE CHARACTERISTICS

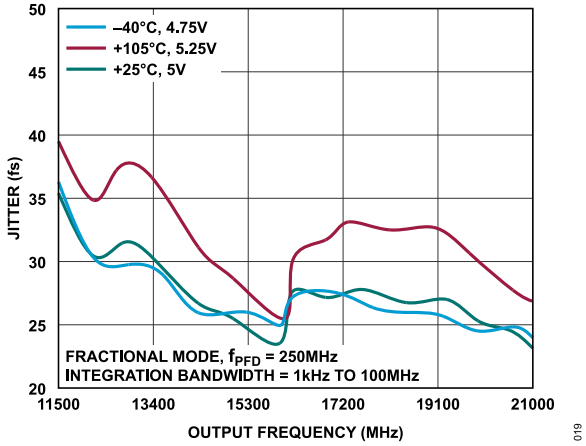


Figure 19. 1 kHz to 100 MHz Integrated Jitter in Fractional Mode, f_{PFD} = 250 MHz

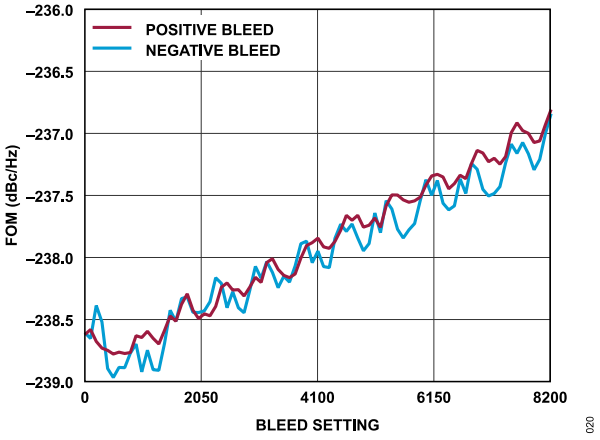


Figure 20. FOM, $L_{1/f}$ Integer Mode vs. Bleed Setting, f_{PFD} = 500 MHz, RFOUT = 20 GHz

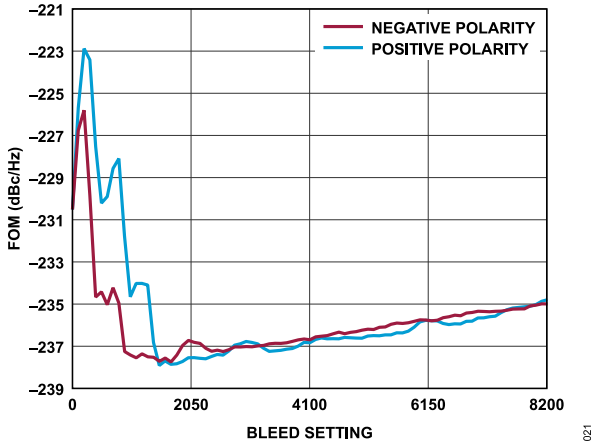


Figure 21. FOM, $L_{1/f}$ Fractional Mode vs. Bleed Setting, f_{PFD} = 250 MHz, RFOUT = 20.001 GHz

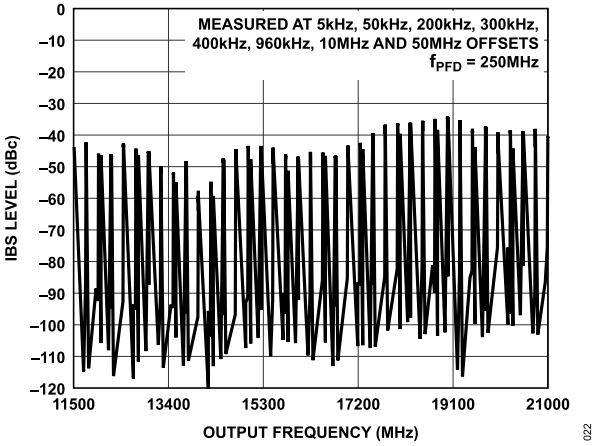


Figure 22. Worst Case Integer Boundary Spurs (IBS) Level vs. Output Frequency with f_{PFD} = 250 MHz

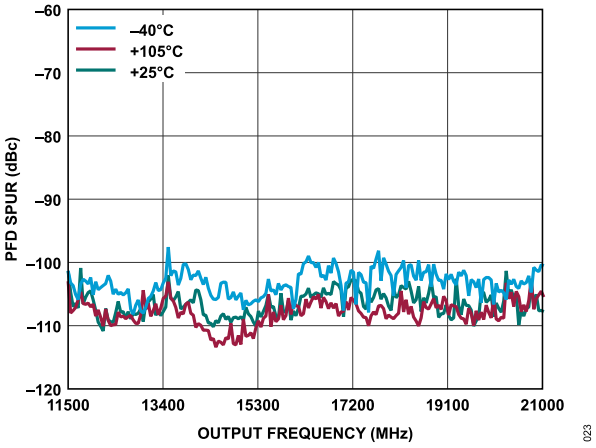


Figure 23. PFD Spur vs. Output Frequency at Various Temperatures

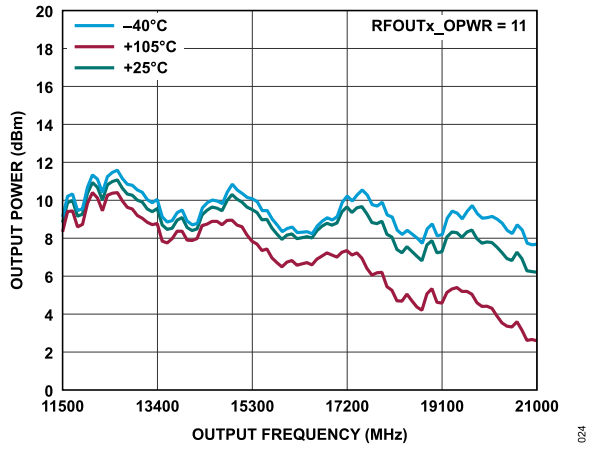


Figure 24. Differential Output Power vs. Output Frequency at Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

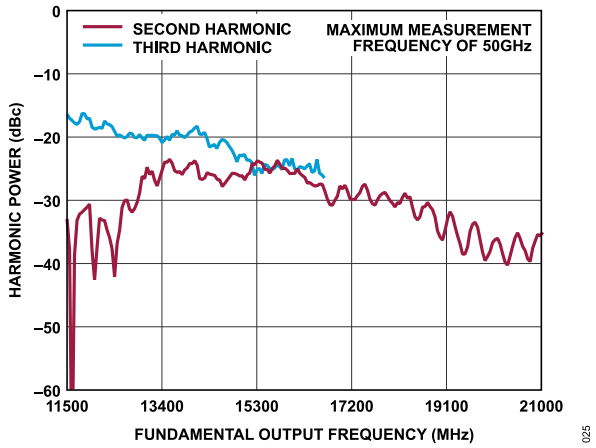


Figure 25. Harmonic Power vs. Fundamental Output Frequency

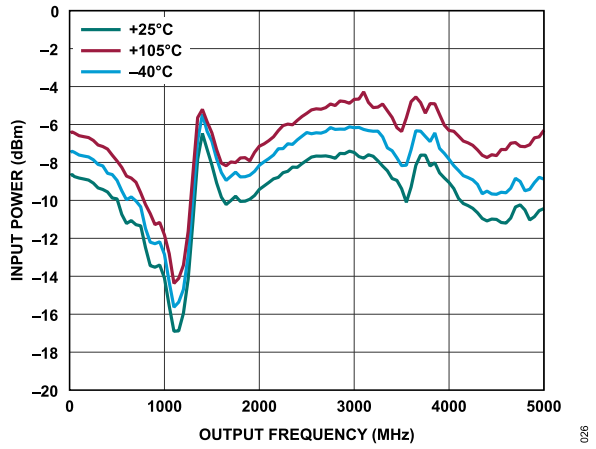


Figure 26. Minimum Input Signal for REF_OK = 1 for Delayed Match Amplifier (DMA) Buffer at Various Temperatures

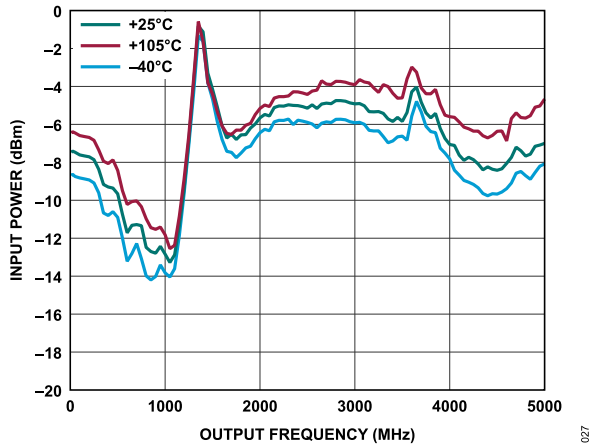


Figure 27. Minimum Input Signal for REF_OK = 1 for LNA Buffer at Various Temperatures

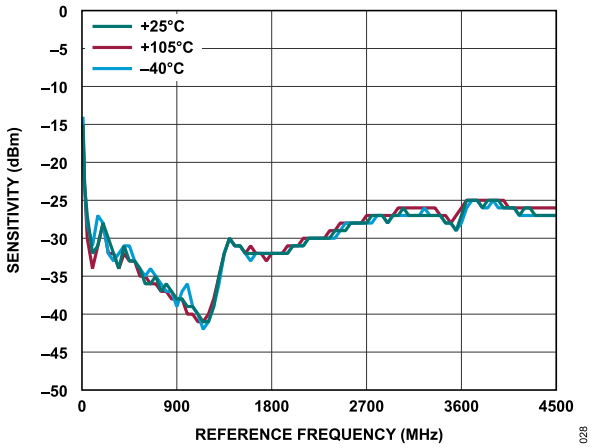


Figure 28. Reference Sensitivity for DMA Buffer at Various Temperatures

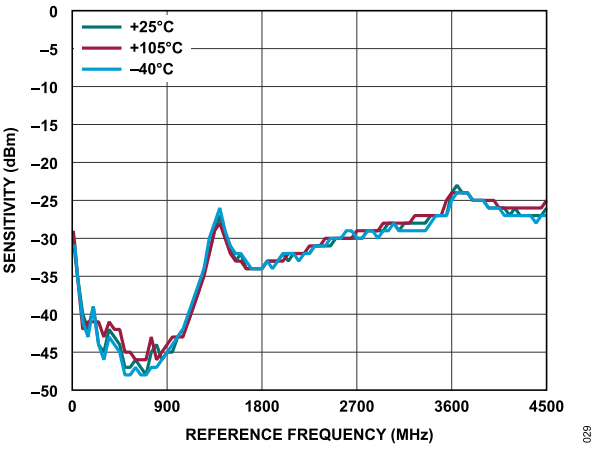


Figure 29. Reference Sensitivity for LNA Buffer at Various Temperatures

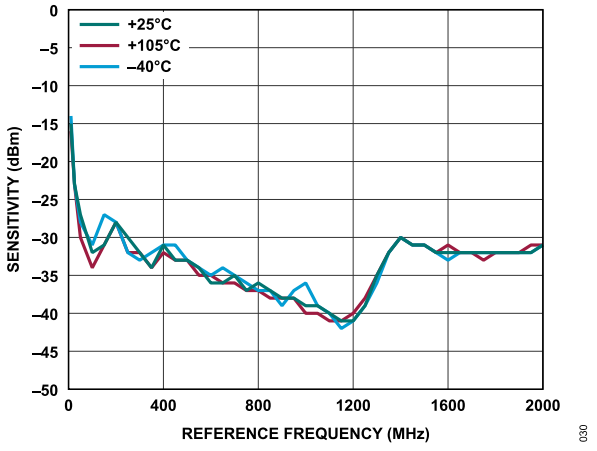


Figure 30. Reference Doubler Sensitivity for DMA Buffer at Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

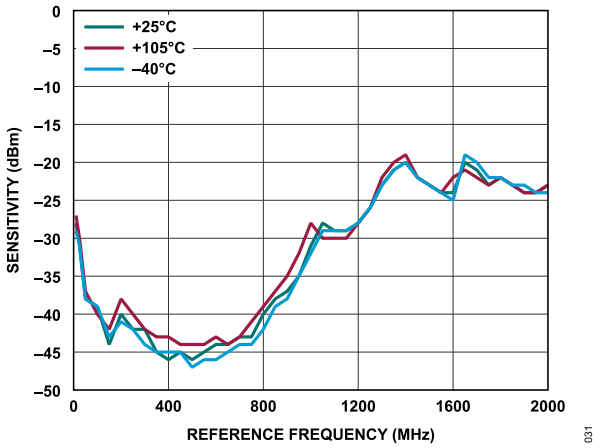


Figure 31. Reference Doubler Sensitivity for LNA Buffer at Various Temperatures

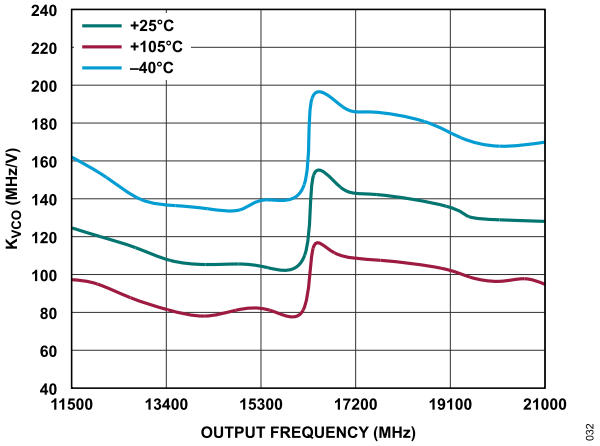


Figure 32. K_{VCO} vs. Output Frequency at Various Temperatures

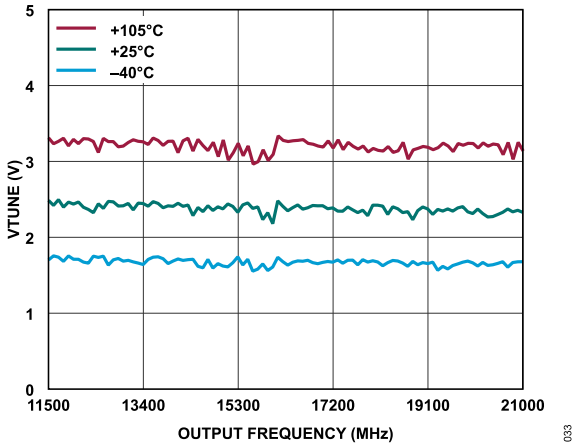


Figure 33. VTUNE vs. Output Frequency at Various Temperatures

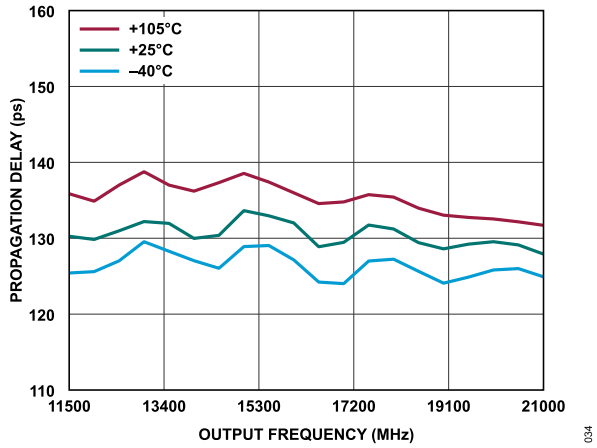


Figure 34. Propagation Delay vs. Output Frequency

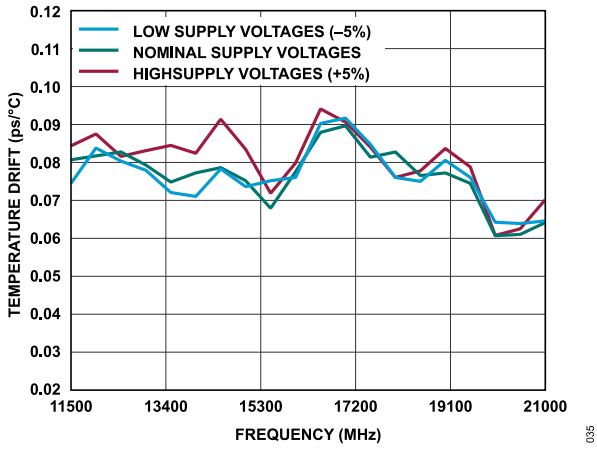


Figure 35. Temperature Drift vs. Frequency

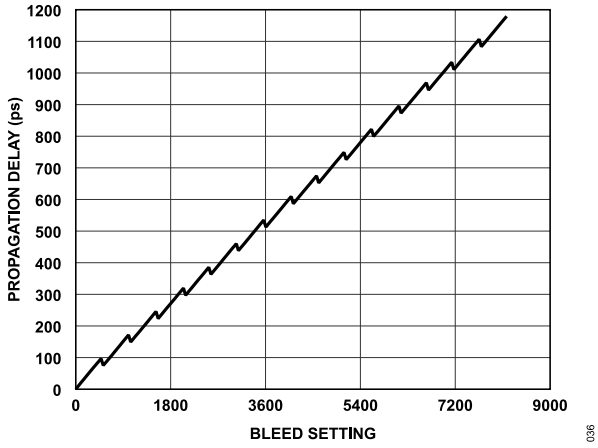


Figure 36. Propagation Delay vs. Bleed Setting

TYPICAL PERFORMANCE CHARACTERISTICS

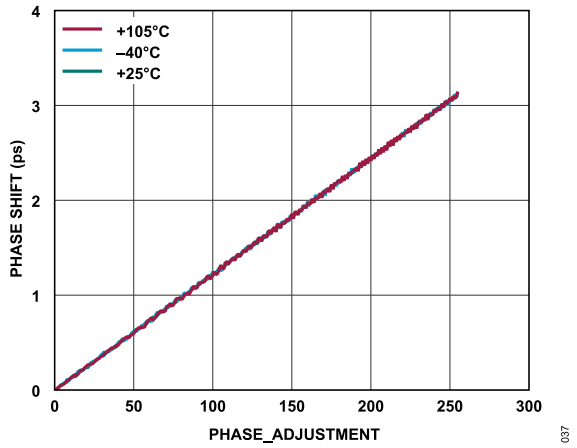


Figure 37. Phase Shift vs. PHASE_ADJUSTMENT for Various Temperatures

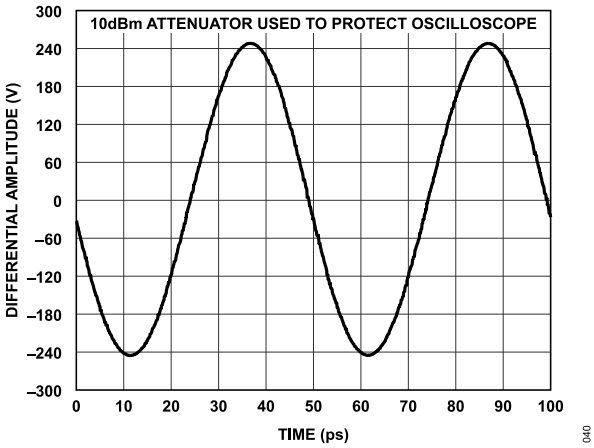


Figure 40. Differential Amplitude vs. Time at 20 GHz

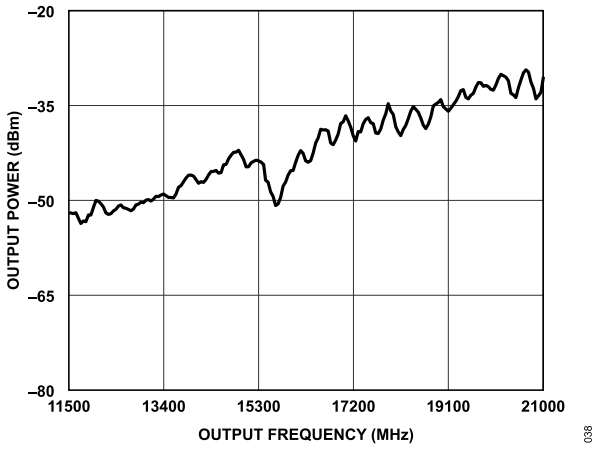


Figure 38. Output Power when Buffer Powered Down (PD_RFOUTx = 1) vs. Output Frequency

Figure 39. VCO Current vs. Output Frequency

THEORY OF OPERATION

INTRODUCTION

A PLL is a complex feedback system that can conceptually be considered a frequency multiplier. The system multiplies the frequency input at REFP/REFN and outputs a higher frequency at RFOUTxP/RFOUTxN. The PFD, charge pump, output divider, feedback divider, VCO, and external loop filter form a feedback loop to accurately control the output frequency (see Figure 41). When operating in integer mode, the reference divider or reference doubler sets the frequency resolution. When operating in fractional mode, the fractional-N divider sets the frequency resolution.

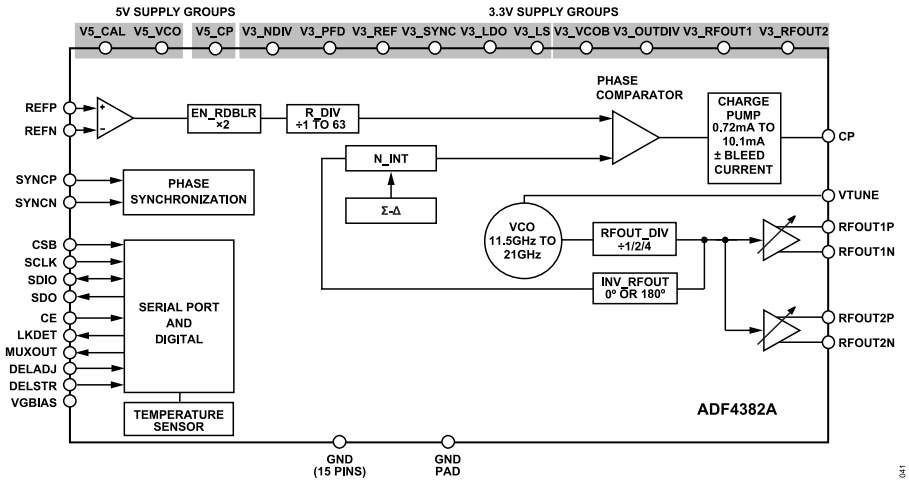


Figure 41. PLL Loop Diagram

THEORY OF OPERATION

OUTPUT FREQUENCY

When the loop is locked, the f_{VCO} (in Hz) produced at the output of the VCO is determined by f_{REF} and the O, R, and N values given by the following equation.

$$f_{VCO} = f_{REF} \times \frac{D \times N \times O}{R}$$

where *N* is given by the following:

$$N = \mathrm{N_{INT}} + \frac{\mathrm{FRAC1WORD} + \frac{\mathrm{FRAC2WORD}}{\mathrm{MOD2WORD}}}{MOD1WORD}$$

Here, f_{PFD} is given by the following:

$$f_{PFD} = \frac{f_{REF} \times D}{R}$$

and f_{VCO} can be alternatively expressed as follows:

$$f_{VCO} = f_{PFD} \times N \times O$$

The output frequency, f_{RFOUT}, produced at the output of the output divider is given by the following:

$$f_{RFOUT} = \frac{f_{VCO}}{O}$$

CIRCUIT DESCRIPTION

Reference Input Buffer

The reference frequency of the PLL is applied differentially on the REFP and REFN pins. These high impedance inputs are self biased and must be AC-coupled with 1 µF capacitors (see Figure 42 for a simplified schematic). Alternatively, the inputs can be used single ended by applying the reference frequency at REFP and bypassing REFN to GND with a 1 µF capacitor.

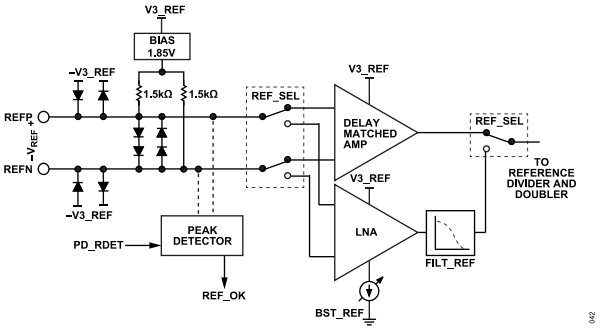


Figure 42. Reference Input Stage

A high quality signal must be applied to the REFP and REFN inputs as these inputs provide the frequency reference to the entire PLL. To achieve the in-band phase noise performance of the ADF4382A, apply a continuous wave signal or a square wave with a slew rate of at least 1000 V/µs. See the Reference Source Considerations section for more information on reference input signal requirements and interfacing.

The REF_SEL bit (Register 0x030, Bit 5) can be set to either a CML reference input or sine wave or slow slew-rate reference input. When REF_SEL is set to 0, the delay matched amplifier (DMA) buffer is selected. The DMA is optimized for high slew rate signals, such as square waves or higher frequency and higher amplitude sine waves. The DMA has a controlled propagation delay from the reference input to clock output, which eases time zero and over temperature multichip clock alignment.

When the REF_SEL bit is set to 1, the LNA is selected. The LNA is optimized for low slew rate signals, such as lower frequency or lower amplitude sine waves.

The REF_SEL bit must be set correctly to optimize the in-band phase noise performance and propagation delay, t_{PD}. See Table 7 for recommended settings.

Table 7. REF_SEL Programming

REF_SEL	Sine Wave Slew Rate (V/µs)	Square Wave	Optimized t_{PD}
0	≥1000	Preferred	Yes
1	<1000	Not applicable	Not applicable

To calculate the slew rate of a sine wave, use the following equation:

$$\text{Slew Rate} = 2 \times \pi \times f \times V$$

where:
f is the sine wave frequency.
V is the sine wave amplitude (in V peak)

The FILT_REF bit (Register 0x02F, Bit 6) controls the reference input LPF of the LNA and must be set only for sine wave signals less than 20 MHz to limit the wideband noise of the reference. The FILT_REF bit must be set correctly to reach the normalized in-band phase noise floor (L_{NORM}). Square wave inputs have FILT_REF set to 0. Table 8 shows the recommended settings.

Table 8. FILT_REF Programming

FILT_REF	Sine Wave f_{REF} (MHz)	Square Wave f_{REF}
0	≥20	All f_{REF}
1	<20	Not applicable

The BST_REF bit (Register 0x02F, Bit 7) must be set based upon the input signal level to prevent the LNA reference input buffer from saturating. The BST_REF programming is the same whether the input is a sine wave or a square wave. See Table 9 for recommended settings.

Table 9. BST_REF Programming

BST_REF	Sine Wave f_{REF} (dBM)
0	≥8
1	<8

THEORY OF OPERATION

Reference Peak Detector

A reference input peak detection circuit is provided on the REFP and REFN inputs to detect the presence of a reference signal and provides the REF_OK status flag available through Bit 3, Register 0x058. The circuit has hysteresis to prevent the REF_OK flag from chattering at the detection threshold.

The peak detector approximates an RMS detector; therefore, sine and square wave inputs give different detection thresholds by a factor of 4/π. See Table 10 for REF_OK detection values.

Table 10. REF_OK Status Output vs. Reference Input

REF_OK	Sine Wave f_{REF} (mV p-p)	Square Wave f_{REF} (mV p-p)
1	≥200	≥155
0	<180	<140

Reference Divider (R) and Doubler (D)

When the EN_RDBLR bit (Register 0x020, Bit 6) is set to 1, a frequency multiplier is used to double the frequency driven to the reference divider. A 6-bit divider, R_DIV (Register 0x020, Bits[5:0]), in series with reference doubler is used to reduce the frequency seen at the PFD. Its divide ratio, R, can be set to any integer from 1 to 63, inclusive. Use the R_DIV bits to directly program the R divide ratio. See the Output Frequency section for the relationship between R and D and the f_{REF}, f_{PFD}, f_{VCO}, and f_{RFOUT} frequencies.

Phase/Frequency Detector (PFD)

The PFD, in conjunction with the charge pump, produces source and sink current pulses proportional to the phase difference between the outputs of the reference divider or reference doubler and feedback divider. These source and sink pulses are required to phase lock the loop, forcing a phase alignment at the inputs of the PFD. See Figure 43 for a simplified schematic of the PFD.

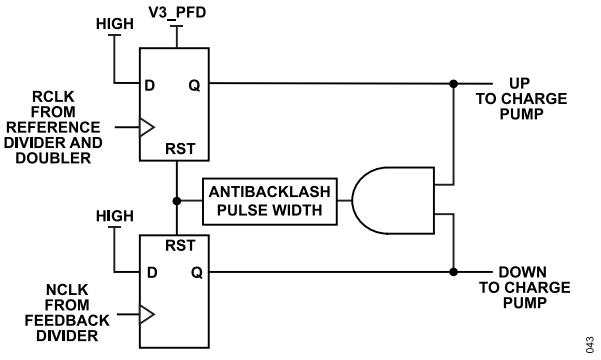


Figure 43. Simplified PFD Schematic

Charge Pump

The charge pump, controlled by the PFD, forces sink (down) or source (up) current pulses onto the CP pin, which must be connected to an appropriate loop filter. See Figure 44 for a simplified schematic of the charge pump.

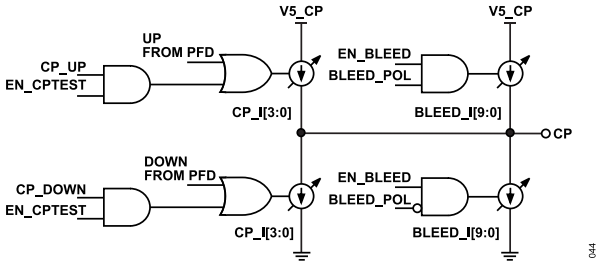


Figure 44. Simplified Charge Pump Schematic

The output current magnitude I_{CP} can be set from 0.79 mA to 11.1 mA using the CP_I bits (Register 0x001F, Bits[3:0]). A larger I_{CP} can result in lower in-band noise due to the lower impedance of the loop filter components, while a smaller I_{CP} can result in better spurious performance. See Table 11 for charge pump programming values.

Table 11. CP Programming

CP_I, Bits[3:0]	I_{CP} (mA)
0	0.79
1	0.99
2	1.19
3	1.38
4	1.59
5	1.98
6	2.39
7	2.79
8	3.18
9	3.97
10	4.77
11	5.57
12	6.33
13	7.91
14	9.51
15	11.1

THEORY OF OPERATION

Charge Pump Test Mode

When the EN_CPTEST bit (Register 0x02E, Bit 2) is set to 1, the CP_UP and CP_DOWN bits (Bit 1 and Bit 0, respectively) in the same register can be programmed to force a constant I_{CP} source or sink current, respectively, on the CP pin. The EN_CPTEST or CP_UP and CP_DOWN bits must be set to 0 to allow the loop to lock. These bits can be used as an aid to debug PLL-related issues during the hardware and software development phase of a project. For normal operation, set EN_CPTEST, CP_UP, and CP_DOWN to 0.

Table 12. Charge Pump Test Mode

EN_CPTEST	CP_UP	CP_DOWN	CP Pin State	Debug Test
1	0	0	High-Z	VCO open loop
1	1	0	~V_{V5_CP}	Charge pump output voltage verification
1	0	1	~GND	Charge pump output voltage verification
0	0	0	Normal operation	Not applicable

Charge Pump Bleed Current Optimization

A small programmable constant charge pump current, known as bleed current, can be used to optimize the phase noise and fractional spurious signals in fractional mode, which also changes the propagation delay from the REFP and REFN input pins to the RFOUTP and RFOUTN output pins. In fractional mode, after setting the bleed current for best performance, the output can be shifted by using the phase word which is effectively used in the Σ-Δ modulator (SDM). In integer mode, bleed current can be used to shift the output in both directions.

To enable the bleed current, set the EN_BLEED bit to 1. When the BLEED_POL bit is set to 1, a small constant source current is forced onto the CP pin. When the register BLEED_POL is set to 0, a small constant sink current is forced onto the CP pin.

The 13-bit bit field BLEED_I (Register 0x01D, Bits[7:0] and Register 0x01E, Bits[4:0]) is used to select the bleed current. This bit field consists of both a coarse bleed and a find bleed value. The 4 MSBs are used to calculate the coarse bleed current, and the 9 LSBs are used to calculate the fine bleed current as shown in the following equations.

$$I_{COARSE\ BLEED} = COARSE\_BLEED \times 202\ \mu A$$

$$I_{FINE\ BLEED} = FINE\_BLEED \times 567\ nA$$

$$I_{TOTAL\ BLEED} = I_{COARSE\ BLEED} + I_{FINE\ BLEED}$$

The propagation delay of the output frequency corresponds to the $I_{TOTAL\ BLEED}$ as follows:

$$t_{PROPAGATION\ DELAY} = \frac{I_{TOTAL\ BLEED}}{I_{CP}} \times t_{PFD}$$

where:

$I_{COARSE\ BLEED}$ is the coarse bleed current.
COARSE_BLEED represents the 4 upper MSBs of the BLEED_I bit field.
$I_{FINE\ BLEED}$ is the fine bleed current.
FINE_BLEED represents the lower 9 LSBs of the BLEED_I bit field.
I_{CP} is the charge pump current value selected.

Bleed Current Modes

The ADF4382A spurious performance can be optimized by programming t_{BLEED} setting based on the frequency of operation. The recommended t_{BLEED} for the RFOUT frequency of operation for each of the SDM modes are shown in Table 13.

To calculate the required BLEED_I setting required for a specific t_{BLEED} with the bleed current refer to Charge Pump Bleed Current Optimization section.

Table 13. Bleed Setting vs. Frequency for Each SDM Mode

	t_{BLEED} (ps)		
RFOUT	SDM Mode 0	SDM Mode 4	SDM Mode 5
RFOUT ≥ 10 GHz	300	510	720
3.996 GHz ≤ RFOUT< 10 GHz	625	625 + (2/RFOUT)	900 + (1.7/RFOUT)
1.8 GHz ≤ RFOUT < 3.996 GHz	1000	1350	1400 + (4/RFOUT)
RFOUT < 1.8 GHz	3600	3600	3600 + (4/RFOUT)

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Lock Detector

The lock detector uses internal signals from the PFD to measure the phase difference between the output signal of the reference divider and doubler (RCLK) and the output signal of the feedback divider (NCLK) in Figure 43. This detector is enabled by setting both the EN_LOL and EN_LDWIN bits (Register 0x02D, Bit 5 and Bit 4, respectively) to 1 and presents the lock detector output on the LKDET pin (Pin 27) and the LOCKED bit (Register 058, Bit 0). The lock detector output can also be presented on the MUXOUT pin (Pin 37 by programming the MUXOUT bits in Register 02E, Bits[7:4], to 0001.

The PFD RCLK and NCLK phase difference must be less than the phase difference lock window time, t_{LDWIN}, for a set number of PFD cycles before the lock detector output indicates the PLL has locked. The desired number of PFD cycles vary depending on whether the lock detect accuracy or speed is prioritized. Five loop filter time constants can be used as an initial estimate of the desired number of PFD cycles, as shown in the following equation:

$$\text{PFD Cycles} = \frac{5}{2 \times \pi \times LFBW}$$

where:
LFBW = loop filter bandwidth.

Note that LD_COUNT bits (Register 0x02C, Bits[4:0]) are used to select the desired number of PFD cycles. Use Table 14 to select the LD_COUNT value for the desired number of PFD cycles.

Table 14. LD_COUNT Programming

LD_COUNT[4:0]	PFD Cycles
0	27
1	35
2	51
3	67
4	99
5	131
6	195
7	259
8	387
9	515
10	771
11	1027
12	1539
13	2051
14	3075
15	4099
16	6147
17	8195
18	12291
19	16387
20	24579
21	32771

Table 14. LD_COUNT Programming (Continued)

LD_COUNT[4:0]	PFD Cycles
22	49155
23	65539
24	98307
25	131075
26	196611
27	262147
28	393219
29	524291
30	786345
31	1048579

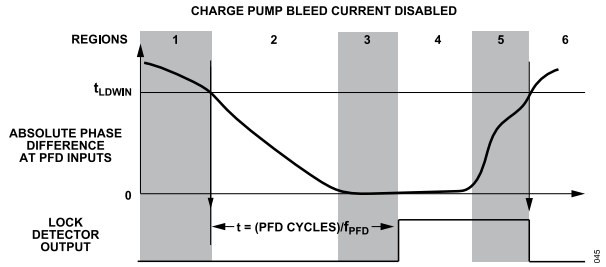

Figure 45. Lock Detector Timing, Bleed Current Disabled

Table 15. Lock Detector Timing, Bleed Current Disabled

Region	Absolute Phase Difference at PFD	Lock Detector State
1	$>t_{LDWIN}$	Low
2	$<t_{LDWIN}$	Low, counts PFD cycles
3	~0	Low, counts PFD cycles
4	~0	High, greater than or equal to the desired PFD cycle count
5	$<t_{LDWIN}$	High
6	$>t_{LDWIN}$	Low (immediately)

When the charge pump bleed current is enabled, a phase offset is applied to the PFD inputs. This phase offset, t_{IDEL}, is proportional to the amount of bleed current. Region 3 and Region 4 in Figure 45 and Figure 46 highlight the PFD phase difference the PLL settles to when the charge pump bleed current is disabled or enabled, respectively.

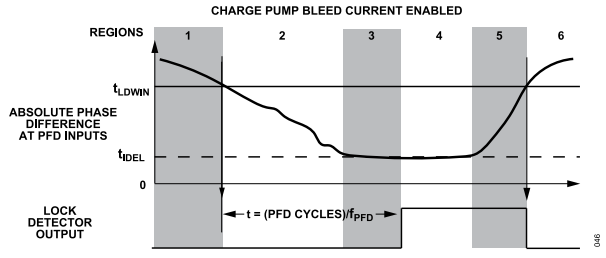

Figure 46. Lock Detector Timing, Bleed Current Enabled

For proper operation of the lock detector, the absolute value of t_{IDEL} must be less than t_{LDWIN}. The user sets the phase difference lock

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window time (t_{LDWIN}) for a valid lock condition with the LDWIN_PW bit field (Register 0x02, Bits[7:5]).

Table 16. LDWIN_PW Programming

LDWIN_PW [7:5]	Mode of Operation
000	Integer mode, 500 MHz maximum PFD with bleed ≤ 85 ps
001	Integer mode, 500 MHz maximum PFD with bleed > 85 ps
010	Fractional mode, 250 MHz maximum PFD, RFOUT ≥ 6.4 GHz
011	Fractional mode, 250 MHz maximum PFD, RFOUT ≥ 5 GHz
100	Fractional PLL, 200 MHz maximum PFD, RFOUT ≥ 4 GHz
101	Fractional PLL, 100 MHz maximum PFD, RFOUT ≥ 2 GHz
110	Fractional PLL, 50 MHz maximum PFD, RFOUT ≥ 1 GHz
111	Fractional PLL, 40 MHz maximum PFD, RFOUT ≥ 800 MHz

MUXOUT

The state of the MUXOUT pin is determined by the MUXOUT bits (Register 0x02E, Bits[7:4]), which allow the user access to various internal nodes. The MUXOUT pin and MUXOUT bits are commonly used as an additional lock status output or to debug PLL-related issues during the hardware and software development phase of a project. The CMOS_OV bit (Register 0x03D, Bit 5) determines if the logic high level for the MUXOUT pin, LKDET pin, SDO pin, and SDIO pin is 3.3 V or 1.8 V.

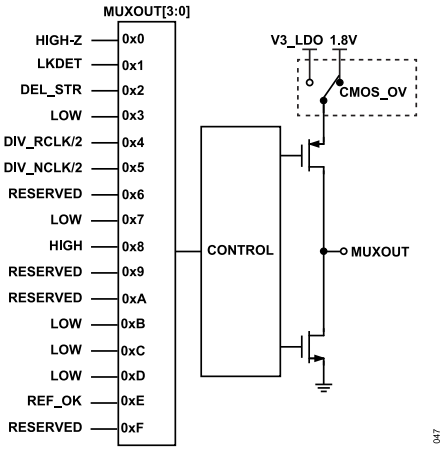

Figure 47. MUXOUT

Temperature Sensor

The temperature sensor is composed of an 8-bit ADC, which measures the proportional to absolute temperature (PTAT) voltage with respect to the reference voltage (VREF) of a bandgap. The purpose of the temperature sensor is to measure changes in the die temperature and not the absolute junction temperature. The maximum ADC clock frequency is 400 kHz. The ADC clock is generated from the RCLK.

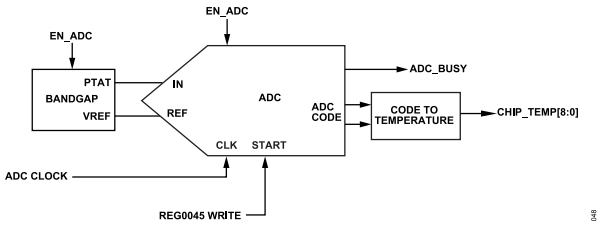

Figure 48. Temperature Sensor

Before an ADC measurement can occur, program the registers of the ADF4382A as shown in Table 17.

Table 17. ADC Register Setup

Bit Fields	Value
EN_DRCLK, EN_DNCLK	1
ADC_ST_CNV, EN_ADC, EN_ADC_CLK	1
PD_ADC	0

After the bits in Table 17 are programmed, start an ADC conversion with a register write to Register 0x045. An ADC conversion requires 17 clock cycles to complete. In Register 0x058, Bit 2, the ADC_BUSY bit monitors the conversion status. During a conversion, ADC_BUSY is set to 1, and when the conversion is complete, ADC_BUSY is set to 0. Measurements are recorded in the CHIP_TEMP bit fields, Bits[8:0], in Register 0x05B and Register 0x05C.

Double Buffering

Double buffering refers to a main and subordinate configuration for the bit fields shown in Table 18.

Only the subordinate bit fields control the actual state of the ADF4382A. When double buffering is enabled for a bit field, the serial interface only writes to the main bit field. The subordinate bit field retains its previous value until a register write is sent to Register 0x010. After writing to Register 0x010, all the main bit fields are automatically loaded to their respective subordinate bit fields. Writing to Register 0x010 also starts the autocalibration of the VCO (see the Standard Power-Up and Initialization Sequence, Automatic VCO Calibration section), which allows the user to update several bit fields that change the output frequency of the ADF4382A and starts a new VCO calibration on the same register write. When double buffering is disabled, the SPI writes directly to the subordinate bit field.

Table 18. Double Buffer Enabled Bit Fields

Double Buffer Enabled Bits	Double Buffered Bit Fields
Not applicable, always enabled	N_INT, R_DIV, EN_RDBLR, CP_I
RFOUTODIV_DB	RFOUT_DIV
DCLK_DIV_DB	DCLK_DIV1
DEL_CTRL_DB	INV_RFKOUT, BLEED_I, BLEED_POL

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Serial Port

The SPI-compatible serial port provides control and monitoring functionality. The CMOS_OV bit (Register 0x03D, Bit 5) determines if the logic high level for the SDO and SDIO SPI output pins is 3.3 V or 1.8 V. The CMOS_OV bit also sets the output level for the MUXOUT and LKDET pins.

The serial port can be programmed to support several different configurations in Register 0x000 and Register 0x001.

The SDO_ACTIVE bit (Register 0x000, Bit 3) determines if the serial port is configured as a 3-wire or 4-wire serial interface (see the timing diagrams in Figure 2, Figure 3 and Figure 4).

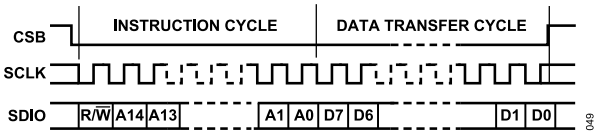

Figure 49. Serial Interface, MSB First (LSB_FIRST = 0)

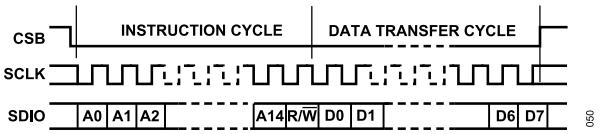

Figure 50. Serial Interface, LSB First (LSB_FIRST = 1)

The SPI register map can be programmed with single instructions, as shown in Figure 49 and Figure 50, or in streaming mode. Streaming mode allows for efficient data transfer read or write cycles to multiple registers. Streaming mode allows the user to program a bit stream composed of one register address in the instruction header and data for that register address, which is then followed by data in subsequent register addresses.

VCO

The VCO core consists of two separate VCOs both of which uses 512 overlapping bands, which allows the device to cover a wide frequency range without large VCO tuning sensitivity (K_{VCO}). The output frequency can be further extended by utilizing the output divider.

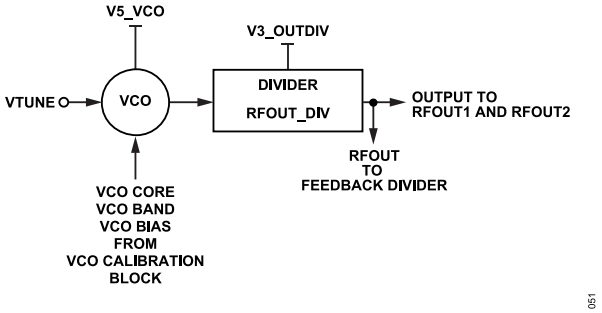

Figure 51. VCO and Clock Output Divider

The correct VCO core, band, and bias are chosen automatically by performing a VCO calibration. After a VCO calibration is performed for a specific frequency, the VCO core, band, and bias values can be recorded for that particular device. These values can be programmed manually later when the same device and frequency are used, thereby avoiding the VCO calibration time.

VCO Calibration

A VCO calibration is required to select the correct VCO core, band, and bias settings for a specific VCO frequency. This procedure assumes that the device is powered up, the desired reference frequency is present on the REFP and REFN pins, and all other registers are programmed correctly. Figure 52 and Figure 53 are provided as visual aids for this procedure.

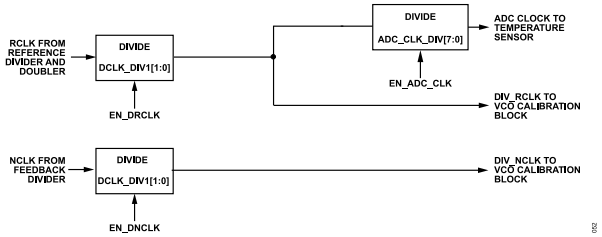

Figure 52. VCO Calibration Dividers

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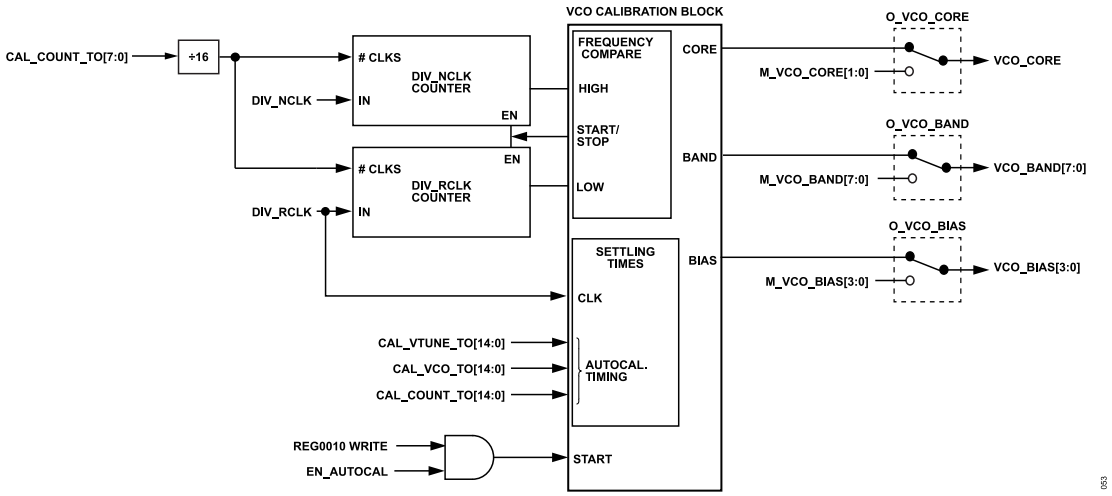

Figure 53. VCO Calibration Block

The following calibration timeout bit fields must be programmed for autocalibration:

- CAL_VTUNE_TO: At the beginning of the calibration, VTUNE is precharged to a nominal voltage, which is dependent on the temperature of operation. CAL_VTUNE_TO sets the precharge time as follows:

$$\text{CAL\_VTUNE\_TO} = \text{Ceil}\left(\text{Target VTUNE Calibration Timeout} \times \frac{f_{PFD}}{2^{\text{DCLK\_DIV1}}}\right)$$

  The largest value capacitor in the loop filter directly affects the time taken to precharge to VTUNE. Refer to the Calibration Time Performance Consideration section for more details.
- CAL_COUNT_TO: CAL_COUNT_TO is the count calibration timeout. During autocalibration, there are nine band decisions to be made to select the final band of operation for the selected frequency. CAL_COUNT_TO is used to program the time taken for each band decision. This time affects the calibration accuracy. Use the following equation to set the decision time of each band:

$$\text{CAL\_COUNT\_TO} = \text{Ceil}\left(\frac{\text{Target Band Decision Time} \times f_{PFD}}{2^{\text{DCLK\_DIV1}} \times 16}\right)$$

- CAL_VCO_TO: This bit field is used to set the time required for frequency settling after each band decision. To se this time, use the following equation:

$$\text{CAL\_VCO\_TO} = \text{Ceil}\left(\frac{\text{Target VCO Frequency Settling Timeout} \times f_{PFD}}{2^{DCLK\_DIV1}}\right)$$

To perform a VCO calibration, set up the following several registers as outlined in the following procedure:

1. Set DCLK_DIV1 and DCLK_MODE to the values listed in Table 19 and record f_{DIV_RCLK} for later use.
2. Calculate and set the minimum required values for CAL_VTUNE_TO, CAL_VCO_TO, and CAL_COUNT_TO as per their corresponding formulas previously described in this section.
3. Set the N_INT, RFOUT_DIV, and R_DIV bits and the EN_RDBLR bit by programming Register 0x010 last. Any writes to Register 0x010 start the VCO autocalibration.
4. Monitor the ADC_BUSY bit and FSM_BUSY bit (Register 0x058, Bit 2 and Bit 3, respectively). The calibration is finished when ADC_BUSY transitions from high to low, followed with FSM_BUSY transitioning from high to low.
5. After the VCO calibration is complete, disable the calibration clocks to limit unwanted spurious content by setting EN_DRCLK = EN_DNCLK = 0.

Table 19. DCLK_DIV1 and DCLK_MODE Setup

f_{PFD} (MHz)	DCLK_DIV1	DCLK_MODE	f_{DIV_RCLK} (MHz)
≤11	0	0	f_{FPD}
>11 and ≤160	0	1	$f_{FPD}/2$
>160 and ≤320	1	1	$f_{PFD}/4$
>320	2	1	$f_{PFD}/8$

Total Autocalibration Time

Use each of the calibration timeout values to calculate the total autocalibration time as follows:

Total Autocalibration Time = Target VTUNE Calibration Timeout + (2/f_{DIV_RCLK}) + (10 × VTUNE Setting Time) + V_{CAL} Low Time

where:

$$\text{VTUNE Settling Time} = \text{Target VTUNE Calibration Timeout} + (2 \times f_{DIV\_RCLK})$$

$$f_{DIV\_RCLK} = \frac{f_{PFD}}{2^{DCLK\_DIV1 + DCLK\_MODE}}$$

$$V_{CAL}\text{ Low Time} = \frac{2}{f_{DIV\_RCLK}}$$

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Calibration Time Performance Consideration

When programming the VCO calibration time as per the VCO Calibration section, the jitter performance can be affected by the overall calibration time. For applications where taking a longer time to autocalibrate is not an issue, for example, fixed frequency applications, it is recommended to program an autocalibration time of 250 µs to optimize jitter and phase noise performance. For other applications requiring faster autocalibration times and reduced overall lock times, an autocalibration time of 100 µs can be used. However, this time may degrade jitter with temperature changes over the complete −40°C to +105°C operating range.

Table 20. Recommended Calibration Times

Autocalibration Time (µs)	CAL_VTUNE_TO Time	CAL_COUNT_TO Time (µs)	CAL_VCO_TO Time (µs)
100	Determined by the largest loop filter capacitor	8.5	1
250	Determined by the largest loop filter capacitor	23.5	1

The CAL_VTUNE_TO time is determined by the charging time of the maximum value capacitor in the loop filter. Calculate the charge time by using the following equation:

$$t_{CHARGE} = (C \times V)/I$$

where:
C is the largest capacitor value in loop filter.
V is the VTUNE voltage change for lock and leave over temperature, which is typically 0.8 V.
I is the VCO calibration generator current of 4.2 mA.

Core Bias Table

As part of the initialization process, the core bias table must be programmed with the predefined values provided in Table 26 (see Register 0x100 through Register 0x111). These are specifically optimized VCO bias values for different frequency bands of operation. After performing a device initialization, the VCO bias registers are not reprogrammed until a subsequent power-on reset executes.

RF Output Divider (O)

A 3-bit divider, RFOUT_DIV (Register 11, Bits[7:5]), is used to divide the frequency seen at the output buffer and feedback divider. The divide ratio can be set to 1, 2, or 4. RFOUT_DIV is located inside the PLL. Therefore, any change to RFOUT_DIV requires a change to the N_INT bit fields (Register 0x010, Bits[7:0] and Register 0x011, Bits[3:0]) to maintain the same f_{PFD} and results in the PLL losing lock for a few loop time constants.

Table 21. RFOUT_DIV Programming

RFOUT_DIV	Divisor	Output Frequency Range (GHz)
0	1	11.5 ≤ RFOUT ≤ 21
1	2	5.75 ≤ RFOUT ≤ 10.5
2	4	2.875 ≤ RFOUT ≤ 5.25

Output Invert (INV_RFOUT)

The output invert, INV_RFOUT (Register 0x011, Bit 4), is used to shift the output signal 180°. INV_RFOUT is located inside the PLL, and any change to INV_RFOUT results in the PLL losing lock for few loop time constants.

Feedback Divider (N)

The feedback divider provides a division ratio in the PLL feedback path. The division ratio consists of the N_INT (Register 0x011, Bits[3:0] and Register 0x010, Bits[7:0]), FRAC1WORD (Register 0x15, Bit 0; Register 0x14, Bits[23:16]; Register 0x013, Bits[15:8], and Register 0x012, Bits[7:0]), FRAC2WORD (Register 0x19, Bits[23:16]; Register0x18, Bits[15:8]; and Register0x17, Bits[7:0]), and MOD2WORD (Register 0x1C, Bits[23:16]; Register 0x1B, Bits[15:8]; and Register 0x1A, Bits[7:0]) bit field values that this divider comprises together with the fixed modulus MOD1WORD (2^{25}). See the Applications Information section for the relationship between N_INT, FRAC1WORD, MOD1WORD, FRAC2WORD, MOD2WORD, RFOUT_DIV, together with R and D, and the f_{REF}, f_{PFD}, f_{VCO} and f_{OUT} frequencies.

Phase Adjust

One of the following two methods can be used to perform a phase adjustment of the RFOUT signals relative to their initial phase:

- Bleed current mode
- Σ-Δ mode

To enable bleed current mode, set DEL_MODE = 0. To enable Σ-Δ mode, set DEL_MODE = 1.

Bleed Current Phase Adjustment

A small programmable constant charge pump current, known as a bleed current, can be applied to the charge pump to adjust the phase. Bleed current phase adjustment is used in integer mode. Bleed current can also be applied in fractional mode to optimize performance (see the Charge Pump Bleed Current Optimization section for more details). The LSB step size depends on the RFOUT frequency. PHASE_ADJ_POL determines the direction of the phase adjustment. When PHASE_ADJ_POL = 0, the phase value is decreased. When PHASE_ADJ_POL = 1, the phase value is increased.

Ensure the following bit fields are programmed accordingly to enable bleed current adjustment:

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1. Set EN_BLEED = 1.
2. Set EN_PHASE_RESYNC = 1.
3. Set DEL_MODE = 0.
4. Use PHASE_ADJUSTMENT to determine the amount by which the phase is adjusted as follows:

$$\text{PHASE\_ADJUSTMENT} = \left(\frac{\text{Phase in Degrees} \times 511}{250\ \mu\text{A}}\right) \times I_{CP} \times \frac{f_{PFD}}{360 \times \text{RFOUT}}$$

The maximum adjustment time that can achieved using the bleed current method is t_{RFOUT}.

The bleed current applied can be read back from DEL_CNT.

Σ-Δ Modulator Phase Adjustment

The Σ-Δ modulator can be used to adjust the phase of the RFOUT signal by applying an offset value. The device must be used in fractional mode to adjust the Σ-Δ modulator, which is the case whether a fractional or integer frequency is used. Note that the in-band figure of merit degrades by 2 dB as compared with using integer mode. In addition, the maximum f_{PFD} is then 250 MHz in fractional mode, as compared to 625 MHz in integer mode.

An advantage of using fractional mode for adjusting the phase is that the range is infinite, which means that each time a phase adjust is performed, the phase increments by the value stored in the PHASE_ADJUSTMENT bits (Register 0x033, Bits[7:0]) without any limit to the number of times this can be done.

Ensure that the following bit fields are programmed accordingly to enable Σ-Δ phase adjustment:

1. Set EN_PHASE_RESYNC = 1.
2. Set DEL_MODE = 1.
3. Use PHASE_ADJUSTMENT to determine the amount by which the phase is adjusted for the Σ-Δ modulator as follows:

$$\text{PHASE\_ADJUSTMENT} = \left(\frac{\text{Phase in Degrees}}{360}\right) \times 2^{12}$$

PHASE_ADJ_POL selects the direction of adjustment. PHASE_ADJ_POL = 0 is positive and PHASE_ADJ_POL = 1 is negative. The PHASE_ADJUSTMENT value currently applied can be read back from the CUM_PHASE_ADJ bits (Register 0x061, Bits[7:0]). The maximum value is 8192 decimal. If this value is exceeded, the value overflows and wraps around.

When the required phase offsets are known prior to initializing the device, the PHASE_WORD bits can be used to program an initial phase offset using the same PHASE_ADJUSTMENT formula in this section.

Phase Adjust Pins

The ADF4382A has a 2-wire digital interface bus protocol that allows external control of the phase. This bus consists of DELSTR (Pin 29) and DELADJ (Pin 28). The signals are CMOS output signals with 1.8 V logic. This interface can be used in both bleed current and Σ-Δ mode phase adjustment. To enable the 2-wire interface, set EN_AUTO_ALIGN = 1.

DELSTR is an active high signal that is used to assert a phase adjustment. The amount by which the phase is adjusted is set in PHASE_ADJUSTMENT. The phase is adjusted on the falling edge of the signal.

DELADJ is an active high signal that controls the direction of the adjustment. If the signal is set to 0 while DELSTR is high, the RFOUT signal phase adjusts to earlier in time relative to the initial phase. If the signal is set to 1 while DELSTR is high, the RF output signal advances in time relative to the initial phase.

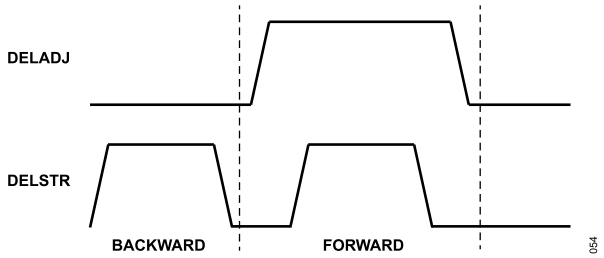

Figure 54. DELSTR and DELADJ Timing Diagrams

RF Output Buffer

The low noise, differential output buffer in Figure 55 produces a differential output voltage. The output amplitude level and common-mode voltage is programmable with the RFOUT1_OPWR (Register 0x029, Bits[3:0]) and RFOUT2_OPWR (Register 0x029, Bits[7:4]) bits. Each output can be either AC- or DC-coupled and terminated with 100 Ω differentially. If a single-ended output is desired, each side of the output must be individually AC-coupled and terminated with 50 Ω. External inductors are required to achieve the highest output power. A 1.4 nH, 0402 sized, pull-up inductor connected to the RFOUTx 3.3 V supply (V3_RFOUTx) is recommended.

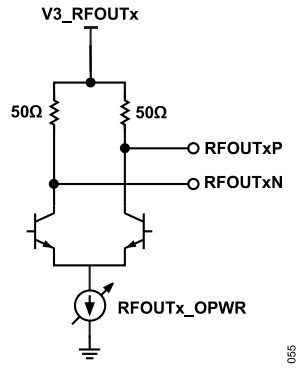

Figure 55. Simplified RF Output Buffer Schematic

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Mute RF Output

The RFOUTxP and RFOUTxN pins can be muted by using the MUTE_RFOUTx bit fields (Register 0x04, Bits[5:3] and Bits[2:0], respectively.

Table 22. MUTE_RFOUTx, Bit 0 through Bit 7, Controls

MUTE_RFOUTx, Bits	Function
0	Normal operation
1	Mute low and disable the emitter follower driver
2	Mute high and disable the emitter follower driver
3	Mute low and leave the emitter follower driver on
4	Mute low and disable the emitter follower driver during calibration
5	Mute low and keep the emitter follower running during calibration
6	Mute low and disable the emitter follower driver when LOCKED = 0
7	Mute low and keep the emitter follower running when LOCKED = 0

It is recommended to use options that keep the emitter follower on to minimize current fluctuations.

APPLICATIONS INFORMATION

POWER-UP AND INITIALIZATION SEQUENCE

The following steps describe the recommended power-up and initialization sequence of the ADF4382A:

1. Apply specified voltages to the V_{5V}, $V_{3.3V\_1}$, and $V_{3.3V\_2}$ power supply groups. The ADF4382A is in full power-down mode at this point and SPI programming is not possible.
2. Set the CE pin to a logic high. It is acceptable to connect the CE pin to the V3_LDO pin via a pull-up resistor. Therefore, Step 1 and Step 2 are performed coincidentally.
3. After waiting ≥200 µs for all SPI register bits to settle to their power-on reset (POR) state, begin programming the SPI to configure the ADF4382A to a desired state. The following is the recommended SPI programming sequence:
   a. Set the SDO_ACTIVE and CMOS_OV bits to a desired state for future readback operations.
   b. Program all register addresses in descending order, Register 0x053 to Register 0x010. There are several required reserved register field settings provided in Register Map that are required for proper device operation.
4. The ADF4382A remains in power-down mode until the PD_ALL bit is programmed to 0. After PD_ALL is disabled, VTUNE is precharged in the loop filter to reduce VCO calibration time. The precharge time required before starting a VCO calibration depends on the largest value of capacitor in the loop filter. The wait time is: $750 \times C_{MAX}$, where C_{MAX} is the maximum value capacitor in the loop filter. The minimum precharge time is 50 µs.
5. A write to Register 0x010 starts a VCO autocalibration. At this point, the ADF4382A is fully operational and new frequencies can be programmed as often as desired. The following steps are information for the PD_ALL bit and the CE pin.
6. Setting PD_ALL to 1 power down the ADF4382A, retaining the latest programmed SPI settings and full SPI programming capability.
7. If only the state of PD_ALL was modified in Step 6, setting PD_ALL to 0 returns the ADF4382A to the frequency programmed in Step 5. After a 10 µs wait, all circuit blocks are completely powered up internally. This 10 µs wait does not include the frequency settling time associated with the loop filter bandwidth.
8. Toggling the CE pin level causes the ADF4382A to return to full power-down mode and return the SPI registers to the POR state (see Step 2 and Step 3).

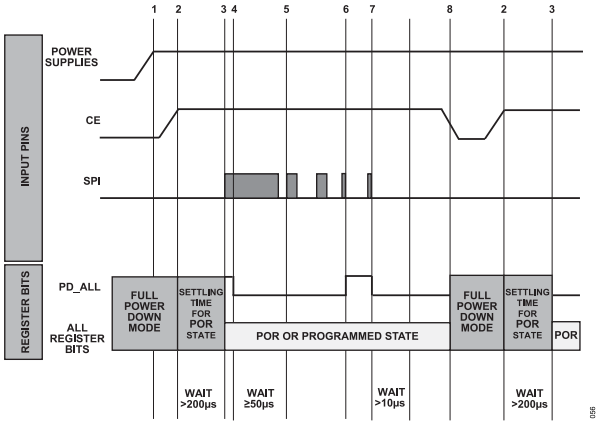

Figure 56. Power-Up and Initialization

Programming Procedure

There are two different methods to power up the ADF4382A. The most commonly used method is provided in the Standard Power-Up and Initialization Sequence, Automatic VCO Calibration section is mandatory at the initial device power-up.

The method provided in the Fast Power-Up and Initialization, Manually Programmed VCO Calibration Settings section is an optional power-up procedure after the initial power-up.

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Standard Power-Up and Initialization Sequence, Automatic VCO Calibration

The following standard power-up and initialization sequence is the recommended procedure to power up and program the ADF4382A:

1. Follow Step 1 through Step 5 in the Power-Up and Initialization Sequence section.
2. It is optional to monitor the status of the VCO calibration bits, ADC_BUSY and FSM_BUSY (Register 0x058, Bit 2 and Bit 1, respectively. A VCO calibration is completed when ADC_BUSY transitions from high to low followed by FSM_BUSY transitioning from high to low.
3. After the VCO calibration is complete, disable the VCO calibration clocks by setting EN_DRCLK = EN_DNCLK = EN_ADC_CLK = 0. Disabling the VCO calibration clocks reduces unwanted spurious content.
4. The PLL is locked when the lock detector sets the LKDET pin (Pin 27) and the LOCKED bit (Register 0x58, Bit 0) high.
5. When changing the frequency, take the following steps:
   a. Program only the modified registers in descending order.
   b. Write to Register 0x010 to start a new VCO autocalibration as the final step whether it is modified or not.

Fast Power-Up and Initialization, Manually Programmed VCO Calibration Settings

For fast frequency hopping applications, much shorter lock time is required. The ADF4382A can be manually programmed with predetermined calibration values to decrease overall lock time by bypassing VCO calibration. The calibration values are first obtained by performing an autocalibration and reading back the corresponding band, core, and bias values for a given frequency. These values can then be manually programmed to the ADF4382A on subsequent device initializations. The values of the readbacks vary with each device due to process variation.

The following steps outline the procedure to perform a manual VCO calibration after initialization:

1. Perform an autocalibration with the target frequency required.
2. Record the VCO_CORE and VCO_BAND.
3. If VCO_CORE = 0, read the VCO bias value from VCO0_BIAS_RDBK. If VCO_CORE = 1, read the VCO bias value from VCO1_BIAS_RDBK. The value read is used as the M_VCO_BIAS value.
4. On subsequent power-up and initialization sequences, program the override (O_VCO_CORE, O_VCO_BAND, and O_VCO_BIAS) and manual VCO bits (M_VCO_CORE, M_VCO_BAND, and M_VCO_BIAS) as documented in Table 23. All other bit fields are programmed as normal.
5. Repeat the sequence for each target frequency.

Table 23. Manually Programmed VCO Calibration Settings

Bit Fields	Value	Description
O_VCO_DB	0x1	Manually calibrated values are double buffered by programming N_INT.
EN_AUTOCAL	0x0	Disables autocalibration.
EN_DRCLK	0x0	Disables DIV_RCLK to the digital block
EN_DNCLK	0x0	Disables DIV_NCLK to the digital block.
EN_ADC_CLK	0x0	Disables the ADC clock.
O_VCO_CORE	0x1	Overrides the VCO core with value in M_VCO_CORE.
O_VCO_BAND	0x1	Overrides the VCO band with M_VCO_BAND.
O_VCO_BIAS	0x1	Overrides the VCO bias with M_VCO_BIAS.
M_VCO_CORE	Program with recorded values	Selects the VCO core when O_VCO_CORE = 1.
M_VCO_BAND	Program with recorded values	Selects the band within the core when O_VCO_BAND = 1.
M_VCO_BIAS	Program with recorded values	Selects the bias value used when O_VCO_BIAS = 1.

Loop Filter Design

A stable loop filter design requires care in selecting the loop filter components of the ADF4382A. It is recommended to download and install ADIsimPLL for loop filter design and simulation. ADIsimPLL has an integrated tutorial for first time users and a help manual for more complex topics. There are also several ADIsimPLL training videos available on the ADIsimPLL web page. After a loop filter is designed and simulated, it is recommended to verify the new loop filter using the ADF4382A evaluation hardware. A full loop filter design tutorial is beyond the scope of this data sheet. However, some best practices are shown in the following list. ADIsimPLL aids in defining and simulating these parameters. Any significant change to these items requires a new loop filter design.

A stable loop filter must meet the following criteria:

- Loop filter phase margin > 45°
- Loop filter bandwidth < f_{PFD} ÷ 10

The desired loop filter bandwidth is determined by the following features of the ADF4382A:

- I_{CP}
- K_{VCO}
- PFD frequency
- Reference input phase noise (see the Reference Phase Noise section).
- Trade-off between minimizing jitter or settling time

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The VTUNE pin has an internal 54 pF capacitor to GND that must be included in the loop filter design. ADIsimPLL takes this internal capacitance into account automatically.

Another consideration when selecting the loop filter components is the largest value capacitor in the loop filter design because this will directly affect the minimum VTUNE precharge time before a VCO calibration. The minimum precharge time is calculated as follows:

$$t_{PRECHARGE} = \frac{C \times V}{I}$$

where:
I is the VCO calibration generator current (6 mA).
C is the largest loop filter capacitance.
V is the nominal charge pump voltage.

For example, using a capacitance value of 10 nF and charge pump voltage of 3.6 V results in the following:

$$t_{PRECHARGE} = \frac{10\ nF \times 3.6V}{6\ mA} = 6\ \mu s$$

Refer to the VCO Calibration section for programming the pre-charge time dependent bit fields.

REFERENCE SOURCE CONSIDERATIONS

Reference Input Network

The reference input buffer of the ADF4382A shown in Figure 42 provides a flexible interface to either differential or single-ended frequency sources. Figure 57 to Figure 62 show the recommended interfaces for different reference signal types. All characteristic impedance (Z_0) signal traces are 50 Ω transmission lines.

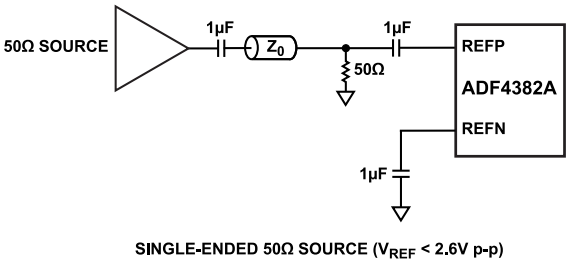

Figure 57. Single-Ended 50 Ω Source (V_{REF} < 2.6 V p-p)

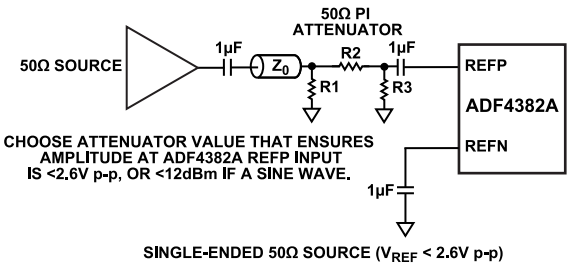

Figure 58. Single-Ended 50 Ω Source (V_{REF} < 2.6 V p-p)

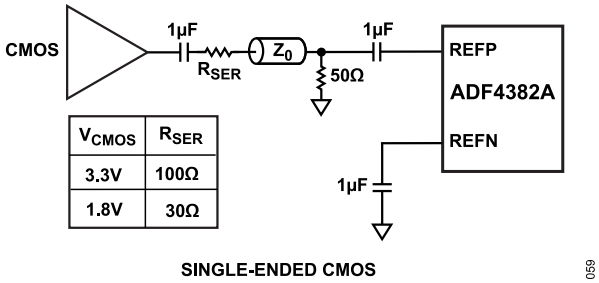

Figure 59. Single-Ended CMOS (R_{SER} Is the Series Resistance.)

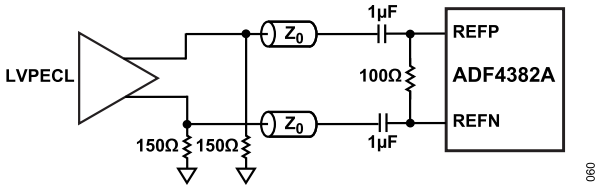

Figure 60. Differential, Low Voltage, Positive Emitter-Coupled Logic (LVPECL)

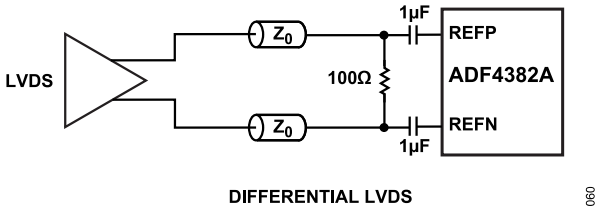

Figure 61. Differential LVDS

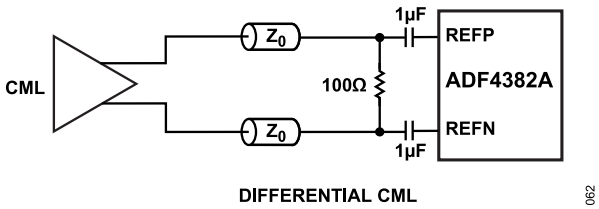

Figure 62. Differential CML

Reference Phase Noise

The ADF4382A achieves an in-band normalized phase noise floor of L_{NORM} = −239 dBc/Hz in integer mode and L_{NORM}= −237 dBc/Hz in fractional mode.

To calculate the equivalent input phase noise floor (L_{IN}) use the following formula:

$$L_{IN} = L_{NORM} + 10 \times \log_{10}(f_{REF})$$

For example, a 100 MHz reference input frequency gives an L_{IN} of −157 dBc/Hz in fractional mode. The phase noise of the reference frequency source must be at least 6 dB less than L_{IN} to avoid impacting and increasing the overall system phase noise.

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To maintain typical L_{NORM} performance, Table 7 provides criteria for selecting the optimal REF_SEL (Register 0x030, Bit 5) setting based on the input reference signal type and amplitude

OUTPUT PHASE NOISE CHARACTERISTICS

In-Band Output Phase Noise

Use the following equations to calculate the in-band phase noise floor (L_{OUT}) produced at f_{OUT}:

$$L_{OUT} = L_{NORM} + 10 \times \log_{10}\left(f_{PFD}\right) + 20 \times \log_{10}\left(\frac{f_{OUT}}{f_{PFD}}\right)$$

or

$$L_{OUT} = \ L_{NORM} + 10 \times \log_{10}\left(f_{PFD}\right) + 20 \times \log_{10}\left(\frac{N}{O}\right)$$

Output Phase Noise Due to 1/f Noise

In-band phase noise at low offset frequencies can be influenced by the 1/f noise of the ADF4382A depending on the f_{PFD}. Use the normalized in-band 1/f noise ($L_{1/f}$) of −287 dBc/Hz to approximate the output 1/f phase noise at a given frequency offset (f_{OFFSET}) as follows:

$$L_{OUT(1/f)} = \ L_{1/f} + 20 \times \log_{10}\left(f_{OUT}\right) - 10 \times \log_{10}\left(f_{OFFSET}\right)$$

Unlike the in-band noise floor (L_{OUT}), the 1/f noise ($L_{OUT}(1/f)$) does not change with f_{PFD} and is not constant over offset frequency. For an example of in-band phase noise for f_{PFD} equal to 100 MHz and 500 MHz for integer mode, see Figure 63. The total phase noise is the summation of L_{OUT} and $L_{OUT(1/f)}$ calculated by the following formula:

$$L_{OUT(TOTAL)} = 10 \times \log_{10}\left(10^{L_{OUT}/10} + 10^{L_{OUT}(1/f)/10}\right)$$

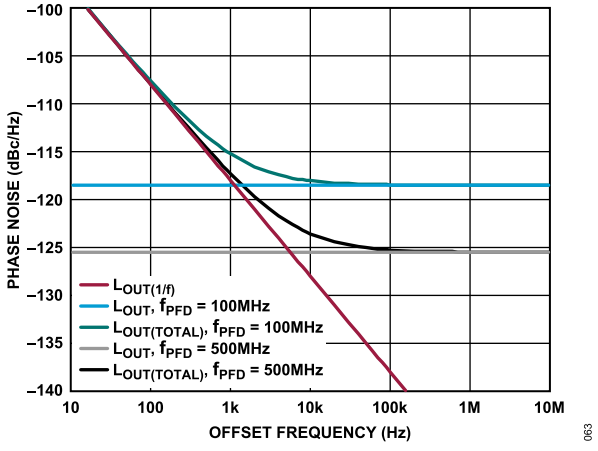

Figure 63. Theoretical In-Band Phase Noise, f_{OUT} = 10 GHz

OUTPUT PHASE SYNCHRONIZATION OF MULTIPLE ADF4382A DEVICES

To synchronize multiple ADF4382A devices, use one of the following two methods:

- EZSync™ method, which uses SPI register writes for synchronization
- Timed synchronization method , which uses the SYNCx pin on the ADF4382A for synchronization

EZSync Method

The EZSync synchronization method allows synchronization of the output phases of multiple devices without the need for a separate synchronization signal, which has the advantage of reducing PCB layout complexity in systems using multiple ADF4382A devices.

EZSync relies on sending a synchronization request through the SPI by setting SW_SYNC = 1 instead of the SYNC pin. The problems with sending the request over the SPI are that the SPI is a slow protocol and does not have any time accuracy. Sending the request in the same reference period is also another challenge and even impossible for a huge number of ADF4382A devices used. With EZSync, these problems are solved by starting and stopping the DC-coupled reference signal glitchlessly, which removes the setup and hold time concern with sending a request through the SPI. The reference signals must stop and start accurately and without any glitch or without any runt pulse. The clock generation and distribution devices from Analog Devices, such as the LTC6953, are recommended as these devices are compatible with EZSync.

The following steps outline the procedure to perform an EZSync with two ADF4382A devices (assumes the LTC6953 is set up in SYNC mode):

1. Set up each ADF4382A as follows:
    a. Initialize the ADF4382A with the default initialization settings.
    b. Set TIMED_SYNC (Register 0x01E, Bit 5) = 1.
    c. Set EN_REF_RST (Register 0x01E, Bit 6) = 1.
    d. Set EN_PHASE_RESYNC (Register 0x01E, Bit 7) = 1.
    e. Set SYNC_SEL (Register 0x053, Bit 5) = 1.
2. Verify that both ADF4382A devices are locked.
3. Synchronize both ADF4382A RFOUT signals:
    a. On an oscilloscope, first verify that both ADF4382A parts are not synchronized
    b. Set SW_SYNC (Register 0x01F, Bit 7) = 1 on each ADF4382A.
    c. Set SSRQ (Address hOC, Bit 0) = 1 on LTC6953.
    d. Set SW_SYNC = 0 on each ADF4382A.
    e. Set SSRQ = 0 on LTC6953.

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4. On the oscilloscope, verify that the outputs from both ADF4382A devices are synchronized (aside from cable mismatch).

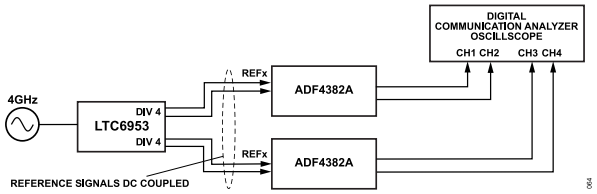

Figure 64. EZSync Configuration

Timed Synchronization Method

The timed synchronization method uses an external synchronization signal to synchronize multiple ADF4382A devices, which is the more traditional method for synchronization of devices. This method requires an additional external signal from the clock distribution device to provide the synchronization signal. Each synchronization signal must be matched for accurate output phase matching. A rising edge of the synchronization pulse on the SYNC pin of the ADF4382A triggers the start of the synchronization process which puts the device into a reset state. On the falling edge of the synchronization pulse, the RFOUT signal phase on each ADF4382A is then aligned to a known phase relative to the reference phase.

The following steps outline the procedure to perform a timed synchronization with two ADF4382A devices using the LTC6953:

1. Set up the LTC6953 as follows:
   a. Program the REF outputs for /4 (assumes the reference frequency (f_{REF}) = 1 GHz).
   b. Program the SYNC outputs for /512.
   c. Program to the SYNC mode by setting SRQMD = 1 and toggle SSRQ from 0 to 1.
   d. Program to SYSREF pulse mode by setting SRQMD = 0 and SYSCT = 0.
2. Set up the ADF4382A as follows:
   a. Set TIMED_SYNC (Register 0x01E, Bit 5) = 1.
   b. Set EN_REF_RST (Register 0x01E, Bit 6) = 1.
   c. Set EN_PHASE_RESYNC (Register 0x01E, Bit 7) = 1.
   d. Set SYNC_SEL (Register 0x053, Bit 5) = 0.
   e. Set R_DIV (Register 0x020, Bits[5:0]) = 4.
   f. Set EN_DRCLK (Register 0x02D, Bit 6) = 1.
   g. Verify that the ADF4382A devices are locked.
3. Synchronize both ADF4382A devices:
   a. Verify that both ADF4382A outputs are not synchronized.
   b. Toggle the SSRQ bit on the LTC6953, and outputs on both ADF4382A devices should now be phase synchronized.

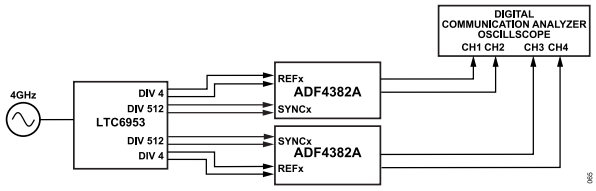

Figure 65. Timed Synchronization Configuration

PHASE SYNCHRONIZATION SETTINGS

To optimize phase noise and spurious performance on the ADF4382A, there are a number of bit fields that must be programmed based on the f_{PFD} used. Table 24 shows the optimal settings for phase synchronization.

Table 24. Phase Synchronization Settings

	RDIV = 3, 6, 12, 14, 15, 24, 26 to 31, 46, 48 to 63			RDIV = 1, 2, 4, 5, 7 to 11, 13, 16 to 23, 25, 32 to 45, 47		
PFD Frequency	**REF_CK_FALL**	**REF_DC_SEL**	**xx_DEL[1]**	**REF_CK_FALL**	**REF_DC_SEL**	**xx_DEL[1]**
$f_{PFD} \geq 225$ MHz	0	0	3	0	0	3
200 MHz $\leq f_{PFD} < 225$ MHz	0	0	4	0	0	4
148 MHz $\leq f_{PFD} < 200$ MHz	1	3	1	1	3	0
130 MHz $\leq f_{PFD} < 148$ MHz	1	3	3	1	3	1
85 MHz $\leq f_{PFD} < 130$ MHz	1	3	4	1	3	1
$f_{PFD} < 85$ MHz	1	2	0	1	2	1

[1] xx_DEL denotes SYNC_DEL, DNCLK_DEL, and DRCLK_DEL.

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PHASE RESYNCHRONIZATION

Phase resynchronization is a feature that allows a consistent phase on the RFOUT signal with respect to the input reference at each output frequency, which is useful in applications requiring synchronization of multiple ADF4382A devices. After multiple devices are synchronized, any additional resynchronizing (for example, after a frequency change) is not needed.

The following sequence is the phase resynchronization method procedure:

1. Power up and initialize the ADF4382A devices.
2. Program all ADF4382A devices to the same frequency.
3. Perform an initial synchronization (timed synchronization or EZSync).
4. Enable phase resynchronization mode by taking the following steps:
   a. Set DEL_MODE (Register 0x032, Bit 5) = 1.
   b. Set EN_PHASE_RESYNC (Register 0x01E, Bit 7) = 1.
   c. Set EN_REF_RST Register 0x01E , Bit 6) = 1.
   d. Set EN_DRCLK (Register 0x02D, Bit 6) = 1.
   e. Program the t_{RESYNC} default to 100 µs by
      $t_{RESYNC} = \frac{RESYNC\_WAIT}{f_{PFD}}$
      for f_{PFD} = 250 MHz and t_{RESYNC} = 25,000.

Σ-Δ MODULATOR OPTIMIZATION MODES

The ADF4382A can be configured in three different Σ-Δ modulator modes for performance optimization. A different Σ-Δ modulator mode can be configured to optimize for either phase jitter or spurious performance by configuring the EFM3_MODE bits (Register 0x032, Bits[2:0]) to select SDM mode.

A common feature used in fractional spur reduction known as dithering can be incorporated in addition to the Σ-Δ modulator optimization. This dithering involves reducing spurs by applying a randomization to the fractional N-divider feedback value. EN_DITHER1, DITHER1_SCALE, and EN_DITHER2 control the amount of dithering that is applied.

Some common fractional spur mechanisms that can be reduced with Σ-Δ modulator optimization are as follows:

- FRAC1WORD multiples of 8192.
- Fractional values close to 2^N. These values increase in level towards the upper region of each core.
- Fractional values of multiples 1/1000.

Table 25. SDM Mode Optimization

EFM3_MODE	Minimum N Divider	Optimization	Description
0	10	Best jitter performance	This is the default mode used, and fractional spurs are present. These spurs can be reduced by using dithering.
4	23	Best spurious performance	This setting removes the fractional spur mechanism while degrading jitter performance as compared with EFM_MODE = 0 performance.
5	27	Phase noise profile optimization	The phase noise profile can appear more linear and up to 1 dB of phase noise improvement at frequency offsets ≥10 MHz. Dither can be applied to further reduce fractional spurs.

REGISTER MAP

Table 26. ADF4382A Register Map

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x000	REG0000	[7:0]	SOFT_ RESET_R	LSB_ FIRST_R	ADDRESS_ ASCENSION _R	SDO_ ACTIVE_R	SDO_ ACTIVE	ADDRESS_ ASCENSIO N	LSB_ FIRST	SOFT_ RESET	0x00	R/W
0x001	REG0001	[7:0]	SINGLE_ INSTRUC- TION	0	MASTER_ READ BACK_ CONTROL	0	RESERVED	0	0	RESERVED	0x00	R/W
0x002	REG0002	[7:0]	RESERVED				CHIP_STATUS				0x00	R
0x003	REG0003	[7:0]	RESERVED				CHIP_TYPE				0x00	R
0x004	REG0004	[7:0]	PRODUCT_ID[7:0]								0x00	R
0x005	REG0005	[7:0]	PRODUCT_ID[15:8]								0x00	R
0x006	REG0006	[7:0]	RESERVED				DEVICE_REVISION				0x00	R
0x00A	REG000A	[7:0]	SCRATCHPAD								0x00	R/W
0x00C	REG000C	[7:0]	VENDOR_ID[7:0]								0x56	R
0x00D	REG000D	[7:0]	VENDOR_ID[15:8]								0x04	R
0x010	REG0010	[7:0]	N_INT[7:0]								0x80	R/W
0x011	REG0011	[7:0]	RFOUT_DIV			INV_RFOUT	N_INT[11:8]				0x00	R/W
0x012	REG0012	[7:0]	FRAC1WORD[7:0]								0x00	R/W
0x013	REG0013	[7:0]	FRAC1WORD[15:8]								0x00	R/W
0x014	REG0014	[7:0]	FRAC1WORD[23:16]								0x00	R/W
0x015	REG0015	[7:0]	M_VCO_ BAND[0]	M_VCO_ CORE	BIAS_DEC_MODE			INT_MODE	PFD_POL	FRAC1- WORD[24]	0x00	R/W
0x016	REG0016	[7:0]	M_VCO_BAND[8:1]								0x00	R/W
0x017	REG0017	[7:0]	FRAC2WORD[7:0]								0x00	R/W
0x018	REG0018	[7:0]	FRAC2WORD[15:8]								0x00	R/W
0x019	REG0019	[7:0]	FRAC2WORD[23:16]								0x00	R/W
0x01A	REG001A	[7:0]	MOD2WORD[7:0]								0x00	R/W
0x01B	REG001B	[7:0]	MOD2WORD[15:8]								0x00	R/W
0x01C	REG001C	[7:0]	MOD2WORD[23:16]								0x00	R/W
0x01D	REG001D	[7:0]	BLEED_I[7:0]								0x00	R/W
0x01E	REG001E	[7:0]	EN_PHASE_ RESYNC	EN_REF_ RST	TIMED_ SYNC	BLEED_I[12:8]					0x00	R/W
0x01F	REG001F	[7:0]	SW_SYNC	RESERVED	BLEED_ POL	EN_BLEED	CP_I				0x00	R/W
0x020	REG0020	[7:0]	EN_ AUTOCAL	EN_RDBLR	R_DIV						0x01	R/W
0x021	REG0021	[7:0]	PHASE_WORD[7:0]								0x00	R/W
0x022	REG0022	[7:0]	PHASE_WORD[15:8]								0x00	R/W
0x023	REG0023	[7:0]	PHASE_WORD[23:16]								0x00	R/W
0x024	REG0024	[7:0]	REF_CK_ FALL	REF_DC_SEL		DCLK_DIV_ SEL	DNCLK_DIV1		DCLK_DIV1		0x00	R/W
0x025	REG0025	[7:0]	RESYNC_WAIT[7:0]								0x00	R/W
0x026	REG0026	[7:0]	RESYNC_WAIT[15:8]								0x00	R/W
0x027	REG0027	[7:0]	0				0				0x00	R/W
0x028	REG0028	[7:0]	PHASE_ RESYNC_ RB_SEL	LSB_P1	VAR_ MOD_EN	DITHER1_SCALE			EN_ DITHER2	EN_DITHER1	0x00	R/W
0x029	REG0029	[7:0]	RFOUT2_OPWR				RFOUT1_OPWR				0x00	R/W
0x02A	REG002A	[7:0]	0	0	0	PD_SYNC	0	PD_RDET	PD_ADC	0	0x04	R/W

REGISTER MAP

Table 26. ADF4382A Register Map (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x02B	REG002B	[7:0]	PD_ALL	PD_RDIV	PD_NDIV	PD_VCO	PD_LD	PD_PFDCP	PD_RFOUT1	PD_RFOUT2	0x83	R/W
0x02C	REG002C	[7:0]	LDWIN_PW			LD_COUNT					0x00	R/W
0x02D	REG002D	[7:0]	EN_DNCLK	EN_DRCLK	EN_LOL	EN_LDWIN	PDET_POL	RST_LD	LD_O_CTRL		0x00	R/W
0x02E	REG002E	[7:0]	MUXOUT				ABPW_WD	EN_CPTEST	CP_DOWN	CP_UP	0x00	R/W
0x02F	REG002F	[7:0]	BST_REF	FILT_REF	RDBLR_DC						0x00	R/W
0x030	REG0030	[7:0]	MUTE_NCLK	MUTE_RCLK	REF_SEL	INV_RDBLR	RDBLR_DEL_SEL				0x00	R/W
0x031	REG0031	[7:0]	SYNC_DEL			RST_SYS	EN_ADC_CLK	EN_VCAL	CAL_CT_SEL	DCLK_MODE	0x00	R/W
0x032	REG0032	[7:0]	RESERVED		DEL_MODE	EN_AUTO_ALIGN	PHASE_ADJ_POL	EFM3_MODE			0x00	R/W
0x033	REG0033	[7:0]	PHASE_ADJUSTMENT								0x00	R/W
0x034	REG0034	[7:0]	PHASE_ADJ		DRCLK_DEL		DNCLK_DEL			RST_CNTR	0x00	R/W
0x035	REG0035	[7:0]	RESERVED		M_VCO_BIAS						0x00	R/W
0x036	REG0036	[7:0]	RFOUTODIV_DB	DCLK_DIV_DB	RESERVED				0	0	0x00	R/W
0x037	REG0037	[7:0]	CAL_COUNT_TO								0x00	R/W
0x038	REG0038	[7:0]	CAL_VTUNE_TO[7:0]								0x00	R/W
0x039	REG0039	[7:0]	O_VCO_DB	CAL_VTUNE_TO[14:8]							0x00	R/W
0x03A	REG003A	[7:0]	CAL_VCO_TO[7:0]								0x00	R/W
0x03B	REG003B	[7:0]	DEL_CTRL_DB	CAL_VCO_TO[14:8]							0x00	R/W
0x03C	REG003C	[7:0]	0								0x00	R/W
0x03D	REG003D	[7:0]	RESERVED	0	CMOS_OV	0	0				0x00	R/W
0x03E	REG003E	[7:0]	ADC_CLK_DIV								0x00	R/W
0x03F	REG003F	[7:0]	1	0	0	0	0	0	EN_ADC	0	0x00	R/W
0x040	REG0040	[7:0]	0	0	MUTE_RFOUT2			MUTE_RFOUT1			0x00	R/W
0x041	REG0041	[7:0]	0		0	0	0	0	0	0	0x00	R/W
0x042	REG0042	[7:0]	0								0x00	R/W
0x044	REG0044	[7:0]	0	VPTAT_CALGEN							0x00	R/W
0x045	REG0045	[7:0]	RESERVED	VCTAT_CALGEN							0x00	R/W
0x04B	REG004B	[7:0]	TEMP_OFFSET								0x00	R/W
0x04D	REG004D	[7:0]	RESERVED					O_VCO_BIAS	O_VCO_BAND	O_VCO_CORE	0x00	R/W
0x050	REG0050	[7:0]	SPARE0								0x00	R/W
0x053	REG0053	[7:0]	SPARE_53	PD_SYNC_MON	SYNC_SEL	RST_SYNC_MON	SYNC_SH_DEL				0x00	R/W
0x054	REG0054	[7:0]	RESERVED							ADC_ST_CNV	0x00	R/W
0x055	REG0055	[7:0]	COUNTER_READBACK[7:0]								0x00	R
0x056	REG0056	[7:0]	COUNTER_READBACK[15:8]								0x00	R
0x057	REG0057	[7:0]	COUNTER_READBACK[23:16]								0x00	R
0x058	REG0058	[7:0]	RESERVED	SYNC_OK	DEL_STR	DEL_ADJ	REF_OK	ADC_BUSY	FSM_BUSY	LOCKED	0x00	R
0x059	REG0059	[7:0]	RESERVED		VCO0_BIAS_RDBK						0x00	R
0x05A	REG005A	[7:0]	RESERVED		VCO1_BIAS_RDBK						0x00	R
0x05B	REG005B	[7:0]	CHIP_TEMP[7:0]								0x00	R

REGISTER MAP

Table 26. ADF4382A Register Map (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x05C	REG005C	[7:0]	RESERVED							CHIP_TEMP[8]	0x00	R
0x05D	REG005D	[7:0]	ADC_CODE								0x00	R
0x05E	REG005E	[7:0]	VCO_BAND[7:0]								0x00	R
0x05F	REG005F	[7:0]	RESERVED						VCO_CORE	VCO_BAND[8]	0x00	R
0x060	REG0060	[7:0]	RESERVED					READBACK_SPARE		RESERVED	0x00	R
0x061	REG0061	[7:0]	CUM_PHASE_ADJ[7:0]								0x00	R
0x062	REG0062	[7:0]	CUM_PHASE_ADJ[15:8]								0x00	R
0x063	REG0063	[7:0]	RESERVED							CUM_PHASE_ADJ[16]	0x00	R
0x064	REG0064	[7:0]	DEL_CNT[7:0]								0x00	R
0x065	REG0065	[7:0]	DEL_CNT[15:8]								0x00	R
0x066	REG0066	[7:0]	FIRST_PASS_VCO_BAND								0x00	R
0x067	REG0067	[7:0]	VERSION								0x00	R
0x100	REG0100	[7:0]	RESERVED		CORE0_BIAS_TABLE_0						0x00	R/W
0x101	REG0101	[7:0]	RESERVED		CORE0_BIAS_TABLE_1						0x00	R/W
0x102	REG0102	[7:0]	RESERVED		CORE0_BIAS_TABLE_2						0x00	R/W
0x103	REG0103	[7:0]	RESERVED		CORE0_BIAS_TABLE_3						0x00	R/W
0x104	REG0104	[7:0]	RESERVED		CORE0_BIAS_TABLE_4						0x00	R/W
0x105	REG0105	[7:0]	RESERVED		CORE0_BIAS_TABLE_5						0x00	R/W
0x106	REG0106	[7:0]	RESERVED		CORE0_BIAS_TABLE_6						0x00	R/W
0x107	REG0107	[7:0]	RESERVED		CORE0_BIAS_TABLE_7						0x00	R/W
0x108	REG0108	[7:0]	RESERVED		CORE0_BIAS_TABLE_8						0x00	R/W
0x109	REG0109	[7:0]	RESERVED		CORE1_BIAS_TABLE_0						0x00	R/W
0x10A	REG010A	[7:0]	RESERVED		CORE1_BIAS_TABLE_1						0x00	R/W
0x10B	REG010B	[7:0]	RESERVED		CORE1_BIAS_TABLE_2						0x00	R/W
0x10C	REG010C	[7:0]	RESERVED		CORE1_BIAS_TABLE_3						0x00	R/W
0x10D	REG010D	[7:0]	RESERVED		CORE1_BIAS_TABLE_4						0x00	R/W
0x10E	REG010E	[7:0]	RESERVED		CORE1_BIAS_TABLE_5						0x00	R/W
0x10F	REG010F	[7:0]	RESERVED		CORE1_BIAS_TABLE_6						0x00	R/W
0x110	REG0110	[7:0]	RESERVED		CORE1_BIAS_TABLE_7						0x00	R/W
0x111	REG0111	[7:0]	RESERVED		CORE1_BIAS_TABLE_8						0x00	R/W

REGISTER MAP

REGISTER DETAILS

Address: 0x000, Reset: 0x00, Name: REG0000

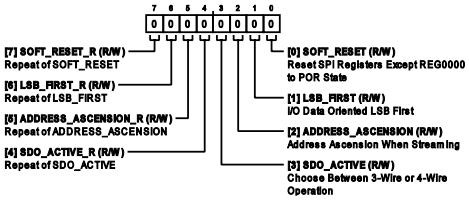

Table 27. Bit Descriptions for REG0000

Bits	Bit Name	Description	Reset	Access
7	SOFT_RESET_R	Repeat of SOFT_RESET.	0x0	R/W
6	LSB_FIRST_R	Repeat of LSB_FIRST.	0x0	R/W
5	ADDRESS_ASCENSION_R	Repeat of ADDRESS_ASCENSION.	0x0	R/W
4	SDO_ACTIVE_R	Repeat of SDO_ACTIVE.	0x0	R/W
3	SDO_ACTIVE	Choose Between 3-Wire or 4-Wire Operation. 0: 3-wire. 1: 4-wire SPI (enables SDO and SDIO becomes an input only).	0x0	R/W
2	ADDRESS_ASCENSION	Address Ascension When Streaming. 0: address autodecrements when streaming. 1: address autoincrements when streaming.	0x0	R/W
1	LSB_FIRST	I/O Data Oriented LSB First. 0: MSB first. 1: LSB first.	0x0	R/W
0	SOFT_RESET	Reset SPI Registers Except REG0000 to POR State. Self-Clearing Reset 0: normal operation. 1: soft reset.	0x0	R/W

Address: 0x001, Reset: 0x00, Name: REG0001

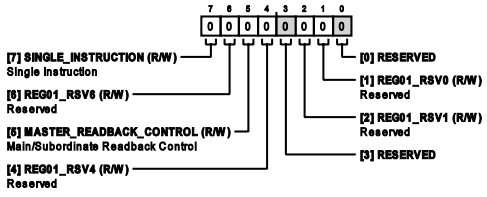

Table 28. Bit Descriptions for REG0001

Bits	Bit Name	Description	Reset	Access
7	SINGLE_INSTRUCTION	Single Instruction. 0: SPI streaming enabled. 1: SPI streaming disabled.	0x0	R/W
6	REG01_RSV6	Reserved. Table 26 provides required reserved register settings.	0x0	R/W

REGISTER MAP

Table 28. Bit Descriptions for REG0001 (Continued)

Bits	Bit Name	Description	Reset	Access
5	MASTER_READBACK_CONTROL	Main/Subordinate Readback Control. 0: for double-buffered bit fields readback subordinate register. 1: for double-buffered bit fields readback main register.	0x0	R/W
4	REG01_RSV4	Reserved. Table 26 provides required reserved register settings.	0x0	R/W
3	RESERVED	Reserved.	0x0	R
2	REG01_RSV1	Reserved. Table 26 provides required reserved register settings.	0x0	R/W
1	REG01_RSV0	Reserved. Table 26 provides required reserved register settings.	0x0	R/W
0	RESERVED	Reserved.	0x0	R

Address: 0x002, Reset: 0x00, Name: REG0002

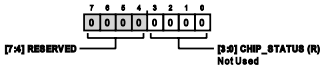

Table 29. Bit Descriptions for REG0002

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	CHIP_STATUS	Not Used.	0x0	R

Address: 0x003, Reset: 0x00, Name: REG0003

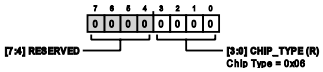

Table 30. Bit Descriptions for REG0003

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	CHIP_TYPE	Chip Type = 0x06.	0x0	R

Address: 0x004, Reset: 0x00, Name: REG0004

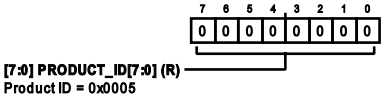

Table 31. Bit Descriptions for REG0004

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[7:0]	Product ID = 0x0005.	0x0	R

REGISTER MAP

Address: 0x005, Reset: 0x00, Name: REG0005

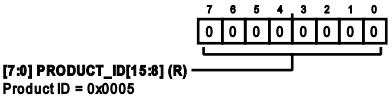

Table 32. Bit Descriptions for REG0005

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[15:8]	Product ID = 0x0005.	0x0	R

Address: 0x006, Reset: 0x00, Name: REG0006

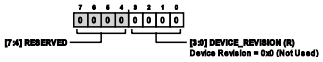

Table 33. Bit Descriptions for REG0006

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	DEVICE_REVISION	Device Revision = 0x0 (Not Used).	0x0	R

Address: 0x00A, Reset: 0x00, Name: REG000A

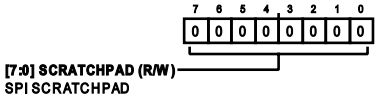

Table 34. Bit Descriptions for REG000A

Bits	Bit Name	Description	Reset	Access
[7:0]	SCRATCHPAD	SPI SCRATCHPAD.	0x0	R/W

Address: 0x00C, Reset: 0x56, Name: REG000C

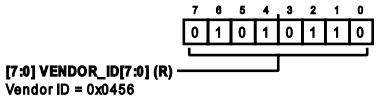

Table 35. Bit Descriptions for REG000C

Bits	Bit Name	Description	Reset	Access
[7:0]	VENDOR_ID[7:0]	Vendor ID = 0x0456.	0x56	R

Address: 0x00D, Reset: 0x04, Name: REG000D

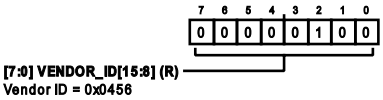

Table 36. Bit Descriptions for REG000D

Bits	Bit Name	Description	Reset	Access
[7:0]	VENDOR_ID[15:8]	Vendor ID = 0x0456.	0x4	R

REGISTER MAP

Address: 0x010, Reset: 0x80, Name: REG0010

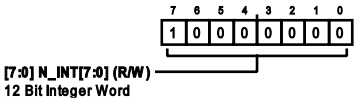

Table 37. Bit Descriptions for REG0010

Bits	Bit Name	Description	Reset	Access
[7:0]	N_INT[7:0]	12 Bit Integer Word.	0x80	R/W

Address: 0x011, Reset: 0x00, Name: REG0011

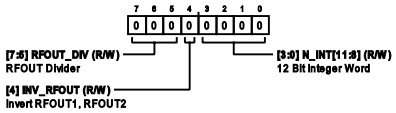

Table 38. Bit Descriptions for REG0011

Bits	Bit Name	Description	Reset	Access
[7:5]	RFOUT_DIV	RFOUT Divider. 000: divide by 1. 001: divide by 2. 010: divide by 4.	0x0	R/W
4	INV_RFOUT	Invert RFOUT1, RFOUT2. 0: CLK1, CLK2 not inverted. 1: CLK1, CLK2 inverted.	0x0	R/W
[3:0]	N_INT[11:8]	12 Bit Integer Word.	0x0	R/W

Address: 0x012, Reset: 0x00, Name: REG0012

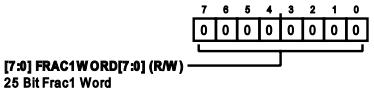

Table 39. Bit Descriptions for REG0012

Bits	Bit Name	Description	Reset	Access
[7:0]	FRAC1WORD[7:0]	25 Bit Frac1 Word.	0x0	R/W

Address: 0x013, Reset: 0x00, Name: REG0013

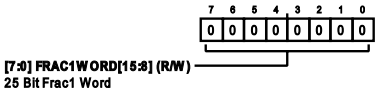

Table 40. Bit Descriptions for REG0013

Bits	Bit Name	Description	Reset	Access
[7:0]	FRAC1WORD[15:8]	25 Bit Frac1 Word.	0x0	R/W

REGISTER MAP

Address: 0x014, Reset: 0x00, Name: REG0014

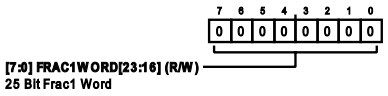

Table 41. Bit Descriptions for REG0014

Bits	Bit Name	Description	Reset	Access
[7:0]	FRAC1WORD[23:16]	25 Bit Frac1 Word.	0x0	R/W

Address: 0x015, Reset: 0x00, Name: REG0015

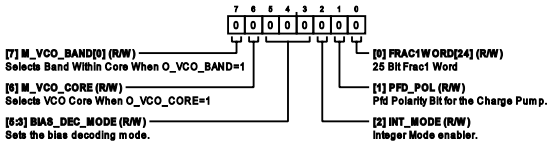

Table 42. Bit Descriptions for REG0015

Bits	Bit Name	Description	Reset	Access
7	M_VCO_BAND[0]	Selects Band Within Core When O_VCO_BAND = 1, 255 = lowest frequency. 0 = highest frequency.	0x0	R/W
6	M_VCO_CORE	Selects VCO Core When O_VCO_CORE=1. 0: VCO 0 highest frequency. 1: VCO 1 lowest frequency.	0x0	R/W
[5:3]	BIAS_DEC_MODE	Sets the bias decoding mode.	0x0	R/W
2	INT_MODE	Integer Mode Enabler. 0: fractional mode. 1: integer mode.	0x0	R/W
1	PFD_POL	PFD Polarity Bit for the Charge Pump.	0x0	R/W
0	FRAC1WORD[24]	25 Bit Frac1 Word.	0x0	R/W

Address: 0x016, Reset: 0x00, Name: REG0016

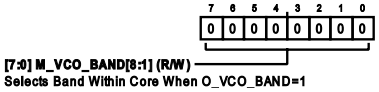

Table 43. Bit Descriptions for REG0016

Bits	Bit Name	Description	Reset	Access
[7:0]	M_VCO_BAND[8:1]	Selects Band Within Core When O_VCO_BAND = 1. 255 = lowest frequency. 0 = highest frequency.	0x0	R/W

REGISTER MAP

Address: 0x017, Reset: 0x00, Name: REG0017

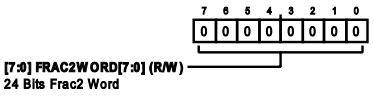

Table 44. Bit Descriptions for REG0017

Bits	Bit Name	Description	Reset	Access
[7:0]	FRAC2WORD[7:0]	24 Bits Frac2 Word.	0x0	R/W

Address: 0x018, Reset: 0x00, Name: REG0018

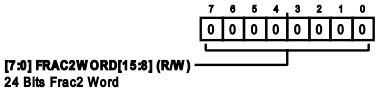

Table 45. Bit Descriptions for REG0018

Bits	Bit Name	Description	Reset	Access
[7:0]	FRAC2WORD[15:8]	24 Bits Frac2 Word.	0x0	R/W

Address: 0x019, Reset: 0x00, Name: REG0019

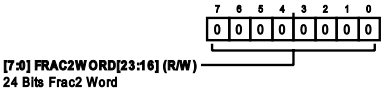

Table 46. Bit Descriptions for REG0019

Bits	Bit Name	Description	Reset	Access
[7:0]	FRAC2WORD[23:16]	24 Bits Frac2 Word.	0x0	R/W

Address: 0x01A, Reset: 0x00, Name: REG001A

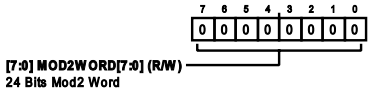

Table 47. Bit Descriptions for REG001A

Bits	Bit Name	Description	Reset	Access
[7:0]	MOD2WORD[7:0]	24 Bits Mod2 Word.	0x0	R/W

Address: 0x01B, Reset: 0x00, Name: REG001B

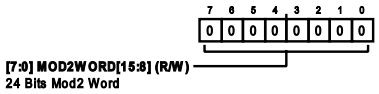

Table 48. Bit Descriptions for REG001B

Bits	Bit Name	Description	Reset	Access
[7:0]	MOD2WORD[15:8]	24 Bits Mod2 Word.	0x0	R/W

REGISTER MAP

Address: 0x01C, Reset: 0x00, Name: REG001C

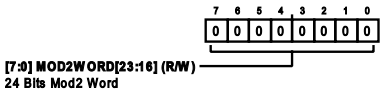

Table 49. Bit Descriptions for REG001C

Bits	Bit Name	Description	Reset	Access
[7:0]	MOD2WORD[23:16]	24 Bits Mod2 Word.	0x0	R/W

Address: 0x01D, Reset: 0x00, Name: REG001D

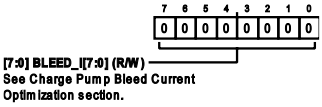

Table 50. Bit Descriptions for REG001D

Bits	Bit Name	Description	Reset	Access
[7:0]	BLEED_I[7:0]	See Charge Pump Bleed Current Optimization section.	0x0	R/W

Address: 0x01E, Reset: 0x00, Name: REG001E

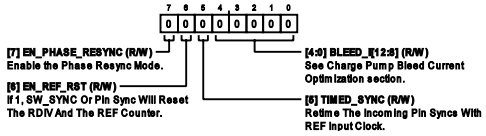

Table 51. Bit Descriptions for REG001E

Bits	Bit Name	Description	Reset	Access
7	EN_PHASE_RESYNC	Enable the Phase Resync Mode.	0x0	R/W
6	EN_REF_RST	If 1, SW_SYNC Or Pin Sync Will Reset The RDIV And The REF Counter.	0x0	R/W
5	TIMED_SYNC	Retime The Incoming Pin Syncs With REF Input Clock. 0: RDIV and REF counter are reset asynchronously. 1: incoming pin syncs are retimed to the REF input clock.	0x0	R/W
[4:0]	BLEED_I[12:8]	See Charge Pump Bleed Current Optimization section.	0x0	R/W

Address: 0x01F, Reset: 0x00, Name: REG001F

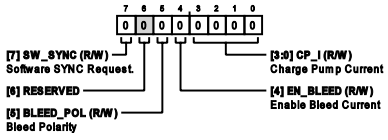

Table 52. Bit Descriptions for REG001F

Bits	Bit Name	Description	Reset	Access
7	SW_SYNC	Software SYNC Request.	0x0	R/W
6	RESERVED	Reserved.	0x0	R/W
5	BLEED_POL	Bleed Polarity.	0x0	R/W

REGISTER MAP

Table 52. Bit Descriptions for REG001F (Continued)

Bits	Bit Name	Description	Reset	Access
		0: current sink. 1: current source.		
4	EN_BLEED	Enable Bleed Current. 0: bleed current disabled. 1: bleed current enabled.	0x0	R/W
[3:0]	CP_I	Charge Pump Current. 0000: 0.79 mA. 0001: 0.99 mA. 0010: 1.19 mA. 0011: 1.38 mA. 0100: 1.59 mA. 0101: 1.98 mA. 0110: 2.39 mA. 0111: 2.79 mA. 1000: 3.18 mA. 1001: 3.97 mA. 1010: 4.77 mA. 1011: 5.57 mA. 1100: 6.33 mA. 1101: 7.91 mA. 1110: 9.51 mA. 1111: 11.1 mA.	0x0	R/W

Address: 0x020, Reset: 0x01, Name: REG0020

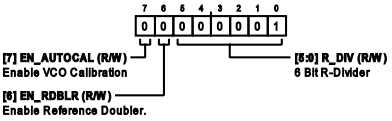

Table 53. Bit Descriptions for REG0020

Bits	Bit Name	Description	Reset	Access
7	EN_AUTOCAL	Enable VCO Calibration. 0: VCO Calibration Disabled. 1: VCO calibration enabled.	0x0	R/W
6	EN_RDBLR	Enable Reference Doubler. 0: doubler disabled. 1: doubler enabled.	0x0	R/W
[5:0]	R_DIV	6 Bit R-Divider.	0x1	R/W

Address: 0x021, Reset: 0x00, Name: REG0021

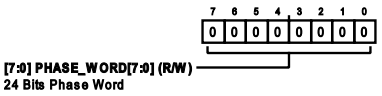

Table 54. Bit Descriptions for REG0021

Bits	Bit Name	Description	Reset	Access
[7:0]	PHASE_WORD[7:0]	24 Bits Phase Word.	0x0	R/W

REGISTER MAP

Address: 0x022, Reset: 0x00, Name: REG0022

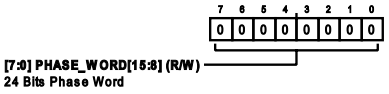

Table 55. Bit Descriptions for REG0022

Bits	Bit Name	Description	Reset	Access
[7:0]	PHASE_WORD[15:8]	24 Bits Phase Word.	0x0	R/W

Address: 0x023, Reset: 0x00, Name: REG0023

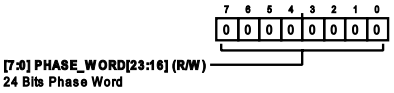

Table 56. Bit Descriptions for REG0023

Bits	Bit Name	Description	Reset	Access
[7:0]	PHASE_WORD[23:16]	24 Bits Phase Word.	0x0	R/W

Address: 0x024, Reset: 0x00, Name: REG0024

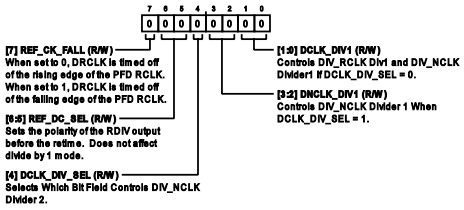

Table 57. Bit Descriptions for REG0024

Bits	Bit Name	Description	Reset	Access
7	REF_CK_FALL	When set to 0, DRCLK is timed off of the rising edge of the PFD RCLK. When set to 1, DRCLK is timed off of the falling edge of the PFD RCLK.	0x0	R/W
[6:5]	REF_DC_SEL	Sets the polarity of the RDIV output before the retime. Does not affect divide by 1 mode. 00: never invert (standard mode). 01: always invert. 10: automatically keep high duty cycle between 50% and 67%. 11: automatically keep high duty cycle between 33% and 50%.	0x0	R/W
4	DCLK_DIV_SEL	Selects Which Bit Field Controls DIV_NCLK Divider 2.	0x0	R/W
[3:2]	DNCLK_DIV1	Controls DIV_NCLK Divider 1 When DCLK_DIV_SEL = 1.	0x0	R/W
[1:0]	DCLK_DIV1	Controls DIV_RCLK Div1 and DIV_NCLK Divider1 If DCLK_DIV_SEL = 0. 00: divide by 1. 01: divide by 2. 10: divide by 4. 11: divide by 8.	0x0	R/W

REGISTER MAP

Address: 0x025, Reset: 0x00, Name: REG0025

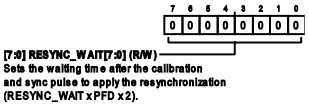

Table 58. Bit Descriptions for REG0025

Bits	Bit Name	Description	Reset	Access
[7:0]	RESYNC_WAIT[7:0]	Sets the waiting time after the calibration and sync pulse to apply the resynchronization (RESYNC_WAIT x PFD x 2).	0x0	R/W

Address: 0x026, Reset: 0x00, Name: REG0026

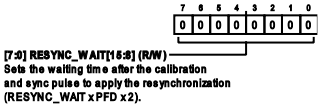

Table 59. Bit Descriptions for REG0026

Bits	Bit Name	Description	Reset	Access
[7:0]	RESYNC_WAIT[15:8]	Sets the waiting time after the calibration and sync pulse to apply the resynchronization (RESYNC_WAIT x PFD x 2).	0x0	R/W

Address: 0x027, Reset: 0x00, Name: REG0027

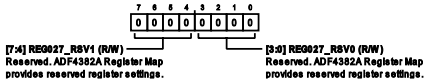

Table 60. Bit Descriptions for REG0027

Bits	Bit Name	Description	Reset	Access
[7:4]	REG027_RSV1	Reserved. Table 26 provides required reserved register settings.	0x0	R/W
[3:0]	REG027_RSV0	Reserved. Table 26 provides required reserved register settings.	0x0	R/W

Address: 0x028, Reset: 0x00, Name: REG0028

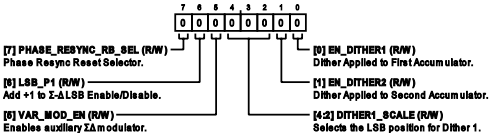

Table 61. Bit Descriptions for REG0028

Bits	Bit Name	Description	Reset	Access
7	PHASE_RESYNC_RB_SEL	Phase Resync Reset Selector.	0x0	R/W
6	LSB_P1	Add +1 to Σ-Δ LSB Enable/Disable.	0x0	R/W
5	VAR_MOD_EN	Enables Auxiliary Σ-Δ Modulator.	0x0	R/W
[4:2]	DITHER1_SCALE	Selects the LSB position for Dither 1.	0x0	R/W
1	EN_DITHER2	Dither Applied to Second Accumulator.	0x0	R/W
0	EN_DITHER1	Dither Applied to First Accumulator.	0x0	R/W

REGISTER MAP

Address: 0x029, Reset: 0x00, Name: REG0029

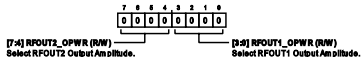

Table 62. Bit Descriptions for REG0029

Bits	Bit Name	Description	Reset	Access
[7:4]	RFOUT2_OPWR	Select RFOUT2 Output Amplitude.	0x0	R/W
[3:0]	RFOUT1_OPWR	Select RFOUT1 Output Amplitude.	0x0	R/W

Address: 0x02A, Reset: 0x04, Name: REG002A

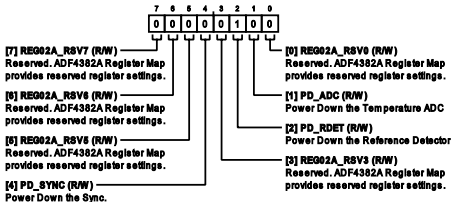

Table 63. Bit Descriptions for REG002A

Bits	Bit Name	Description	Reset	Access
7	REG02A_RSV7	Reserved. Table 26 provides required reserved register settings.	0x0	R/W
6	REG02A_RSV6	Reserved. Table 26 provides required reserved register settings.	0x0	R/W
5	REG02A_RSV5	Reserved. Table 26 provides required reserved register settings.	0x0	R/W
4	PD_SYNC	Power Down the Sync.	0x0	R/W
3	REG02A_RSV3	Reserved. Table 26 provides required reserved register settings.	0x0	R/W
2	PD_RDET	Power Down the Reference Detector. 0: normal operation. 1: power down the reference detector.	0x1	R/W
1	PD_ADC	Power Down the Temperature ADC.	0x0	R/W
0	REG02A_RSV0	Reserved. Table 26 provides required reserved register settings.	0x0	R/W

Address: 0x02B, Reset: 0x83, Name: REG002B

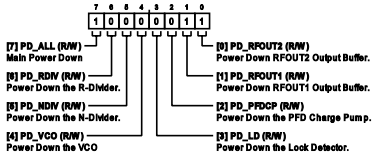

Table 64. Bit Descriptions for REG002B

Bits	Bit Name	Description	Reset	Access
7	PD_ALL	Main Power Down. 0: normal operation.	0x1	R/W

REGISTER MAP

Table 64. Bit Descriptions for REG002B (Continued)

Bits	Bit Name	Description	Reset	Access
		1: power down.		
6	PD_RDIV	Power Down the R-Divider.	0x0	R/W
5	PD_NDIV	Power Down the N-Divider.	0x0	R/W
4	PD_VCO	Power Down the VCO.	0x0	R/W
3	PD_LD	Power Down the Lock Detector. 0: normal operation. 1: power down the lock detector.	0x0	R/W
2	PD_PFDCP	Power Down the PFD Charge Pump.	0x0	R/W
1	PD_RFOUT1	Power Down RFOUT1 Output Buffer. 0: normal operation. 1: power down RFOUT1 Output.	0x1	R/W
0	PD_RFOUT2	Power Down RFOUT2 Output Buffer. 0: normal operation. 1: power down RFOUT2 Output.	0x1	R/W

Address: 0x02C, Reset: 0x00, Name: REG002C

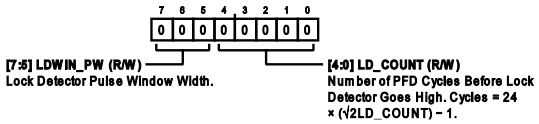

Table 65. Bit Descriptions for REG002C

Bits	Bit Name	Description	Reset	Access
[7:5]	LDWIN_PW	Lock Detector Pulse Window Width.	0x0	R/W
[4:0]	LD_COUNT	Number of PFD Cycles Before Lock Detector Goes High. Cycles = 24 × (√2LD_COUNT) − 1.	0x0	R/W

Address: 0x02D, Reset: 0x00, Name: REG002D

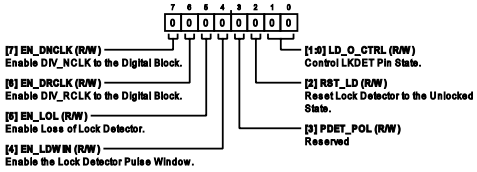

Table 66. Bit Descriptions for REG002D

Bits	Bit Name	Description	Reset	Access
7	EN_DNCLK	Enable DIV_NCLK to the Digital Block. 0: DIV_NCLK off. 1: DIV_NCLK on.	0x0	R/W
6	EN_DRCLK	Enable DIV_RCLK to the Digital Block. 0: DIG_RCLK Off. 1: DIG_RCLK On.	0x0	R/W
5	EN_LOL	Enable Loss of Lock Detector. 0: disable loss of lock detector.	0x0	R/W

REGISTER MAP

Table 66. Bit Descriptions for REG002D (Continued)

Bits	Bit Name	Description	Reset	Access
		1: enable loss of lock detector.		
4	EN_LDWIN	Enable the Lock Detector Pulse Window. 0: lock detector pulse window disabled. 1: lock detector pulse window enabled.	0x0	R/W
3	PDET_POL	Reserved.	0x0	R/W
2	RST_LD	Reset Lock Detector to the Unlocked State. 0: reset inactive. 1: reset active.	0x0	R/W
[1:0]	LD_O_CTRL	Control LKDET Pin State.	0x0	R/W

Address: 0x02E, Reset: 0x00, Name: REG002E

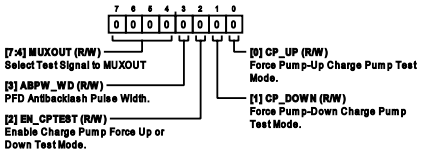

Table 67. Bit Descriptions for REG002E

Bits	Bit Name	Description	Reset	Access
[7:4]	MUXOUT	Select Test Signal to MUXOUT. 0000: High-Z. 0001: LKDET. 0010: DEL_STR. 0011: low. 0100: DIV_RCLK/2. 0101: DIV_NCLK/2. 0110: reserved. 0111: low. 1000: high. 1001: reserved. 1010: reserved. 1011: low. 1100: low. 1101: low. 1110: REF_OK. 1111: reserved.	0x0	R/W
3	ABPW_WD	PFD Antibacklash Pulse Width.	0x0	R/W
2	EN_CPTEST	Enable Charge Pump Force Up or Down Test Mode. 0: charge pump force up or down test mode off (normal operation). 1: charge pump force up or down test mode on.	0x0	R/W
1	CP_DOWN	Force Pump-Down Charge Pump Test Mode. 0: force pump down off. 1: force pump down on.	0x0	R/W
0	CP_UP	Force Pump-Up Charge Pump Test Mode. 0: force pump up off. 1: force pump up on.	0x0	R/W

REGISTER MAP

Address: 0x02F, Reset: 0x00, Name: REG002F

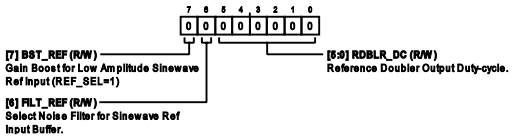

Table 68. Bit Descriptions for REG002F

Bits	Bit Name	Description	Reset	Access
7	BST_REF	Gain Boost for Low Amplitude Sinewave Ref Input (REF_SEL = 1). 0: use for large ref input signals > 8 dBm when REF_SEL = 1. 1: use for ref input signals < 8 dBm when REF_SEL = 1.	0x0	R/W
6	FILT_REF	Select Noise Filter for Sinewave Ref Input Buffer. 0: noise filter off. 1: noise filter on.	0x0	R/W
[5:0]	RDBLR_DC	Reference Doubler Output Duty-Cycle.	0x0	R/W

Address: 0x030, Reset: 0x00, Name: REG0030

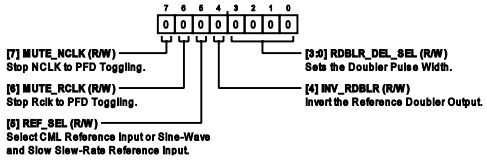

Table 69. Bit Descriptions for REG0030

Bits	Bit Name	Description	Reset	Access
7	MUTE_NCLK	Stop NCLK to PFD Toggling.	0x0	R/W
6	MUTE_RCLK	Stop RCLK to PFD Toggling.	0x0	R/W
5	REF_SEL	Select CML Reference Input or Sine-Wave and Slow Slew-Rate Reference Input. 0: CML reference input. 1: sine-wave or slow slew-rate reference input.	0x0	R/W
4	INV_RDBLR	Invert the Reference Doubler Output. 0: doubler output not inverted. 1: doubler output inverted.	0x0	R/W
[3:0]	RDBLR_DEL_SEL	Sets the Doubler Pulse Width.	0x0	R/W

REGISTER MAP

Address: 0x031, Reset: 0x00, Name: REG0031

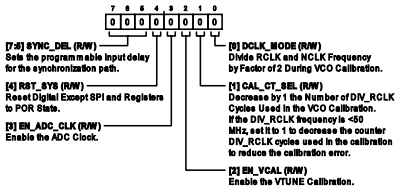

Table 70. Bit Descriptions for REG0031

Bits	Bit Name	Description	Reset	Access
[7:5]	SYNC_DEL	Sets the programmable input delay for the synchronization path.	0x0	R/W
4	RST_SYS	Reset Digital Except SPI and Registers to POR State. 0: reset inactive. 1: reset active.	0x0	R/W
3	EN_ADC_CLK	Enable the ADC Clock. 0: disable ADC clock. 1: enable ADC clock.	0x0	R/W
2	EN_VCAL	Enable the VTUNE Calibration.	0x0	R/W
1	CAL_CT_SEL	Decrease by 1 the Number of DIV_RCLK Cycles Used in the VCO Calibration. If the DIV_RCLK frequency is <50 MHz, set it to 1 to decrease the counter DIV_RCLK cycles used in the calibration to reduce the calibration error.	0x0	R/W
0	DCLK_MODE	Divide RCLK and NCLK Frequency by Factor of 2 During VCO Calibration. 0: disable frequency reduction. 1: enable frequency reduction.	0x0	R/W

Address: 0x032, Reset: 0x00, Name: REG0032

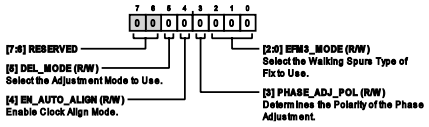

Table 71. Bit Descriptions for REG0032

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R/W
5	DEL_MODE	Select the Adjustment Mode to Use. 0: charge pump bleed mode. 1: Σ-Δ mode.	0x0	R/W
4	EN_AUTO_ALIGN	Enable Clock Align Mode. 0: autoalign disabled. 1: autoalign enabled.	0x0	R/W
3	PHASE_ADJ_POL	Determines the Polarity of the Phase Adjustment. 0: subtracts the selected phase value. 1: add the selected phase value.	0x0	R/W
[2:0]	EFM3_MODE	Select the Walking Spurs Type of Fix to Use.	0x0	R/W

REGISTER MAP

Address: 0x033, Reset: 0x00, Name: REG0033

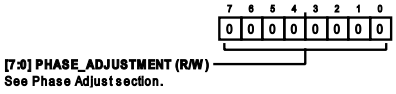

Table 72. Bit Descriptions for REG0033

Bits	Bit Name	Description	Reset	Access
[7:0]	PHASE_ADJUSTMENT	See Phase Adjust section.	0x0	R/W

Address: 0x034, Reset: 0x00, Name: REG0034

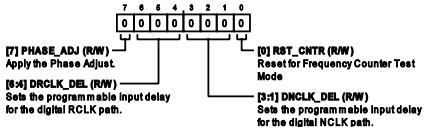

Table 73. Bit Descriptions for REG0034

Bits	Bit Name	Description	Reset	Access
7	PHASE_ADJ	Apply the Phase Adjust.	0x0	R/W
[6:4]	DRCLK_DEL	Sets the programmable input delay for the digital RCLK path.	0x0	R/W
[3:1]	DNCLK_DEL	Sets the programmable input delay for the digital NCLK path.	0x0	R/W
0	RST_CNTR	Reset for Frequency Counter Test Mode.	0x0	R/W

Address: 0x035, Reset: 0x00, Name: REG0035

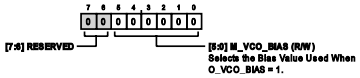

Table 74. Bit Descriptions for REG0035

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R/W
[5:0]	M_VCO_BIAS	Selects the Bias Value Used When O_VCO_BIAS = 1.	0x0	R/W

Address: 0x036, Reset: 0x00, Name: REG0036

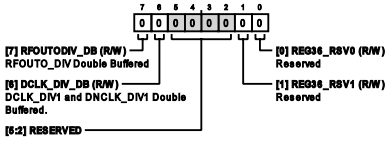

Table 75. Bit Descriptions for REG0036

Bits	Bit Name	Description	Reset	Access
7	RFOUTODIV_DB	RFOUTO_DIV Double Buffered. 0: CLKO_DIV not double buffered. 1: CLKO_DIV double buffered.	0x0	R/W

REGISTER MAP

Table 75. Bit Descriptions for REG0036 (Continued)

Bits	Bit Name	Description	Reset	Access
6	DCLK_DIV_DB	DCLK_DIV1 and DNCLK_DIV1 Double Buffered. 0: not double buffered. 1: double buffered.	0x0	R/W
[5:2]	RESERVED	Reserved.	0x0	R/W
1	REG36_RSV1	Reserved.	0x0	R/W
0	REG36_RSV0	Reserved. 0: Do not use the look-up table (LUT) for the calibration. 1: use the LUT for the calibration.	0x0	R/W

Address: 0x037, Reset: 0x00, Name: REG0037

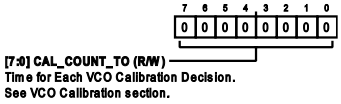

Table 76. Bit Descriptions for REG0037

Bits	Bit Name	Description	Reset	Access
[7:0]	CAL_COUNT_TO	Time for Each VCO Calibration Decision. See VCO Calibration section.	0x0	R/W

Address: 0x038, Reset: 0x00, Name: REG0038

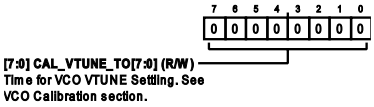

Table 77. Bit Descriptions for REG0038

Bits	Bit Name	Description	Reset	Access
[7:0]	CAL_VTUNE_TO[7:0]	Time for VCO VTUNE Settling. See VCO Calibration section.	0x0	R/W

Address: 0x039, Reset: 0x00, Name: REG0039

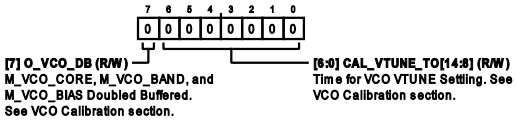

Table 78. Bit Descriptions for REG0039

Bits	Bit Name	Description	Reset	Access
7	O_VCO_DB	M_VCO_CORE, M_VCO_BAND, and M_VCO_BIAS Doubled Buffered. See VCO Calibration section. 0: core, bias and band not double buffered. 1: core, bias and band double buffered.	0x0	R/W
[6:0]	CAL_VTUNE_TO[14:8]	Time for VCO VTUNE Settling. See VCO Calibration section.	0x0	R/W

REGISTER MAP

Address: 0x03A, Reset: 0x00, Name: REG003A

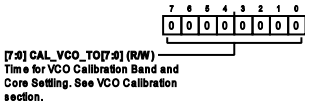

Table 79. Bit Descriptions for REG003A

Bits	Bit Name	Description	Reset	Access
[7:0]	CAL_VCO_TO[7:0]	Time for VCO Calibration Band and Core Settling. See VCO Calibration section.	0x0	R/W

Address: 0x03B, Reset: 0x00, Name: REG003B

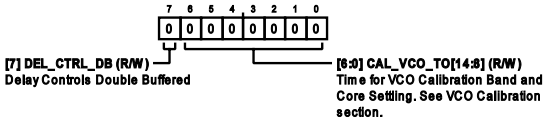

Table 80. Bit Descriptions for REG003B

Bits	Bit Name	Description	Reset	Access
7	DEL_CTRL_DB	Delay Controls Double Buffered. 0: not double buffered. 1: double buffered.	0x0	R/W
[6:0]	CAL_VCO_TO[14:8]	Time for VCO Calibration Band and Core Settling. See VCO Calibration section.	0x0	R/W

Address: 0x03C, Reset: 0x00, Name: REG003C

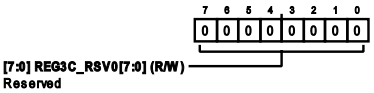

Table 81. Bit Descriptions for REG003C

Bits	Bit Name	Description	Reset	Access
[7:0]	REG3C_RSV0[7:0]	Reserved. Table 26 provides required reserved register settings.	0x0	R/W

Address: 0x03D, Reset: 0x00, Name: REG003D

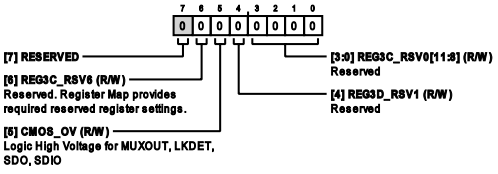

Table 82. Bit Descriptions for REG003D

Bits	Bit Name	Description	Reset	Access
7	RESERVED	Reserved.	0x0	R/W
6	REG3C_RSV6	Reserved. Table 26 provides required reserved register settings.	0x0	R/W
5	CMOS_OV	Logic High Voltage for MUXOUT, LKDET, SDO, SDIO. 0: 1.8 V logic. 1: 3.3 V logic.	0x0	R/W

REGISTER MAP

Table 82. Bit Descriptions for REG003D (Continued)

Bits	Bit Name	Description	Reset	Access
4	REG3D_RSV1	Reserved. Table 26 provides required reserved register settings.	0x0	R/W
[3:0]	REG3C_RSV0[11:8]	Reserved. Table 26 provides required reserved register settings.	0x0	R/W

Address: 0x03E, Reset: 0x00, Name: REG003E

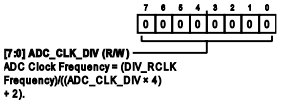

Table 83. Bit Descriptions for REG003E

Bits	Bit Name	Description	Reset	Access
[7:0]	ADC_CLK_DIV	ADC Clock Frequency = (DIV_RCLK Frequency)/((ADC_CLK_DIV × 4) + 2).	0x0	R/W

Address: 0x03F, Reset: 0x00, Name: REG003F

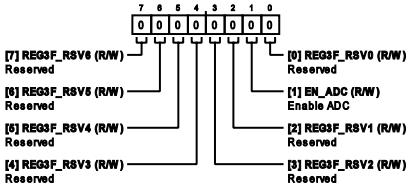

Table 84. Bit Descriptions for REG003F

Bits	Bit Name	Description	Reset	Access
7	REG3F_RSV6	Reserved. Table 26 provides required reserved register settings.	0x0	R/W
6	REG3F_RSV5	Reserved. Table 26 provides required reserved register settings.	0x0	R/W
5	REG3F_RSV4	Reserved. Table 26 provides required reserved register settings.	0x0	R/W
4	REG3F_RSV3	Reserved. Table 26 provides required reserved register settings.	0x0	R/W
3	REG3F_RSV2	Reserved. Table 26 provides required reserved register settings.	0x0	R/W
2	REG3F_RSV1	Reserved. Table 26 provides required reserved register settings.	0x0	R/W
1	EN_ADC	Enable ADC. 0: ADC disabled. 1: ADC enabled.	0x0	R/W
0	REG3F_RSV0	Reserved. Table 26 provides required reserved register settings.	0x0	R/W

Address: 0x040, Reset: 0x00, Name: REG0040

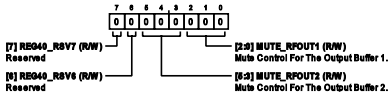

Table 85. Bit Descriptions for REG0040

Bits	Bit Name	Description	Reset	Access
7	REG40_RSV7	Reserved. Table 26 provides required reserved register settings.	0x0	R/W
6	REG40_RSV6	Reserved. Table 26 provides required reserved register settings.	0x0	R/W

REGISTER MAP

Table 85. Bit Descriptions for REG0040 (Continued)

Bits	Bit Name	Description	Reset	Access
[5:3]	MUTE_RFOUT2	Mute Control For The Output Buffer 2.	0x0	R/W
[2:0]	MUTE_RFOUT1	Mute Control For The Output Buffer 1.	0x0	R/W

Address: 0x041, Reset: 0x00, Name: REG0041

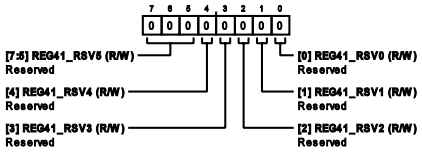

Table 86. Bit Descriptions for REG0041

Bits	Bit Name	Description	Reset	Access
[7:5]	REG41_RSV5	Reserved. Table 26 provides required reserved register settings.	0x0	R/W
4	REG41_RSV4	Reserved. Table 26 provides required reserved register settings.	0x0	R/W
3	REG41_RSV3	Reserved. Table 26 provides required reserved register settings.	0x0	R/W
2	REG41_RSV2	Reserved. Table 26 provides required reserved register settings.	0x0	R/W
1	REG41_RSV1	Reserved. Table 26 provides required reserved register settings.	0x0	R/W
0	REG41_RSV0	Reserved. Table 26 provides required reserved register settings.	0x0	R/W

Address: 0x042, Reset: 0x00, Name: REG0042

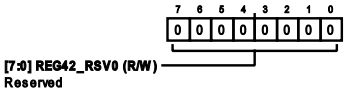

Table 87. Bit Descriptions for REG0042

Bits	Bit Name	Description	Reset	Access
[7:0]	REG42_RSV0	Reserved. Table 26 provides required reserved register settings.	0x0	R/W

Address: 0x044, Reset: 0x00, Name: REG0044

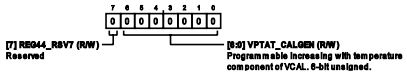

Table 88. Bit Descriptions for REG0044

Bits	Bit Name	Description	Reset	Access
7	REG44_RSV7	Reserved. Table 26 provides required reserved register settings.	0x0	R/W
[6:0]	VPTAT_CALGEN	Programmable increasing with temperature component of VCAL. 6-bit unsigned.	0x0	R/W

REGISTER MAP

Address: 0x045, Reset: 0x00, Name: REG0045

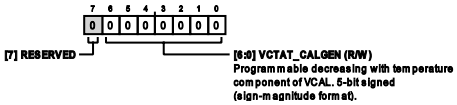

Table 89. Bit Descriptions for REG0045

Bits	Bit Name	Description	Reset	Access
7	RESERVED	Reserved.	0x0	R/W
[6:0]	VCTAT_CALGEN	Programmable decreasing with temperature component of VCAL. 5-bit signed (sign-magnitude format).	0x0	R/W

Address: 0x04B, Reset: 0x00, Name: REG004B

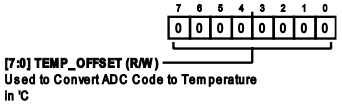

Table 90. Bit Descriptions for REG004B

Bits	Bit Name	Description	Reset	Access
[7:0]	TEMP_OFFSET	Used to Convert ADC Code to Temperature in °C.	0x0	R/W

Address: 0x04D, Reset: 0x00, Name: REG004D

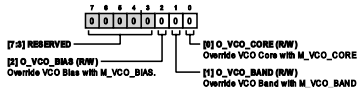

Table 91. Bit Descriptions for REG004D

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R/W
2	O_VCO_BIAS	Override VCO Bias with M_VCO_BIAS.	0x0	R/W
1	O_VCO_BAND	Override VCO Band with M_VCO_BAND. 0: VCO band code from VCO calibration state machine. 1: VCO band code from M_VCO_BAND.	0x0	R/W
0	O_VCO_CORE	Override VCO Core with M_VCO_CORE. 0: VCO core select from VCO calibration State machine. 1: VCO core select from M_VCO_CORE.	0x0	R/W

Address: 0x050, Reset: 0x00, Name: REG0050

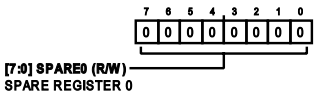

Table 92. Bit Descriptions for REG0050

Bits	Bit Name	Description	Reset	Access
[7:0]	SPARE0	SPARE REGISTER 0.	0x0	R/W

REGISTER MAP

Address: 0x053, Reset: 0x00, Name: REG0053

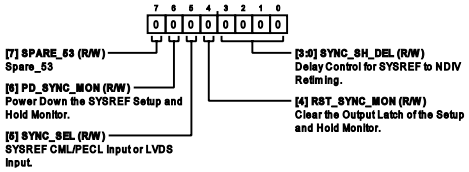

Table 93. Bit Descriptions for REG0053

Bits	Bit Name	Description	Reset	Access
7	SPARE_53	Spare_53.	0x0	R/W
6	PD_SYNC_MON	Power Down the SYSREF Setup and Hold Monitor. 0: normal operation. 1: power down the SYSREF setup and hold monitor.	0x0	R/W
5	SYNC_SEL	SYSREF CML/PECL Input or LVDS Input. 0: CML/PECL input. 1: LVDS input.	0x0	R/W
4	RST_SYNC_MON	Clear the Output Latch of the Setup and Hold Monitor. 0: reset inactive. 1: reset active.	0x0	R/W
[3:0]	SYNC_SH_DEL	Delay Control for SYSREF to NDIV Retiming.	0x0	R/W

Address: 0x054, Reset: 0x00, Name: REG0054

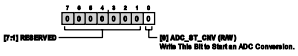

Table 94. Bit Descriptions for REG0054

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	ADC_ST_CNV	Write This Bit to Start an ADC Conversion.	0x0	R/W

Address: 0x055, Reset: 0x00, Name: REG0055

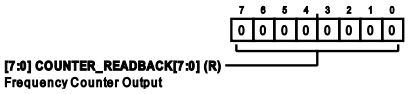

Table 95. Bit Descriptions for REG0055

Bits	Bit Name	Description	Reset	Access
[7:0]	COUNTER_READBACK[7:0]	Frequency Counter Output.	0x0	R

REGISTER MAP

Address: 0x056, Reset: 0x00, Name: REG0056

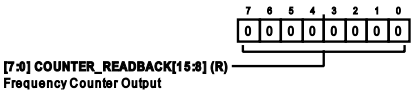

Table 96. Bit Descriptions for REG0056

Bits	Bit Name	Description	Reset	Access
[7:0]	COUNTER_READBACK[15:8]	Frequency Counter Output.	0x0	R

Address: 0x057, Reset: 0x00, Name: REG0057

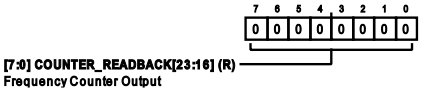

Table 97. Bit Descriptions for REG0057

Bits	Bit Name	Description	Reset	Access
[7:0]	COUNTER_READBACK[23:16]	Frequency Counter Output.	0x0	R

Address: 0x058, Reset: 0x00, Name: REG0058

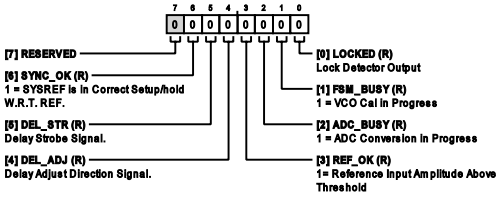

Table 98. Bit Descriptions for REG0058

Bits	Bit Name	Description	Reset	Access
7	RESERVED	Reserved.	0x0	R
6	SYNC_OK	1 = SYSREF is in Correct Setup and Hold with Respect to REF.	0x0	R
5	DEL_STR	Delay Strobe Signal.	0x0	R
4	DEL_ADJ	Delay Adjust Direction Signal. 0: negative adjustment. 1: positive adjustment.	0x0	R
3	REF_OK	1 = Reference Input Amplitude Above Threshold.	0x0	R
2	ADC_BUSY	1 = ADC Conversion in Progress.	0x0	R
1	FSM_BUSY	1 = VCO Calibration in Progress.	0x0	R
0	LOCKED	Lock Detector Output.	0x0	R

REGISTER MAP

Address: 0x059, Reset: 0x00, Name: REG0059

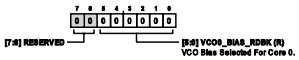

Table 99. Bit Descriptions for REG0059

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	VCO0_BIAS_RDBK	VCO Bias Selected for Core 0.	0x0	R

Address: 0x05A, Reset: 0x00, Name: REG005A

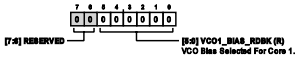

Table 100. Bit Descriptions for REG005A

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	VCO1_BIAS_RDBK	VCO Bias Selected for Core 1.	0x0	R

Address: 0x05B, Reset: 0x00, Name: REG005B

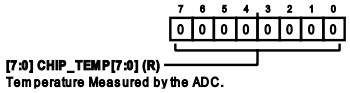

Table 101. Bit Descriptions for REG005B

Bits	Bit Name	Description	Reset	Access
[7:0]	CHIP_TEMP[7:0]	Temperature Measured by the ADC. Bit 8 = sign, and Bits[7:0] = magnitude.	0x0	R

Address: 0x05C, Reset: 0x00, Name: REG005C

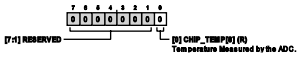

Table 102. Bit Descriptions for REG005C

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	CHIP_TEMP[8]	Temperature Measured by the ADC. Bit 8 = sign, and Bits[7:0] = magnitude.	0x0	R

Address: 0x05D, Reset: 0x00, Name: REG005D

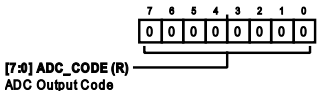

Table 103. Bit Descriptions for REG005D

Bits	Bit Name	Description	Reset	Access
[7:0]	ADC_CODE	ADC Output Code.	0x0	R

REGISTER MAP

Address: 0x05E, Reset: 0x00, Name: REG005E

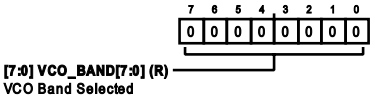

Table 104. Bit Descriptions for REG005E

Bits	Bit Name	Description	Reset	Access
[7:0]	VCO_BAND[7:0]	VCO Band Selected.	0x0	R

Address: 0x05F, Reset: 0x00, Name: REG005F

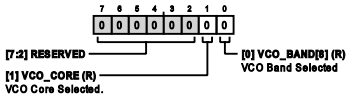

Table 105. Bit Descriptions for REG005F

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x0	R
1	VCO_CORE	VCO Core Selected.	0x0	R
0	VCO_BAND[8]	VCO Band Selected.	0x0	R

Address: 0x060, Reset: 0x00, Name: REG0060

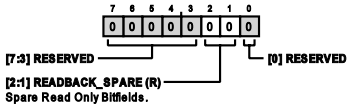

Table 106. Bit Descriptions for REG0060

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:1]	READBACK_SPARE	Spare Read Only Bit Fields.	0x0	R
0	RESERVED	Reserved.	0x0	R

Address: 0x061, Reset: 0x00, Name: REG0061

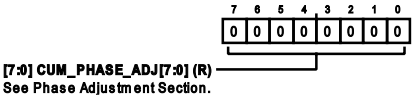

Table 107. Bit Descriptions for REG0061

Bits	Bit Name	Description	Reset	Access
[7:0]	CUM_PHASE_ADJ[7:0]	See Σ-Δ Modulator Phase Adjustment Section.	0x0	R

REGISTER MAP

Address: 0x062, Reset: 0x00, Name: REG0062

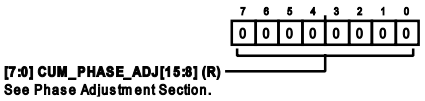

Table 108. Bit Descriptions for REG0062

Bits	Bit Name	Description	Reset	Access
[7:0]	CUM_PHASE_ADJ[15:8]	See Σ-Δ Modulator Phase Adjustment Section.	0x0	R

Address: 0x063, Reset: 0x00, Name: REG0063

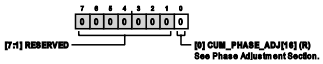

Table 109. Bit Descriptions for REG0063

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	CUM_PHASE_ADJ[16]	See Σ-Δ Modulator Phase Adjustment Section.	0x0	R

Address: 0x064, Reset: 0x00, Name: REG0064

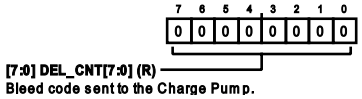

Table 110. Bit Descriptions for REG0064

Bits	Bit Name	Description	Reset	Access
[7:0]	DEL_CNT[7:0]	Bleed Code Sent to the Charge Pump.	0x0	R

Address: 0x065, Reset: 0x00, Name: REG0065

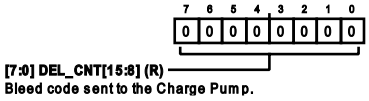

Table 111. Bit Descriptions for REG0065

Bits	Bit Name	Description	Reset	Access
[7:0]	DEL_CNT[15:8]	Bleed Code Sent to the Charge Pump.	0x0	R

Address: 0x066, Reset: 0x00, Name: REG0066

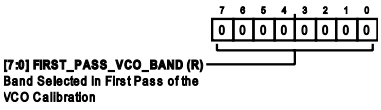

Table 112. Bit Descriptions for REG0066

Bits	Bit Name	Description	Reset	Access
[7:0]	FIRST_PASS_VCO_BAND	Band Selected in First Pass of the VCO Calibration.	0x0	R

REGISTER MAP

Address: 0x067, Reset: 0x00, Name: REG0067

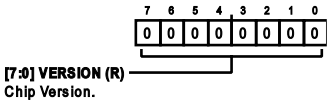

Table 113. Bit Descriptions for REG0067

Bits	Bit Name	Description	Reset	Access
[7:0]	VERSION	Chip Version.	0x0	R

Address: 0x100, Reset: 0x00, Name: REG0100

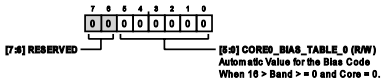

Table 114. Bit Descriptions for REG0100

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	CORE0_BIAS_TABLE_0	Automatic Value for the Bias Code When 16 > Band > = 0 and Core = 0.	0x0	R/W

Address: 0x101, Reset: 0x00, Name: REG0101

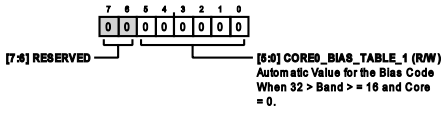

Table 115. Bit Descriptions for REG0101

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	CORE0_BIAS_TABLE_1	Automatic Value for the Bias Code When 32 > Band > = 16 and Core = 0.	0x0	R/W

Address: 0x102, Reset: 0x00, Name: REG0102

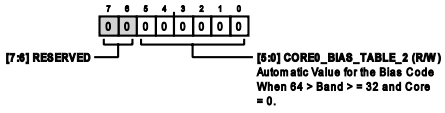

Table 116. Bit Descriptions for REG0102

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	CORE0_BIAS_TABLE_2	Automatic Value for the Bias Code When 64 > Band > = 32 and Core = 0.	0x0	R/W

REGISTER MAP

Address: 0x103, Reset: 0x00, Name: REG0103

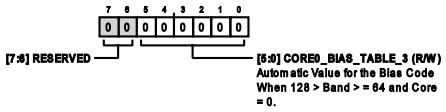

Table 117. Bit Descriptions for REG0103

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	CORE0_BIAS_TABLE_3	Automatic Value for the Bias Code When 128 > Band > = 64 and Core = 0.	0x0	R/W

Address: 0x104, Reset: 0x00, Name: REG0104

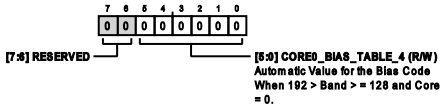

Table 118. Bit Descriptions for REG0104

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	CORE0_BIAS_TABLE_4	Automatic Value for the Bias Code When 192 > Band > = 128 and Core = 0.	0x0	R/W

Address: 0x105, Reset: 0x00, Name: REG0105

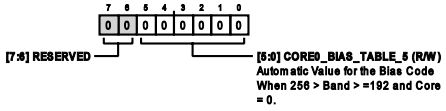

Table 119. Bit Descriptions for REG0105

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	CORE0_BIAS_TABLE_5	Automatic Value for the Bias Code When 256 > Band > =192 and Core = 0.	0x0	R/W

Address: 0x106, Reset: 0x00, Name: REG0106

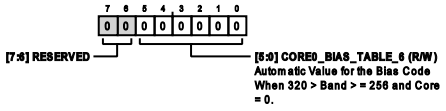

Table 120. Bit Descriptions for REG0106

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	CORE0_BIAS_TABLE_6	Automatic Value for the Bias Code When 320 > Band > = 256 and Core = 0.	0x0	R/W

REGISTER MAP

Address: 0x107, Reset: 0x00, Name: REG0107

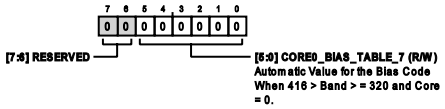

Table 121. Bit Descriptions for REG0107

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	CORE0_BIAS_TABLE_7	Automatic Value for the Bias Code When 416 > Band > = 320 and Core = 0.	0x0	R/W

Address: 0x108, Reset: 0x00, Name: REG0108

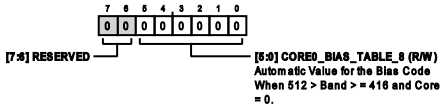

Table 122. Bit Descriptions for REG0108

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	CORE0_BIAS_TABLE_8	Automatic Value for the Bias Code When 512 > Band > = 416 and Core = 0.	0x0	R/W

Address: 0x109, Reset: 0x00, Name: REG0109

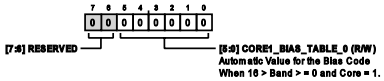

Table 123. Bit Descriptions for REG0109

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	CORE1_BIAS_TABLE_0	Automatic Value for the Bias Code When 16 > Band > = 0 and Core = 1.	0x0	R/W

Address: 0x10A, Reset: 0x00, Name: REG010A

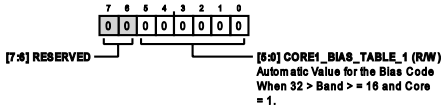

Table 124. Bit Descriptions for REG010A

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	CORE1_BIAS_TABLE_1	Automatic Value for the Bias Code When 32 > Band > = 16 and Core = 1.	0x0	R/W

REGISTER MAP

Address: 0x10B, Reset: 0x00, Name: REG010B

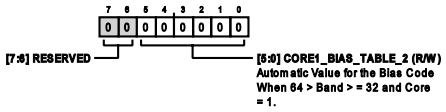

Table 125. Bit Descriptions for REG010B

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	CORE1_BIAS_TABLE_2	Automatic Value for the Bias Code When 64 > Band > = 32 and Core = 1.	0x0	R/W

Address: 0x10C, Reset: 0x00, Name: REG010C

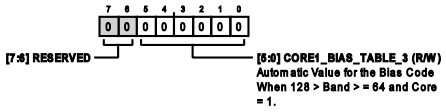

Table 126. Bit Descriptions for REG010C

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	CORE1_BIAS_TABLE_3	Automatic Value for the Bias Code When 128 > Band > = 64 and Core = 1.	0x0	R/W

Address: 0x10D, Reset: 0x00, Name: REG010D

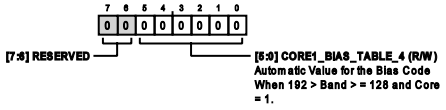

Table 127. Bit Descriptions for REG010D

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	CORE1_BIAS_TABLE_4	Automatic Value for the Bias Code When 192 > Band > = 128 and Core = 1.	0x0	R/W

Address: 0x10E, Reset: 0x00, Name: REG010E

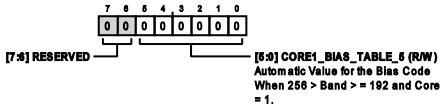

Table 128. Bit Descriptions for REG010E

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	CORE1_BIAS_TABLE_5	Automatic Value for the Bias Code When 256 > Band > = 192 and Core = 1.	0x0	R/W

REGISTER MAP

Address: 0x10F, Reset: 0x00, Name: REG010F

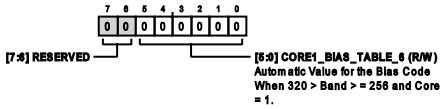

Table 129. Bit Descriptions for REG010F

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	CORE1_BIAS_TABLE_6	Automatic Value for the Bias Code When 320 > Band > = 256 and Core = 1.	0x0	R/W

Address: 0x110, Reset: 0x00, Name: REG0110

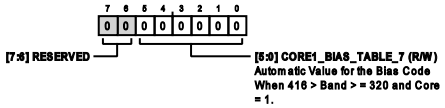

Table 130. Bit Descriptions for REG0110

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	CORE1_BIAS_TABLE_7	Automatic Value for the Bias Code When 416 > Band > = 320 and Core = 1.	0x0	R/W

Address: 0x111, Reset: 0x00, Name: REG0111

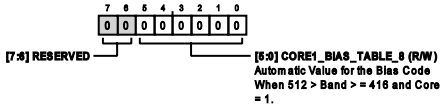

Table 131. Bit Descriptions for REG0111

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	CORE1_BIAS_TABLE_8	Automatic Value for the Bias Code When 512 > Band > = 416 and Core = 1.	0x0	R/W

OUTLINE DIMENSIONS

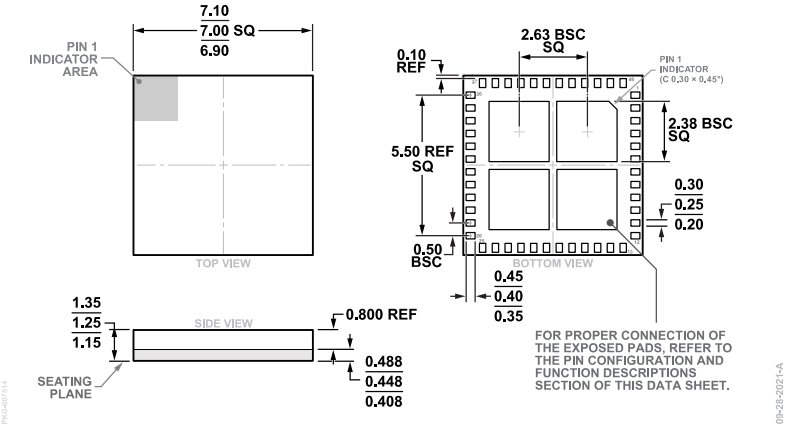

Figure 66. 48-Terminal Land Grid Array Package [LGA]
(CC-48-10)
Dimensions shown in millimeters

Updated: December 05, 2023

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADF4382ABCCZ	−40°C to +105°C	48-Terminal Land Grid Array [LGA]		CC-48-10
ADF4382ABCCZ-RL7	−40°C to +105°C	48-Terminal Land Grid Array [LGA]	Reel, 500	CC-48-10

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Table 132. Evaluation Boards

Model[1]	Description
EV-ADF4382ASD2Z	Evaluation Board

[1] Z = RoHS-Compliant Part.