

## CC2564C Dual-Mode *Bluetooth*<sup>®</sup> Controller

### 1 Device Overview

#### 1.1 Features

- TI's Single-Chip *Bluetooth*<sup>®</sup> Solution With Bluetooth Basic Rate (BR), Enhanced Data Rate (EDR), and Low Energy (LE) Support
- Bluetooth 4.2 Component Qualified (Declaration ID: D032801); Compliant up to the HCI Layer
- Highly Optimized for Size-Constrained and Low-Cost Designs:
  - Single-Ended 50-Ω RF Interface
  - Package Footprint: 76 Terminals, 0.6-mm Pitch, 8-mm × 8-mm (VQFN-MR)
- BR and EDR Features Include:
  - Up to Seven Active Devices
  - Scatternet: Up to Three Piconets Simultaneously, One as Master and Two as Slaves
  - Up to Two Synchronous Connection Oriented (SCO) Links on the Same Piconet
  - Support for All Voice Air-Coding—Continuously Variable Slope Delta (CVSD), A-Law,  $\mu$ -Law, Modified Subband Coding (mSBC), and Transparent (Uncoded)
  - Provide an Assisted Mode for HFP 1.6 Wideband Speech (WBS) Profile or A2DP Profile to Reduce Host Processing and Power
  - Support of Multiple Bluetooth Profiles With Enhanced QoS
- Low Energy Features Include:
  - Multiple Sniff Instances Tightly Coupled to Achieve Minimum Power Consumption
  - Independent Buffering for Low Energy Allows Large Numbers of Multiple Connections Without Affecting BR or EDR Performance
  - Built-In Coexistence and Prioritization Handling for BR, EDR, and Low Energy
  - Capabilities of Link Layer Topology Scatternet—Can Act Concurrently as Peripheral and Central
  - Network Support for up to 10 Devices
  - Time Line Optimization Algorithms to Achieve Maximum Channel Utilization
- Best-in-Class Bluetooth (RF) Performance (TX Power, RX Sensitivity, Blocking)
  - Class 1 TX Power up to +12 dBm
  - Internal Temperature Detection and Compensation to Ensure Minimal Variation in RF Performance Over Temperature, No External Calibration Required
  - Improved Adaptive Frequency Hopping (AFH) Algorithm With Minimum Adaptation Time
  - Longer Range, Including Twice the Range of Other Low-Energy-Only Solutions
- Advanced Power Management for Extended Battery Life and Ease of Design
  - On-Chip Power Management, Including Direct Connection to Battery
  - Low Power Consumption for Active, Standby, and Scan Bluetooth Modes
  - Shutdown and Sleep Modes to Minimize Power Consumption
- Physical Interfaces:
  - UART Interface With Support for Maximum Bluetooth Data Rates
    - UART Transport Layer (H4) With Maximum Rate of 4 Mbps
    - Three-Wire UART Transport Layer (H5) With Maximum Rate of 4 Mbps
  - Fully Programmable Digital Pulse-Code Modulation (PCM)–Inter-IC Sound (I2S) Codec Interface
- Flexibility for Easy Stack Integration and Validation Into MCUs and MPUs
- CC256x Bluetooth Hardware Evaluation Tool: PC-Based Application to Evaluate RF Performance of the Device and Configure Service Pack

#### 1.2 Applications

- Wireless Audio Solutions
- mPOS
- Medical Devices
- Set-Top Boxes (STBs)
- Wearable Devices
- Sensor Hub, Sensor Gateway
  - Home and Factory Automation



### 1.3 Description

The TI CC2564C device is a complete *Bluetooth*® BR, EDR, and low energy HCI solution that reduces design effort and enables fast time to market. Based on TI's seventh-generation Bluetooth core, the CC2564C device provides a product-proven solution that is Bluetooth 4.2 compliant. When coupled with a [microcontroller unit \(MCU\)](#), this HCI device offers best-in-class RF performance with about twice the range of other Bluetooth low-energy solutions. Furthermore, TI's power-management hardware and software algorithms provide significant power savings in all commonly used Bluetooth BR, EDR, and low energy modes of operation.

The TI dual-mode Bluetooth stack software is certified and provided royalty free for MCUs and MPUs. The iPod® (MFi) protocol is supported by add-on software packages. For more information, see [TI Dual-Mode Bluetooth Stack](#). Multiple profiles and sample applications are supported including the following:

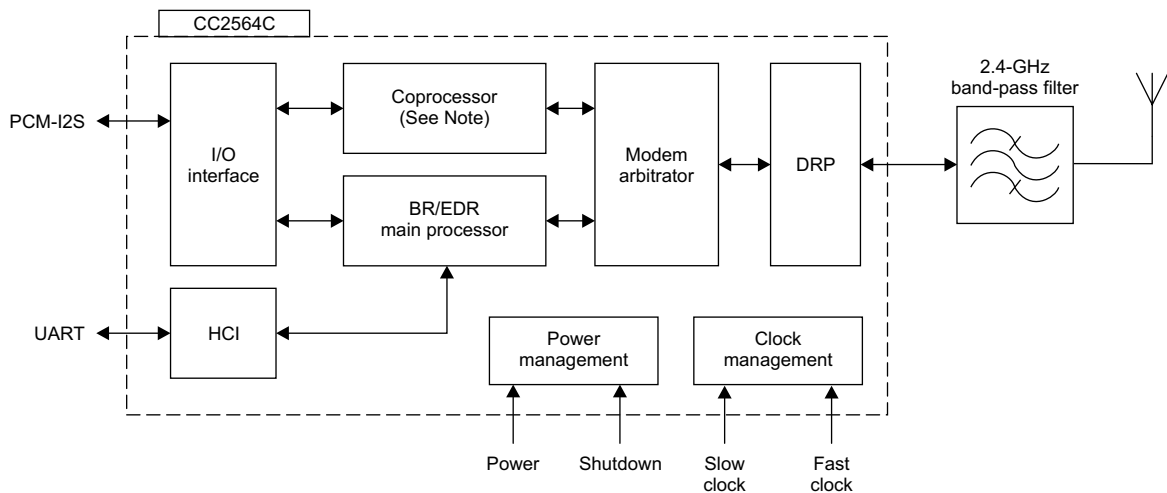
- Serial port profile (SPP)
- Advanced audio distribution profile (A2DP)
- Audio/video remote control profile (AVRCP)
- Hands-free profile (HFP)
- Human interface device (HID)
- Generic attribute profile (GATT)
- Several Bluetooth low energy profiles and services

Device Information<sup>(1)</sup>

| PART NUMBER | PACKAGE  | BODY SIZE                   |
|-------------|----------|-----------------------------|
| CC2564CRVM  | RVM (76) | 8.00 mm × 8.00 mm × 0.60 mm |

(1) For more information on these devices, see [Section 9](#).

### 1.4 Functional Block Diagram



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Note: The following technologies and assisted modes cannot be used simultaneously with the coprocessor: Bluetooth low energy, assisted HFP 1.6 (WBS), and assisted A2DP. Only one technology or assisted mode can be used at a time.

Figure 1-1. Functional Block Diagram

## Table of Contents

|   |                           |  |                           |
|---|---------------------------|--|---------------------------|
| <b>1 Device Overview</b> .....  | <b><a href="#">1</a></b>  | 6.2 Functional Block Diagram .....   | <a href="#">23</a>        |
| 1.1 Features .....  | <a href="#">1</a>         | 6.3 Clock Inputs .....   | <a href="#">23</a>        |
| 1.2 Applications .....  | <a href="#">1</a>         | 6.4 Functional Blocks .....  | <a href="#">27</a>        |
| 1.3 Description .....   | <a href="#">2</a>         | 6.5 Bluetooth BR and EDR Features .....  | <a href="#">38</a>        |
| 1.4 Functional Block Diagram .....  | <a href="#">2</a>         | 6.6 Bluetooth low energy Description .....                                       | <a href="#">39</a>        |
| <b>2 Revision History</b> .....   | <b><a href="#">3</a></b>  | 6.7 Bluetooth Transport Layers .....   | <a href="#">40</a>        |
| <b>3 Device Comparison</b> .....  | <b><a href="#">4</a></b>  | 6.8 Changes from the CC2564B Device to the<br>CC2564C Device .....               | <a href="#">40</a>        |
| 3.1 Related Products .....  | <a href="#">4</a>         | <b>7 Applications, Implementation, and Layout</b> .....                          | <b><a href="#">41</a></b> |
| <b>4 Terminal Configuration and Functions</b> .....                       | <b><a href="#">5</a></b>  | 7.1 Reference Design Schematics and BOM for Power<br>and Radio Connections ..... | <a href="#">41</a>        |
| 4.1 VQFN-MR Pin Diagram .....   | <a href="#">5</a>         | 7.2 PCB Layout Guidelines .....  | <a href="#">43</a>        |
| <b>5 Specifications</b> .....   | <b><a href="#">8</a></b>  | <b>8 Device and Documentation Support</b> .....                                  | <b><a href="#">47</a></b> |
| 5.1 Absolute Maximum Ratings .....  | <a href="#">8</a>         | 8.1 Third-Party Products Disclaimer .....  | <a href="#">47</a>        |
| 5.2 ESD Ratings .....   | <a href="#">8</a>         | 8.2 Tools and Software .....   | <a href="#">47</a>        |
| 5.3 Power-On Hours .....  | <a href="#">8</a>         | 8.3 Device Nomenclature .....  | <a href="#">47</a>        |
| 5.4 Recommended Operating Conditions .....                                | <a href="#">9</a>         | 8.4 Community Resources .....  | <a href="#">47</a>        |
| 5.5 Power Consumption Summary .....                                       | <a href="#">9</a>         | 8.5 Trademarks .....   | <a href="#">48</a>        |
| 5.6 Electrical Characteristics .....                                      | <a href="#">11</a>        | 8.6 Electrostatic Discharge Caution .....  | <a href="#">48</a>        |
| 5.7 Thermal Resistance Characteristics for VQFN-MR<br>(RVM) Package ..... | <a href="#">11</a>        | 8.7 Glossary .....   | <a href="#">48</a>        |
| 5.8 Timing and Switching Characteristics .....                            | <a href="#">12</a>        | <b>9 Mechanical, Packaging, and Orderable<br/>    Information</b> .....          | <b><a href="#">49</a></b> |
| <b>6 Detailed Description</b> .....                                       | <b><a href="#">23</a></b> |  |                           |
| 6.1 Overview .....  | <a href="#">23</a>        |  |                           |

## 2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from April 8, 2016 to October 27, 2016 | Page              |
|--|-------------------|
| • Updated document to PRODUCTION DATA .....    | <a href="#">1</a> |

### 3 Device Comparison

Table 3-1 lists the features of the CC2564C device.

**Table 3-1. CC2564C Device Features**

| DEVICE  | DESCRIPTION                          | TECHNOLOGY SUPPORTED |            | ASSISTED MODES SUPPORTED <sup>(1)</sup> |      |
|---------|--------------------------------------|----------------------|------------|---|------|
|         |                                      | BR, EDR              | LOW ENERGY | HFP 1.6 (WBS)                           | A2DP |
| CC2564C | Bluetooth 4.2 + Bluetooth low energy | √                    | √          | √                                       | √    |

(1) The assisted modes (HFP 1.6 and A2DP) are not supported simultaneously. Furthermore, the assisted modes are not supported simultaneously with Bluetooth low energy.

#### 3.1 Related Products

**Wireless Connectivity** The wireless connectivity portfolio offers a wide selection of low-power RF solutions suitable for a broad range of application. The offerings range from fully customized solutions to turnkey offerings with precertified hardware and software (protocol).

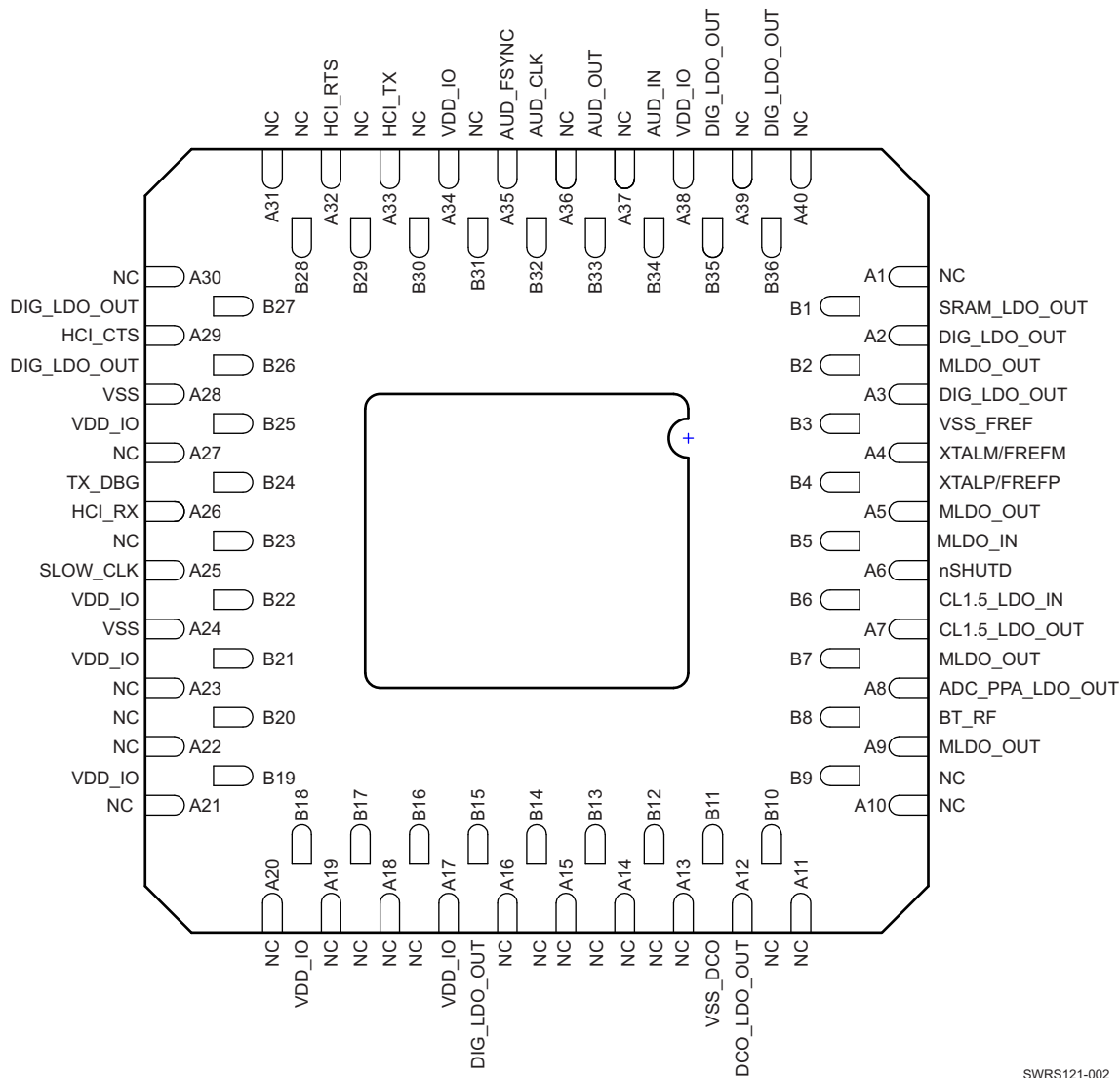
**Companion Products** Review products that are frequently purchased or used with the CC2564C product.

**Reference Designs for CC2564** The TI Designs Reference Design Library is a robust reference design library spanning analog, embedded processor, and connectivity. Created by TI experts to help you jump-start your system design, all TI Designs include schematic or block diagrams, BOMs and design files to speed your time to market. Search and download designs at [ti.com/tidesigns](http://ti.com/tidesigns).

## 4 Terminal Configuration and Functions

### 4.1 VQFN-MR Pin Diagram

Figure 4-1 shows the bottom view of the pin diagram (VQFN-MR package).



SWRS121-002

Figure 4-1. VQFN-MR Package Pin Diagram Bottom View

### 4.1.1 Pin Attributes (VQFN-MR Package)

Table 4-1 describes the pin attributes for the VQFN-MR package.

**Table 4-1. Pin Attributes (VQFN-MR Package)**

| NAME                            | NO.                             | PULL AT RESET | DEF. DIR. <sup>(1)</sup> | I/O Type <sup>(2)</sup> | DESCRIPTION  |
|---------------------------------|---------------------------------|---------------|--------------------------|-------------------------|--|
| <b>I/O Signals</b>              |                                 |               |                          |                         |  |
| AUD_CLK                         | B32                             | PD            | I/O                      | HY, 4 mA                | PCM clock<br>Fail-safe   |
| AUD_FSYNC                       | A35                             | PD            | I/O                      | 4 mA                    | PCM frame-sync signal<br>Fail-safe   |
| AUD_IN                          | B34                             | PD            | I                        | 4 mA                    | PCM data input<br>Fail-safe  |
| AUD_OUT                         | B33                             | PD            | O                        | 4 mA                    | PCM data output<br>Fail-safe   |
| HCI_CTS                         | A29                             | PU            | I                        | 8 mA                    | HCI UART clear-to-send<br>The device is allowed to send data when HCI_CTS is low.              |
| HCI_RX                          | A26                             | PU            | I                        | 8 mA                    | HCI universal asynchronous receiver/transmitter (UART) data receive                            |
| HCI_RTS                         | A32                             | PU            | O                        | 8 mA                    | HCI UART request-to-send<br>The host is allowed to send data when HCI_RTS is low.              |
| HCI_TX                          | A33                             | PU            | O                        | 8 mA                    | HCI UART data transmit   |
| TX_DBG                          | B24                             | PU            | O                        | 2 mA                    | TI internal debug messages. TI recommends leaving an internal test point.                      |
| <b>Clock Signals</b>            |                                 |               |                          |                         |  |
| SLOW_CLK                        | A25                             |               | I                        |                         | 32.768-kHz clock in<br>Fail-safe   |
| XTALP/FREFP                     | B4                              |               | I                        |                         | Fast clock in analog (sine wave)<br>Output terminal of fast-clock crystal<br>Fail-safe         |
| XTALM/FREFM                     | A4                              |               | I                        |                         | Fast clock in digital (square wave)<br>Input terminal of fast-clock crystal<br>Fail-safe       |
| <b>Analog Signals</b>           |                                 |               |                          |                         |  |
| BT_RF                           | B8                              |               | I/O                      |                         | Bluetooth RF I/O   |
| nSHUTD                          | A6                              | PD            | I                        |                         | Shutdown input (active low)  |
| <b>Power and Ground Signals</b> |                                 |               |                          |                         |  |
| ADC_PPA_LDO_OUT                 | A8                              |               | O                        |                         | ADC/PPA LDO output   |
| CL1.5_LDO_IN                    | B6                              |               | I                        |                         | Power amplifier (PA) LDO input<br>Connect directly to battery                                  |
| CL1.5_LDO_OUT                   | A7                              |               | O                        |                         | PA LDO output  |
| DCO_LDO_OUT                     | A12                             |               | O                        |                         | DCO LDO output   |
| DIG_LDO_OUT                     | A2, A3, B15, B26, B27, B35, B36 |               | O                        |                         | Digital LDO output<br>QFN pin B26 or B27 must be shorted to other DIG_LDO_OUT pins on the PCB. |
| MLDO_IN                         | B5                              |               | I                        |                         | Main LDO input<br>Connect directly to battery  |
| MLDO_OUT                        | A5, A9, B2, B7                  |               | I/O                      |                         | Main LDO output (1.8-V nominal)  |
| SRAM_LDO_OUT                    | B1                              |               | O                        |                         | SRAM LDO output  |

(1) I = input; O = output; I/O = bidirectional

(2) I/O Type: Digital I/O cells. HY = input hysteresis, current = typical output current

**Table 4-1. Pin Attributes (VQFN-MR Package) (continued)**

| NAME     | NO.                                    | PULL AT RESET | DEF. DIR. <sup>(1)</sup> | I/O Type <sup>(2)</sup> | DESCRIPTION                      |
|----------|--|---------------|--------------------------|-------------------------|----------------------------------|
| VDD_IO   | A17, A34, A38, B18, B19, B21, B22, B25 |               | I                        |                         | I/O power supply (1.8-V nominal) |
| VSS      | A24, A28                               |               | I                        |                         | Ground                           |
| VSS_DCO  | B11                                    |               | I                        |                         | DCO ground                       |
| VSS_FREF | B3                                     |               | I                        |                         | Fast clock ground                |

#### 4.1.2 Connections for Unused Signals (VQFN-MR Package)

Section 4.1.2 lists the connections for unused signals for the VQFN-MR package.

| FUNCTION | PIN NUMBER | DESCRIPTION     |
|----------|------------|-----------------|
| NC       | A1         | Not connected   |
| NC       | A10        | Not connected   |
| NC       | A11        | Not connected   |
| NC       | A14        | Not connected   |
| NC       | A18        | Not connected   |
| NC       | A19        | Not connected   |
| NC       | A20        | Not connected   |
| NC       | A21        | Not connected   |
| NC       | A22        | Not connected   |
| NC       | A23        | Not connected   |
| NC       | A27        | Not connected   |
| NC       | A30        | Not connected   |
| NC       | A31        | Not connected   |
| NC       | A40        | Not connected   |
| NC       | B9         | Not connected   |
| NC       | B10        | Not connected   |
| NC       | B16        | Not connected   |
| NC       | B17        | Not connected   |
| NC       | B20        | Not connected   |
| NC       | B23        | Not connected   |
| NC       | A13        | TI internal use |
| NC       | A15        | TI internal use |
| NC       | A16        | TI internal use |
| NC       | A36        | TI internal use |
| NC       | A37        | TI internal use |
| NC       | A39        | TI internal use |
| NC       | B12        | TI internal use |
| NC       | B13        | TI internal use |
| NC       | B14        | TI internal use |
| NC       | B29        | TI internal use |
| NC       | B30        | TI internal use |
| NC       | B31        | TI internal use |
| NC       | B28        | TI internal use |

## 5 Specifications

Unless otherwise indicated, all measurements are taken at the device pins of the TI test evaluation board (EVB). All specifications are over process, voltage, and temperature, unless otherwise indicated.

### 5.1 Absolute Maximum Ratings<sup>(1)</sup>

Over operating free-air temperature range (unless otherwise indicated). All parameters are measured as follows: VDD\_IN = 3.6 V and VDD\_IO = 1.8 V (unless otherwise indicated).

|  |             | MIN  | MAX          | UNIT             |
|--|-------------|------|--------------|------------------|
| Supply voltage   | VDD_IN      | -0.5 | 4.8          | V <sup>(2)</sup> |
|  | VDDIO_1.8 V | -0.5 | 2.145        | V                |
| Input voltage to analog pins <sup>(3)</sup>                  |             | -0.5 | 2.1          | V                |
| Input voltage to all other pins                              |             | -0.5 | VDD_IO + 0.5 | V                |
| Bluetooth RF inputs  |             |      | 10           | dBm              |
| Operating ambient temperature, T <sub>A</sub> <sup>(4)</sup> |             | -40  | 85           | °C               |
| Storage temperature, T <sub>stg</sub>                        |             | -55  | 125          | °C               |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Maximum allowed depends on accumulated time at that voltage: VDD\_IN is defined in [Section 7.1](#).
- (3) Analog pins: BT\_RF, XTALP, and XTALM
- (4) The reference design supports a temperature range of -20°C to +70°C because of the operating conditions of the crystal.

### 5.2 ESD Ratings

|  |   | VALUE | UNIT |
|--|---|-------|------|
| V <sub>(ESD)</sub>   | Electrostatic discharge   |       |      |
|  | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup> | ±500  | V    |
| Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±250  |       |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Power-On Hours

| DEVICE  | CONDITIONS   | POWER-ON HOURS   |
|---------|--|------------------|
| CC2564C | Duty cycle = 25% active and 75% sleep<br>T <sub>ambient</sub> = 85°C | 15,400 (7 years) |



## 5.4 Recommended Operating Conditions

|  |   |                   | MIN           | MAX           | UNIT              |
|--|---|-------------------|---------------|---------------|-------------------|
| VDD_IN   | Power supply voltage  |                   | 1.7           | 4.8           | V                 |
| VDD_IO   | I/O power supply voltage  |                   | 1.62          | 1.92          | V                 |
| V <sub>IH</sub>  | High-level input voltage  | Default condition | 0.65 × VDD_IO | VDD_IO        | V                 |
| V <sub>IL</sub>  | Low-level input voltage   | Default condition | 0             | 0.35 × VDD_IO | V                 |
| t <sub>r</sub> and t <sub>f</sub>  | I/O input rise and all times,<br>10% to 90%—asynchronous mode       |                   | 1             | 10            | ns                |
|  | I/O input rise and fall times,<br>10% to 90%—synchronous mode (PCM) |                   | 1             | 2.5           | ns                |
| Maximum ripple on VDD_IN (sine wave) for<br>1.8 V (DC-DC) mode                 | Condition: 0 to 0.1 MHz   |                   |               | 60            | mV <sub>p-p</sub> |
|  | Condition: 0.1 to 0.5 MHz   |                   |               | 50            |                   |
|  | Condition: 0.5 to 2.5 MHz   |                   |               | 30            |                   |
|  | Condition: 2.5 to 3.0 MHz   |                   |               | 15            |                   |
|  | Condition: > 3.0 MHz  |                   |               | 5             |                   |
| Voltage dips on VDD_IN (VBAT)<br>Duration = 577 μs to 2.31 ms, period = 4.6 ms |   |                   |               | 400           | mV                |
| Maximum ambient operating temperature <sup>(1) (2)</sup>                       |   |                   | –40           | 85            | °C                |

(1) The device can be reliably operated for 7 years at T<sub>ambient</sub> of 85°C, assuming 25% active mode and 75% sleep mode (15,400 cumulative active power-on hours).

(2) A crystal-based solution is limited by the temperature range required for the crystal to meet 20 ppm.

## 5.5 Power Consumption Summary

### 5.5.1 Static Current Consumption

| OPERATIONAL MODE                              | MIN | TYP | MAX   | UNIT |
|---|-----|-----|-------|------|
| Shutdown mode <sup>(1)</sup>                  |     | 1   | 7     | μA   |
| Deep sleep mode <sup>(2)</sup>                |     | 40  | 105   | μA   |
| Total I/O current consumption in active mode  |     |     | 1     | mA   |
| Continuous transmission—GFSK <sup>(3)</sup>   |     |     | 107   | mA   |
| Continuous transmission—EDR <sup>(4)(5)</sup> |     |     | 112.5 | mA   |

(1) VBAT + VIO + V<sub>SHUTDOWN</sub>

(2) VBAT + VIO

(3) At maximum output power dBm

(4) At maximum output power dBm

(5) Both π/4 DQPSK and 8DPSK

## 5.5.2 Dynamic Current Consumption

### 5.5.2.1 Current Consumption for Different Bluetooth BR and EDR Scenarios

Conditions: VDD\_IN = 3.6 V, 25°C, 26-MHz XTAL, nominal unit, 10-dBm output power

| OPERATIONAL MODE  | MASTER AND SLAVE | AVERAGE CURRENT | UNIT |
|---|------------------|-----------------|------|
| SCO link HV3  | Master and slave | 13.7            | mA   |
| Extended SCO (eSCO) link EV3 64 kbps, no retransmission           | Master and slave | 13.2            | mA   |
| eSCO link 2-EV3 64 kbps, no retransmission                        | Master and slave | 10              | mA   |
| GFSK full throughput: TX = DH1, RX = DH5                          | Master and slave | 40.5            | mA   |
| EDR full throughput: TX = 2-DH1, RX = 2-DH5                       | Master and slave | 41.2            | mA   |
| EDR full throughput: TX = 3-DH1, RX = 3-DH5                       | Master and slave | 41.2            | mA   |
| Sniff, four attempts, 1.28 seconds                                | Master and slave | 145             | μA   |
| Page or inquiry scan 1.28 seconds, 11.25 ms                       | Master and slave | 320             | μA   |
| Page (1.28 seconds) and inquiry (2.56 seconds) scans, 11.25 ms    | Master and slave | 445             | μA   |
| A2DP source   | Master           | 13.9            | mA   |
| A2DP sink   | Master           | 15.2            | mA   |
| Assisted A2DP source  | Master           | 16.9            | mA   |
| Assisted A2DP sink  | Master           | 18.1            | mA   |
| Assisted WBS EV3; retransmit effort = 2; maximum latency = 8 ms   | Master and slave | 17.5 and 18.5   | mA   |
| Assisted WBS 2EV3; retransmit effort = 2; maximum latency = 12 ms | Master and slave | 11.9 and 13     | mA   |

### 5.5.2.2 Current Consumption for Different Low-Energy Scenarios

Conditions: VDD\_IN = 3.6 V, 25°C, nominal unit, 10-dBm output power

| MODE                        | DESCRIPTION   | AVERAGE CURRENT | UNIT |
|-----------------------------|---|-----------------|------|
| Advertising, nonconnectable | Advertising in all three channels<br>1.28-seconds advertising interval<br>15 bytes advertise data | 114             | μA   |
| Advertising, discoverable   | Advertising in all three channels<br>1.28-seconds advertising interval<br>15 bytes advertise data | 138             | μA   |
| Scanning                    | Listening to a single frequency per window<br>1.28-seconds scan interval<br>11.25-ms scan window  | 324             | μA   |
| Connected                   | Master role   | 169             | μA   |
|                             | Slave role  | 199             |      |

## 5.6 Electrical Characteristics

| RATING  |                     | CONDITION     | MIN                  | MAX                  | UNIT      |         |
|---|---------------------|---------------|----------------------|----------------------|-----------|---------|
| High-level output voltage, $V_{OH}$                   |                     | At 2, 4, 8 mA | $0.8 \times VDD\_IO$ | $VDD\_IO$            | V         |         |
|   |                     | At 0.1 mA     | $VDD\_IO - 0.2$      | $VDD\_IO$            |           |         |
| Low-level output voltage, $V_{OL}$                    |                     | At 2, 4, 8 mA | 0                    | $0.2 \times VDD\_IO$ | V         |         |
|   |                     | At 0.1 mA     | 0                    | 0.2                  |           |         |
| I/O input impedance                                   |                     | Resistance    | 1                    |                      | $M\Omega$ |         |
|   |                     | Capacitance   |                      | 5                    | pF        |         |
| Output rise and fall times, 10% to 90% (digital pins) |                     | $C_L = 20$ pF |                      | 10                   | ns        |         |
| I/O pull currents                                     | PCM-I2S bus, TX_DBG | PU            | Typical = 6.5        | 3.5                  | 9.7       | $\mu A$ |
|   |                     | PD            | Typical = 27         | 9.5                  | 55        |         |
|   | All others          | PU            | Typical = 100        | 50                   | 300       |         |
|   |                     | PD            | Typical = 100        | 50                   | 360       |         |

## 5.7 Thermal Resistance Characteristics for VQFN-MR (RVM) Package

over operating free-air temperature range (unless otherwise noted)

| THERMAL METRICS <sup>(1)</sup> |                            | $C/W$ <sup>(2)</sup> |
|--------------------------------|----------------------------|----------------------|
| $R\theta_{ja}$                 | Junction-to-free-air       | 34.6                 |
| $R\theta_{jctop}$              | Junction-to-case-top       | 17.9                 |
| $R\theta_{jcbottom}$           | Junction-to-case-bottom    | 1.6                  |
| $R\theta_{jb}$                 | Junction-to-board          | 12.0                 |
| $\Phi_{jt}$                    | Junction-to-package-top    | 0.2                  |
| $\Phi_{jb}$                    | Junction-to-package-bottom | 12.0                 |

- (1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).
- (2) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [ $R\theta_{JC}$ ] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
  - JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
  - JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
  - JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*
- Power dissipation of 2 W and an ambient temperature of 70°C is assumed.

## 5.8 Timing and Switching Characteristics

### 5.8.1 Device Power Supply

The CC2564C power-management hardware and software algorithms provide significant power savings, which is a critical parameter in an MCU-based system.

The power-management module is optimized for drawing extremely low currents.

#### 5.8.1.1 Power Sources

The CC2564C device requires two power sources:

- VDD\_IN: main power supply for the device
- VDD\_IO: power source for the 1.8-V I/O ring

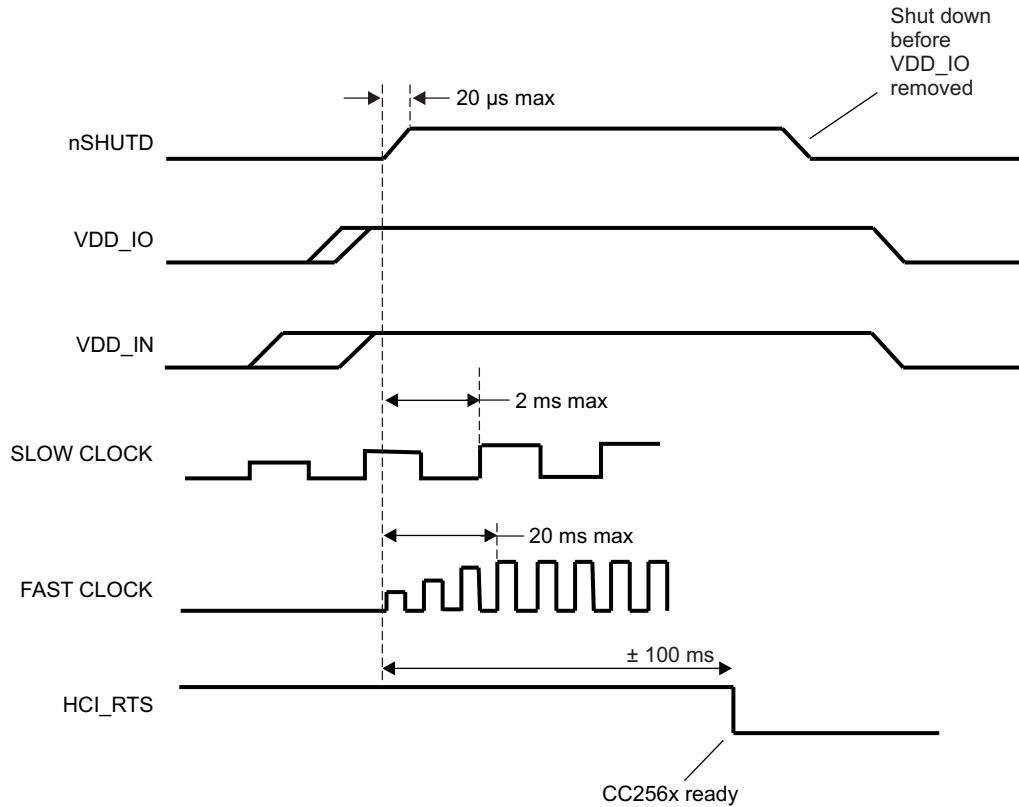
The HCI module includes several on-chip voltage regulators for increased noise immunity and can be connected directly to the battery.

#### 5.8.1.2 Device Power-Up and Power-Down Sequencing

The device includes the following power-up requirements (see [Figure 5-1](#)):

- nSHUTD must be low. VDD\_IN and VDD\_IO are don't care I/O pins when nSHUTD is low. However, signals are not allowed on the I/O pins if I/O power is not supplied, because the I/Os are not fail-safe. Exceptions are SLOW\_CLK\_IN and AUD\_xxx, which are fail-safe and can tolerate external voltages with no VDD\_IO and VDD\_IN.
- VDD\_IO and VDD\_IN must be stable before releasing nSHUTD.
- The fast clock must be stable within 20 ms of nSHUTD going high.
- The slow clock must be stable within 2 ms of nSHUTD going high.

The device indicates that the power-up sequence is complete by asserting RTS low, which occurs up to 100 ms after nSHUTD goes high. If RTS does not go low, the device is not powered up. In this case, ensure that the sequence and requirements are met.



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Figure 5-1. Power-Up and Power-Down Sequencing

### 5.8.1.3 Power Supplies and Shutdown—Static States

The nSHUTD signal puts the device in ultra-low-power mode and performs an internal reset to the device. The rise time for nSHUTD must not exceed 20 µs; nSHUTD must be low for a minimum of 5 ms.

To prevent conflicts with external signals, all I/O pins are set to the high-impedance (Hi-Z) state during shutdown and power up of the device. The internal pull resistors are enabled on each I/O pin, as described in Section 4.1.1. Table 5-1 lists and describes the static operation states.

Table 5-1. Power Modes

|   | VDD_IN <sup>(1)</sup> | VDD_IO <sup>(1)</sup> | nSHUTD <sup>(1)</sup> | PM_MODE     | COMMENTS   |
|---|-----------------------|-----------------------|-----------------------|-------------|--|
| 1 | None                  | None                  | Asserted              | Shutdown    | I/O state is undefined. No I/O voltages are allowed on nonfail-safe pins.    |
| 2 | None                  | None                  | Deasserted            | Not allowed | I/O state is undefined. No I/O voltages are allowed on nonfail-safe pins.    |
| 3 | None                  | Present               | Asserted              | Shutdown    | I/Os are defined as tri-state pins with internal pullup or pulldown enabled. |
| 4 | None                  | Present               | Deasserted            | Not allowed | I/O state is undefined. No I/O voltages are allowed on nonfail-safe pins.    |
| 5 | Present               | None                  | Asserted              | Shutdown    | I/O state is undefined.  |
| 6 | Present               | None                  | Deasserted            | Not allowed | I/O state is undefined. No I/O voltages are allowed on nonfail-safe pins.    |
| 7 | Present               | Present               | Asserted              | Shutdown    | I/Os are defined as tri-state pins with internal pullup or pulldown enabled. |
| 8 | Present               | Present               | Deasserted            | Active      | See Section 5.8.1.4.   |

(1) The terms *None* or *Asserted* can imply any of the following conditions: directly pulled to ground or driven low, pulled to ground through a pulldown resistor, or left NC or floating (high-impedance output stage).

### 5.8.1.4 I/O States in Various Power Modes

#### CAUTION

Some device I/Os are not fail-safe (see [Section 4.1.1](#)). Fail-safe means that the pins do not draw current from an external voltage applied to the pin when I/O power is not supplied to the device. External voltages are not allowed on these I/O pins when the I/O supply voltage is not supplied because of possible damage to the device.

[Table 5-2](#) lists the I/O states in various power modes.

**Table 5-2. I/O States in Various Power Modes**

| I/O NAME  | SHUTDOWN <sup>(1)</sup> |      | DEFAULT ACTIVE <sup>(1)</sup> |      | DEEP SLEEP <sup>(1)</sup> |      |
|-----------|-------------------------|------|-------------------------------|------|---------------------------|------|
|           | I/O State               | Pull | I/O State                     | Pull | I/O State                 | Pull |
| HCI_RX    | Z                       | PU   | I                             | PU   | I                         | PU   |
| HCI_TX    | Z                       | PU   | O-H                           |      | O                         |      |
| HCI_RTS   | Z                       | PU   | O-H                           |      | O                         |      |
| HCI_CTS   | Z                       | PU   | I                             | PU   | I                         | PU   |
| AUD_CLK   | Z                       | PD   | I                             | PD   | I                         | PD   |
| AUD_FSYNC | Z                       | PD   | I                             | PD   | I                         | PD   |
| AUD_IN    | Z                       | PD   | I                             | PD   | I                         | PD   |
| AUD_OUT   | Z                       | PD   | Z                             | PD   | Z                         | PD   |
| TX_DBG    | Z                       | PU   | O                             |      |                           |      |

(1) I = input, O = output, Z = Hi-Z, – = no pull, PU = pullup, PD = pulldown, H = high, L = low

### 5.8.1.5 nSHUTD Requirements

| PARAMETER                         |   | MIN  | MAX  | UNIT |
|-----------------------------------|---|------|------|------|
| V <sub>IH</sub>                   | Operation mode level <sup>(1)</sup>                 | 1.42 | 1.98 | V    |
| V <sub>IL</sub>                   | Shutdown mode level <sup>(1)</sup>                  | 0    | 0.4  | V    |
|                                   | Minimum time for nSHUT_DOWN low to reset the device | 5    |      | ms   |
| t <sub>r</sub> and t <sub>f</sub> | Rise and fall times                                 |      | 20   | μs   |

(1) An internal pulldown retains shutdown mode when no external signal is applied to this pin.

## 5.8.2 Clock Specifications

### 5.8.2.1 Slow Clock Requirements

An external source must supply the slow clock and connect to the SLOW\_CLK\_IN pin (for example, the host or external crystal oscillator). The source must be a digital signal in the range of 0 to 1.8 V. The accuracy of the slow-clock frequency must be 32.768 kHz  $\pm$ 250 ppm for Bluetooth use (as specified in the Bluetooth specification). The external slow clock must be stable within 64 slow-clock cycles (2 ms) following the release of nSHUTD.

| CHARACTERISTICS                                    |  | CONDITION               | MIN                  | TYP   | MAX                  | UNIT       |
|--|--|-------------------------|----------------------|-------|----------------------|------------|
| Input slow-clock frequency                         |  |                         |                      | 32768 |                      | Hz         |
| Input slow-clock accuracy (Initial + temp + aging) |  | Bluetooth               |                      |       | $\pm$ 250            | ppm        |
| $t_r$ and $t_f$                                    | Input transition time $t_r$ and $t_f$ (10% to 90%) |                         |                      |       | 200                  | ns         |
| Frequency input duty cycle                         |  |                         | 15%                  | 50%   | 85%                  |            |
| $V_{IH}$   | Slow-clock input voltage limits                    | Square wave, DC-coupled | 0.65 $\times$ VDD_IO |       | VDD_IO               | V peak     |
| $V_{IL}$   |  |                         | 0                    |       | 0.35 $\times$ VDD_IO | V peak     |
| Input impedance                                    |  |                         | 1                    |       |                      | M $\Omega$ |
| Input capacitance                                  |  |                         |                      |       | 5                    | pF         |

### 5.8.2.2 External Fast Clock Crystal Requirements and Operation

| CHARACTERISTICS                                    |                               | CONDITION  | MIN | TYP      | MAX      | UNIT     |
|--|-------------------------------|--|-----|----------|----------|----------|
| $f_{in}$   | Supported crystal frequencies |  |     | 26, 38.4 |          | MHz      |
| Frequency accuracy (Initial + temperature + aging) |                               |  |     |          | $\pm$ 20 | ppm      |
| Crystal oscillator negative resistance             |                               | 26 MHz, external capacitance = 8 pF<br>$I_{osc} = 0.5$ mA  | 650 | 940      |          | $\Omega$ |
|  |                               | 26 MHz, external capacitance = 20 pF<br>$I_{osc} = 2.2$ mA | 490 | 710      |          |          |

### 5.8.2.3 Fast Clock Source Requirements (–40°C to +85°C)

| CHARACTERISTICS                                   | CONDITION                          | MIN      | TYP      | MAX    | UNIT      |
|---|------------------------------------|----------|----------|--------|-----------|
| Supported frequencies, $F_{REF}$                  |                                    |          | 26, 38.4 |        | MHz       |
| Reference frequency accuracy                      | Initial + temp + aging             |          |          | ±20    | ppm       |
| Fast-clock input voltage limits                   | Square wave, DC-coupled            | $V_{IL}$ | –0.2     | 0.37   | V         |
|   |                                    | $V_{IH}$ | 1.0      | 2.1    | V         |
|   | Sine wave, AC-coupled              |          | 0.4      | 1.6    | $V_{p-p}$ |
|   | Sine wave, DC-coupled              |          | 0.4      | 1.6    | $V_{p-p}$ |
|   | Sine wave input limits, DC-coupled |          | 0.0      | 1.6    | V         |
| Fast-clock input rise time (as % of clock period) | Square wave, DC-coupled            |          |          | 10%    |           |
| Duty cycle  |                                    | 35%      | 50%      | 65%    |           |
| Phase noise for 26 MHz                            | @ offset = 1 kHz                   |          |          | –123.4 | dBc/Hz    |
|   | @ offset = 10 kHz                  |          |          | –133.4 |           |
|   | @ offset = 100 kHz                 |          |          | –138.4 |           |

### 5.8.3 Peripherals

#### 5.8.3.1 UART

Figure 5-2 shows the UART timing diagram.

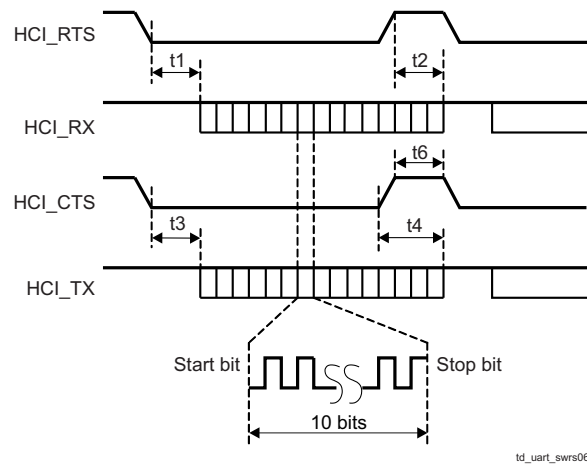


Figure 5-2. UART Timing

Table 5-3 lists the UART timing characteristics.

Table 5-3. UART Timing Characteristics

| SYMBOL | CHARACTERISTICS             | CONDITION                 | MIN    | TYP | MAX   | UNIT |
|--------|-----------------------------|---------------------------|--------|-----|-------|------|
|        | Baud rate                   |                           | 37.5   |     | 4000  | kbps |
|        | Baud rate accuracy per byte | Receive and transmit      | –2.5%  |     | 1.5%  |      |
|        | Baud rate accuracy per bit  | Receive and transmit      | –12.5% |     | 12.5% |      |
| t1     | RTS low to RX_DATA on       |                           | 0      | 2   |       | µs   |
| t2     | RTS high to RX_DATA off     | Interrupt set to 1/4 FIFO |        |     | 16    | byte |
| t3     | CTS low to TX_DATA on       |                           | 0      | 2   |       | µs   |
| t4     | CTS high to TX_DATA off     | Hardware flow control     |        |     | 1     | byte |
| t6     | CTS-high pulse width        |                           | 1      |     |       | bit  |



Figure 5-3 shows the UART data frame.

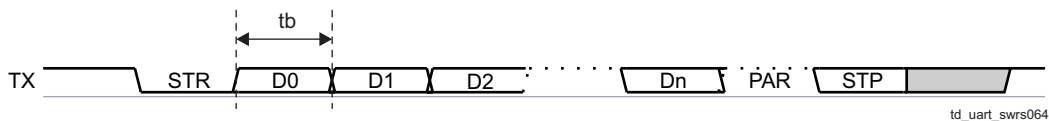


Figure 5-3. Data Frame

Table 5-4 describes the symbols used in Figure 5-3.

Table 5-4. Data Frame Key

| SYMBOL  | DESCRIPTION           |
|---------|-----------------------|
| STR     | Start bit             |
| D0...Dn | Data bits (LSB first) |
| PAR     | Parity bit (optional) |
| STP     | Stop bit              |

5.8.3.2 PCM

Figure 5-4 shows the interface timing for the PCM.

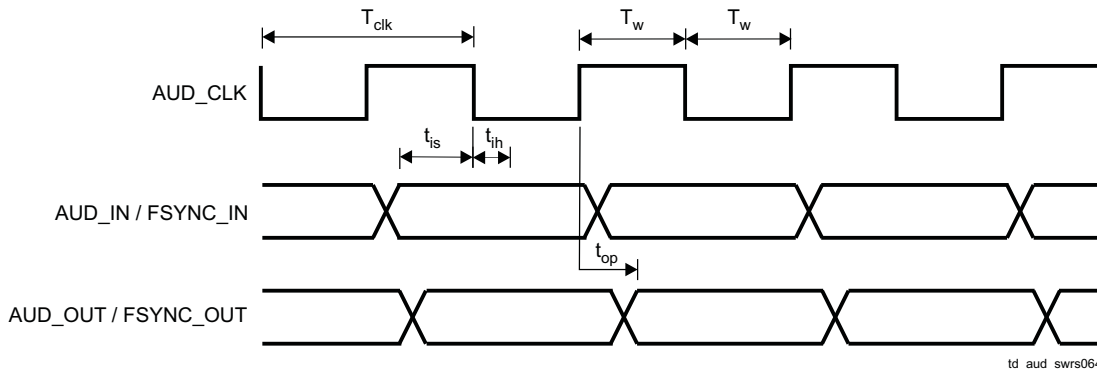


Figure 5-4. PCM Interface Timing

Table 5-5 lists the associated PCM master parameters.

Table 5-5. PCM Master

| SYMBOL    | PARAMETER                  | CONDITION  | MIN                   | MAX               | UNIT |
|-----------|----------------------------|------------|-----------------------|-------------------|------|
| $t_{clk}$ | Cycle time                 |            | 244.14<br>(4.096 MHz) | 15625<br>(64 kHz) | ns   |
| $t_w$     | High or low pulse width    |            | 50% of $T_{clk}$ min  |                   | ns   |
| $t_{is}$  | AUD_IN setup time          |            | 25                    |                   | ns   |
| $t_{ih}$  | AUD_IN hold time           |            | 0                     |                   | ns   |
| $t_{op}$  | AUD_OUT propagation time   | 40-pF load | 0                     | 10                | ns   |
| $t_{op}$  | FSYNC_OUT propagation time | 40-pF load | 0                     | 10                | ns   |

Table 5-6 lists the associated PCM slave parameters.

**Table 5-6. PCM Slave**

| SYMBOL    | PARAMETER                | CONDITION  | MIN               | MAX | UNIT |
|-----------|--------------------------|------------|-------------------|-----|------|
| $t_{clk}$ | Cycle time               |            | 66.67<br>(15 MHz) |     | ns   |
| $t_w$     | High or low pulse width  |            | 40% of $T_{clk}$  |     | ns   |
| $T_{is}$  | AUD_IN setup time        |            | 8                 |     | ns   |
| $t_{ih}$  | AUD_IN hold time         |            | 0                 |     | ns   |
| $t_{is}$  | AUD_FSYNC setup time     |            | 8                 |     | ns   |
| $t_{ih}$  | AUD_FSYNC hold time      |            | 0                 |     | ns   |
| $t_{op}$  | AUD_OUT propagation time | 40-pF load | 0                 | 21  | ns   |

## 5.8.4 RF Performance

### 5.8.4.1 Bluetooth BR and EDR RF Performance

All parameters in this section that are fast-clock dependent are verified using a 26-MHz XTAL and 38.4-MHz TCXO.

#### 5.8.4.1.1 Bluetooth Receiver—In-Band Signals

| CHARACTERISTICS                                      | CONDITION                                  |                | MIN   | TYP   | MAX  | BLUETOOTH SPECIFICATION | UNIT     |
|--|--|----------------|-------|-------|------|-------------------------|----------|
| Operation frequency range                            |  |                | 2402  |       | 2480 |                         | MHz      |
| Channel spacing                                      |  |                |       | 1     |      |                         | MHz      |
| Input impedance                                      |  |                |       | 50    |      |                         | $\Omega$ |
| Sensitivity, dirty TX on <sup>(1)</sup>              | GFSK, BER = 0.1%                           |                | -91.5 | -95   |      | -70                     | dBm      |
|  | $\pi/4$ -DQPSK, BER = 0.01%                |                | -90.5 | -94.5 |      | -70                     |          |
|  | 8DPSK, BER = 0.01%                         |                | -81   | -87.5 |      | -70                     |          |
| BER error floor at sensitivity + 10 dB, dirty TX off | $\pi/4$ -DQPSK                             |                | 1E-6  | 1E-7  |      | 1E-5                    |          |
|  | 8DPSK                                      |                | 1E-6  |       |      | 1E-5                    |          |
| Maximum usable input power                           | GFSK, BER = 0.1%                           |                | -5    |       |      | -20                     | dBm      |
|  | $\pi/4$ -DQPSK, BER = 0.1%                 |                | -10   |       |      |                         |          |
|  | 8DPSK, BER = 0.1%                          |                | -10   |       |      |                         |          |
| Intermodulation characteristics                      | Level of interferers (for n = 3, 4, and 5) |                | -36   | -30   |      | -39                     | dBm      |
| C/I performance <sup>(2)</sup><br>Image = -1 MHz     | GFSK, cochannel                            |                |       | 8     | 10   | 11                      | dB       |
|  | EDR, cochannel                             | $\pi/4$ -DQPSK |       | 9.5   | 11   | 13                      |          |
|  |  | 8DPSK          |       | 16.5  | 20   | 21                      |          |
|  | GFSK, adjacent $\pm 1$ MHz                 |                |       | -10   | -5   | 0                       |          |
|  | EDR, adjacent $\pm 1$ MHz, (image)         | $\pi/4$ -DQPSK |       | -10   | -5   | 0                       |          |
|  |  | 8DPSK          |       | -5    | -1   | 5                       |          |
|  | GFSK, adjacent +2 MHz                      |                |       | -38   | -35  | -30                     |          |
|  | EDR, adjacent, +2 MHz                      | $\pi/4$ -DQPSK |       | -38   | -35  | -30                     |          |
|  |  | 8DPSK          |       | -38   | -30  | -25                     |          |
|  | GFSK, adjacent -2 MHz                      |                |       | -28   | -20  | -20                     |          |
|  | EDR, adjacent -2 MHz                       | $\pi/4$ -DQPSK |       | -28   | -20  | -20                     |          |
|  |  | 8DPSK          |       | -22   | -13  | -13                     |          |
|  | GFSK, adjacent $\geq  \pm 3 $ MHz          |                |       | -45   | -43  | -40                     |          |
|  | EDR, adjacent $\geq  \pm 3 $ MHz           | $\pi/4$ -DQPSK |       | -45   | -43  | -40                     |          |
| 8DPSK  |  |                | -44   | -36   | -33  |                         |          |
| RF return loss                                       |  |                |       | -10   |      |                         | dB       |
| RX mode LO leakage                                   | Frf = (received RF - 0.6 MHz)              |                |       | -63   | -58  |                         | dBm      |

(1) Sensitivity degradation up to 3 dB may occur for minimum and typical values where the Bluetooth frequency is a harmonic of the fast clock.

(2) Numbers show ratio of desired signal to interfering signal. Smaller numbers indicate better C/I performance.

#### 5.8.4.1.2 Bluetooth Receiver—General Blocking

| CHARACTERISTICS   | CONDITION        | MIN | TYP | UNIT |
|---|------------------|-----|-----|------|
| Blocking performance over full range, according to Bluetooth specification <sup>(1)</sup> | 30 to 2000 MHz   |     | -6  | dBm  |
|   | 2000 to 2399 MHz |     | -6  |      |
|   | 2484 to 3000 MHz |     | -6  |      |
|   | 3 to 12.75 GHz   |     | -6  |      |

(1) Exceptions are taken out of the total 24 allowed in the Bluetooth specification.

### 5.8.4.1.3 Bluetooth Transmitter—GFSK

| CHARACTERISTICS                        |                                      | MIN | TYP | MAX | BLUETOOTH SPECIFICATION | UNIT |
|--|--------------------------------------|-----|-----|-----|-------------------------|------|
| Maximum RF output power <sup>(1)</sup> | VDD_IN = VBAT                        |     | 12  |     |                         | dBm  |
|  | VDD_IN = external regulator to 1.8 V |     | 10  |     |                         |      |
| Power variation over Bluetooth band    |                                      | -1  |     | 1   |                         | dB   |
| Gain control range                     |                                      |     | 30  |     |                         | dB   |
| Power control step                     |                                      |     | 5   |     | 2 to 8                  | dB   |
| Adjacent channel power  M-N  = 2       |                                      |     | -45 |     | ≤ -20                   | dBm  |
| Adjacent channel power  M-N  > 2       |                                      |     | -50 |     | ≤ -40                   | dBm  |

(1) To modify maximum output power, use an HCI VS command.

### 5.8.4.1.4 Bluetooth Transmitter—EDR

| CHARACTERISTICS                     |                |                                      | MIN | TYP | MAX | BLUETOOTH SPECIFICATION | UNIT |
|-------------------------------------|----------------|--------------------------------------|-----|-----|-----|-------------------------|------|
| EDR output power <sup>(1)</sup>     | $\pi/4$ -DQPSK | VDD_IN = VBAT                        |     | 5.5 |     |                         | dBm  |
|                                     |                | VDD_IN = external regulator to 1.8 V |     | 5.5 |     |                         |      |
|                                     | 8DPSK          | VDD_IN = VBAT                        |     | 5.5 |     |                         |      |
|                                     |                | VDD_IN = external regulator to 1.8 V |     | 5.5 |     |                         |      |
| EDR relative power                  |                |                                      | -2  |     | 1   | -4 to +1                | dB   |
| Power variation over Bluetooth band |                |                                      | -1  |     | 1   |                         | dB   |
| Gain control range                  |                |                                      |     | 30  |     |                         | dB   |
| Power control step                  |                |                                      |     | 5   |     | 2 to 8                  | dB   |
| Adjacent channel power  M-N  = 1    |                |                                      |     | -36 |     | ≤ -26                   | dBc  |
| Adjacent channel power  M-N  = 2    |                |                                      |     | -30 |     | ≤ -20                   | dBm  |
| Adjacent channel power  M-N  > 2    |                |                                      |     | -42 |     | ≤ -40                   | dBm  |

(1) To modify maximum output power, use an NCI VS command.

### 5.8.4.1.5 Bluetooth Modulation—GFSK

| CHARACTERISTICS                     |                            | CONDITION  |  | MIN | TYP | MAX | BLUETOOTH SPECIFICATION | UNIT           |
|-------------------------------------|----------------------------|--|--|-----|-----|-----|-------------------------|----------------|
|                                     | -20-dB bandwidth           | GFSK   |  |     | 925 |     | ≤ 1000                  | kHz            |
| F1 avg                              | Modulation characteristics | $\Delta f_{1avg}$  | Mod data = 4 1 s,<br>4 0 s:<br>111100001111... |     | 165 |     | 140 to 175              | kHz            |
| F2 max                              |                            | $\Delta f_{2max} \geq$ limit for at least 99.9% of all $\Delta f_{2max}$ | Mod data = 1010101...                          |     | 130 |     | > 115                   | kHz            |
|                                     |                            | $\Delta f_{2avg}, \Delta f_{1avg}$                                       |  |     |     | 88% |                         | > 80%          |
| Absolute carrier frequency drift    | DH1                        |  |  | -25 |     | 25  | < ±25                   | kHz            |
|                                     | DH3 and DH5                |  |  | -35 |     | 35  | < ±40                   |                |
| Drift rate                          |                            |  |  |     |     | 15  | < 20                    | kHz/50 $\mu$ s |
| Initial carrier frequency tolerance |                            | f0-fTX   |  | -75 |     | +75 | < ±75                   | kHz            |

### 5.8.4.1.6 Bluetooth Modulation—EDR

| CHARACTERISTICS                     | CONDITION | MIN | TYP | MAX | BLUETOOTH SPECIFICATION | UNIT |
|-------------------------------------|-----------|-----|-----|-----|-------------------------|------|
| Carrier frequency stability         |           |     |     | ±5  | ≤ 10                    | kHz  |
| Initial carrier frequency tolerance |           |     |     | ±75 | ±75                     | kHz  |
| RMS DEVM <sup>(1)</sup>             | π/4-DQPSK |     | 6%  |     | 20%                     |      |
|                                     | 8DPSK     |     | 6%  |     | 13%                     |      |
| 99% DEVM <sup>(1)</sup>             | π/4-DQPSK |     |     | 30% | 30%                     |      |
|                                     | 8DPSK     |     |     | 20% | 20%                     |      |
| Peak DEVM <sup>(1)</sup>            | π/4-DQPSK |     | 14% |     | 35%                     |      |
|                                     | 8DPSK     |     | 16% |     | 25%                     |      |

(1) Maximum performance refers to maximum TX power.

### 5.8.4.1.7 Bluetooth Transmitter—Out-of-Band and Spurious Emissions

| CHARACTERISTICS                 | CONDITION                        | TYP | MAX | UNIT |
|---------------------------------|----------------------------------|-----|-----|------|
| Second harmonic <sup>(1)</sup>  | Measured at maximum output power | -14 | -2  | dBm  |
| Third harmonic <sup>(1)</sup>   |                                  | -10 | -6  | dBm  |
| Fourth harmonics <sup>(1)</sup> |                                  | -19 | -11 | dBm  |

(1) Meets FCC and ETSI requirements with external filter shown in [Figure 7-1](#).

### 5.8.4.2 Bluetooth low energy RF Performance

All parameters in this section that are fast-clock dependent are verified using a 26-MHz XTAL and a 38.4-MHz TCXO.

#### 5.8.4.2.1 Bluetooth low energy Receiver—In-Band Signals

| CHARACTERISTIC                                   | CONDITION                              | MIN  | TYP | MAX  | BLUETOOTH low energy SPECIFICATION | UNIT |
|--|--|------|-----|------|------------------------------------|------|
| Operation frequency range                        |  | 2402 |     | 2480 |                                    | MHz  |
| Channel spacing                                  |  |      | 2   |      |                                    | MHz  |
| Input impedance                                  |  |      | 50  |      |                                    | Ω    |
| Sensitivity, dirty TX on <sup>(1)</sup>          | PER = 30.8%; dirty TX on               |      | -96 |      | ≤ -70                              | dBm  |
| Maximum usable input power                       | GMSK, PER = 30.8%                      | -5   |     |      | ≥ -10                              | dBm  |
| Intermodulation characteristics                  | Level of interferers (for n = 3, 4, 5) |      | -30 |      | ≥ -50                              | dBm  |
| C/I performance <sup>(2)</sup><br>Image = -1 MHz | GMSK, cochannel                        |      | 8   |      | ≤ 21                               | dB   |
|  | GMSK, adjacent ±1 MHz                  |      | -5  |      | ≤ 15                               |      |
|  | GMSK, adjacent +2 MHz                  |      | -45 |      | ≤ -17                              |      |
|  | GMSK, adjacent -2 MHz                  |      | -22 |      | ≤ -15                              |      |
|  | GMSK, adjacent ≥  ±3  MHz              |      | -47 |      | ≤ -27                              |      |
| RX mode LO leakage                               | Frf = (received RF - 0.6 MHz)          |      | -63 |      |                                    | dBm  |

(1) Sensitivity degradation up to 3 dB may occur where the Bluetooth low energy frequency is a harmonic of the fast clock.

(2) Numbers show wanted signal-to-interfering signal ratio. Smaller numbers indicate better C/I performance.

### 5.8.4.2.2 Bluetooth low energy Receiver—General Blocking

| CHARACTERISTICS  | CONDITION        | MIN | TYP | BLUETOOTH low energy SPECIFICATION | UNIT |
|--|------------------|-----|-----|------------------------------------|------|
| Blocking performance over full range, according to Bluetooth low energy specification <sup>(1)</sup> | 30 to 2000 MHz   |     | -15 | ≥ -30                              | dBm  |
|  | 2000 to 2399 MHz |     | -15 | ≥ -35                              |      |
|  | 2484 to 3000 MHz |     | -15 | ≥ -35                              |      |
|  | 3 to 12.75 GHz   |     | -15 | ≥ -30                              |      |

(1) Exceptions are taken out of the total 10 allowed in the Bluetooth low energy specification.

### 5.8.4.2.3 Bluetooth low energy Transmitter

| CHARACTERISTICS                                |                                      | MIN | TYP               | MAX | BLUETOOTH low energy SPECIFICATION | UNIT |
|--|--------------------------------------|-----|-------------------|-----|------------------------------------|------|
| RF output power                                | VDD_IN = VBAT                        |     | 12 <sup>(1)</sup> |     | ≤ 10                               | dBm  |
|  | VDD_IN = External regulator to 1.8 V |     | 10                |     | ≤ 10                               |      |
| Power variation over Bluetooth low energy band |                                      |     |                   |     | 1                                  | dB   |
| Adjacent channel power  M-N  = 2               |                                      |     |                   | -45 | ≤ -20                              | dBm  |
| Adjacent channel power  M-N  > 2               |                                      |     |                   | -50 | ≤ -30                              | dBm  |

(1) To achieve the Bluetooth low energy specification of 10-dBm maximum, an insertion loss of > 2 dB is assumed between the RF ball and the antenna. Otherwise, use an HCI VS command to modify the output power.

### 5.8.4.2.4 Bluetooth low energy Modulation

| CHARACTERISTICS |                                     | CONDITION                                       |  | MIN  | TYP | MAX | BLUETOOTH low energy SPECIFICATION | UNIT      |
|-----------------|-------------------------------------|---|--|------|-----|-----|------------------------------------|-----------|
| Δf1 avg         |                                     | Δf1avg  | Mod data = 4 1s, 4 0 s:<br>1111000011110000... | 240  | 250 | 260 | 225 to 275                         | kHz       |
| Δf2 max         | Modulation characteristics          | Δf2max ≥ limit for at least 99.9% of all Δf2max | Mod data = 1010101...                          | 185  | 210 |     | ≥ 185                              | kHz       |
|                 |                                     | Δf2avg, Δf1avg                                  |  | 0.85 | 0.9 |     | ≥ 0.8                              |           |
|                 | Absolute carrier frequency drift    |   |  | -25  |     | 25  | ≤ ±50                              | kHz       |
|                 | Drift rate                          |   |  |      |     | 15  | ≤ 20                               | kHz/50 ms |
|                 | Initial carrier frequency tolerance |   |  | -75  |     | 75  | ≤ ±100                             | kHz       |

### 5.8.4.2.5 Bluetooth low energy Transceiver, Out-Of-Band and Spurious Emissions

| CHARACTERISTICS                 | CONDITION                        | TYP | MAX | UNIT |
|---------------------------------|----------------------------------|-----|-----|------|
| Second harmonic <sup>(1)</sup>  | Measured at maximum output power | -14 | -2  | dBm  |
| Third harmonic <sup>(1)</sup>   |                                  | -10 | -6  | dBm  |
| Fourth harmonics <sup>(1)</sup> |                                  | -19 | -11 | dBm  |

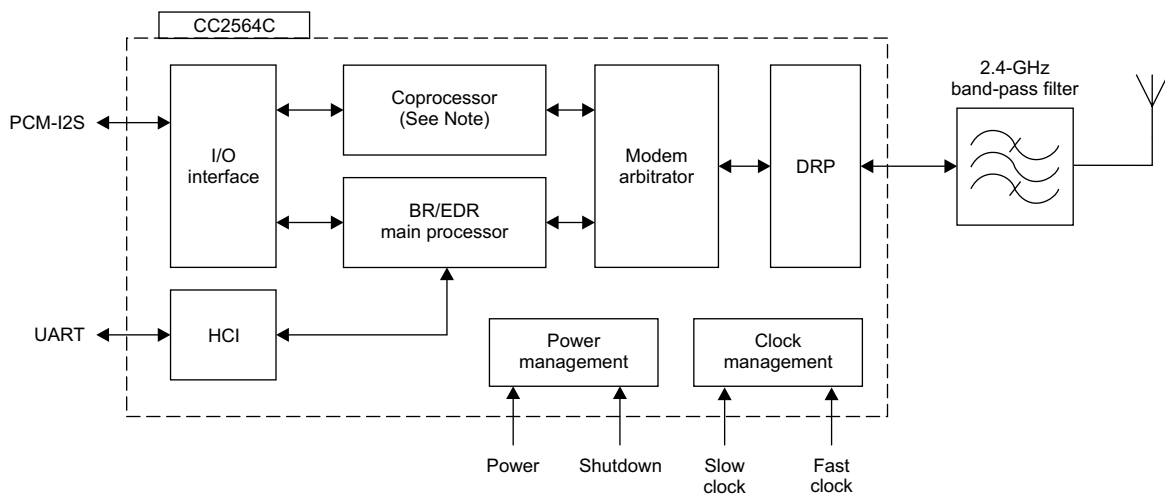
(1) Meets FCC and ETSI requirements with external filter shown in [Figure 7-1](#).

## 6 Detailed Description

### 6.1 Overview

The CC2564C architecture comprises a DRP and a point-to-multipoint baseband core. The architecture is based on a single-processor ARM7TDMI® core. The device includes several on-chip peripherals to enable easy communication with a host system and the Bluetooth BR, EDR, and low energy core.

### 6.2 Functional Block Diagram



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NOTE: The following technologies and assisted modes cannot be used simultaneously with the coprocessor: Bluetooth low energy, assisted HFP 1.6 (WBS), and assisted A2DP. Only one technology or assisted mode can be used at a time.

**Figure 6-1. CC2564C Functional Block Diagram**

### 6.3 Clock Inputs

This section describes the available clock inputs. For specifications, see [Section 5.8.2](#).

#### 6.3.1 Slow Clock

An external source must supply the slow clock and connect to the SLOW\_CLK\_IN pin (for example, the host or external crystal oscillator). The source must be a digital signal in the range of 0 V to 1.8 V. The accuracy of the slow-clock frequency must be 32.768 kHz  $\pm$ 250 ppm for Bluetooth use (as specified in the Bluetooth specification). The external slow clock must be stable within 64 slow-clock cycles (2 ms) following the release of nSHUTD.

#### 6.3.2 Fast Clock Using External Clock Source

An external clock source is fed to an internal pulse-shaping cell to provide the fast-clock signal for the device. The device incorporates an internal, automatic clock-scheme detection mechanism that automatically detects the fast-clock scheme used and configures the FREF cell accordingly. This mechanism ensures that the electrical characteristics (loading) of the fast-clock input remain static regardless of the scheme used and eliminates any power-consumption penalty-versus-scheme used.

The frequency variation of the fast-clock source must not exceed  $\pm$ 20 ppm (as defined by the Bluetooth specification).

The external clock can be AC- or DC-coupled, sine or square wave.

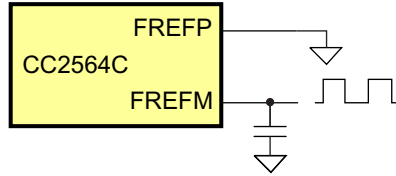
**6.3.2.1 External F<sub>REF</sub> DC-Coupled**

Figure 6-2 and Figure 6-3 show the clock configuration when using a square wave, DC-coupled external source for the fast-clock input.

**NOTE**

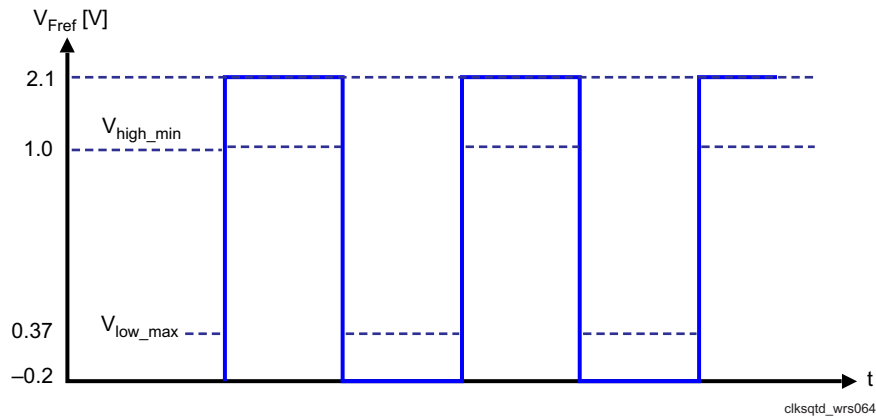
A shunt capacitor with a range of 10 nF must be added on the oscillator output to reject high harmonics and shape the signal to be close to a sinusoidal waveform.

TI recommends using only a dedicated LDO to feed the oscillator. Do not use the same VIO for the oscillator and the CC2564C device.



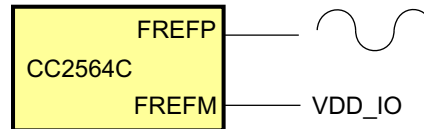
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**Figure 6-2. Clock Configuration (Square Wave, DC-Coupled)**



**Figure 6-3. External Fast Clock (Square Wave, DC-Coupled)**

Figure 6-4 and Figure 6-5 show the clock configuration when using a sine wave, DC-coupled external source for the fast clock input.



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**Figure 6-4. Clock Configuration (Sine Wave, DC-Coupled)**



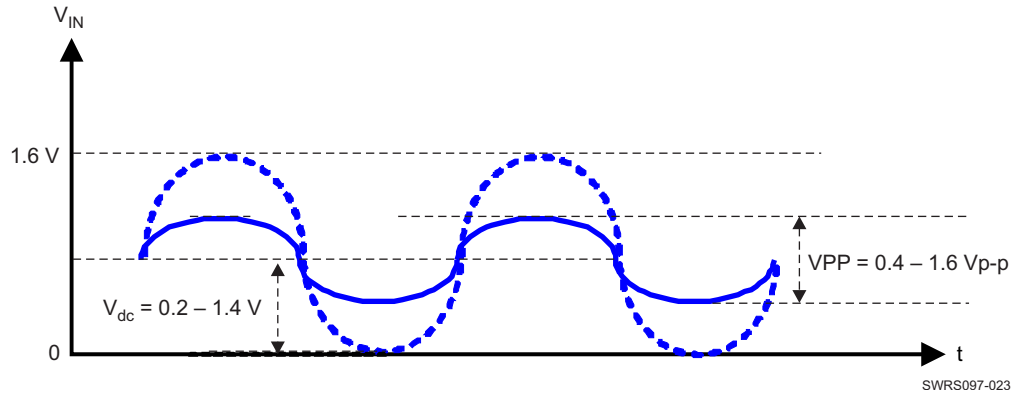
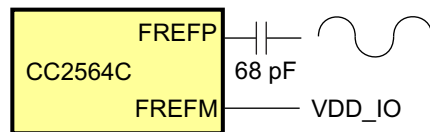


Figure 6-5. External Fast Clock (Sine Wave, DC-Coupled)

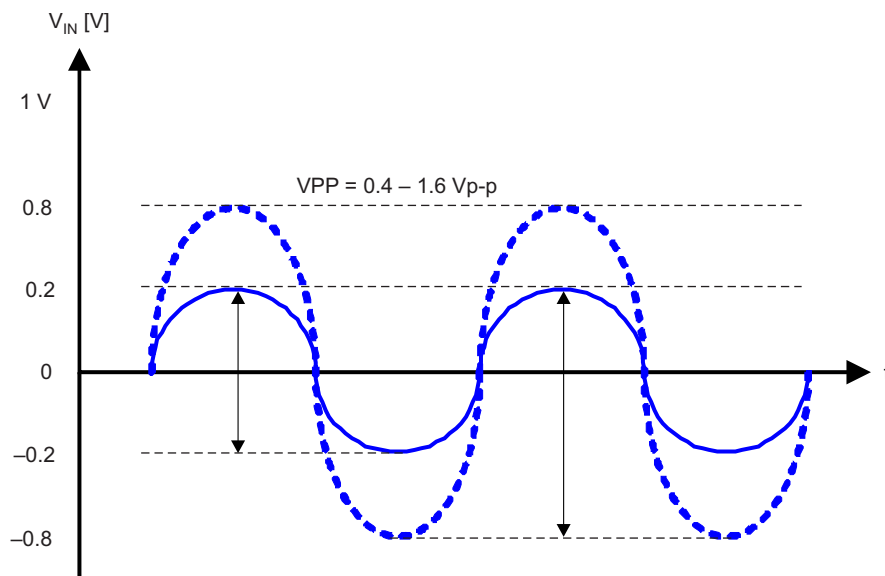
6.3.2.2 External F<sub>REF</sub> Sine Wave, AC-Coupled

Figure 6-6 and Figure 6-7 show the configuration when using a sine wave, AC-coupled external source for the fast-clock input.



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Figure 6-6. Clock Configuration (Sine Wave, AC-Coupled)



SWRS097-022

Figure 6-7. External Fast Clock (Sine Wave, AC-Coupled)

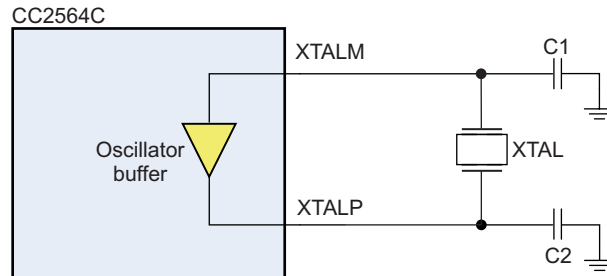
In cases where the input amplitude is greater than 1.6 V<sub>p-p</sub>, the amplitude can be reduced to within limits. Using a small series capacitor forms a voltage divider with the internal input capacitance of approximately 2 pF to provide the required amplitude at the device input.

### 6.3.2.3 Fast Clock Using External Crystal

The CC2564C device incorporates an internal crystal oscillator buffer to support a crystal-based fast-clock scheme. The supported crystal frequencies are 26 and 38.4 MHz.

The frequency accuracy of the fast-clock source must not exceed  $\pm 20$  ppm (including the accuracy of the capacitors, as specified in the Bluetooth specification).

Figure 6-8 shows the recommended fast-clock circuitry.



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**Figure 6-8. Fast-Clock Crystal Circuit**

Table 6-1 lists component values for the fast-clock crystal circuit.

**Table 6-1. Fast-Clock Crystal Circuit Component Values**

| FREQ (MHz) | C1 (pF) <sup>(1)</sup> | C2 (pF) <sup>(1)</sup> |
|------------|------------------------|------------------------|
| 26         | 12                     | 12                     |

- (1) To achieve the required accuracy, values for C1 and C2 must be taken from the crystal manufacturer's data sheet and layout considerations.

## 6.4 Functional Blocks

### 6.4.1 RF

The CC2564C device is the third generation of Bluetooth single-chip devices using DRP architecture from TI. Modifications and new features added to the DRP further improve radio performance.

Figure 6-9 shows the DRP block diagram.

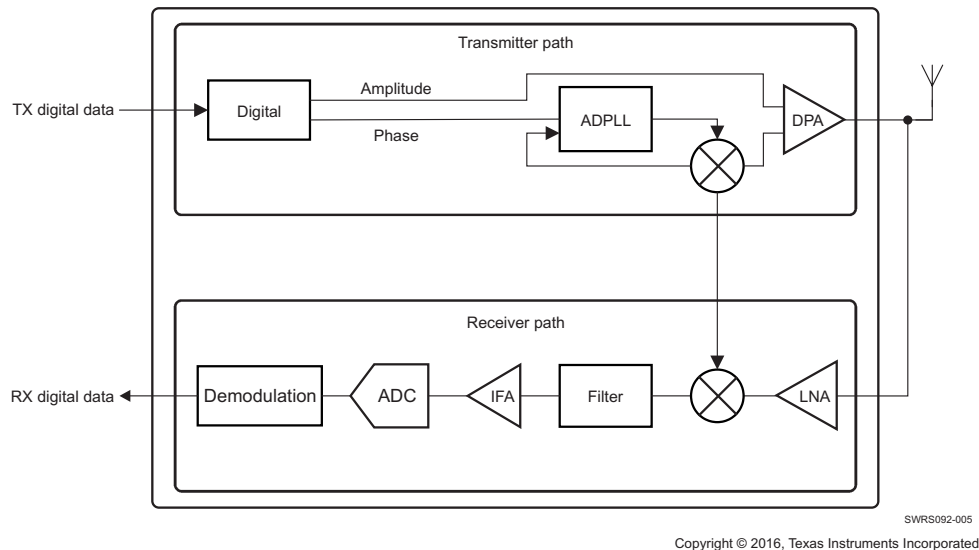


Figure 6-9. DRP Block Diagram

#### 6.4.1.1 Receiver

The receiver uses near-zero-IF architecture to convert the RF signal to baseband data. The signal received from the external antenna is input to a single-ended low-noise amplifier (LNA) and passed to a mixer that downconverts the signal to IF, followed by a filter and amplifier. The signal is then quantized by a sigma-delta analog-to-digital converter (ADC) and further processed to reduce the interference level.

The demodulator digitally downconverts the signal to zero-IF and recovers the data stream using an adaptive-decision mechanism. The demodulator includes EDR processing with:

- State-of-the-art performance
- A maximum-likelihood sequence estimator (MLSE) to improve the performance of basic-rate GFSK sensitivity
- Adaptive equalization to enhance EDR modulation

New features include:

- LNA input range narrowed to increase blocking performance
- Active spur cancellation to increase robustness to spurs

### 6.4.1.2 Transmitter

The transmitter is an all-digital, sigma-delta phase-locked loop (ADPLL) based with a digitally controlled oscillator (DCO) at 2.4 GHz as the RF clock. The transmitter directly modulates the digital PLL. The power amplifier is also digitally controlled. The transmitter uses the polar-modulation technique. While the phase-modulated control word is fed to the ADPLL, the amplitude-modulated controlled word is fed to the class-E amplifier to generate a Bluetooth standard-compliant RF signal.

New features include:

- Improved TX output power
- LMS algorithm to improve the differential error vector magnitude (DEVm)

### 6.4.2 Host Controller Interface

The CC2564C device incorporates one UART module dedicated to the HCI transport layer. The HCI transports commands, events, and ACL between the device and the host using HCI data packets.

The CC2564C device supports the H4 protocol (4-wire UART) with hardware flow control and the H5 protocol (3-wire UART) with software flow control. The CC2564C device automatically detects the protocol on reception of the first command.

The maximum baud rate of the UART module is 4 Mbps; however, the default baud rate after power up is set to 115.2 kbps. The baud rate can thereafter be changed with a VS command. The device responds with a command complete event (still at 115.2 kbps), after which the baud rate change occurs.

The UART module includes the following features:

- Receiver detection of break, idle, framing, FIFO overflow, and parity error conditions
- Transmitter underflow detection
- CTS and RTS hardware flow control (H4 protocol)
- XON and XOFF software flow control (H5 protocol)

[Table 6-2](#) lists the UART module default settings.

**Table 6-2. UART Module Default Settings**

| PARAMETER   | VALUE      |
|-------------|------------|
| Bit rate    | 115.2 kbps |
| Data length | 8 bits     |
| Stop bit    | 1          |
| Parity      | None       |

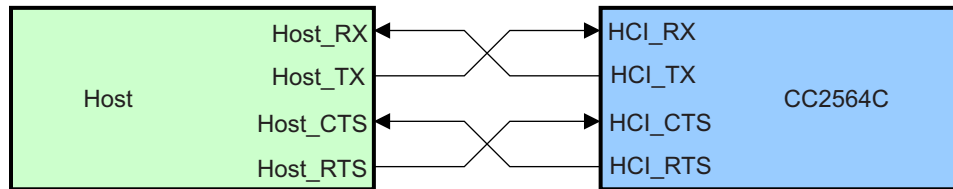
### 6.4.2.1 4-Wire UART Interface—H4 Protocol

The H4 UART Interface includes four signals:

- TX
- RX
- CTS
- RTS

Flow control between the host and the CC2564C device is byte-wise by hardware.

Figure 6-10 shows the H4 UART interface.



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**Figure 6-10. H4 UART Interface**

When the UART RX buffer of the device passes the flow control threshold, it sets the HCI\_RTS signal high to stop transmission from the host.

When the HCI\_CTS signal is set high, the device stops transmission on the interface. If HCI\_CTS is set high while transmitting a byte, the device finishes transmitting the byte and stops the transmission.

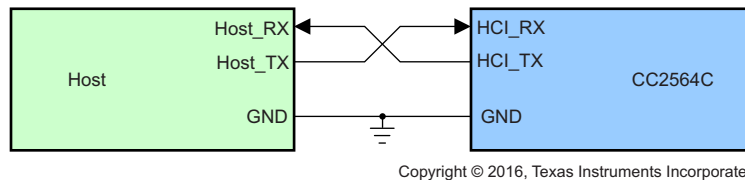
The H4 protocol device includes a mechanism that handles the transition between active mode and sleep mode. The protocol occurs through the CTS and RTS UART lines and is known as the enhanced HCI low level (eHCILL) power-management protocol.

For more information on the H4 UART protocol, see *Volume 4 Host Controller Interface, Part A UART Transport Layer of the Bluetooth Core Specifications* ([www.bluetooth.org/en-us/specification/adoptedspecifications](http://www.bluetooth.org/en-us/specification/adoptedspecifications)).

### 6.4.2.2 3-Wire UART Interface—H5 Protocol

The H5 UART interface consists of three signals (see [Figure 6-11](#)):

- TX
- RX
- GND



**Figure 6-11. H5 UART Interface**

The H5 protocol supports the following features:

- Software flow control (XON/XOFF)
- Power management using the software messages:
  - WAKEUP
  - WOKEN
  - SLEEP
- CRC data integrity check

For more information on the H5 UART protocol, see *Volume 4 Host Controller Interface, Part D Three-Wire UART Transport Layer of the Bluetooth Core Specifications* ([www.bluetooth.org/en-us/specification/adoptedspecifications](http://www.bluetooth.org/en-us/specification/adoptedspecifications)).

### 6.4.3 Digital Codec Interface

The codec interface is a fully programmable port to support seamless interfacing with different PCM and I2S codec devices. The interface includes the following features:

- Two voice channels
- Master and slave modes
- All voice coding schemes defined by the Bluetooth specification: linear, A-Law, and  $\mu$ -Law
- Long and short frames
- Different data sizes, order, and positions
- High flexibility to support a variety of codecs
- Bus sharing: Data\_Out is in the Hi-Z state when the interface is not transmitting voice data.

### 6.4.3.1 Hardware Interface

The interface includes four signals:

- Clock: configurable direction (input or output)
- Frame\_Sync and Word\_Sync: configurable direction (input or output)
- Data\_In: input
- Data\_Out: output or tri-state signal

The CC2564C device can be the master of the interface when generating the Clock and Frame\_Sync signals or the slave when receiving these two signals.

For slave mode, clock input frequencies of up to 15 MHz are supported. At clock rates above 12 MHz, the maximum data burst size is 32 bits.

For master mode, the device can generate any clock frequency from 64 kHz to 4.096 MHz.

### 6.4.3.2 I2S

When the codec interface is configured to support the I2S protocol, these settings are recommended:

- Bidirectional, full-duplex interface
- Two time slots per frame: time slot 0 for the left channel audio data; and time slot 1 for the right channel audio data
- The length of each time slot is configurable up to 40 serial clock cycles, and the length of the frame is configurable up to 80 serial clock cycles

### 6.4.3.3 Data Format

The data format is fully configurable:

- The data length can be from 8 to 320 bits in 1-bit increments when working with 2 channels, or up to 640 bits when working with 1 channel. The data length can be set independently for each channel.
- The data position within a frame is also configurable within 1 clock (bit) resolution and can be set independently (relative to the edge of the Frame\_Sync signal) for each channel.
- The Data\_In and Data\_Out bit order can be configured independently. For example; Data\_In can start with the most significant bit (MSB); Data\_Out can start with the least significant bit (LSB). Each channel is separately configurable. The inverse bit order (that is, LSB first) is supported only for sample sizes up to 24 bits.
- Data\_In and Data\_Out are not required to be the same length.
- The Data\_Out line is configured to Hi-Z output between data words. Data\_Out can also be set for permanent Hi-Z output, regardless of the data output. This configuration allows the device to be a bus slave in a multislave PCM environment. At power up, Data\_Out is configured as Hi-Z output.

### 6.4.3.4 Frame-Idle Period

The codec interface handles frame-idle periods, during which the clock pauses and becomes 0 at the end of the frame after all data are transferred.

The device supports frame-idle periods both as master and slave of the codec bus.

When the device is the master of the interface, the frame-idle period is configurable. There are two configurable parameters:

- Clk\_Idle\_Start: indicates the number of clock cycles from the beginning of the frame to the beginning of the frame-idle period. After Clk\_Idle\_Start clock cycles, the clock becomes 0.
- Clk\_Idle\_End: indicates the time from the beginning of the frame to the end of the frame-idle period. The time is given in multiples of clock periods.

The delta between Clk\_Idle\_Start and Clk\_Idle\_End is the clock idle period.

For example, for clock rate = 1 MHz, frame sync period = 10 kHz, Clk\_Idle\_Start = 60, Clk\_Idle\_End = 90.

Between both Frame\_Sync signals there are 70 clock cycles (instead of 100). The clock idle period starts 60 clock cycles after the beginning of the frame and lasts  $90 - 60 = 30$  clock cycles. Thus, the idle period ends  $100 - 90 = 10$  clock cycles before the end of the frame. The data transmission must end before the beginning of the idle period.

Figure 6-12 shows the frame idle timing.

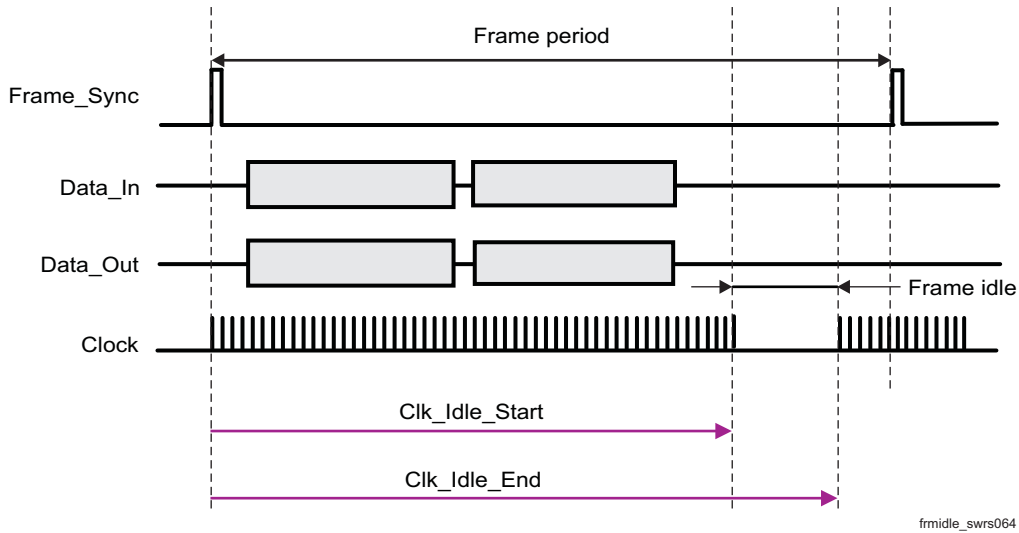


Figure 6-12. Frame Idle Period

### 6.4.3.5 Clock-Edge Operation

The codec interface of the device can work on the rising or the falling edge of the clock and can sample the Frame\_Sync signal and the data at inversed polarity.

Figure 6-13 shows the operation of a falling-edge-clock type of codec. The codec is the master of the bus. The Frame\_Sync signal is updated (by the codec) on the falling edge of the clock and is therefore sampled (by the device) on the next rising clock. The data from the codec is sampled (by the device) on the falling edge of the clock.

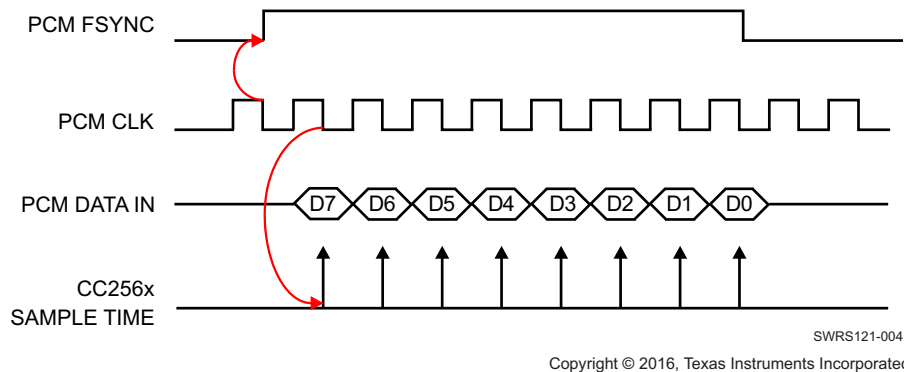
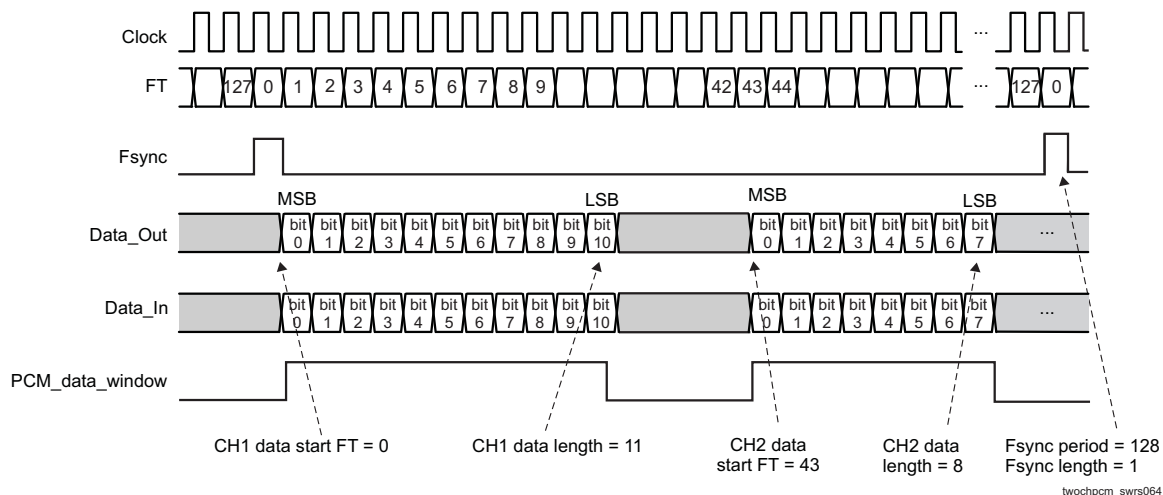


Figure 6-13. Negative Clock Edge Operation

### 6.4.3.6 Two-Channel Bus Example

Figure 6-14 shows a 2-channel bus in which the two channels have different word sizes and arbitrary positions in the bus frame.





NOTE: FT stands for frame timer.

Figure 6-14. 2-Channel Bus Timing

### 6.4.4 Assisted Modes

The CC2564C device contains an embedded coprocessor that can be used for multiple purposes (see Figure 1-1). The CC2564C device uses the coprocessor to perform the LE functionality or to execute the assisted HFP 1.6 (WBS) or assisted A2DP functions. Only one of these functions can be executed at a time because they all use the same resources (that is, the coprocessor; see Table 3-1 for the modes of operation supported by each device).

This section describes the assisted HFP 1.6 (WBS) and assisted A2DP modes of operation. These modes of operation minimize host processing and power by taking advantage of the device coprocessor to perform the voice and audio SBC processing required in HFP 1.6 (WBS) and A2DP profiles. This section also compares the architecture of the assisted modes with the common implementation of the HFP 1.6 and A2DP profiles.

The assisted HFP 1.6 (WBS) and assisted A2DP modes of operation comply fully with the HFP 1.6 and A2DP Bluetooth specifications. For more information on these profiles, see the corresponding Bluetooth Profile Specification ([www.bluetooth.org/en-us/specification/adopted-specifications](http://www.bluetooth.org/en-us/specification/adopted-specifications)).

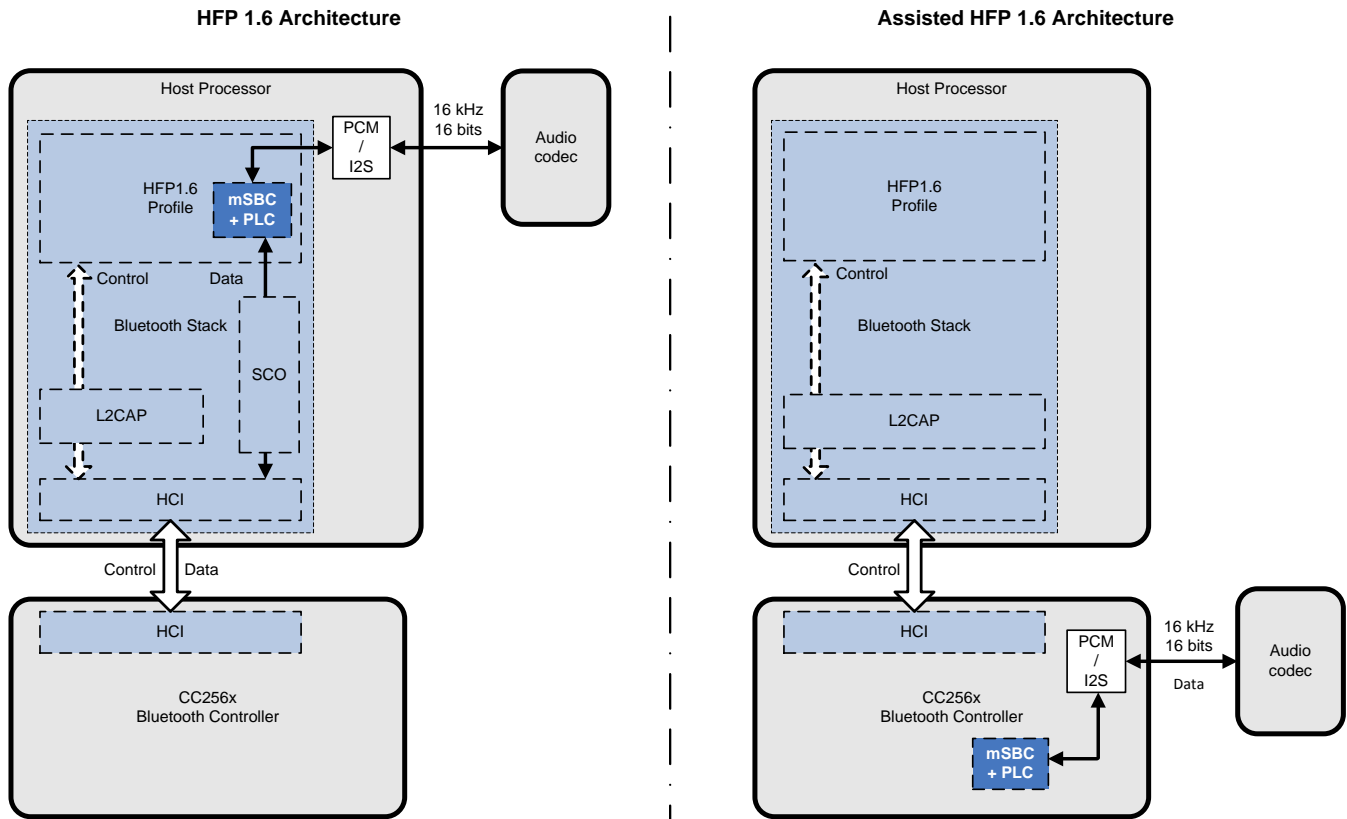
#### 6.4.4.1 Assisted HFP 1.6 (WBS)

The *HFP 1.6 Profile Specification* adds the requirement for WBS support. The WBS feature allows twice the voice quality versus legacy voice coding schemes at the same air bandwidth (64 kbps). This feature is achieved using a voice sampling rate of 16 kHz, a modified subband coding (mSBC) scheme, and a packet loss concealment (PLC) algorithm. The mSBC scheme is a modified version of the mandatory audio coding scheme used in the A2DP profile with the parameters listed in Table 6-3.

Table 6-3. mSBC Parameters

| PARAMETER         | VALUE    |
|-------------------|----------|
| Channel mode      | Mono     |
| Sampling rate     | 16 kHz   |
| Allocation method | Loudness |
| Subbands          | 8        |
| Block length      | 15       |
| Bitpool           | 26       |

The assisted HFP 1.6 mode of operation implements this WBS feature on the embedded CC2564C coprocessor. That is, the mSBC voice coding scheme and the PLC algorithm are executed in the CC2564C coprocessor rather than in the host, thus minimizing host processing and power. One WBS connection at a time is supported, and WBS and NBS connections cannot be used simultaneously in this mode of operation. Figure 6-15 shows the architecture comparison between the common implementation of the HFP 1.6 profile and the assisted HFP 1.6 solution.



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**Figure 6-15. HFP 1.6 Architecture Versus Assisted HFP 1.6 Architecture**

For detailed information on the HFP 1.6 profile, see the *Hands-Free Profile 1.6 Specification* ([www.bluetooth.org/en-us/specification/adopted-specifications](http://www.bluetooth.org/en-us/specification/adopted-specifications)).

**6.4.4.2 Assisted A2DP**

The advanced audio distribution profile (A2DP) enables wireless transmission of high-quality mono or stereo audio between two devices. A2DP defines two roles:

- A2DP source is the transmitter of the audio stream.
- A2DP sink is the receiver of the audio stream.

A typical use case streams music from a tablet, phone, or PC (the A2DP source) to headphones or speakers (the A2DP sink). This section describes the architecture of these roles and compares them with the corresponding assisted-A2DP architecture. To use the air bandwidth efficiently, the audio data must be compressed in a proper format. The A2DP mandates support of the SBC scheme. Other audio coding algorithms can be used; however, both Bluetooth devices must support the same coding scheme. SBC is the only coding scheme spread out in all A2DP Bluetooth devices; thus, it is the only coding scheme supported in the assisted A2DP modes. Table 6-4 lists the recommended parameters for the SBC scheme in the assisted A2DP modes.

**Table 6-4. Recommended Parameters for the SBC Scheme in Assisted A2DP Modes**

| SBC ENCODER SETTINGS <sup>(1)</sup> | MID QUALITY |     |              |     | HIGH QUALITY |     |              |     |
|-------------------------------------|-------------|-----|--------------|-----|--------------|-----|--------------|-----|
|                                     | MONO        |     | JOINT STEREO |     | MONO         |     | JOINT STEREO |     |
| Sampling frequency (kHz)            | 44.1        | 48  | 44.1         | 48  | 44.1         | 48  | 44.1         | 48  |
| Bitpool value                       | 19          | 18  | 35           | 33  | 31           | 29  | 53           | 51  |
| Resulting frame length (bytes)      | 46          | 44  | 83           | 79  | 70           | 66  | 119          | 115 |
| Resulting bit rate (Kbps)           | 127         | 132 | 229          | 237 | 193          | 198 | 328          | 345 |

(1) Other settings: Block length = 16; allocation method = loudness; subbands = 8.

The SBC scheme supports a wide variety of configurations to adjust the audio quality. [Table 6-5](#) through [Table 6-12](#) list the supported SBC capabilities in the assisted A2DP modes.

**Table 6-5. Channel Modes**

| CHANNEL MODE | STATUS    |
|--------------|-----------|
| Mono         | Supported |
| Dual channel | Supported |
| Stereo       | Supported |
| Joint stereo | Supported |

**Table 6-6. Sampling Frequency**

| SAMPLING FREQUENCY (kHz) | STATUS    |
|--------------------------|-----------|
| 16                       | Supported |
| 44.1                     | Supported |
| 48                       | Supported |

**Table 6-7. Block Length**

| BLOCK LENGTH | STATUS    |
|--------------|-----------|
| 4            | Supported |
| 8            | Supported |
| 12           | Supported |
| 16           | Supported |

**Table 6-8. Subbands**

| SUBBANDS | STATUS    |
|----------|-----------|
| 4        | Supported |
| 8        | Supported |

**Table 6-9. Allocation Method**

| ALLOCATION METHOD | STATUS    |
|-------------------|-----------|
| SNR               | Supported |
| Loudness          | Supported |

**Table 6-10. Bitpool Values**

| BITPOOL RANGE              | STATUS    |
|----------------------------|-----------|
| Assisted A2DP sink: 2–54   | Supported |
| Assisted A2DP source: 2–57 | Supported |

**Table 6-11. L2CAP MTU Size**

| L2CAP MTU SIZE (BYTES)         | STATUS    |
|--------------------------------|-----------|
| Assisted A2DP sink: 260–800    | Supported |
| Assisted A2DP source: 260–1021 | Supported |

**Table 6-12. Miscellaneous Parameters**

| ITEM                    | VALUE        | STATUS        |
|-------------------------|--------------|---------------|
| A2DP content protection | Protected    | Not supported |
| AVDTP service           | Basic type   | Supported     |
| L2CAP mode              | Basic mode   | Supported     |
| L2CAP flush             | Nonflushable | Supported     |

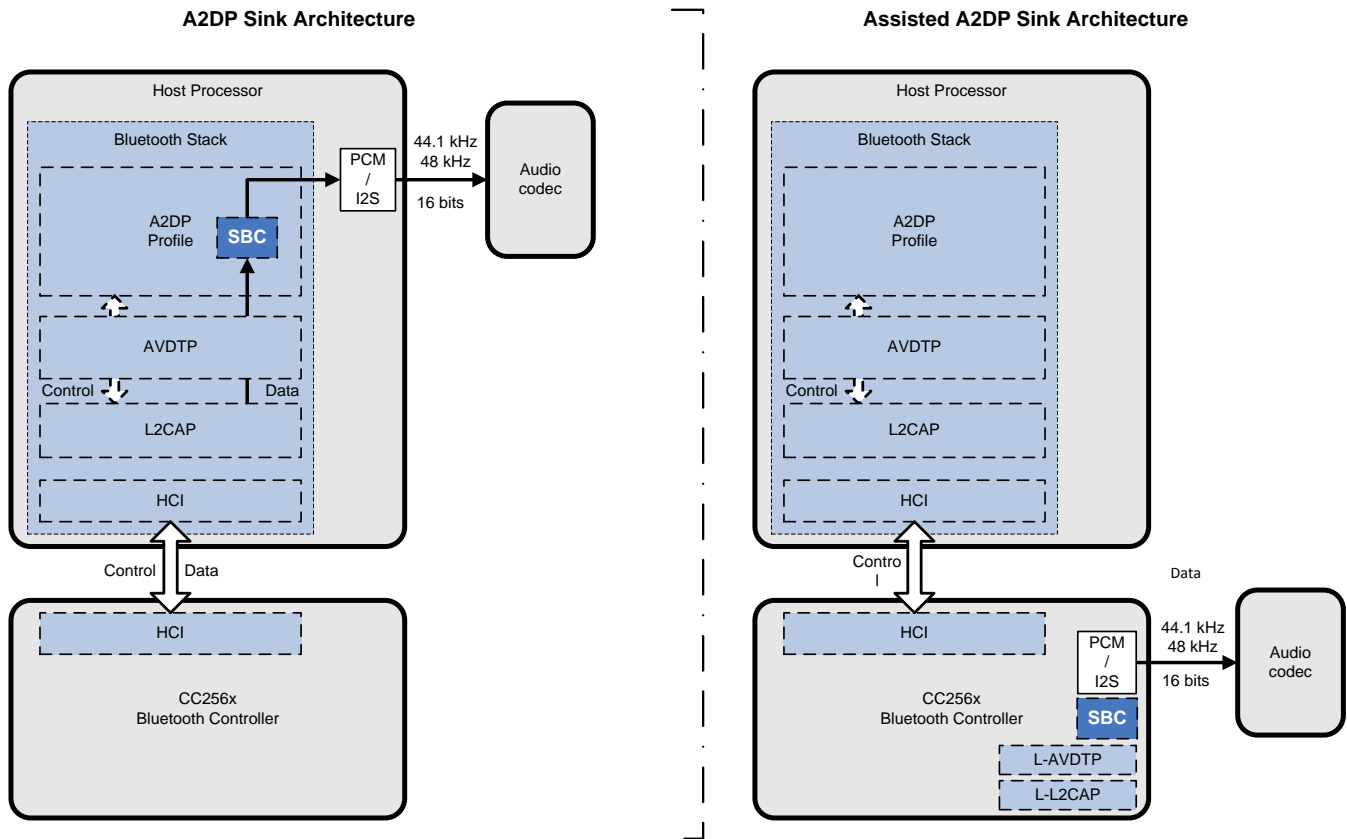
For detailed information on the A2DP profile, see the *A2DP Profile Specification* at [Adopted Bluetooth Core Specifications](#).

#### 6.4.4.2.1 Assisted A2DP Sink

The role of the A2DP sink is to receive the audio stream in an A2DP Bluetooth connection. In this role, the A2DP layer and its underlying layers are responsible for link management and data decoding. To handle these tasks, two logic transports are defined:

- Control and signaling logic transport
- Data packet logic transport

The assisted A2DP takes advantage of this modularity to handle the data packet logic transport in the CC2564C device. First, the assisted A2DP implements a light L2CAP layer (L-L2CAP) and light AVDTP layer (L-AVDTP) to defragment the packets. Then the assisted A2DP performs the SBC decoding on-chip to deliver raw audio data through the device PCM–I2S interface. [Figure 6-16](#) shows the comparison between a common A2DP sink architecture and the assisted A2DP sink architecture.



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**Figure 6-16. A2DP Sink Architecture Versus Assisted A2DP Sink Architecture**

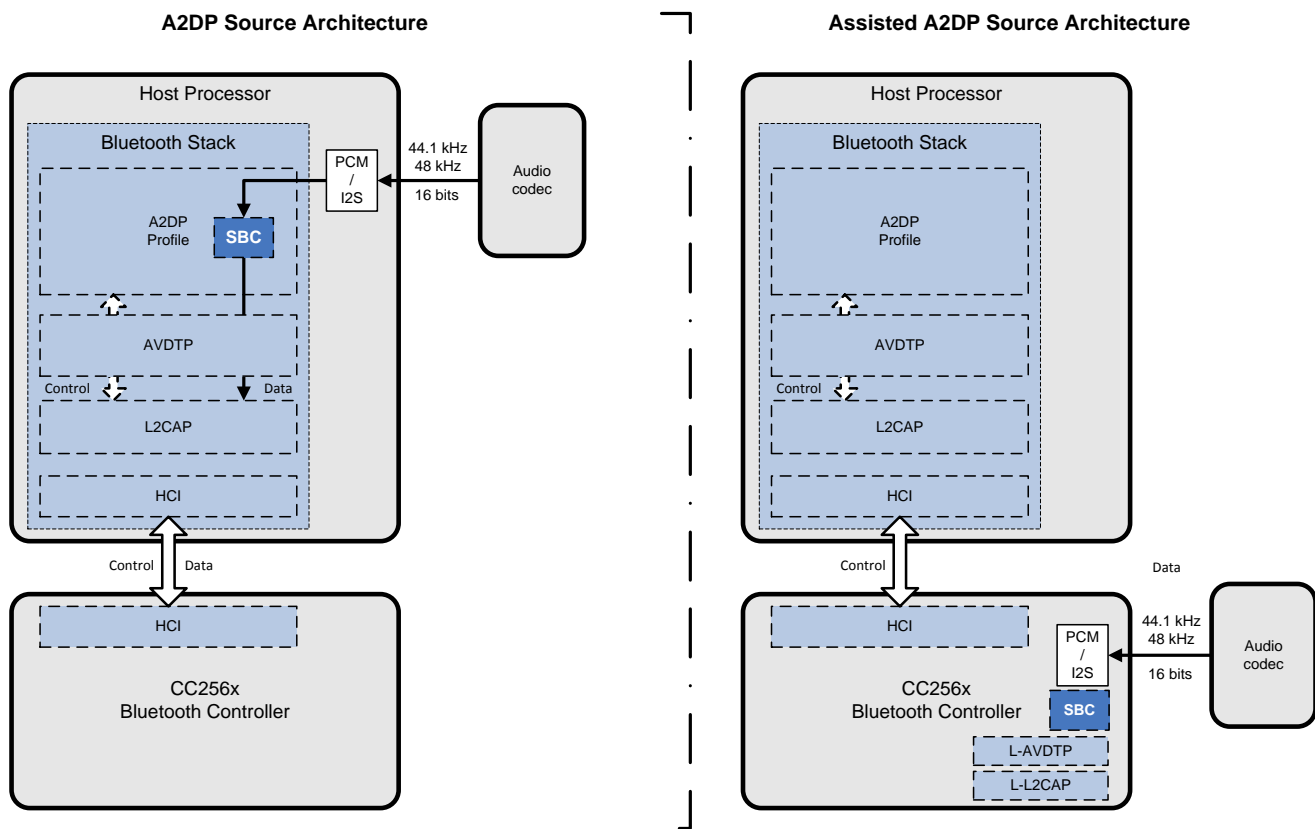
For more information on the A2DP sink role, see the *A2DP Profile Specification* at [Adopted Bluetooth Core Specifications](#).

#### 6.4.4.2.2 Assisted A2DP Source

The role of the A2DP source is to transmit the audio stream in an A2DP Bluetooth connection. In this role, the A2DP layer and its underlying layers are responsible for link management and data encoding. To handle these tasks, two logic transports are defined:

- Control and signaling logic transport
- Data packet logic transport

The assisted A2DP takes advantage of this modularity to handle the data packet logic transport in the CC2564C device. First, the assisted A2DP encodes the raw data from the CC2564C PCM–I2S interface using an on-chip SBC encoder. Then the assisted A2DP implements an L-L2CAP layer and an L-AVDTP layer to fragment and packetize the encoded audio data. [Figure 6-17](#) shows the comparison between a common A2DP source architecture and the assisted A2DP source architecture.



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**Figure 6-17. A2DP Source Architecture Versus Assisted A2DP Source Architecture**

For more information on the A2DP source role, see the A2DP Profile Specification at [Adopted Bluetooth Core Specifications](#).

## 6.5 Bluetooth BR and EDR Features

The CC2564C device complies with the *Bluetooth* 4.2 specification up to the HCI layer (for family members and technology supported, see [Table 3-1](#)):

- Up to seven active devices
- Scatternet: Up to three piconets simultaneously, one as master and two as slaves
- Up to two SCO links on the same piconet
- Very fast AFH algorithm for asynchronous connection-oriented link (ACL) and eSCO link
- Supports typical 12-dBm TX power without an external power amplifier (PA), thus improving Bluetooth link robustness
- DRP single-ended 50-Ω I/O for easy RF interfacing
- Internal temperature detection and compensation to ensure minimal variation in RF performance over temperature
- Includes a 128-bit hardware encryption accelerator as defined by the Bluetooth specifications

- Flexible PCM and I2S digital codec interface:
  - Full flexibility of data format (linear, A-Law,  $\mu$ -Law)
  - Data width
  - Data order
  - Sampling
  - Slot positioning
  - Master and slave modes
  - High clock rates up to 15 MHz for slave mode (or 4.096 MHz for master mode)
- Support for all voice air-coding
  - CVSD
  - A-Law
  - $\mu$ -Law
  - Transparent (uncoded)
  - mSBC
- The CC2564C device provides an assisted mode for the HFP 1.6 (wideband speech [WBS]) profile or A2DP profile to reduce host processing and power.

## 6.6 Bluetooth low energy Description

The CC2564C device complies with the Bluetooth 4.2 specification up to the HCI layer (for the family members and technology supported, see [Table 3-1](#)):

- Solution optimized for proximity and sports use cases
- Supports up to 10 simultaneous connections
- Multiple sniff instances that are tightly coupled to achieve minimum power consumption
- Independent buffering for low energy, allowing large numbers of multiple connections without affecting BR or EDR performance
- Built-in coexistence and prioritization handling

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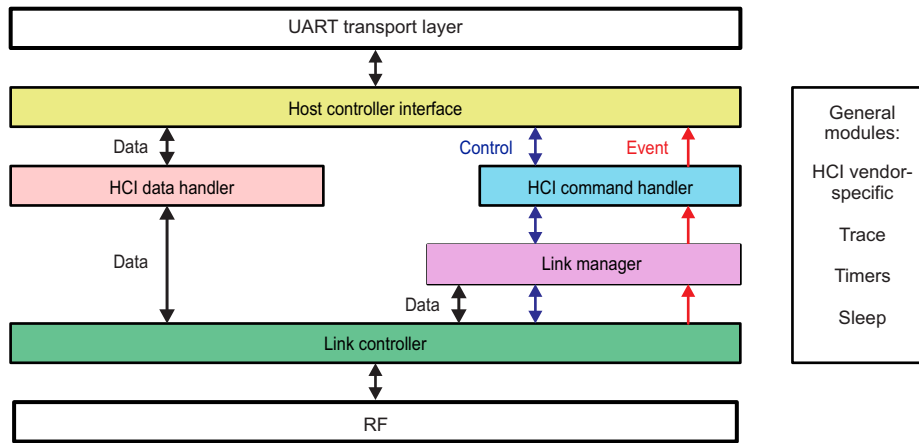
### NOTE

The assisted modes (HFP 1.6 and A2DP) are not available when Bluetooth low energy is enabled.

---

## 6.7 Bluetooth Transport Layers

Figure 6-18 shows the Bluetooth transport layers.



SWRS121-016  
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**Figure 6-18. Bluetooth Transport Layers**

## 6.8 Changes from the CC2564B Device to the CC2564C Device

The CC2564C device includes the following changes:

- Support added for standard HCI command for WBS to replace HCI VS command sequence
  - Part of the Core Specification Addendum 2 (CSA2)
- Easy PCM interface integration when using both WBS (16 kHz) and NBS (8 kHz)
- PLC support added for NBS (8 kHz) when working at 16-kHz PCM clock
- Option added to start and stop the PCM clock as master on the PCM bus even when voice call is not active or set a timer to extend the clock after voice or audio is removed
- Link layer topology support—Acts concurrently as peripheral and central low-energy device
- AFH algorithm enhancements—Improvements to the automatic frequency hopping algorithms



## 7 Applications, Implementation, and Layout

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### NOTE

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

---

### 7.1 Reference Design Schematics and BOM for Power and Radio Connections

[Figure 7-1](#) shows the reference schematics for the VQFN-MR package. For complete schematics and PCB layout guidelines, contact your TI representative.

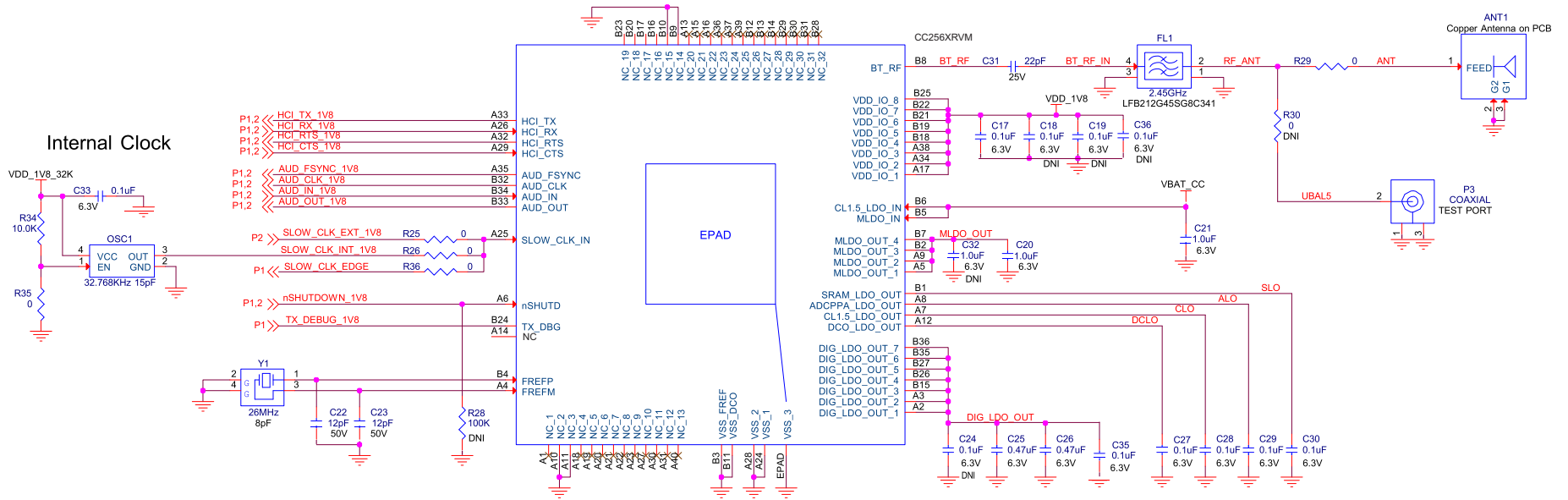


Figure 7-1. Reference Schematics

Table 7-1 lists the BOM for the VQFN-MR package.

**Table 7-1. Bill of Materials**

| QTY | REF. DES. | VALUE            | DESCRIPTION  | MANUFACTURER                     | MANUFACTURER PART NUMBER            | ALT PART                  | NOTES                  |
|-----|-----------|------------------|--|----------------------------------|-------------------------------------|---------------------------|------------------------|
| 1   | ANT1      | NA               | ANT_IIFA_CC2420_32mil_MIR                                  | NA                               | IIFA_CC2420                         | Chip antenna              | Copper antenna on PCB  |
| 6   | Capacitor | 0.1 $\mu$ F      | Capacitor, ceramic; 0.1- $\mu$ F 6.3-V 10% X7R 0402        | Kemet                            | C0402C104K9RACTU                    |                           |                        |
| 2   | Capacitor | 1.0 $\mu$ F      | Capacitor, ceramic; 1.0- $\mu$ F 6.3-V 10% X5R 0402        | Taiyo Yuden                      | JMK105BJ105KV-F                     |                           |                        |
| 2   | Capacitor | 12 pF            | Capacitor, ceramic; 12 pF 6.3-V X5R 10% 0402               | Murata Electronics               | GRM1555C1H120JZ01D                  |                           |                        |
| 2   | Capacitor | 0.47 $\mu$ F     | Capacitor, ceramic; 0.47- $\mu$ F 6.3-V X5R $\pm$ 10% 0402 | Taiyo Yuden                      | JMK105BJ474KV-F                     |                           |                        |
| 1   | FL1       | 2.45 GHz         | Filter, ceramic bandpass, 2.45-GHz SMD                     | Murata Electronics               | LFB212G45SG8C341                    | DEA162450 BT_1260B3 (TDK) | Place brown marking up |
| 1   | OSC1      | 32.768 kHz 15 pF | Oscillator; 32.768-kHz 15-pF 1.5-V 3.3-V SMD               | Abracon Corporation              | ASH7K-32.768KHZ-T                   |                           | Optional               |
| 1   | U5        | CC2564CRVM       | CC2564C dual-mode Bluetooth controller                     | Texas Instruments                | CC2564CRVM                          |                           |                        |
| 1   | Y1        | 26 MHz           | Crystal, 26 MHz  | NDK                              | NX2016SA                            | TZ1325D (Tai-Saw TST)     |                        |
| 1   | C31       | 22 pF            | Capacitor, ceramic; 22-pF 25-V 5% NP0 0201                 | Murata Electronics North America | GRM0335C1E220JD01D (EXS00A-CS06025) |                           |                        |

## 7.2 PCB Layout Guidelines

This section describes the PCB guidelines to speed up the PCB design using the CC256x VQFN device. Following these guidelines ensures that the design will pass Bluetooth SIG certification and also minimizes risk for regulatory certifications including FCC, ETSI, and CE. For more information, see [CC256x QFN PCB Guidelines](#).

### 7.2.1 General PCB Guidelines

General PCB guidelines follow:

- You must verify the recommended PCB stackup in the PCB Design guidelines.
- You must verify the dimensions of the QFN PCB footprint in the *QFN Package Information* section of [CC256x QFN PCB Guidelines](#) and in [Section 6](#).
- The decoupling capacitors must be as close as possible to the QFN device.

## 7.2.2 Power Supply Guidelines

Guidelines for the power supply follow:

- The trace width must be at least 10 mils for the VBAT and VIO traces.
- The length of the traces must be as short as possible (pin to pin).
- Decoupling capacitors must be as close as possible to the QFN device:
  - The MLDO\_IN capacitor must be close to pin B5.
  - The VDD\_IO capacitor must be close to pins B18 and A17.

Guidelines for the LDOs follow:

- The trace width for the trace between x\_LDO\_x pins and decoupling capacitors is at least 5 mils; where possible, the recommended trace width is 10 mils.
- Place the decoupling capacitor of MLDO\_OUT (C20) as close as possible to pin A5.
- These capacitors must close to the following pins:
  - The DIG\_LDO\_OUT capacitor must be close to ball B15.
  - The DIG\_LDO\_OUT capacitor must be close to ball B27.
  - The DIG\_LDO\_OUT capacitor must be close to ball B36.
- The DIG\_LDO\_OUT capacitor connected to ball B36 must be isolated from the top layer GND (see the *Low-Dropout Capacitors* section in [CC256x QFN PCB Guidelines](#)).
- The decoupling capacitors for SRAM, ADCPPA, and CL1.5 LDO\_OUT must be as close as possible to their corresponding pins on the CC256x device.
- Place the device and capacitors together on the top side.
- The ground connection of each capacitor must be directly connected to solid ground layer (layer 2).
- The capacitor that is directly connected to pin A12 should be close to the device.
- Connect the DCO\_LDO\_OUT capacitor isolated from layer 1 ground directly to layer 2 solid ground.

Guidelines for the ground layer follow:

- Layer 2 must be a solid ground plane.
- Isolate VSS\_FREF from ground on the top layer and route it directly to ground on the second layer (see the *Key VSS Ball* section in [CC256x QFN PCB Guidelines](#)).
- Isolate VSS\_DCO (ball B11) from ground. Include VSS\_DCO in the illustration of the DCO\_LDO\_OUT capacitor (see the *DCO\_LDO\_OUT* section in [CC256x QFN PCB Guidelines](#)).
- A minimum of 13 vias on the thermal pad are required to increase ground coupling.
- Connect VSS\_FREF (ball B3) directly to solid ground, not to the thermal pad.

### 7.2.3 User Interfaces

Guidelines for the UART follow:

- The trace width for the UART must be at least 5 mils.
- Run the four UART lines as a bus interface.
- Determine if clocks, DC supply, or RF traces are not near these UART traces.
- The ground plane on layer 2 is solid below these lines and there is ground around these traces on the top layer.

Guidelines for the PCM follow:

- The trace width for the PCM must be at least 5 mils.
- Run the four PCM lines as a bus interface and approximately the same length.
- Determine if clocks, DC supply, RF traces, and LDO capacitors are not near these PCM traces.
- The ground plane on layer 2 is solid below these lines and there is ground around these traces on the top layer.
- Guidelines for TX\_DBG follow:
- Check for an accessible test point on the board from TX\_DBG pin B24.

### 7.2.4 Clock Interfaces

Guidelines for the slow clock follow:

- The trace width for the slow clock must be at least 5 mils.
- The signal lines for the slow clock must be as short as possible.
- The ground plane on layer 2 is solid below these lines and there is ground around these traces on the top layer.

Guidelines for the fast clock follow:

- The trace width for the fast clock must be at least 5 mils.
- Ensure that crystal tuning capacitors are close to crystal pads.
- Make both traces (XTALM and XTALP) parallel as much as possible and approximately the same length.
- The ground plane on layer 2 is solid below these lines and there is ground around these traces on the top layer.

## 7.2.5 RF Interface

Guidelines for the RF Interface follow:

- TI recommends using an RF shield (not mandatory).
- Verify that RF traces are routed on the top layer and matched at 50  $\Omega$  with reference to ground.
- Route the RF line between these NC pins:
  - NC\_2 (A10)
  - NC\_3 (A11)
  - NC\_14 (B9)
  - NC\_15 (B10)

These NC pins are grounded for better RF isolation.

---

### NOTE

These pins are NC at the chip level, but TI recommends grounding them on the PCB layout for better RF isolation.

---

- Ensure the area underneath the BPF pads is grounded on layer 1 and layer 2.
- Keep RF\_IN and RF\_OUT of the BPF pads clear of any ground fill (see the *RF Trace* section in [CC256x QFN PCB Guidelines](#)).
- Follow guidelines specified in the vendor-specific antenna design guides (including placement of antenna).
- Follow guidelines specified in the vendor-specific BPF design guides.
- Verify that the Bluetooth RF trace is a 50- $\Omega$ , impedance-controlled trace with reference to solid ground.
- Ensure that the RF trace length is as short as possible.

## 8 Device and Documentation Support

### 8.1 Third-Party Products Disclaimer

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### 8.2 Tools and Software

#### Design Kits and Evaluation Modules

**CC256x Bluetooth® Hardware Evaluation Tool** This intuitive, user-friendly TI tool is used to evaluate TI's Bluetooth chips and can be downloaded as a complete package from the TI web site. More specifically, the tool is used to configure the properties of the Bluetooth chip through the Service Pack (SP) and also allows testing of RF performance.

For a complete listing of development-support tools, see the TI [CC256x wiki](#). For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

### 8.3 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers. These prefixes represent evolutionary stages of product development from engineering prototypes through fully qualified production devices.

Device development evolutionary flow:

- X** Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.
- P** Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.
- null** Production version of the silicon die that is fully qualified.

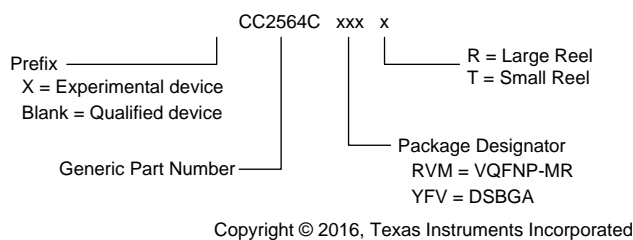
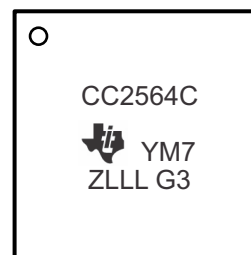


Figure 8-1. CC2564C Device Nomenclature



- Y = Last digit of the year
- M = Month in hex number, 1-C for Jan-Dec
- 7 = Primary site code for ANM
- Z = Secondary site code for ANM
- LLL = Assembly lot code
- = Pin 1 indicator

Figure 8-2. Chip Markings (VQFN-MR Package)

### 8.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** The TI engineer-to-engineer (E2E) community was created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge,

explore ideas and help solve problems with fellow engineers.

[TI Embedded Processors Wiki](#) Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

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iPod is a registered trademark of Apple, Inc.

Bluetooth is a registered trademark of Bluetooth SIG, Inc.

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## 8.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.



## 9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| CC2564CRVMR      | ACTIVE        | VQFNP-MR     | RVM             | 76   | 2500        | Green (RoHS & no Sb/Br) | CU SN                   | Level-3-260C-168 HR  | -40 to 85    | CC2564C                 | <a href="#">Samples</a> |
| CC2564CRVMT      | ACTIVE        | VQFNP-MR     | RVM             | 76   | 250         | Green (RoHS & no Sb/Br) | CU SN                   | Level-3-260C-168 HR  | -40 to 85    | CC2564C                 | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|-----|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CC2564CRVMT | VQFNPMR      | RVM             | 76   | 250 | 180.0              | 16.4               | 8.35    | 8.35    | 1.7     | 12.0    | 16.0   | Q2            |

TAPE AND REEL BOX DIMENSIONS

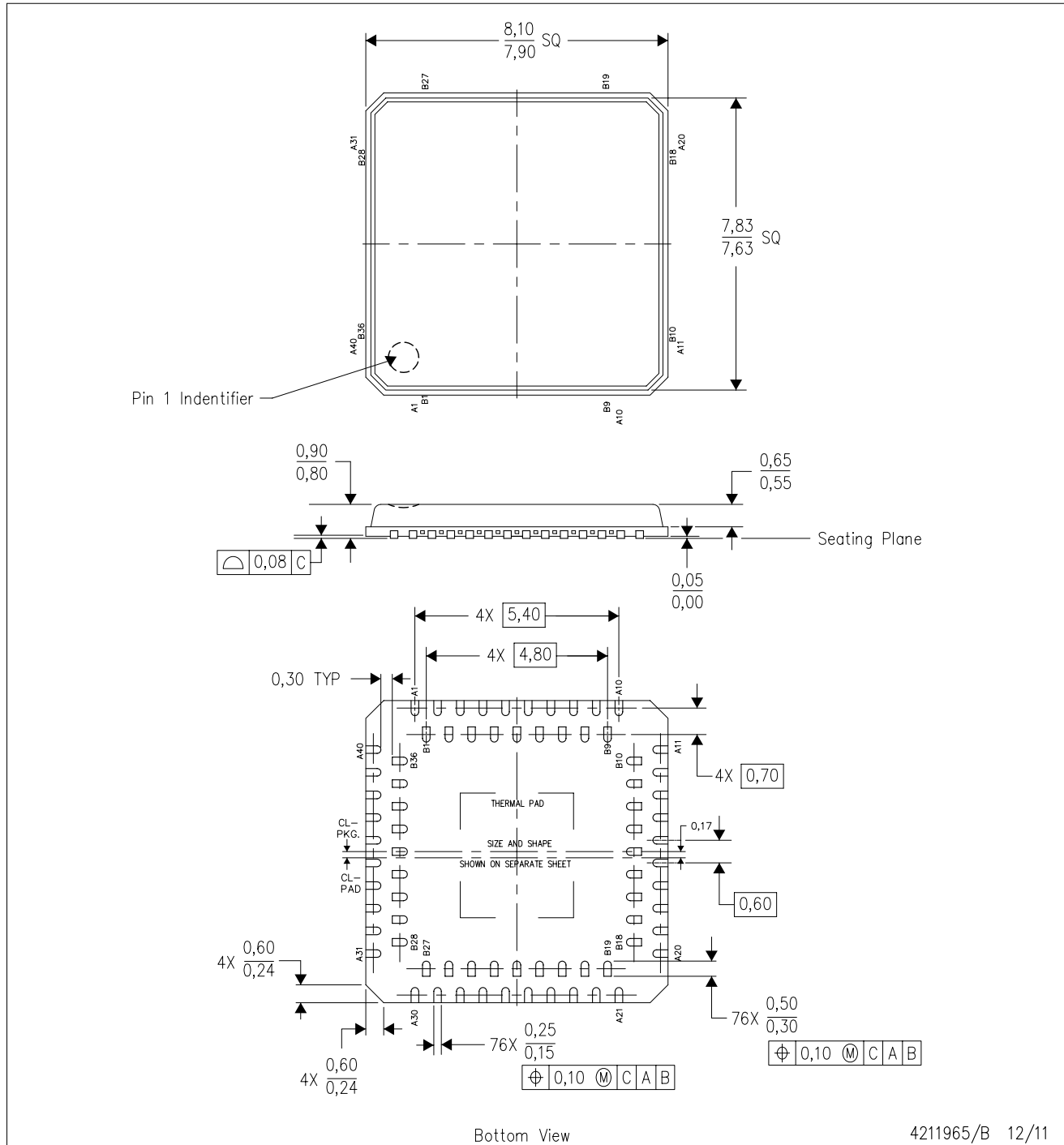


\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|-----|-------------|------------|-------------|
| CC2564CRVMT | VQFNP-MR     | RVM             | 76   | 250 | 213.0       | 191.0      | 55.0        |

RVM (S-PVQFN-N76)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) Package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

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TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.