



DESCRIPTION

The HSN75176ADR used for RS-485/RS-422 communication is a 10Mbps high-speed transceiver for half duplex communication, which includes one driver Device and a receiver.

Equipped with $\pm 8\text{kV}$ human mode ESD protection and failure protection circuit, ensuring that when the receiver input is open or short circuited Receiver output logic high level.

If all transmitters attached to the terminal matching bus are disabled (high resistance), the receiver will output logic high Level.

The HSN75176ADR driver does not limit the swing rate and can ensure a communication rate of up to 10Mbps.

HSN75176ADR has a receiver with 1 Unit load input impedance, up to 32 transceivers can be connected to the bus.

In addition, HSN75176ADR also has an built-in over-temperature protection circuit to ensure the chip is not damaged under high temperature conditions.

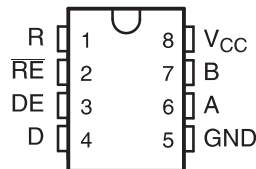
FEATURES

- Provide low current shutdown mode
- Provide industry standard 8-pin SOP packaging
- Up to 32 transceivers are allowed to be mounted on the bus
- True fail safe receiver compatible with EIA/TIA-485
- Built in over temperature protection circuit ensures that the chip is not damaged due to High temperatures
- Provide enhanced ESD protection for RS-485/RS-422 A/B pins

APPLICATIONS

- SCSI "Fast 40" Drivers and Receivers
- Motor Controller/Position Encoder Systems
- Factory Automation

PIN CONFIGURATION



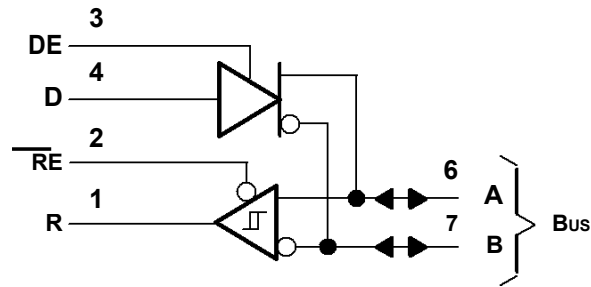
SOP-8

Pin Functions

| PIN | | I/O | DESCRIPTION |
|------------------------|-----|---------------------|--|
| NAME | NO. | | |
| A | 6 | Bus input/output | Driver output or receiver input (complementary to B) |
| B | 7 | Bus input/output | Driver output or receiver input (complementary to A) |
| D | 4 | Digital input | Driver data input |
| DE | 3 | Digital input | Active-HIGH driver enable |
| GND | 5 | Reference potential | Local device ground |
| R | 1 | Digital output | Receiver data output |
| $\overline{\text{RE}}$ | 2 | Digital input | Active-LOW receiver enable |
| V _{CC} | 8 | Supply | 4.75-V to 5.25-V supply |



LOGIC DIAGRAM



FEATUER DESCRIPTION

DRIVER FUNCTION TABLE

| INPUT D | ENABLE DE | OUTPUTS | |
|------------|--------------|---------|---|
| | | A | B |
| H | H | H | L |
| L | H | L | H |
| X | L | Z | Z |

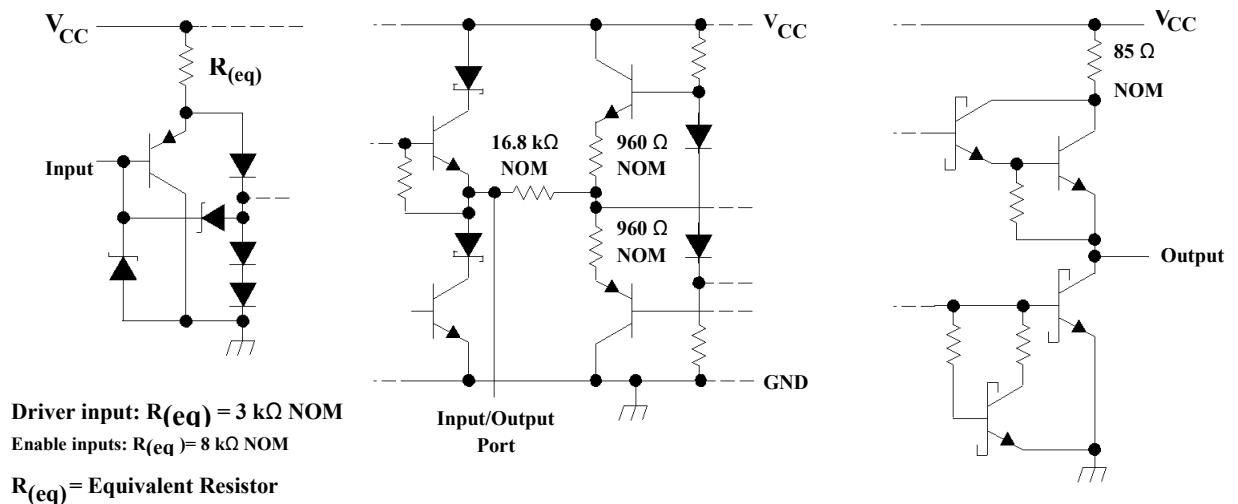
H = high level,
L = low level,
X = irrelevant,
Z = high impedance (off)

RECEIVER FUNCTION TABLE

| DIFFERENTIAL INPUTS A-B | ENABLE RE | OUTPUT R |
|-------------------------------|--------------|-------------|
| $V_{ID} \geq 0.2 V$ | L | H |
| $-0.2 V < V_{ID} < 0.2 V$ | L | ? |
| $V_{ID} \leq -0.2 V$ | L | L |
| X | H | Z |
| Open | L | ? |

H = high level,
L = low level,
? = indeterminate,
X = irrelevant,
Z = high impedance (off)

EQUIVALENT OF EACH INPUT





ABSOLUTE MAXIMUM RATINGS

($V_{CC} = 5V \pm 5\%$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)
over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|---------------|--|-----|-----|------|
| V_{CC} | Supply voltage ⁽²⁾ | | 7 | V |
| | Voltage range at any bus terminal | -10 | 15 | V |
| V_I | Enable input voltage | | 5.5 | V |
| θ_{JA} | Package thermal impedance ⁽³⁾⁽⁴⁾ | | 85 | °C/W |
| T_J | Operating virtual junction temperature | | 150 | °C |
| | Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | | 260 | °C |
| T_{stg} | Storage temperature range | -65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.
- (3) Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} - T_A) / \theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNIT |
|-------------------|---|----------------------------|-----|------|------|
| V_{CC} | Supply voltage | 4.75 | 5 | 5.25 | V |
| V_I or V_{IC} | Voltage at any bus terminal (separately or common mode) | | | 12 | V |
| | | | | -7 | V |
| V_{IH} | High-level input voltage | D, DE, and \overline{RE} | | | V |
| V_{IL} | Low-level input voltage | D, DE, and \overline{RE} | | 0.8 | V |
| V_{ID} | Differential input voltage ⁽¹⁾ | | | ±12 | V |
| I_{OH} | High-level output current | Driver | | -60 | mA |
| | | Receiver | | -400 | µA |
| I_{OL} | Low-level output current | Driver | | 60 | mA |
| | | Receiver | | 8 | mA |
| T_A | Operating free-air temperature | 0 | | 70 | °C |

- (1) Differential input/output bus voltage is measured at the noninverting terminal A, with respect to the inverting terminal B.



DRIVER SECTION Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| SYMBOL | PARAMETER | TEST CONDITIONS ⁽¹⁾ | MIN | TYP ⁽²⁾ | MAX | UNIT | |
|------------------|---|-----------------------------------|-----------------------------------|--------------------|-----------|---------------|----|
| V_{IK} | Input clamp voltage | $I_I = -18 \text{ mA}$ | | | -1.5 | V | |
| V_O | Output voltage | $I_O = 0$ | 0 | | 6 | V | |
| $ V_{OD1} $ | Differential output voltage | $I_O = 0$ | 1.5 | 3.6 | 6 | V | |
| $ V_{OD2} $ | Differential output voltage | $R_L = 100 \Omega$ | $1/2 V_{OD1}$ or 2 ⁽³⁾ | | | | |
| | | $R_L = 54 \Omega$ | 1.5 | 2.5 | 5 | V | |
| V_{OD3} | Differential output voltage | See ⁽⁴⁾ | 1.5 | | 5 | V | |
| $\Delta V_{OD} $ | Change in magnitude of differential output voltage ⁽⁵⁾ | $R_L = 54 \Omega$ or 100Ω | | | ± 0.2 | V | |
| V_{OC} | Common-mode output voltage | $R_L = 54 \Omega$ or 100Ω | | | +3 -1 | V | |
| $\Delta V_{OC} $ | Change in magnitude of common-mode output voltage ⁽⁵⁾ | $R_L = 54 \Omega$ or 100Ω | | | ± 0.2 | V | |
| I_O | Output current | Output disabled ⁽⁶⁾ | $V_O = 12 \text{ V}$ | | 1 | mA | |
| | | | $V_O = -7 \text{ V}$ | | -0.8 | | |
| I_{IH} | High-level input current | $V_I = 2.4 \text{ V}$ | | | 20 | μA | |
| I_{IL} | Low-level input current | $V_I = 0.4 \text{ V}$ | | | -400 | μA | |
| I_{OS} | Short-circuit output current | $V_O = -7 \text{ V}$ | | | -250 | mA | |
| | | $V_O = 0$ | | | -150 | | |
| | | $V_O = V_{CC}$ | | | 250 | | |
| | | $V_O = 12 \text{ V}$ | | | 250 | | |
| I_{CC} | Supply current (total package) | No load | Outputs enabled | | 42 | 70 | mA |
| | | | Outputs disabled | | 26 | 35 | |

- (1) The power-off measurement in ANSI Standard TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.
- (2) All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^\circ\text{C}$.
- (3) The minimum V_{OD2} with a 100- Ω load is either $1/2 V_{OD1}$ or 2 V, whichever is greater.
- (4) See ANSI Standard TIA/EIA-485-A, Figure 3.5, Test Termination Measurement 2.
- (5) $|V_{OD}|$ and $|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} , respectively, that occur when the input is changed from a high level to a low level.
- (6) This applies for both power on and off; refer to ANSI Standard TIA/EIA-485-A for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal.

Switching Characteristics

$V_{CC} = 5 \text{ V}$, $R_L = 110 \Omega$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------|-------------------------------------|-------------------|-----|-----|-----|------|
| $t_{d(OD)}$ | Differential-output delay time | $R_L = 54 \Omega$ | | 15 | 22 | ns |
| $t_{t(OD)}$ | Differential-output transition time | $R_L = 54 \Omega$ | | 20 | 30 | ns |
| t_{PZH} | Output enable time to high level | | | 85 | 120 | ns |
| t_{PZL} | Output enable time to low level | | | 40 | 60 | ns |
| t_{PHZ} | Output disable time from high level | | | 150 | 250 | ns |
| t_{PLZ} | Output disable time from low level | | | 20 | 30 | ns |



Symbol Equivalents

| DATA SHEET PARAMETER | TIA/EIA-422-B | TIA/EIA-485-A |
|-------------------------|---------------------------|--|
| V_O | V_{oa}, V_{ob} | V_{oa}, V_{ob} |
| $ V_{OD1} $ | V_o | V_o |
| $ V_{OD2} $ | $V_t (R_L = 100 \Omega)$ | $V_t (R_L = 54 \Omega)$ |
| $ V_{OD3} $ | | V_t (test termination measurement 2) |
| $\Delta V_{OD} $ | $ V_t - \bar{V}_t $ | $ V_t - \bar{V}_t $ |
| V_{oc} | $ V_{os} $ | $ V_{os} $ |
| $\Delta V_{OC} $ | $ V_{os} - \bar{V}_{os} $ | $ V_{os} - \bar{V}_{os} $ |
| I_{os} | $ I_{sa} , I_{sb} $ | |
| I_O | $ I_{xa} , I_{xb} $ | I_{ia}, I_{ib} |

RECEIVER SECTION Electrical Characteristics

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT | |
|-----------|--|--|----------------------|--------------------|----------|---------------|------|
| V_{IT+} | Positive-going input threshold voltage | $V_O = 2.7 \text{ V}, I_O = -0.4 \text{ mA}$ | | | 0.2 | V | |
| V_{IT-} | Negative-going input threshold voltage | $V_O = 0.5 \text{ V}, I_O = 8 \text{ mA}$ | -0.2 ⁽²⁾ | | | V | |
| V_{hys} | Input hysteresis voltage ($V_{IT+} - V_{IT-}$) | | | 50 | | mV | |
| V_{IK} | Enable Input clamp voltage | $I_I = -18 \text{ mA}$ | | | -1.5 | V | |
| V_{OH} | High-level output voltage | $V_{ID} = 200 \text{ mV}, I_{OH} = -400 \mu\text{A}$ | 2.7 | | | V | |
| V_{OL} | Low-level output voltage | $V_{ID} = -200 \text{ mV}, I_{OL} = 8 \text{ mA}$ | | | 0.45 | V | |
| I_{OZ} | High-impedance-state output current | $V_O = 0.4 \text{ V to } 2.4 \text{ V}$ | | | ± 20 | μA | |
| I_I | Line input current | Other input = 0 V ⁽³⁾ | | | 1 | mA | |
| | | | $V_I = 12 \text{ V}$ | | | | -0.8 |
| I_{IH} | High-level enable input current | $V_{IH} = 2.7 \text{ V}$ | | | 20 | μA | |
| I_{IL} | Low-level enable input current | $V_{IL} = 0.4 \text{ V}$ | | | -100 | μA | |
| r_I | Input resistance | $V_I = 12 \text{ V}$ | 12 | | | k Ω | |
| I_{os} | Short-circuit output current | | -15 | | -85 | mA | |
| I_{CC} | Supply current (total package) | No load | Outputs enabled | | 42 | 55 | mA |
| | | | Outputs disabled | | 26 | 35 | |

(1) All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

(2) The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

(3) This applies for both power on and power off. Refer to EIA Standard TIA/EIA-485-A for exact conditions.

Switching Characteristics

$V_{CC} = 5 \text{ V}, C_L = 15 \text{ pF}, T_A = 25^\circ\text{C}$

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|---|--------------------------------------|-----|-----|-----|------|
| t_{PLH} | Propagation delay time, low- to high-level output | $V_{ID} = 0 \text{ to } 3 \text{ V}$ | | 21 | 35 | ns |
| t_{PHL} | Propagation delay time, high- to low-level output | | | 23 | 35 | |
| t_{PZH} | Output enable time to high level | | | 10 | 20 | ns |
| t_{PZL} | Output enable time to low level | | | 12 | 20 | |
| t_{PHZ} | Output disable time from high level | | | 20 | 35 | ns |
| t_{PLZ} | Output disable time from low level | | | 17 | 25 | |



Parameter Measurement Information

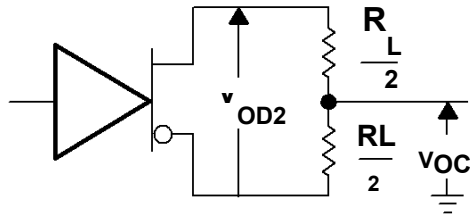


Figure 1. Driver V_{OD} and V_{OC}

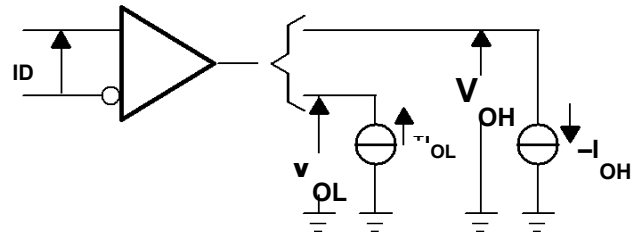
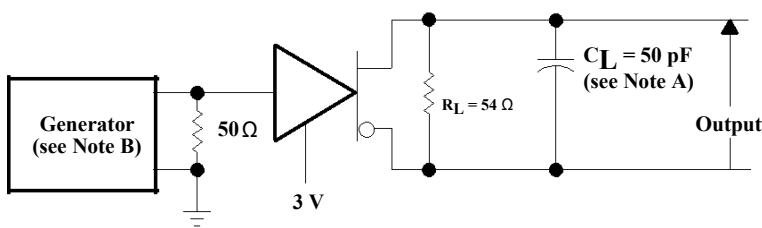
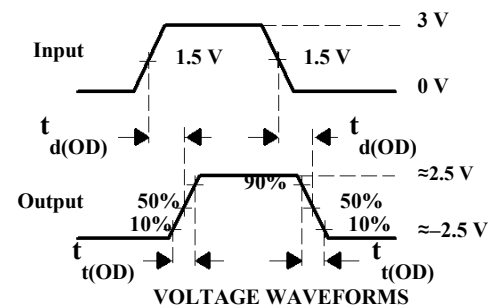


Figure 2. Receiver V_{OH} and V_{OL}



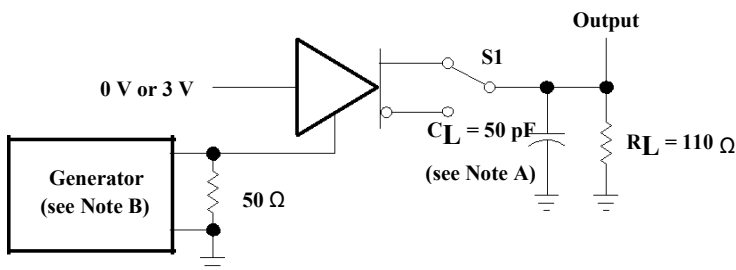
TEST CIRCUIT

- A. C_L includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_0 = 50 \Omega$.



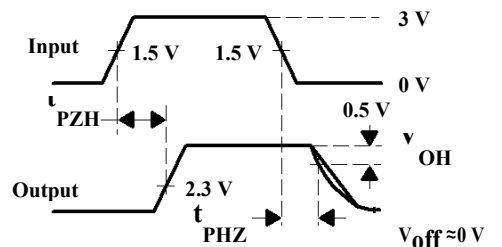
VOLTAGE WAVEFORMS

Figure 3. Driver Test Circuit and Voltage Waveforms



TEST CIRCUIT

- A. C_L includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_0 = 50 \Omega$.

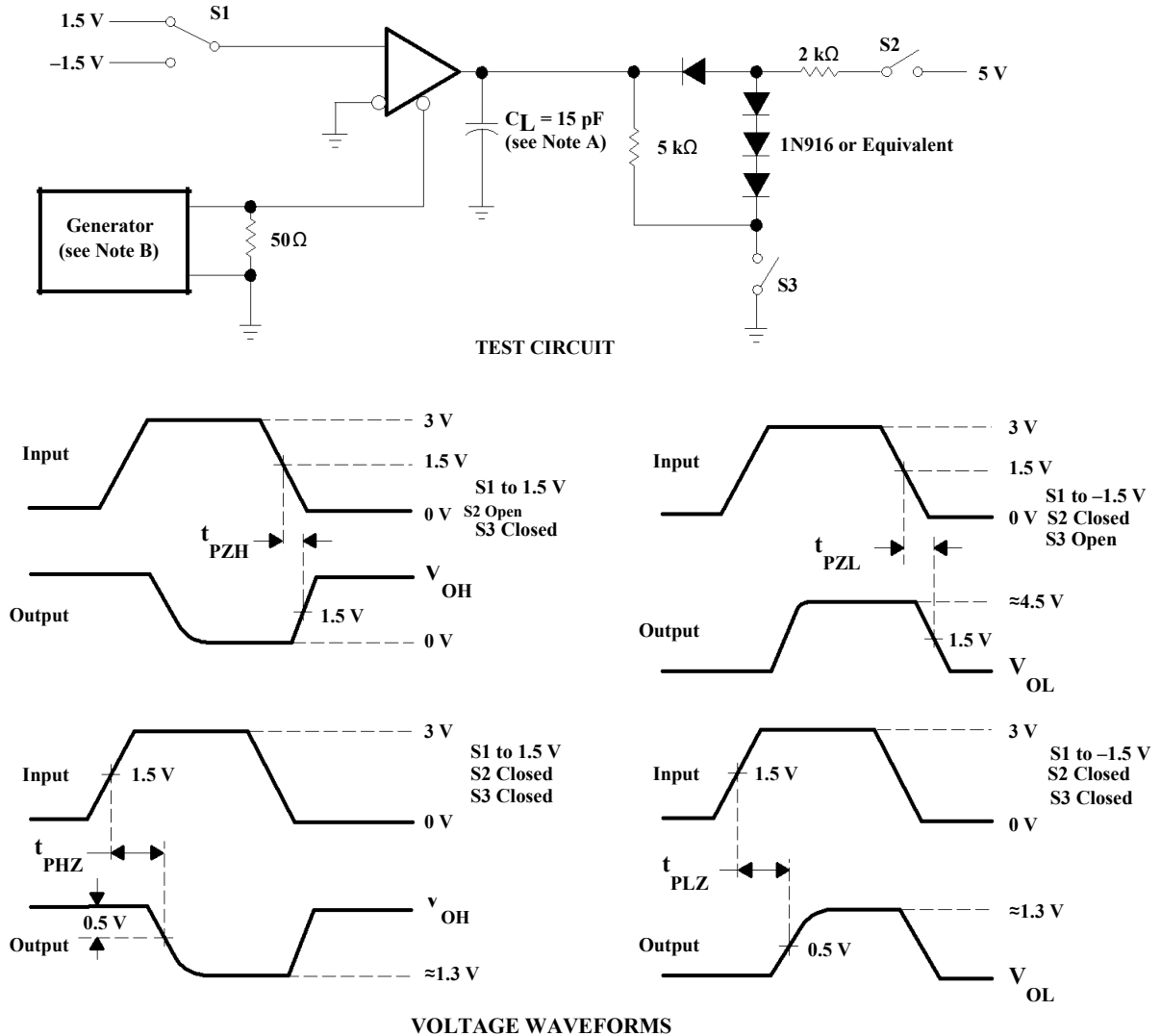


VOLTAGE WAVEFORMS

Figure 4. Driver Test Circuit and Voltage Waveforms

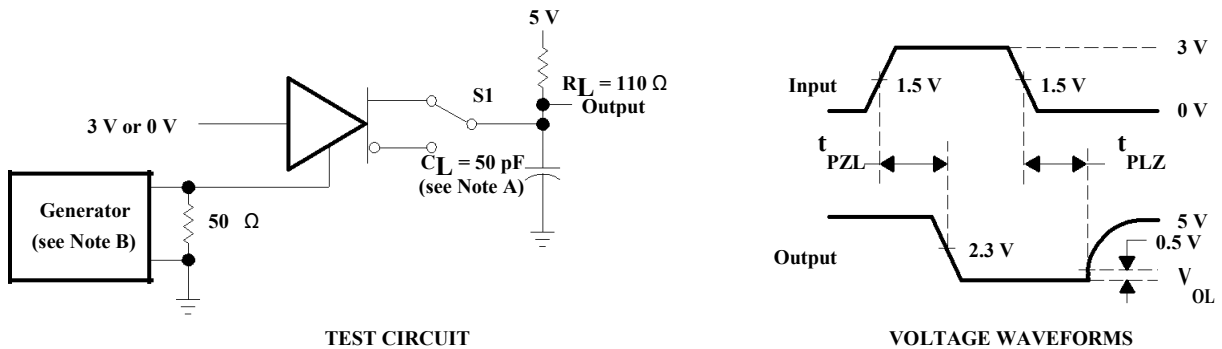


Parameter Measurement Information (continued)



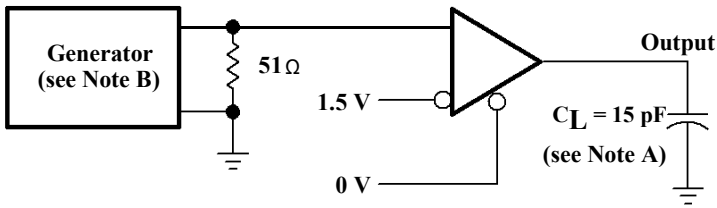
- A. C_L includes probe and jig capacitance.
 B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.

Figure 5. Receiver Test Circuit and Voltage Waveforms



- A. C_L includes probe and jig capacitance.
 B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.

Figure 6. Driver Test Circuit and Voltage Waveforms



TEST CIRCUIT

- A. C_L includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.

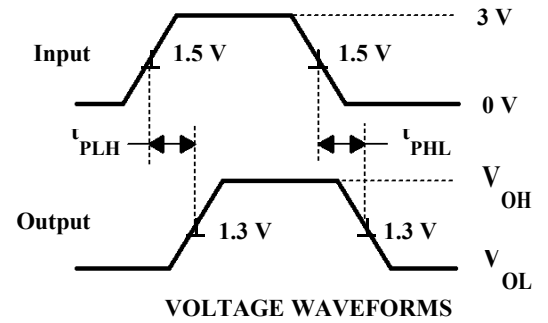


Figure 7. Receiver Test Circuit and Voltage Waveforms

TYPOCAL CHARACTERISTICS

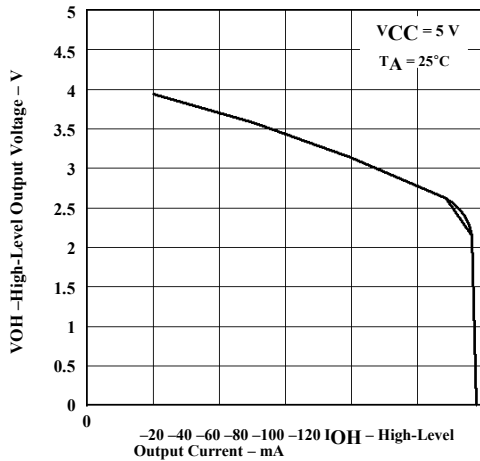


Figure 8. Driver High-Level Output Voltage vs High-Level Output Current

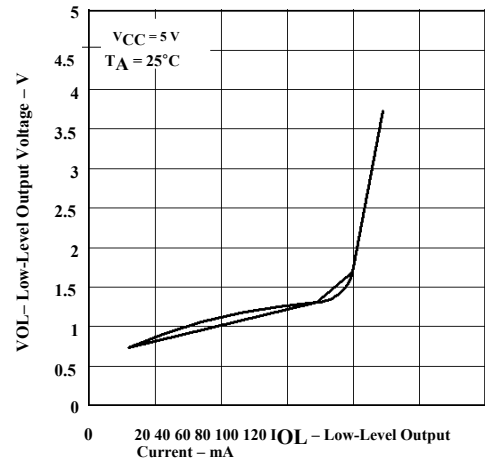


Figure 9. Driver Low-Level Output Voltage vs Low-Level Output Current

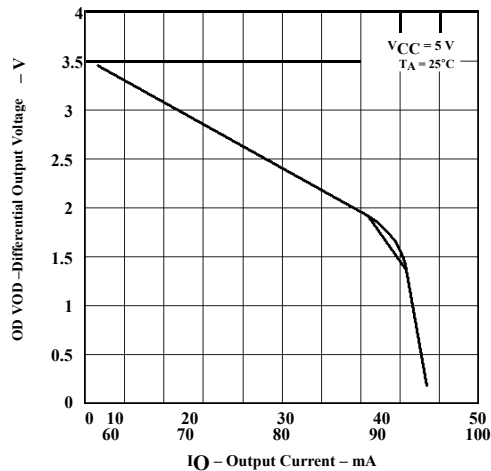


Figure 10. Driver Differential Output Voltage vs Output Current

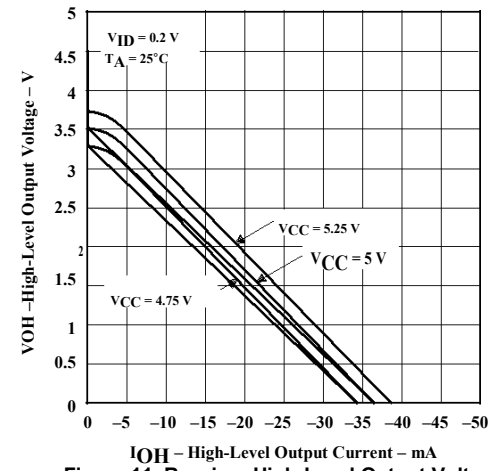


Figure 11. Receiver High-Level Output Voltage vs High-Level Output Current

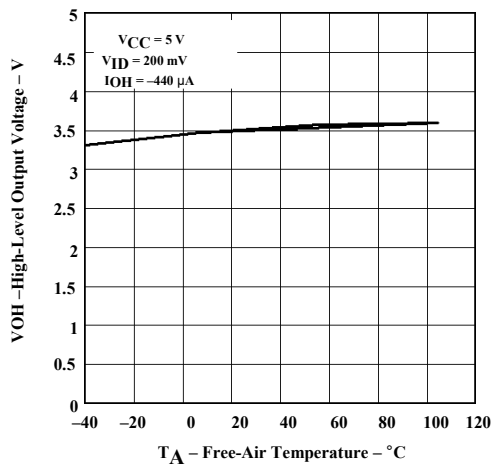


Figure 12. V_{OH} -High-Level Output Voltage vs Free-Air Temperature

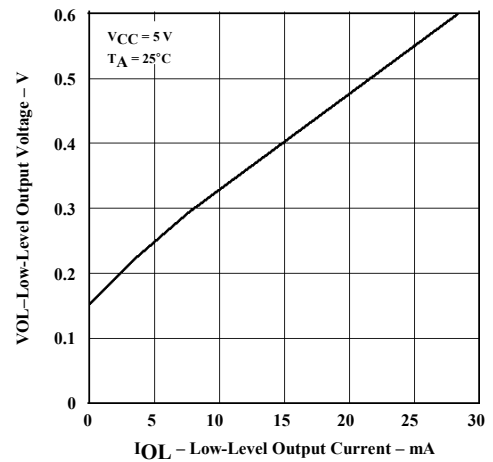


Figure 13. V_{OL} -Low-Level Output Voltage vs Low-Level Output Current

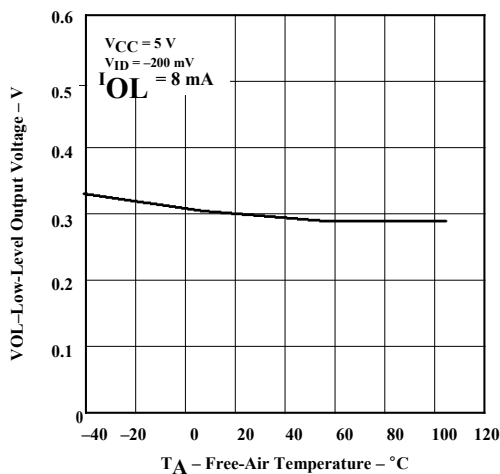


Figure 14. Receiver Low-Level Output Voltage vs Free-Air Temperature

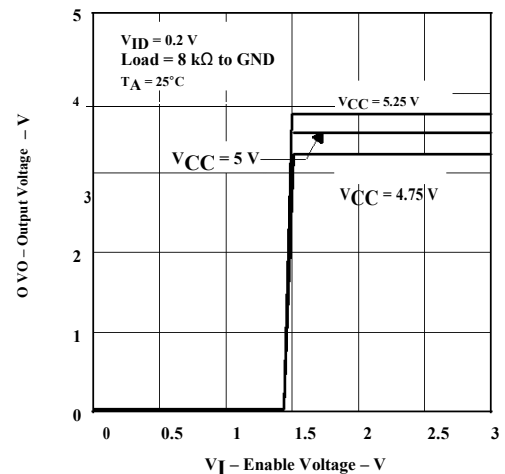


Figure 15. Receiver Output Voltage vs Enable Voltage

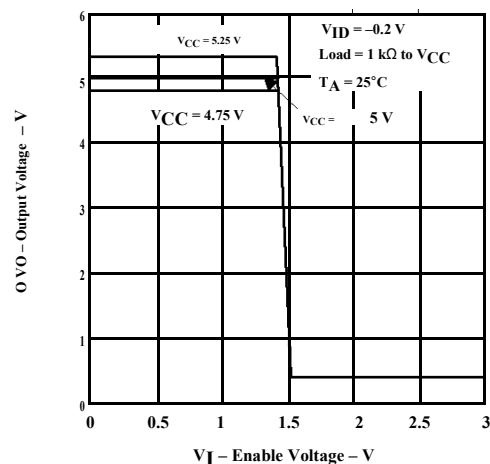
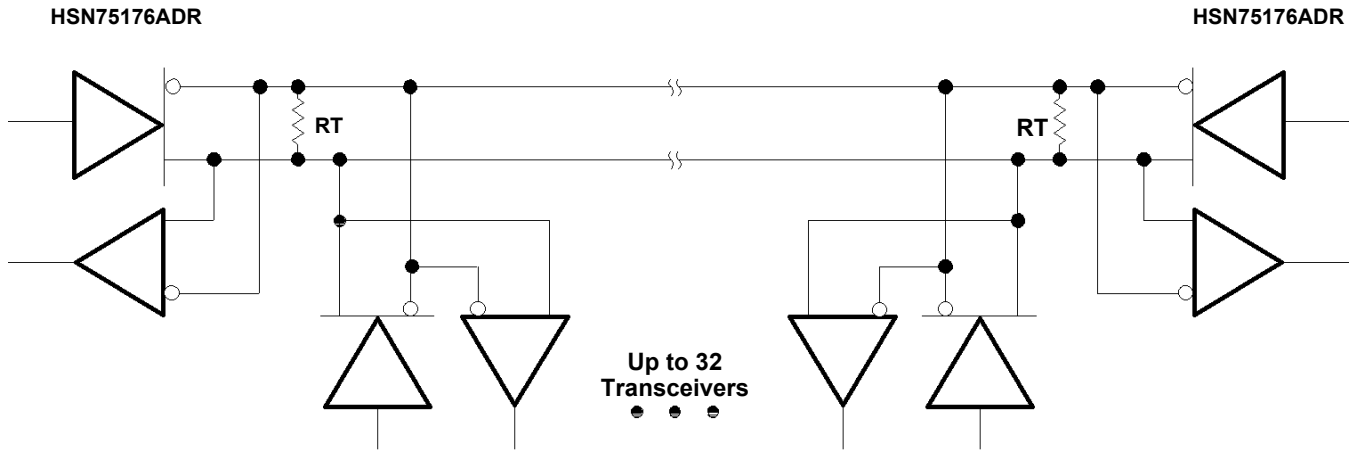


Figure 16. Receiver Output Voltage vs Enable Voltage



APPLICATION INFORMATION



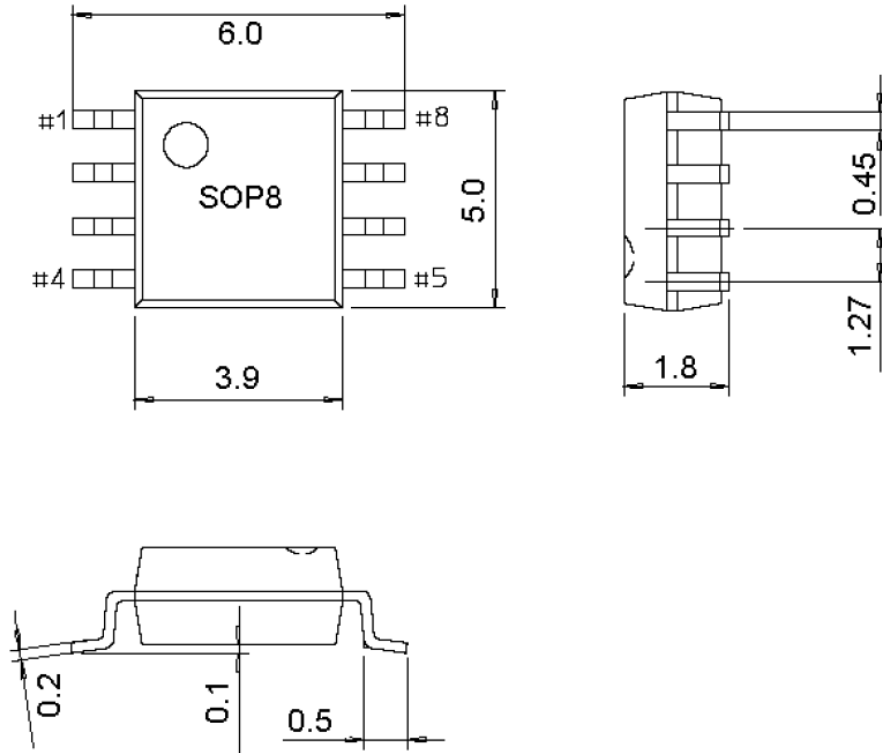
The line should be terminated at both ends in its characteristic impedance ($R_T = Z_0$). Stub lengths off the main line should be kept as short as possible.

Figure 17. Typical Application Circuit



PACKAGE OUTLINE DIMENSIONS

SOP-8





Attention

- Any and all HUA XUAN YANG ELECTRONICS products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your HUA XUAN YANG ELECTRONICS representative nearest you before using any HUA XUAN YANG ELECTRONICS products described or contained herein in such applications.
- HUA XUAN YANG ELECTRONICS assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all HUA XUAN YANG ELECTRONICS products described or contained herein.
- Specifications of any and all HUA XUAN YANG ELECTRONICS products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.
- HUA XUAN YANG ELECTRONICS CO.,LTD. strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all HUA XUAN YANG ELECTRONICS products(including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of HUA XUAN YANG ELECTRONICS CO.,LTD.
- Information (including circuit diagrams and circuit parameters) herein is for example only ; it is not guaranteed for volume production. HUA XUAN YANG ELECTRONICS believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the HUA XUAN YANG ELECTRONICS product that you intend to use.