



PEMD16

50 V, 100 mA NPN/PNP resistor-equipped double transistor;
R1 = 22 k Ω , R2 = 47 k Ω

28 December 2022

Product data sheet

1. General description

NPN/PNP double Resistor-Equipped Transistor (RET) in an ultra small and flat lead SOT666 Surface-Mounted Device (SMD) plastic package.

NPN/NPN complement: PEMH16

PNP/PNP complement: PEMB16

2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplified circuit design
- Reduces component count
- Reduces pick and place costs

3. Applications

- Low current peripheral driver
- Controlling IC inputs
- Replacement of general purpose transistors in digital applications

4. Quick reference data

Table 1. Quick reference data

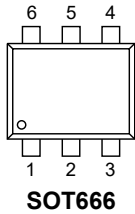
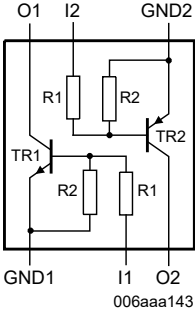
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor; for the PNP transistor with negative polarity						
V _{CEO}	collector-emitter voltage	open base	-	-	50	V
I _O	output current		-	-	100	mA
R1	bias resistor 1 (input)		[1]	22	28.6	k Ω
R2/R1	bias resistor ratio		[1]	2.1	2.6	

[1] See section "Test information" for resistor calculation and test conditions.

50 V, 100 mA NPN/PNP resistor-equipped double transistor; R1 = 22 k Ω , R2 = 47 k Ω

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1	 <p style="text-align: center;">SOT666</p>	
2	I1	input (base) TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input (base) TR2		
6	O1	output (collector) TR1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PEMD16	SOT666	plastic, surface-mounted package; 6 leads; 0.5 mm pitch; 1.6 mm x 1.2 mm x 0.55 mm body	SOT666

7. Marking

Table 4. Marking codes

Type number	Marking code
PEMD16	5H

50 V, 100 mA NPN/PNP resistor-equipped double transistor; R1 = 22 kΩ, R2 = 47 kΩ

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor; for the PNP transistor with negative polarity						
V _{CBO}	collector-base voltage	open emitter		-	50	V
V _{CEO}	collector-emitter voltage	open base		-	50	V
V _{EBO}	emitter-base voltage	open collector		-	5	V
V _I	input voltage	positive (input voltage TR1)		-	40	V
		negative (input voltage TR1)		-	-7	V
		positive (input voltage TR2)		-	7	V
		negative (input voltage TR2)		-	-40	V
I _O	output current			-	100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1] [2]	-	200	mW
Per device						
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1] [2]	-	300	mW
T _j	junction temperature			-	150	°C
T _{amb}	ambient temperature			-65	150	°C
T _{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[2] Reflow soldering is the only recommended soldering method.

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1] [2]	-	-	625	K/W
Per device							
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1] [2]	-	-	417	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Reflow soldering is the only recommended soldering method.

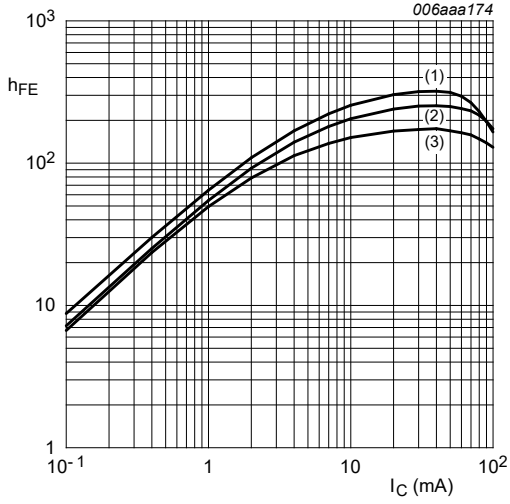
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor; for the PNP transistor with negative polarity						
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = 100 \mu\text{A}$; $I_E = 0 \text{ A}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	50	-	-	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$I_C = 2 \text{ mA}$; $I_B = 0 \text{ A}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	50	-	-	V
I_{CBO}	collector-base cut-off current	$V_{CB} = 50 \text{ V}$; $I_E = 0 \text{ A}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	-	-	100	nA
I_{CEO}	collector-emitter cut-off current	$V_{CE} = 30 \text{ V}$; $I_B = 0 \text{ A}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	-	-	1	μA
		$V_{CE} = 30 \text{ V}$; $I_B = 0 \text{ A}$; $T_j = 150 \text{ }^\circ\text{C}$	-	-	50	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5 \text{ V}$; $I_C = 0 \text{ A}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	-	-	120	μA
h_{FE}	DC current gain	$V_{CE} = 5 \text{ V}$; $I_C = 5 \text{ mA}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	80	-	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 10 \text{ mA}$; $I_B = 0.5 \text{ mA}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	-	-	150	mV
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5 \text{ V}$; $I_C = 100 \mu\text{A}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	-	0.8	0.5	V
$V_{I(on)}$	on-state input voltage	$V_{CE} = 0.3 \text{ V}$; $I_C = 2 \text{ mA}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	2	1.1	-	V
R1	bias resistor 1 (input)		[1]	22	28.6	k Ω
R2/R1	bias resistor ratio		[1]	2.1	2.6	
TR1 (NPN)						
C_c	collector capacitance	$V_{CB} = 10 \text{ V}$; $I_E = 0 \text{ A}$; $i_e = 0 \text{ A}$; $f = 1 \text{ MHz}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	-	-	2.5	pF
TR2 (PNP)						
C_c	collector capacitance	$V_{CB} = -10 \text{ V}$; $I_E = 0 \text{ A}$; $i_e = 0 \text{ A}$; $f = 1 \text{ MHz}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	-	-	3	pF

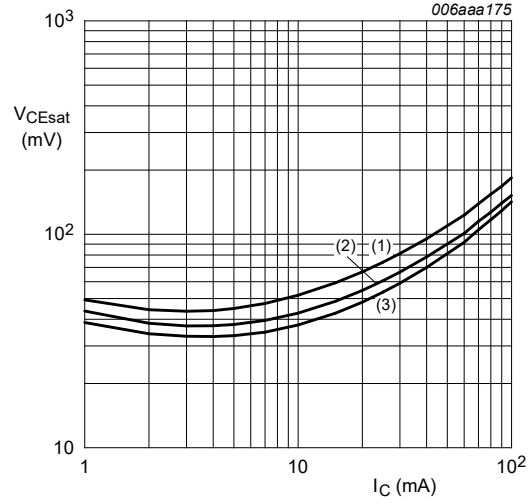
[1] See section "Test information" for resistor calculation and test conditions.

50 V, 100 mA NPN/PNP resistor-equipped double transistor; R1 = 22 kΩ, R2 = 47 kΩ



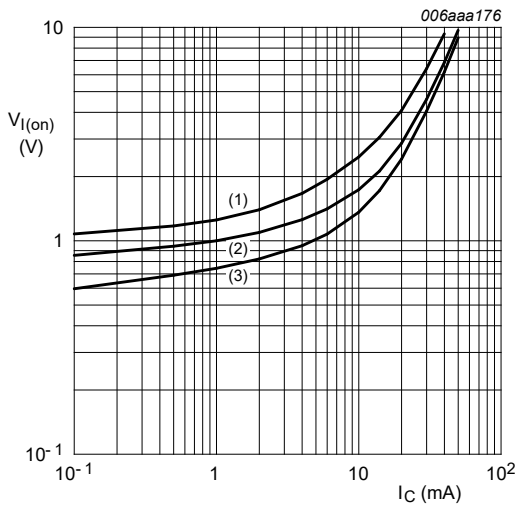
$V_{CE} = 5\text{ V}$
 (1) $T_{amb} = 100\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = -40\text{ °C}$

Fig. 1. TR1 (NPN): DC current gain as a function of collector current; typical values



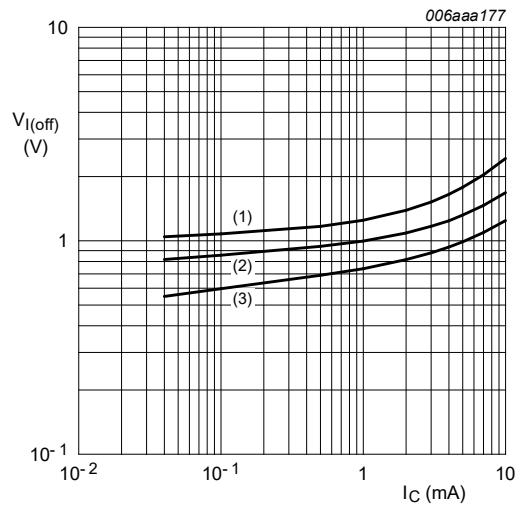
$I_C/I_B = 20$
 (1) $T_{amb} = 100\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = -40\text{ °C}$

Fig. 2. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



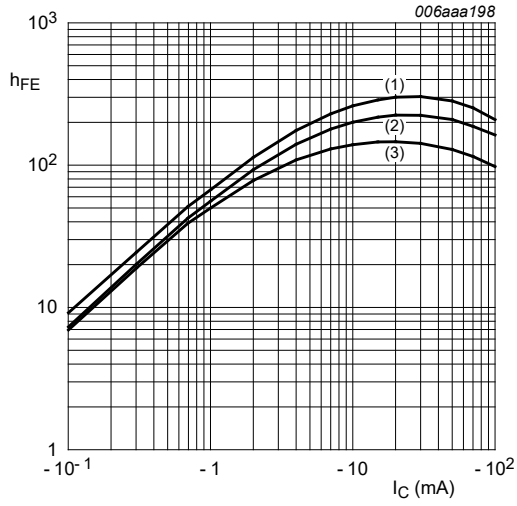
$V_{CE} = 0.3\text{ V}$
 (1) $T_{amb} = -40\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = 100\text{ °C}$

Fig. 3. TR1 (NPN): On-state input voltage as a function of collector current; typical values



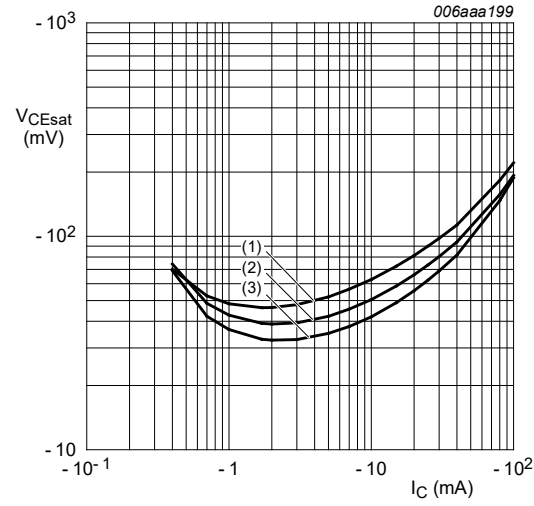
$V_{CE} = 5\text{ V}$
 (1) $T_{amb} = -40\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = 100\text{ °C}$

Fig. 4. TR1 (NPN): Off-state input voltage as a function of collector current; typical values



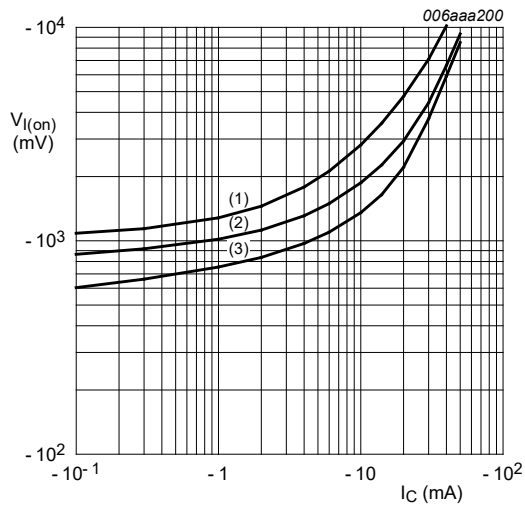
$V_{CE} = -5 \text{ V}$
 (1) $T_{amb} = 100 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = -40 \text{ }^\circ\text{C}$

Fig. 5. TR2 (PNP): DC current gain as a function of collector current; typical values



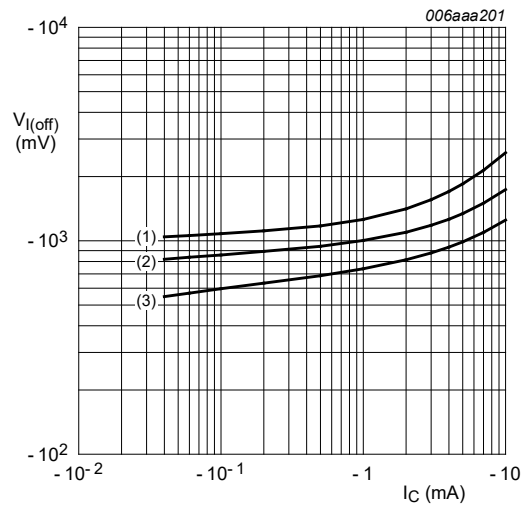
$I_C/I_B = 20$
 (1) $T_{amb} = 100 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = -40 \text{ }^\circ\text{C}$

Fig. 6. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



$V_{CE} = -0.3 \text{ V}$
 (1) $T_{amb} = -40 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

Fig. 7. TR2 (PNP): On-state input voltage as a function of collector current; typical values



$V_{CE} = -5 \text{ V}$
 (1) $T_{amb} = -40 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

Fig. 8. TR2 (PNP): Off-state input voltage as a function of collector current; typical values

11. Test information

Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R_1 = \frac{V(I_2) - V(I_1)}{I_2 - I_1}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R_2}{R_1} = \frac{V(I_3)}{R_1 \cdot I_3} - 1$$

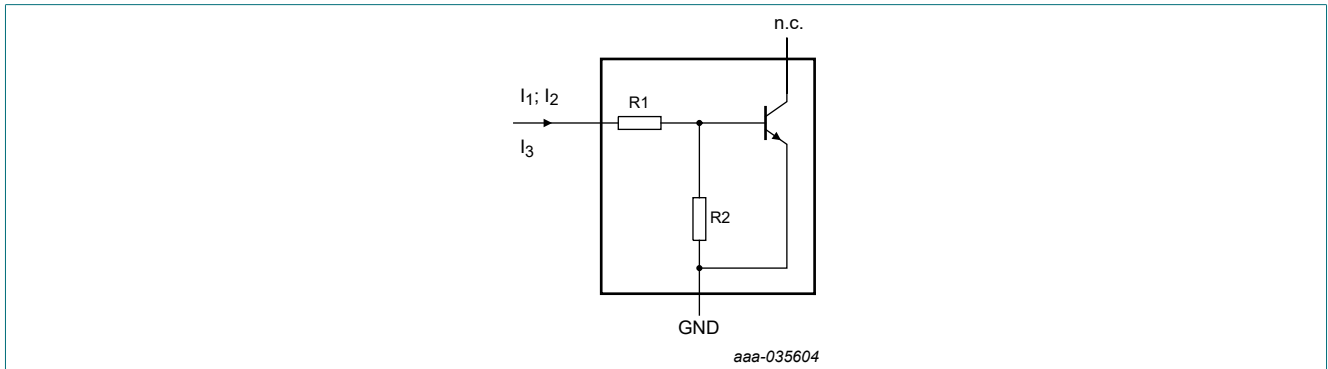


Fig. 9. NPN transistor: Resistor test circuit

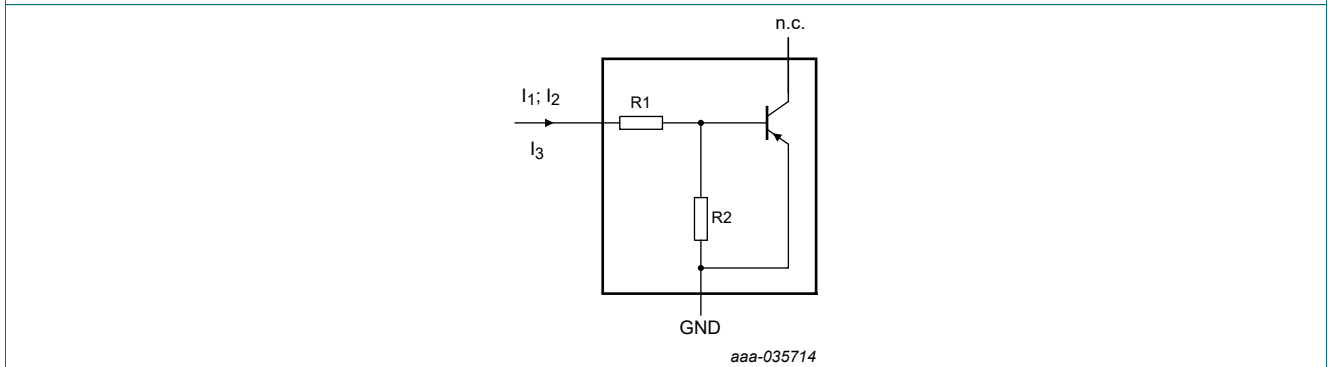


Fig. 10. PNP transistor: Resistor test circuit

Resistor test conditions

Table 8. Resistor test conditions

PEMD16	R1 (kΩ)	R2 (kΩ)	Test conditions		
			I ₁	I ₂	I ₃
TR1 (NPN)	22	47	160 μA	210 μA	-100 μA
TR2 (PNP)	22	47	-160 μA	-210 μA	100 μA

12. Package outline

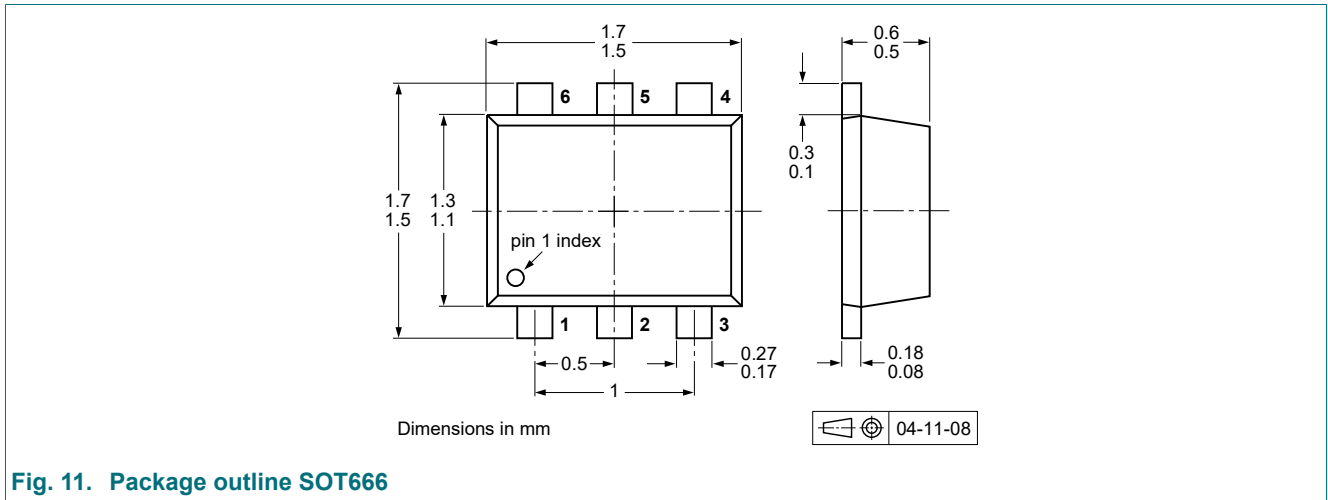


Fig. 11. Package outline SOT666

13. Soldering

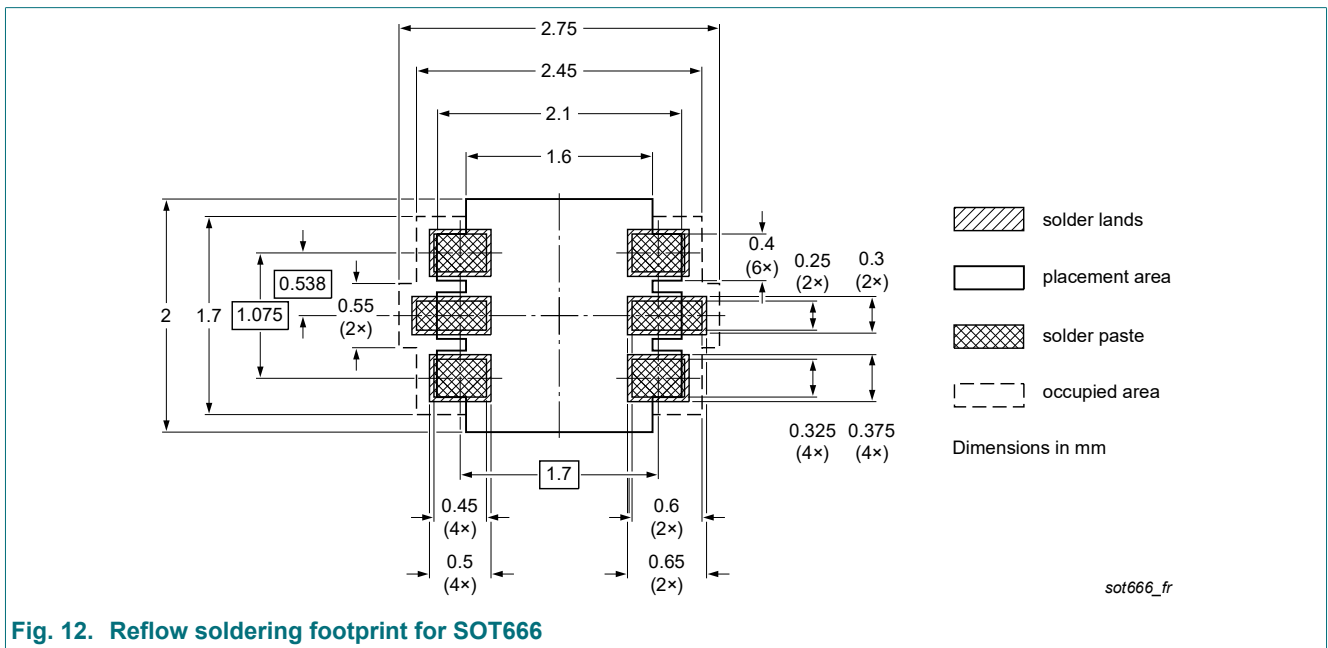


Fig. 12. Reflow soldering footprint for SOT666

50 V, 100 mA NPN/PNP resistor-equipped double transistor; R1 = 22 kΩ, R2 = 47 kΩ

14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PEMD16 v.4	20221228	Product data sheet	-	PEMD16_PUMD16 v.3
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Family data sheet reduced to single type data sheet. Packing information removed. Product(s) changed to non-automotive qualification. 			
PEMD16_PUMD16 v.3	20110628	Product data sheet	-	PEMD16_PUMD16 v.2
PEMD16_PUMD16 v.2	20050607	Product data sheet	-	PUMD16 v.1
PUMD16 v.1	20031022	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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