PS13201

500MHz 75dB Logarithmic/Limiting Amplifier

Data Sheet 210892 issue 3 Jul-12

FEATURES

- 75dB Dynamic Range
- Surface Mount SO Package
- Adjustable Log Slope and Offset
- 0dBm RF Limiting Output
- 60dBm Limiting Range
- 2V Video Output Range
- Low Power (Typ. 1W)
- Temperature Range (T_{CASE}) -55°C to +125°C

APPLICATIONS

- Ultra Wideband Log Receivers
- Channelised and Monopulse Radar
- Instrumentation

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±6.0V
Storage Temperature	-65°C to +175°C
Junction Temperature	+175°C
Thermal Resistance	
Die-to-case	15.5°C/W
Die-to-ambient	76.5°C/W
Applied DC voltage to RF input	±400mV
Applied RF power to RF input	+15dBm

Ordering Information

PS13201 M1C8A4 (Miniature Ceramic package in tubes)
PS13201 C1C8A4 (Miniature Ceramic package in tubes)
PS13201 (Probe-tested bare die)

Equivalent Parts: SL3522

DESCRIPTION

The PS13201 is a monolithic seven stage successive detection logarithmic amplifier integrated circuit for use in the 100MHz to 500MHz frequency range.
It features an on-chip video amplifier with provision for external adjustment of log slope and offset. It also features a balanced RF output. The PS13201 operates from supplies of ±5V.

ESD PROTECTION

To achieve the high frequency performance there are no ESD protection structures on the RF input pins (27, 28). These pins are **highly static sensitive**, typically measured as 250V using MIL-STD-883 method 3015. Therefore, ESD handling precautions are **essential** to avoid degradation of performance or permanent damage to this device.

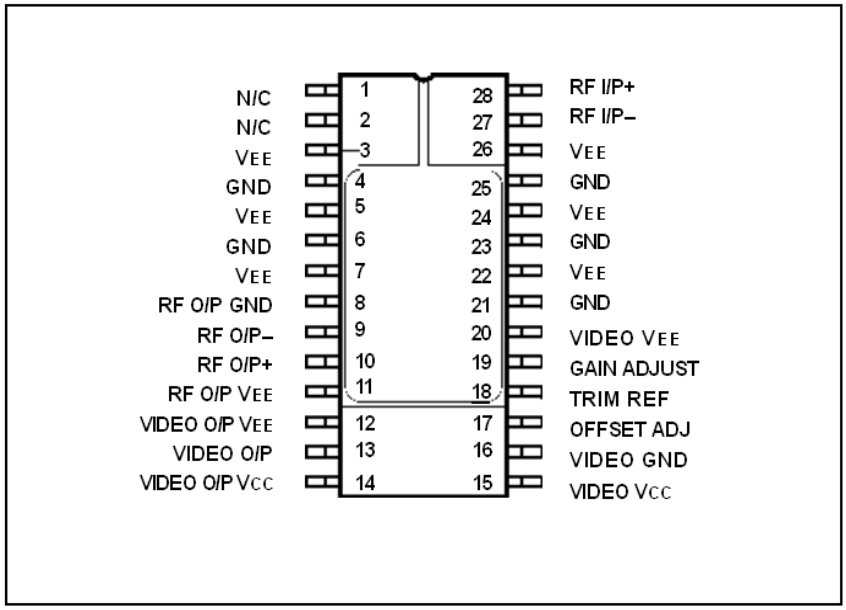

Fig. 1
Pin connections
top view

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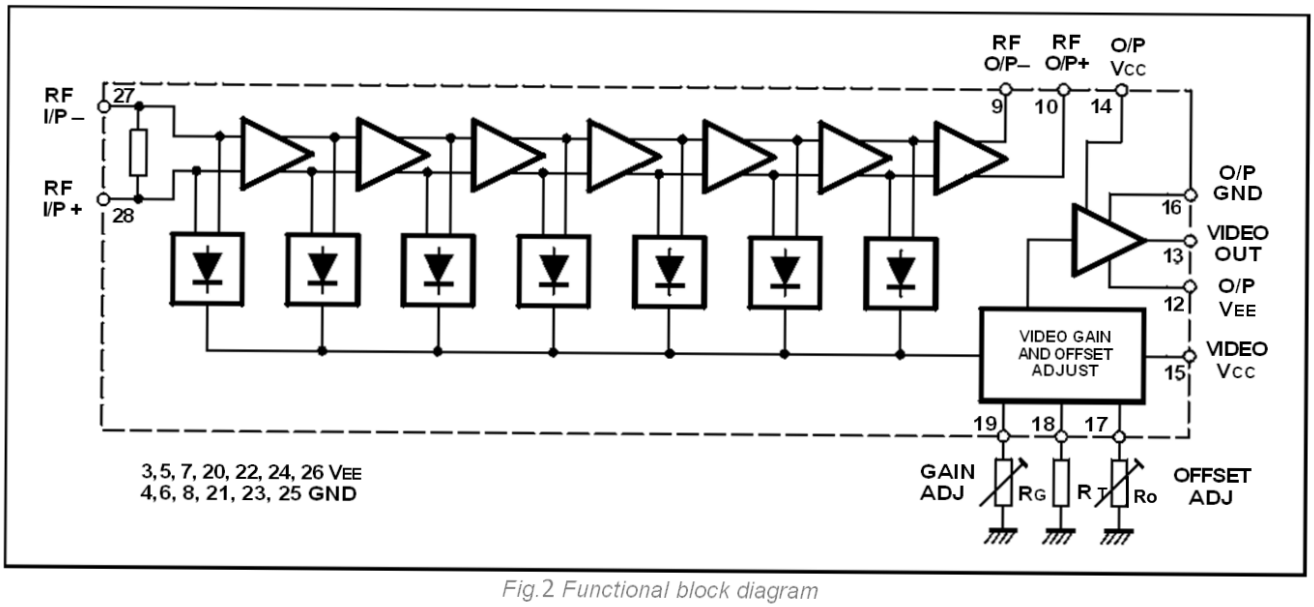

Fig.2 Functional block diagram

ELECTRICAL CHARACTERISTICS

The electrical characteristics are guaranteed over the following range of operating conditions, using test circuit in Fig. 3 (unless otherwise stated):

Temperature range:

Military:	PS13201M1C8A4, PS13201	-55°C to +125°C (T_{CASE})
Commercial:	PS13201C1C8A4	0°C to +70°C (T_{CASE})

Supply voltage:

V_{CC}:	+4.50V to +5.50V (all grades)
V_{EE}:	-4.5V to -5.50V (all grades)

Frequency	100MHz to 500MHz
Rg, Ro, Rt	1.5KΩ
Video output load	200Ω//20pF

Test conditions (unless otherwise stated):

Temperature:	PS13201M1C8A4 :+25°C, +125°C & -55°C (T_{CASE}) PS13201C1C8A4 :+25°C PS13201 : +25°C
Supply voltage:	V_{CC} = +5.0V V_{EE} = -5.0V

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Parameter	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Positive supply current (quiescent)	14, 15		28	35	mA	V_{CC} = +5.0V
Negative supply current (quiescent)	ALL V_{EE} Pins		150 180	175 210	mA mA	V_{EE} = -5.0V See note 1 V_{EE} = -5.0V See note 2
Dynamic range		75 70			dB dB	100 to 400MHz See note 1, 3 See note 1, 4
Linearity		-1 -1 -1.25		+1 +1 +1.25	dB dB dB	T_{CASE} = -55°C T_{CASE} = +25°C T_{CASE} = +125°C
Video output range	13	1.30	1.75	2.00	V	
Video slope	13	18	21	24	mV/dB	
Video slope variation	13	-5		+5	%	See note 5
Video slope adjust range	13	±20	±30		%	R_G = 1kΩ to 2.2kΩ
Video offset	13	-0.1	+0.25	+0.5	V	
Video offset variation	13		-05		mV/°C	T_{CASE} = +25°C
Video offset adjust range	13	±0.5			V	R_O = 1kΩ to 2.2kΩ
Video trim reference voltage	17, 18, 19	-0.59	-0.54	-0.49	V	
Video output impedance	13		10		Ω	See note 8
Video rise time	13		16		ns	10% - 90% (60dB step) See note 7
Input VSWR	27, 28		1.5:1			Zs = 50Ω See note 7
RF bandwidth	9, 10		450		MHz	T_{CASE} = +25°C RFIN = -70dBm See notes 2, 7
RF limiting range	9, 10		60		dB	See notes 2, 6, 7
RF limited output level	9, 10	-3.0	-1.0	+1.0	dBm	R1 = 50Ω single ended, See note 2
RF output impedance	9, 10		50		Ω	Single ended See notes 2, 8
Phase variation with RF Input level			15		Degrees	Freq = 300MHz RF_{IN} = -60 to +10dBm See notes 2, 7
Phase tracking between units			3		Degrees	T_{CASE} = +25°C FREQ = 300MHz See notes 2, 7

Notes

1 RF output buffer OFF (pin 8 disconnected from 0V)
2 RF output buffer ON (pin 8 connected to 0V)
3 Minimum dynamic range under any single set of operating conditions
4 Log linearity guaranteed for pin = -64dBm to +6dBm for ALL supply, temperature and frequency conditions
5 Full range of supply, temperature and frequency conditions
6 Input limiting range typically -50dBm to +10dBm
7 Not tested, but guaranteed by characterisation
8 Not tested, but guaranteed by design

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The PS13201 CANNOT be GUARANTEED to operate below 100MHz and meet the electrical characteristics shown above. However, characterisation has shown that the device can still function adequately down to frequencies of 50MHz, with the following reservations:-

1. The video bandwidth is fixed to approx 40MHz a certain amount of carrier breakthrough on the video O/P (pin 13) will occur, with input signal frequencies below 100MHz.
2. There are 2 RF coupling capacitors (20pF) on-chip, which couple the output signal from stage 3 to the input of stage 4 (ref Fig. 24). These can introduce undesirable limiting phase performance for input signal frequencies below 100MHz.

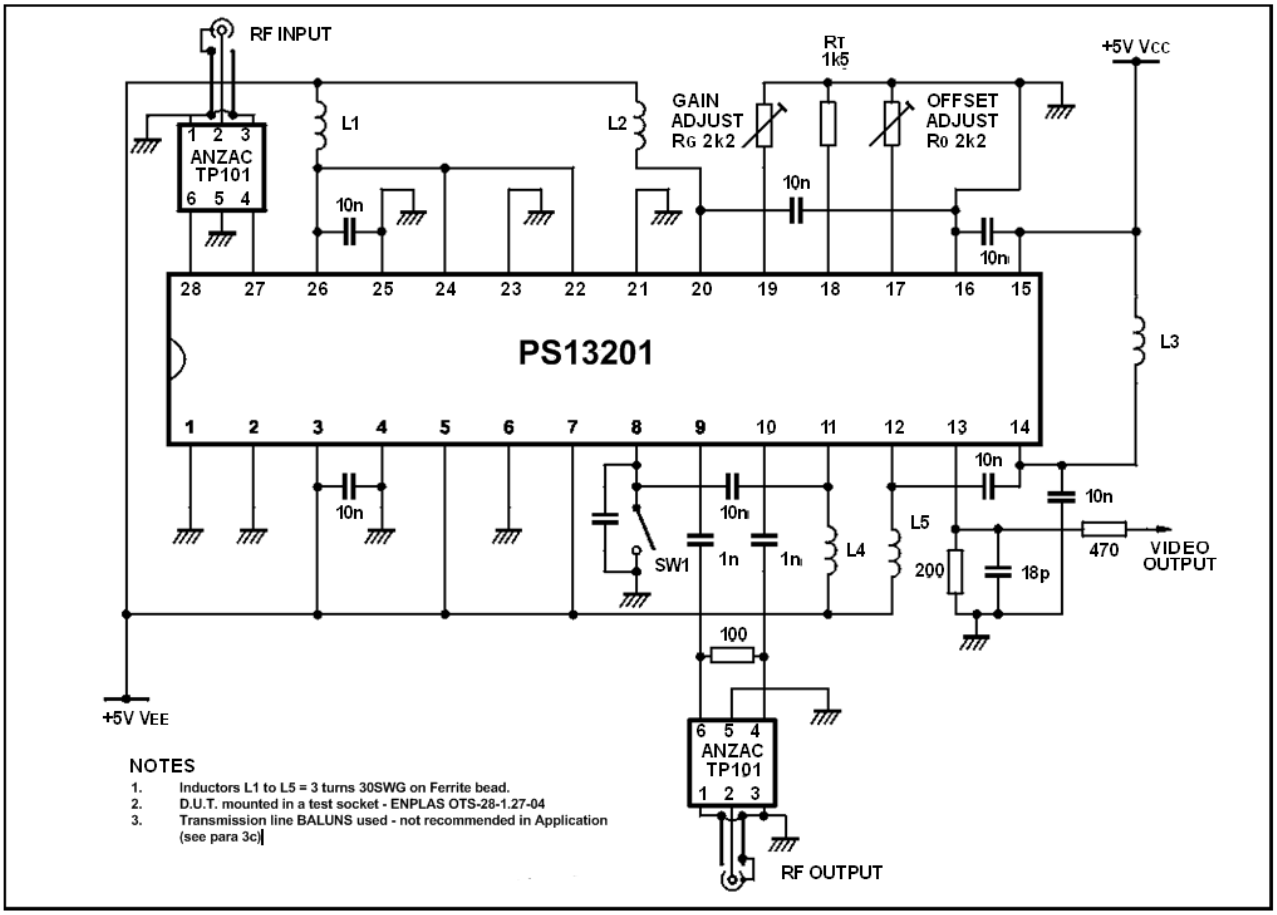

Fig.3 Test circuit

PRODUCT DESCRIPTION

The PS13201 is a complete monolithic successive detection Log/limiting amplifier which can operate over an input frequency range of 100MHz to 500MHz. Producing a log/lin characteristic for input signals between -64dBm and +6dBm, the log amplifier can provide an accuracy of better than ±1.00dB at case temperatures of -55°C and +25°C and an accuracy of better than ±1.25dB at +125°C. The dynamic range is better than 75dB over a frequency range of 100MHz to 400MHz. The graph in fig 4 shows how the dynamic range is guaranteed over frequency.

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The PS13201 consists of 6 Gain stages, 7 Detector stages, a limiting RF Output buffer and a Video Output amplifier. The power supply connections to each section are isolated from each other to aid stability.

The PS13201 consumes 1.1W of power when ALL parts of the circuit are powered up from a ±5.0V power supply. As the circuit uses a differential architecture, the power consumption of the RF gain/detector stages and RF Output Buffer will be independent of RF input signal level. However, the Video Output (pin 13) is driven by a single ended emitter

follower and so the power consumption of the Video amplifier will vary with RF input signal level between pins 27 and 28.(upto 10mA over 2V video output range with max video load of 200Ω //20pF) The PS13201 has a high RF gain (>50dB) across a wide bandwidth (>450MHz) when the limiting RF Output Buffer is enabled. The limiting RF Output Buffer provides a balanced Limited Output level of nominally –1.0dBm on each RF Output connection (pin 9 and 10), for RF input signal levels on pins 27 and 28 in excess of –50dBm.

The limiting RF Output Buffer can be isolated from the other sections of the PS13201, by disconnecting the RF Output Buffer GND (pin 8) from 0V, and leave the pin floating. This feature aids stability in applications NOT requiring a Limited RF Output signal, and lowers the power consumption of the PS13201 to 0.95Watts, when the other sections are powered up from a ±5.0V power supply.

Each of the Gain and Detector stages has approximately 12dB of gain, and a significant amount of on-chip RF decoupling (200pF per stage), also to aid stability. The Video amplifier provides a positive going output signal proportional to the log of the amplitude of an RF input applied between pins 27 and 28. The gain and the offset of the Video amplifier can be adjusted by 3 resistors; RG , RT , and RO which are connected to Gain adjust (pin 19),Trim reference (pin 18) and Offset adjust (pin 17). With RT set to 1.5k∧ , RG can be set to any value between 1kΩ and 2k2Ω and achieve a range in Video Slope of ±20%, centred on 21mV/dB. Similarly, RO can be set to any value between 1kΩ and 2.2KΩ and achieve an offset range of ±0.5V, which should allow the Video Offset to be trimmed to 0V if required.

The RF input pins (27 and 28) have a 50Ω terminating resistor connected between them on–chip. These are capacitively coupled to the I/P gain stage with 20pF on-chip capacitors. (Refer to APPLICATION NOTES section for information on how to connect an RF input signal to the device).

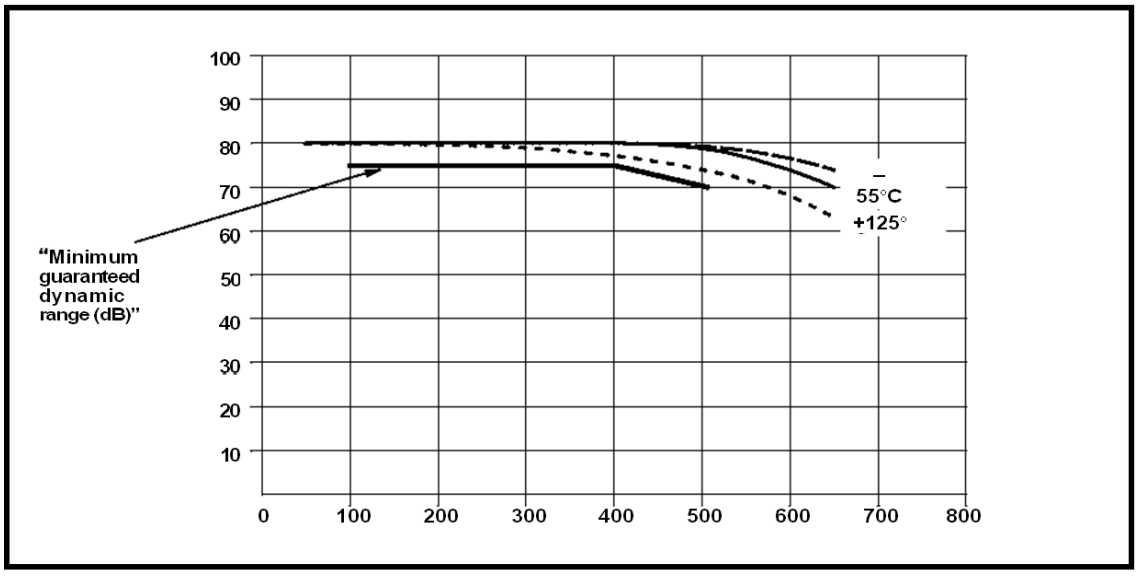

Fig.4 Plot showing guaranteed dynamic range v. frequency
(typical achievable dynamic range lines indicated across temperature)

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APPLICATION NOTES

1) VIDEO–AMPLIFIER

The PS13201 uses a single ended Video amplifier to produce a trimmable Video transfer characteristic. Both the gain (Slope) and Offset of the amplifier can be externally adjusted.

a) Gain and Offset trimming (ref Applications circuits in Figs 5 and 6)

The Gain and Offset control is achieved by adjusting RG and RO respectively. The control is dependent upon their difference from the Trim reference resistor, RT. Adjustment of Gain has an effect on Offset, but adjustment of Offset does NOT affect the Gain. Therefore the Gain should be optimised first. The Offset should only be adjusted once the Gain has been set.

Fig 7 shows the variation of Video Offset with value of RO, for a fixed value of RT and RG = 1k5Ω.
Fig 8 shows the variation of Video Slope with value of RG, for a fixed value of RT and RO = 1k5Ω.

The Video amplifier incorporates temperature compensation for Video gain (Slope). To ensure temperature stability for Video gain (Slope) over the operating temperature range, it is recommended that the resistors with identical temperature coefficients of resistance are used for RT and RG.

The Video amplifier does NOT incorporate temperature compensation for Video Offset. Although it is recommended that a resistor with identical temperature coefficient of resistance to RT be used for RO, it may be necessary to use an additional external temperature compensating network.

b) Video performance

The Video–amplifier has a critically damped rise time of 16ns (10% - 90%).In order to achieve this transient performance, it is important to ensure that:-

i) the resistor connected to Trim reference (pin 18), has a nominal resistance of 1.5kΩ, with a parasitic capacitance LESS than 5pF.

ii) the load applied to the Video Output (pin 13) does NOT exceed 200Ω resistance in parallel with 20pF.

Also, the following decoupling should be incorporated:-

i) The Video Output V_{CC} (pin 14) should be decoupled with a 10nF capacitor to the RETURN line from the video load, connected to Video GND (pin 16), avoiding any common impedance path.

ii) The Video Output Vee (pin 12) should be decoupled with a 10nF capacitor DIRECTLY to Video-Output V_{CC} (pin 14).

2) PS13201 AS A LOG AMPLIFIER with RF output buffer disabled (pin 8 floating)

If the PS13201 is to be used as a logarithmic successive detection amplifier only, with no requirement for a limited RF Output, the RF input (pins 27 and 28) can be driven EITHER differentially or single ended from a 50Ω source. If being used with a single ended input, the SIGNAL should be applied to pin 27 and the RETURN should be connected to pin 28, as shown in the Application circuit diagram in Fig 5.

The PS13201 is VERY stable when used in this way. Although not a crucial requirement, it is recommended that the device should be mounted using a ground plane.

3) PS13201 AS A LOG/LIMITING AMPLIFIER- with RF Output-Buffer ENABLED (pin 8 connected to GND)

If the PS13201 is to be used as a limiting or Log/limiting amplifier with a requirement for a Limited RF Output signal, care is required in the layout of components and connections around the device to ensure stability. The following precautions should be observed (refer to Application circuit diagram in Fig. 6):-

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a) The device should be mounted on a ground plane, ensuring that the impedance between the ground plane and ALL the GND pins is kept as low as possible. If a multilayer PCB is used where the ground plane is connected to the GND pins using through-plated holes (vias), it is essential to ensure that the vias have a very low impedance. ALL supply decoupling capacitors should be RF chip capacitors whose leads should be kept as short as possible.

b) The RF $_{VEE}$ connections (pins 3,5,7,11,20,22,24,26) should be connected to a low impedance copper plane. A two layer PCB should help to achieve this.

c) The RF input (pins 27 and 28) should be driven with a balanced source impedance. One way of achieving this is to use an **isolating** BALUN transformer (50Ω UNBALANCED 50Ω BALANCED) connected between the signal source and the RF input pins. (e.g. Mini circuits TT1–6, TO –75). The device stability is VERY sensitive to an imbalance of the differential source impedance at pins 27 and 28. Use of a transmission line BALUN though, is NOT recommended.

d) The RF Output connections (pins 9 and 10) should each be loaded with matched impedances ideally 50Ω transmission lines. The RF Output lines leading away from the device should be balanced. Driving highly reactive SWR loads is NOT recommended as these can encourage device instability, as can an imbalance of the differential load impedance at pins 9 and 10.

e) The RF Output connections (pins 9 and 10) are DC coupled, and ideally the output pins should be capacitively coupled to their loads using 1nF capacitors. However the RF Outputs can drive a DC load to GND and a DC offset of approx. 400mV will exist on each RF Output pin. IT WILL NOT BE POSSIBLE TO DISABLE THE RF OUTPUT BUFFER UNDER THESE CONDITIONS.

f) The RF output (pins 9 and 10) has a tendency to limit on self noise, particularly at low ambient temperatures (-55°C), when the RF output buffer is enabled.

NOTE that this will effect the limiting range as the gain of the RF output buffer will reduce as the amount of noise limiting increases.

If required the limited RF Output can be attenuated using an attenuation network as shown in fig. 9. Under these conditions the effective RF Output currents will be reduced, allowing the device to operate with a greater margin of stability. It may be possible to run the device without a BALUN transformer on the RF input if the total output impedance on the RF Output >> 50Ω , and the attenuation components are mounted as close as possible to the RF Output connections (pins 9 and 10). The RF input connection could then be configured as in Fig 5.

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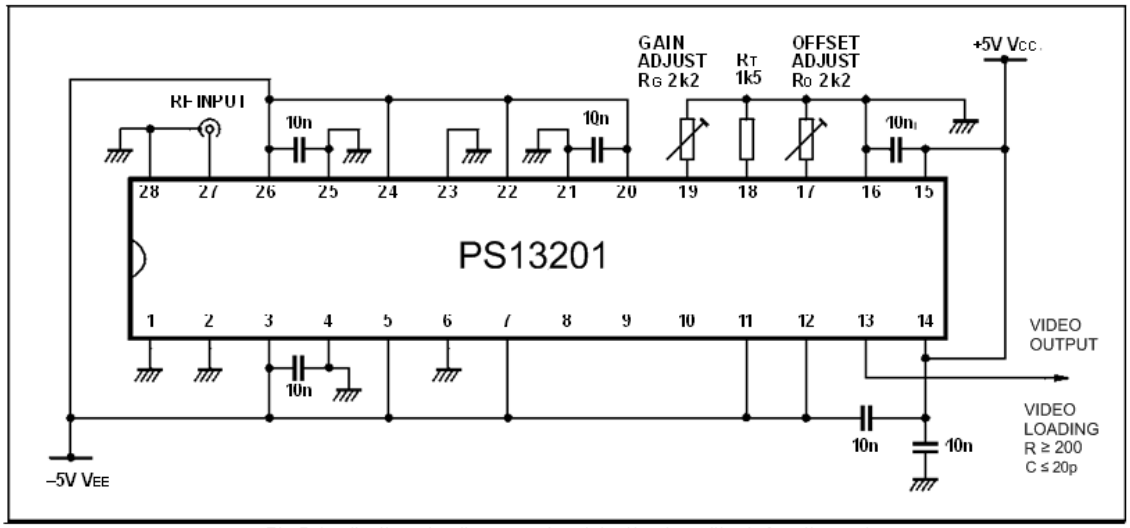

Fig.5 Application circuit successive detection logarithmic function only

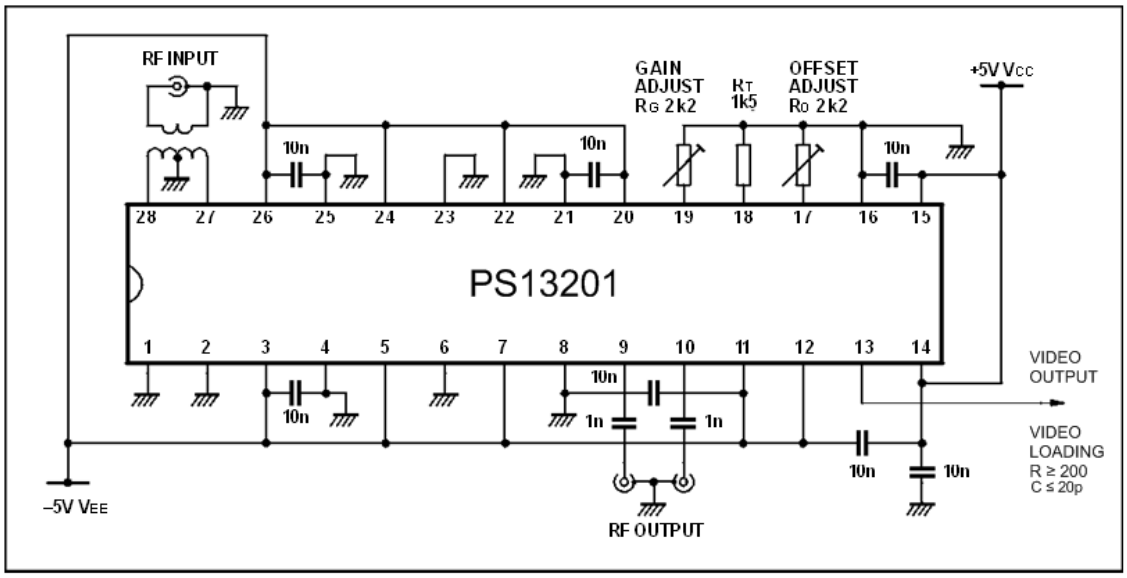

Fig.6 Application circuit - Log / Limiting function

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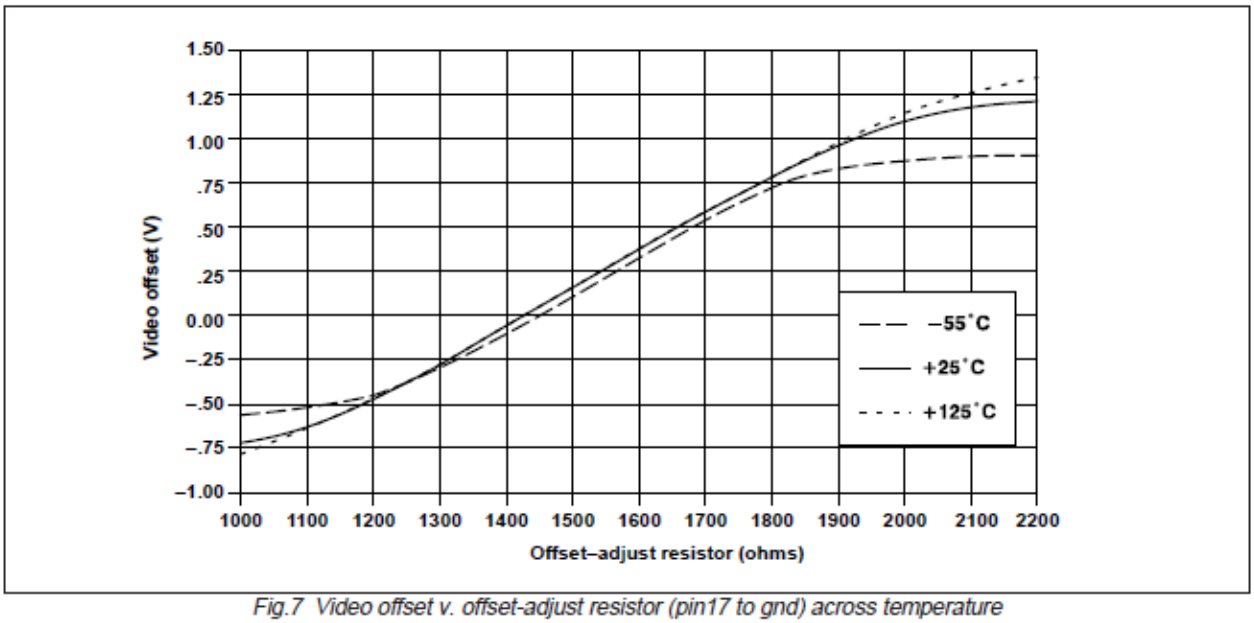

Fig.7 Video offset v. offset-adjust resistor (pin17 to gnd) across temperature

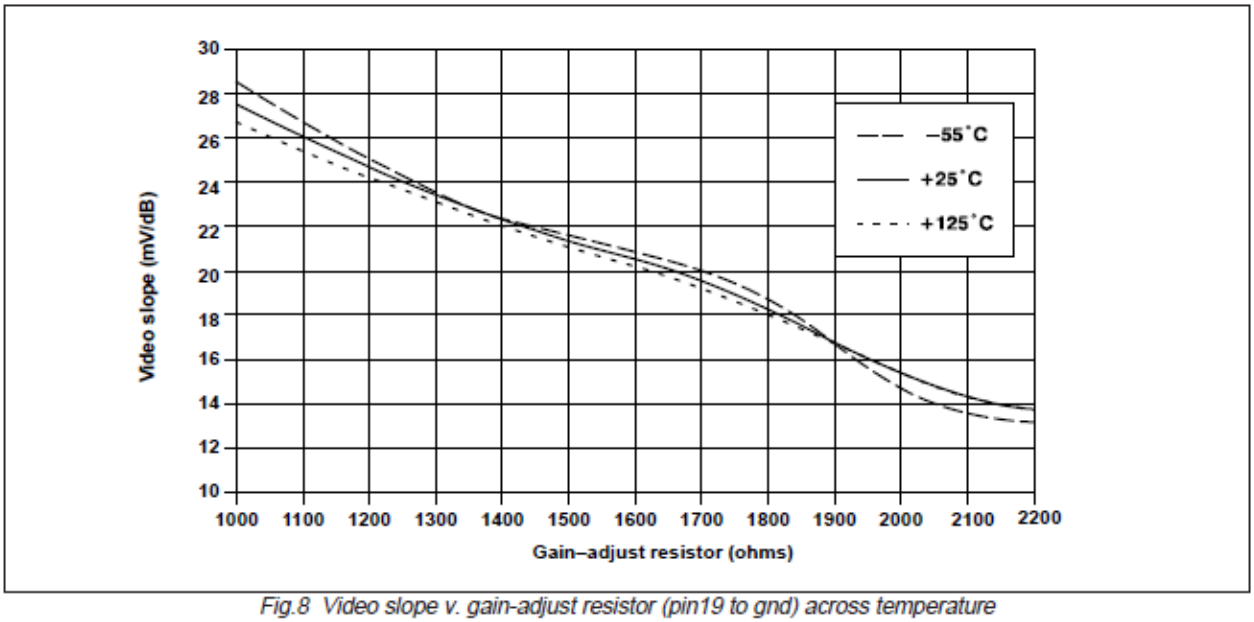

Fig.8 Video slope v. gain-adjust resistor (pin19 to gnd) across temperature

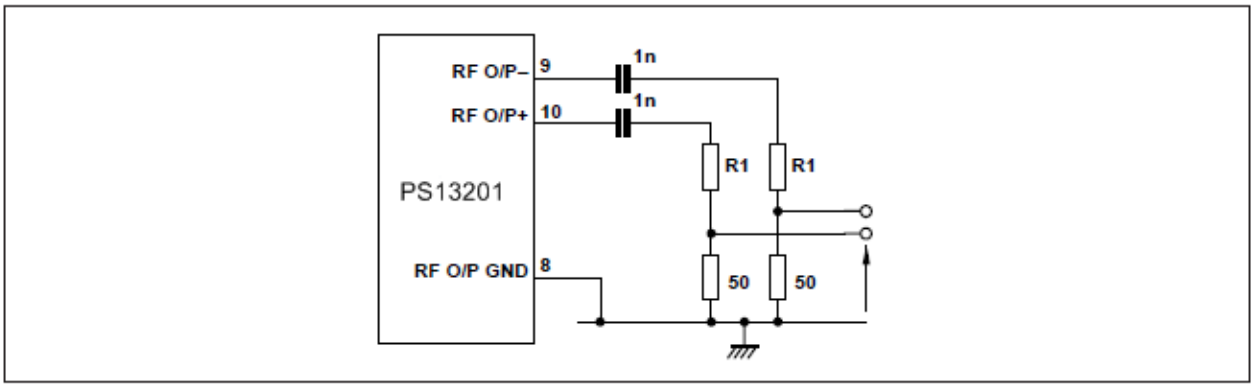

Fig.9 Network for attenuating limited RF output

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A PRACTICAL APPLICATION FOR THE PS13201AS A LOG/LIMITING AMPLIFIER

The PS13201, with the RF Output-Buffer ENABLED, has a large limited RF Output level (0dBm on each of two RF Output pins (9 and10)) and a wide RF bandwidth (450MHz) in a small 28 pin Miniature Ceramic S.O package. As a result, there is a tendency for the device to become unstable unless care is used in the application.

The PCB layout for a "PS13201 DEMONSTRATION BOARD" in Fig. 11 has proved reliably stable. The PCB is a double layer Fibre epoxy board which uses SMDs where possible. A circuit diagram for the Demonstration PCB appears in Fig. 10.

The following points should be noted when this application is realised practically:-

1. A wire needs to connect the two pads connected to pins 14 and 15 of the PS13201, to allow +5V to appear at both pins.
2. ALL the GND connections to the PS13201 are made through the PCB to a Ground plane on the bottom side. It is important to ensure that the impedance of each of these connections is kept to an absolute minimum to prevent instability. If these connections are achieved using through plated holes, it is recommended that they are filled with solder to lower their impedance.
3. The PCB is configured to accept SMA, SMB or SMC connectors for the RF input, RF Output and Video Output connections. These can be changed if necessary to an alternative type, but it is vital to ensure that the ground plane is solidly connected to the Guard Ring which surrounds the RF Output tracks.
4. The PCB is configured to accept a small surface mounting DC isolating BALUN transformer (e.g VANGUARD VE43666, available from Vanguard Electronics Company Inc, 1480 West 178th St. GARDENA, C.A. 90248, U.S.A. Tel:- U.S.A. (213) 323 – 4100) to couple a signal into the RF input connections (pins 27 and 28). It is NOT recommended to attempt operating the PS13201 with the RF Output Buffer enabled, WITHOUT using an input BALUN, although it may be possible, provided the input source impedance to both pins 27 and 28 remains balanced. The centre tap of the secondary winding of the transformer should be soldered to the small ground plane on the upper side of the PCB.
5. The RF Output connection to the PCB is from pin 9 of the PS13201 only, with pin 10 being terminated on the PCB using a 510 resistor. It is important to ensure that both pin 9 and10 are terminated with equal impedances.
6. The RF Output Buffer can be enabled by soldering a link (LK) between pin 8 of the PS13201 and the adjacent guard track around the RF Output lines. Similarly, the buffer can be disabled by removing the same link. When the buffer is disabled, the following components can be omitted:-
7. 1nF capacitors (C1, C2)
8. 10nF capacitor (C8)
9. 510 resistor (RFO)
10. The Slope (gain) and Offset of the Video Output can be adjusted using two 1Kω trimmers, provision for which is included in the PCB layout.
11. The plots in Fig. 12 to fig. 23 are typical of the performance of PS13201 devices used with the PCB layout detailed in Fig.11.

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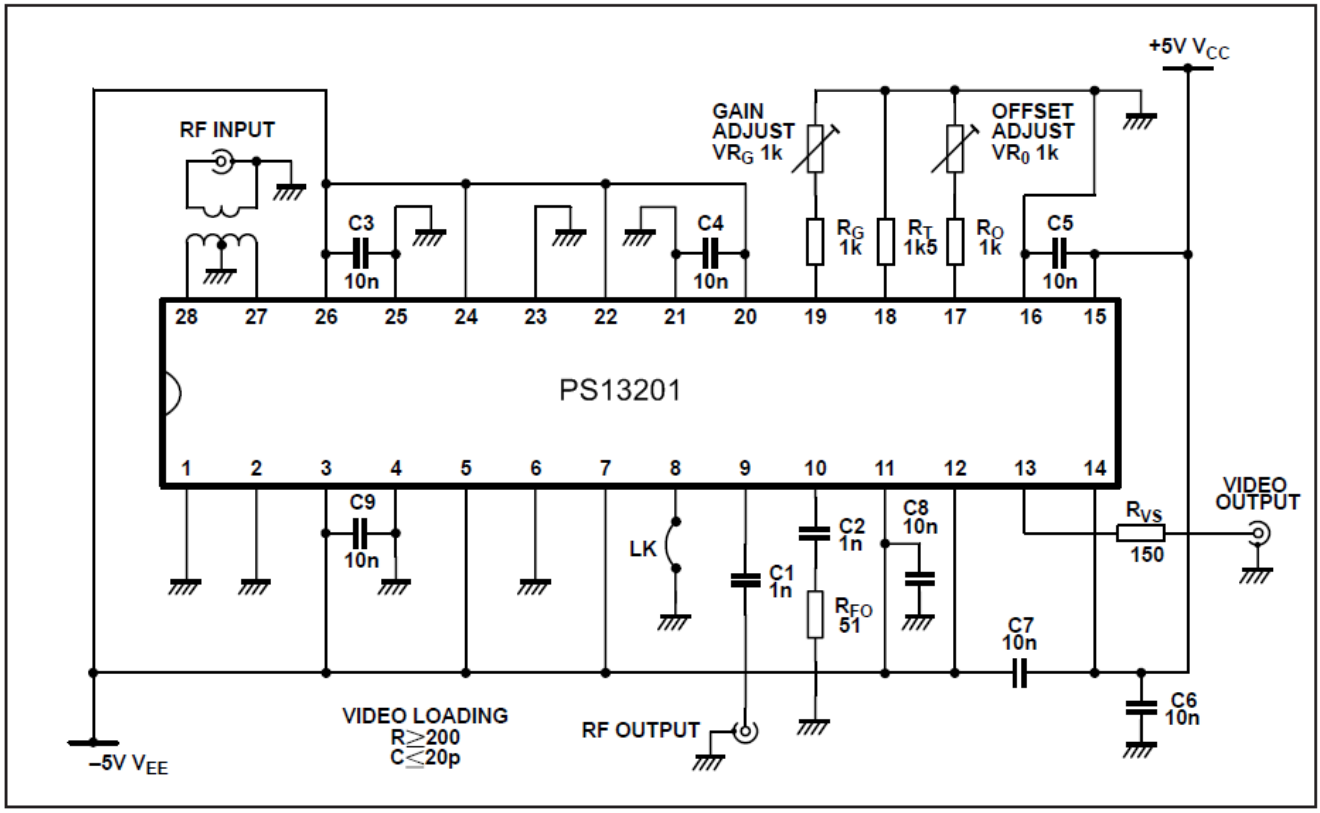

Fig. 10 PS13201 demonstration board circuit design

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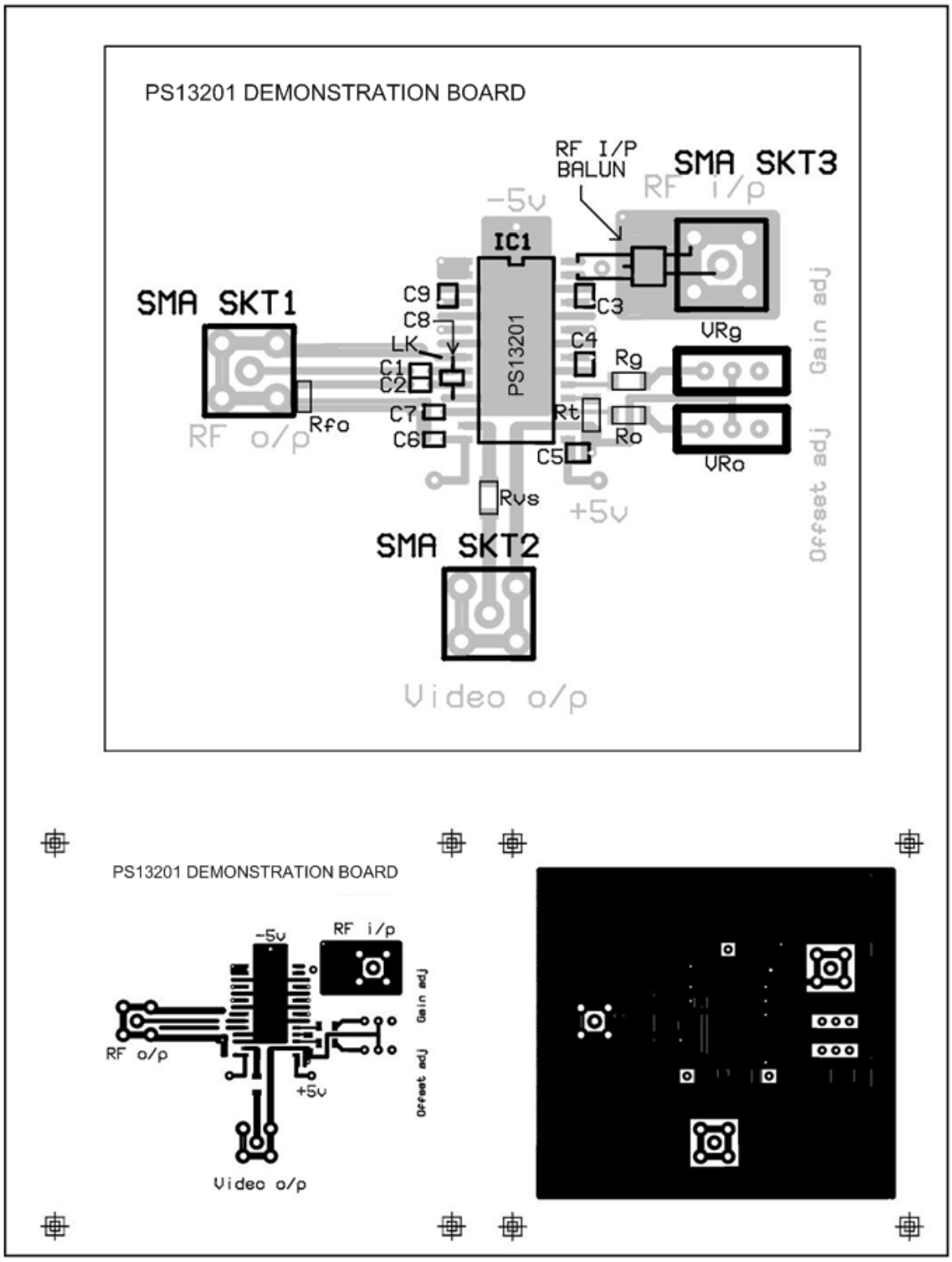

Fig. 11 Demonstration Circuit PCB showing component positions (2x full size) with top and bottom copper masks (full size)

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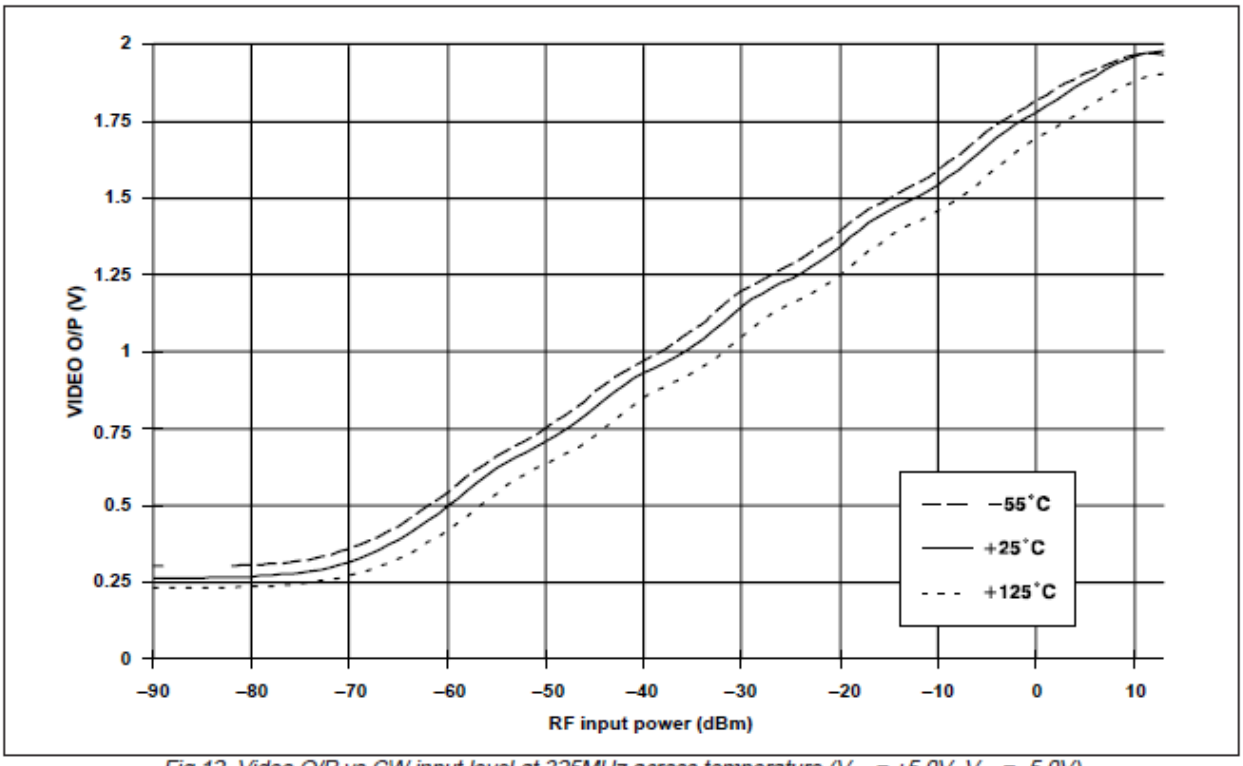

Fig.12 Video O/P vs CW input level at 325MHz across temperature (V_{CC} = +5.0V, V_{EE} = -5.0V)

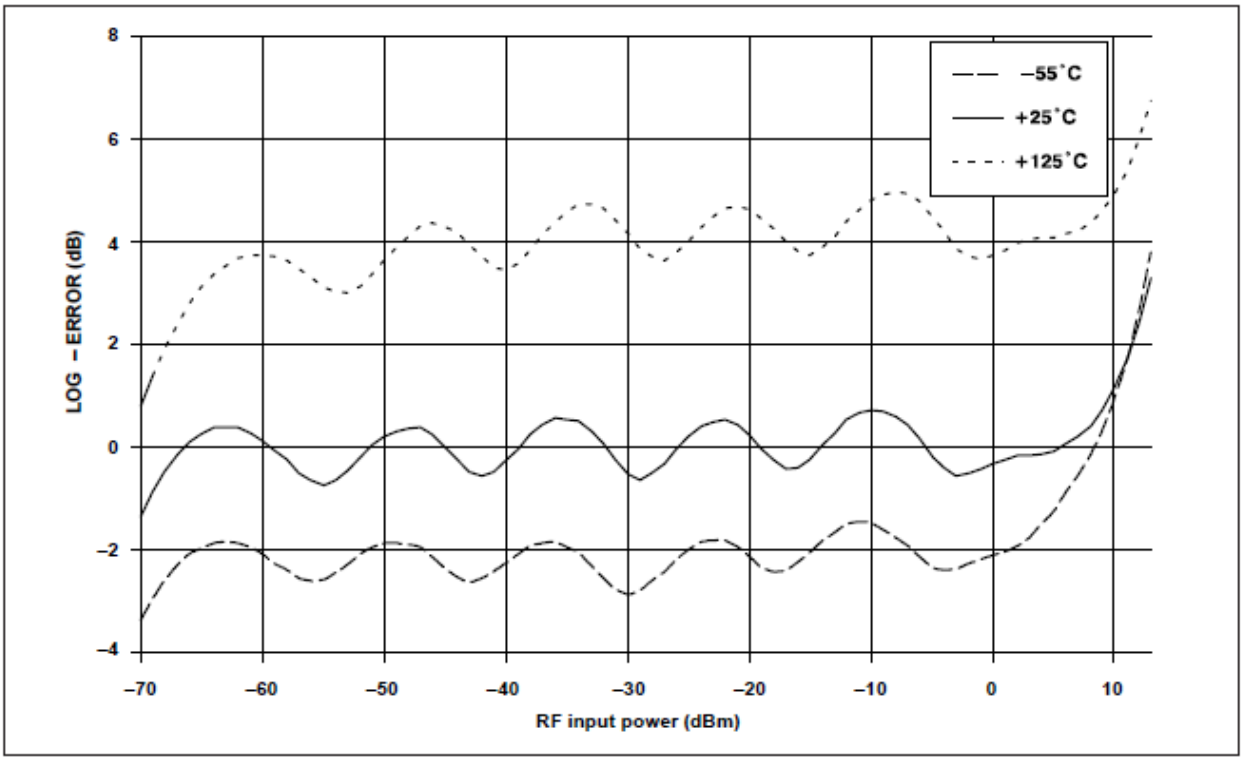

Fig.13 Video O/P log-error, (referenced to single straight line measured at 325MHz, +25°C, 5.0V PSUs) across temperature

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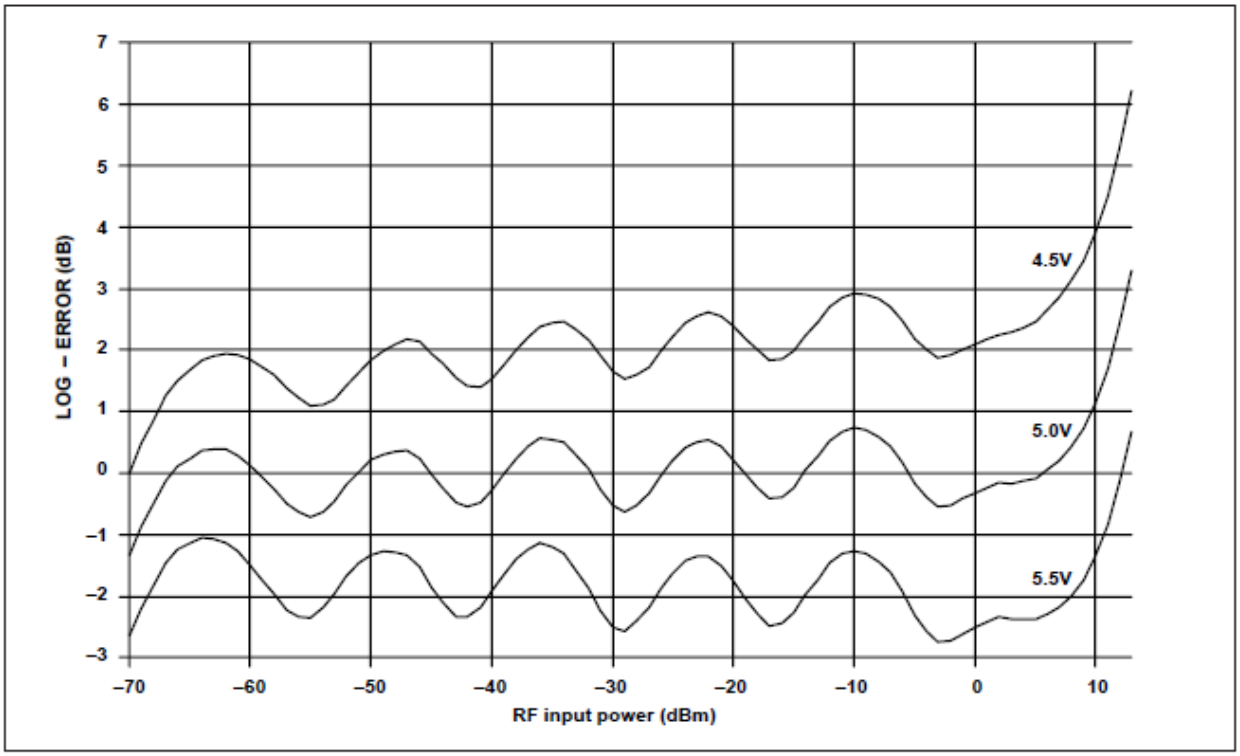

Fig.14 Video log error, (referenced to single straight line measured at 325MHz, 25°C, 5.0V PSUs), across supply voltage

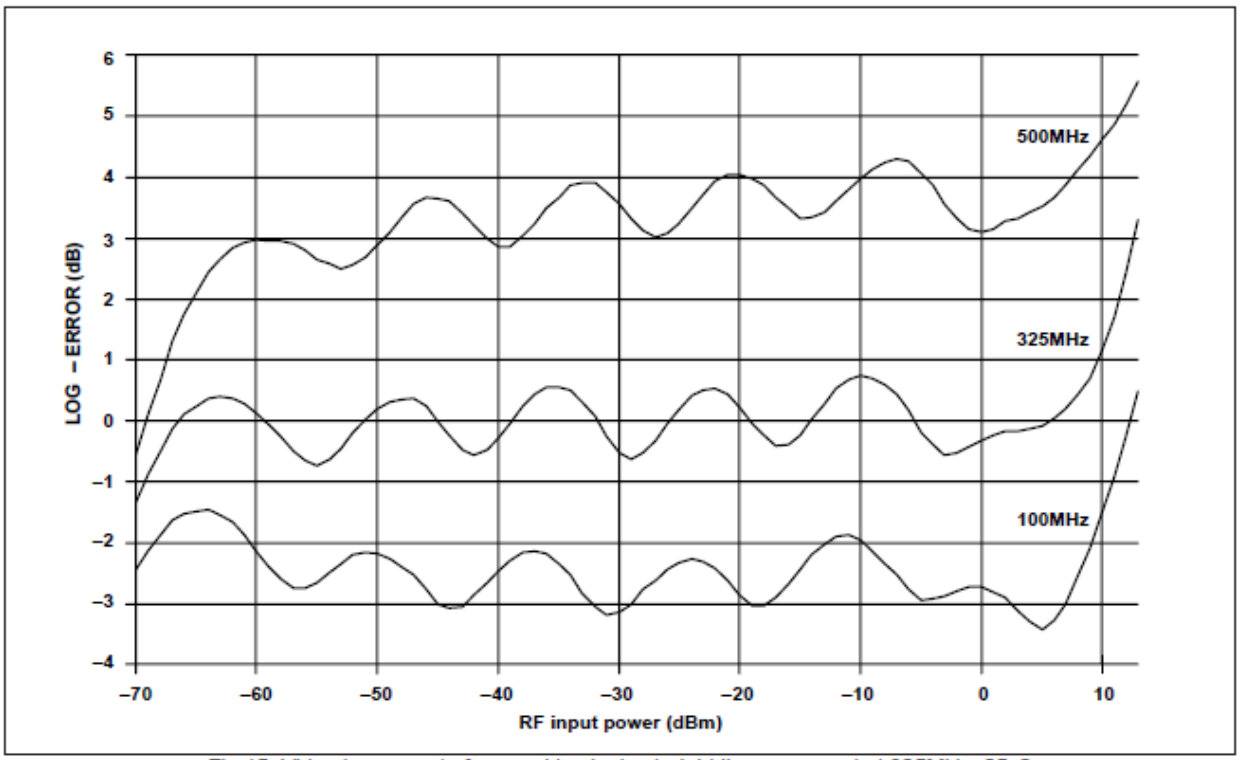

Fig.15 Video log error, (referenced to single straight line measured at 325MHz, 25°C,

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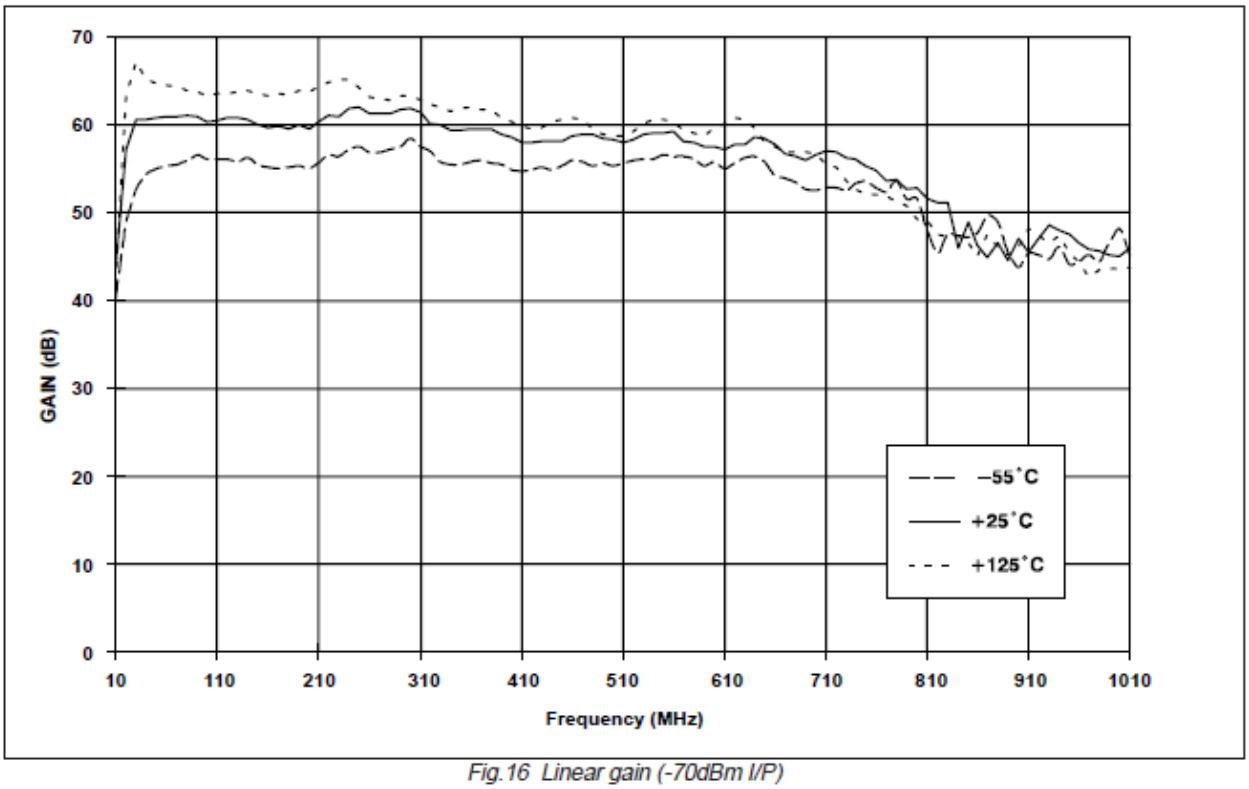

Fig.16 Linear gain (-70dBm I/P)

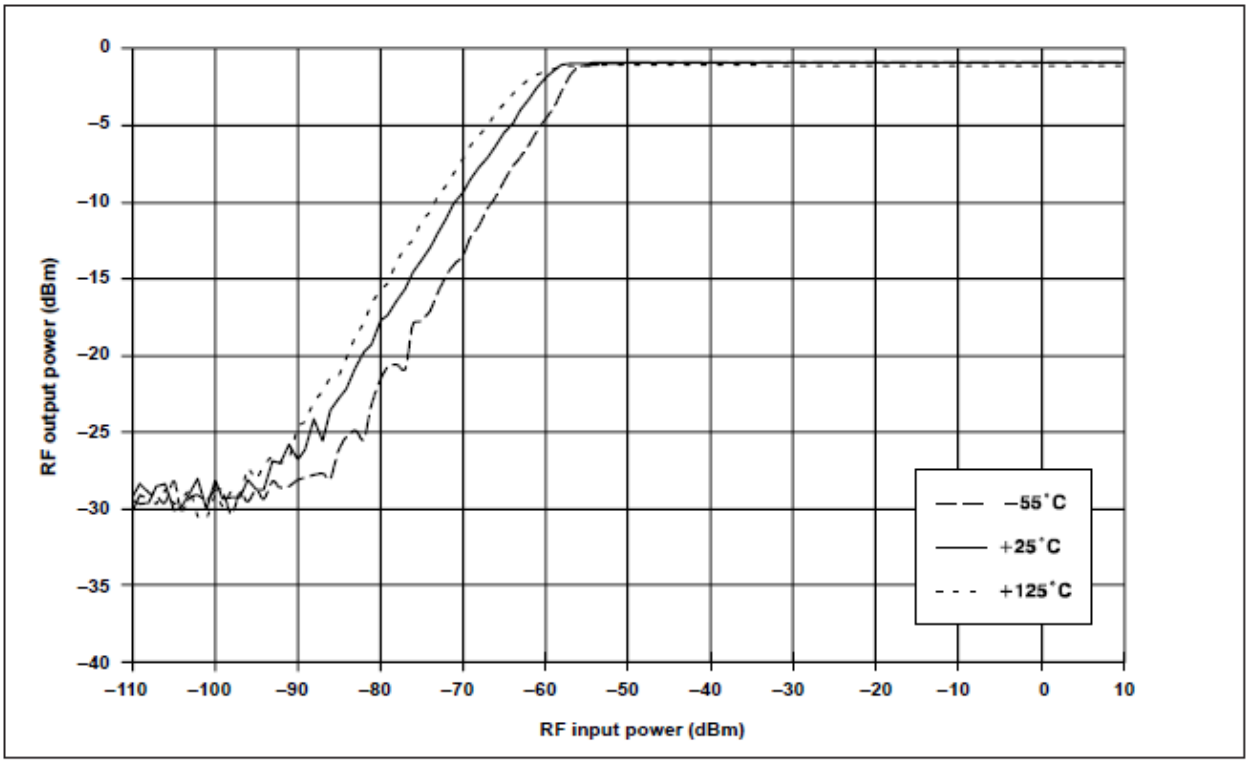

Fig.17 RF input → output limiting transfer characteristic at Frequency = 100MHz

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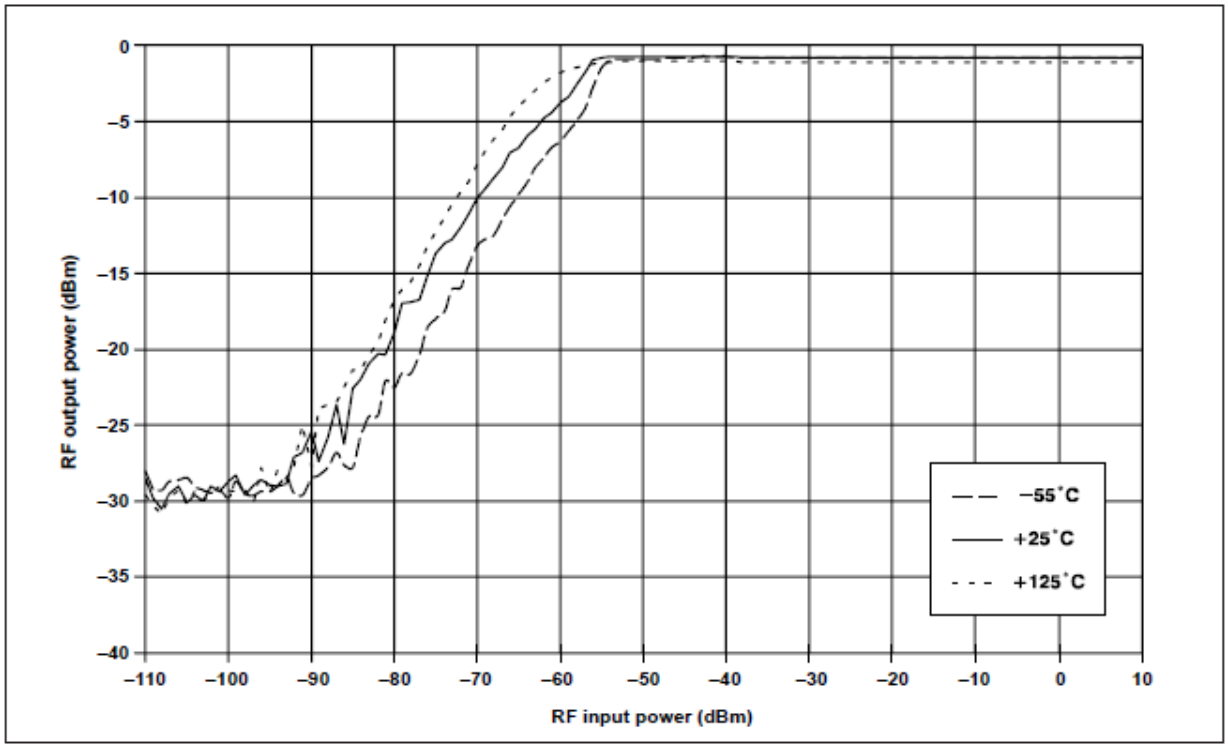

Fig.18 RF input → output limiting transfer characteristic at Frequency = 325MHz

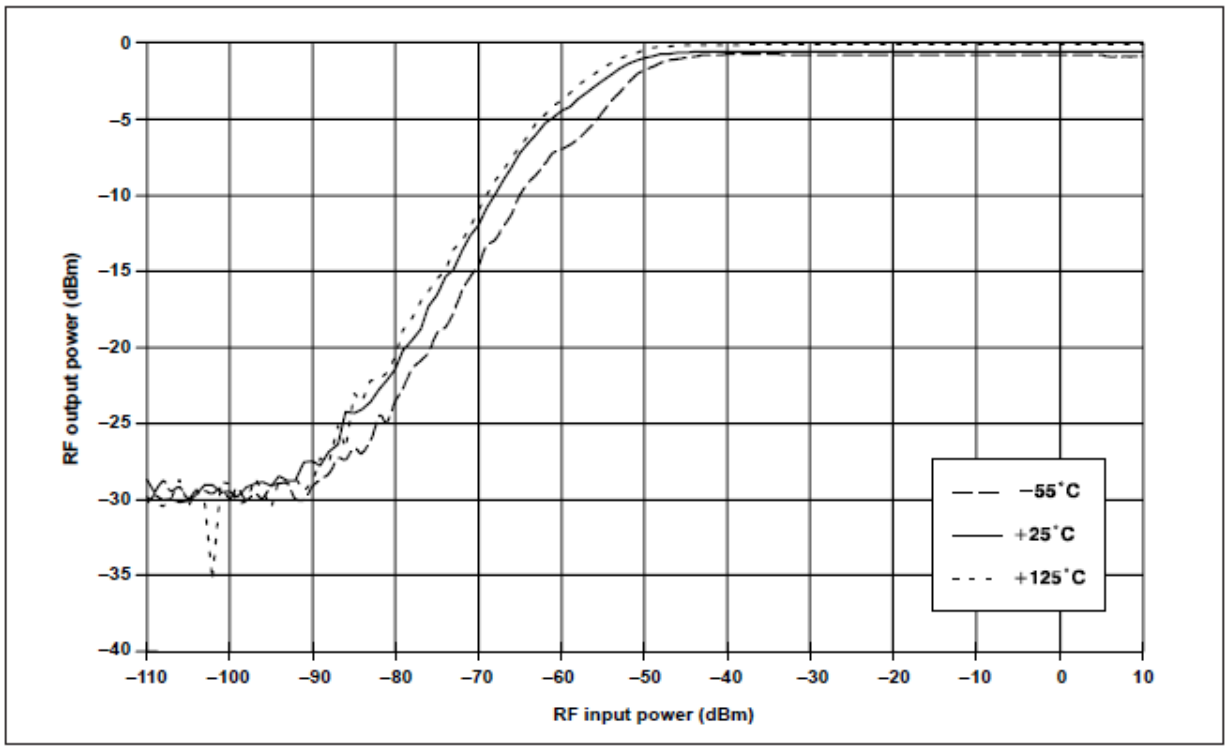

Fig.19 RF input → output limiting transfer characteristic at Frequency = 500MHz

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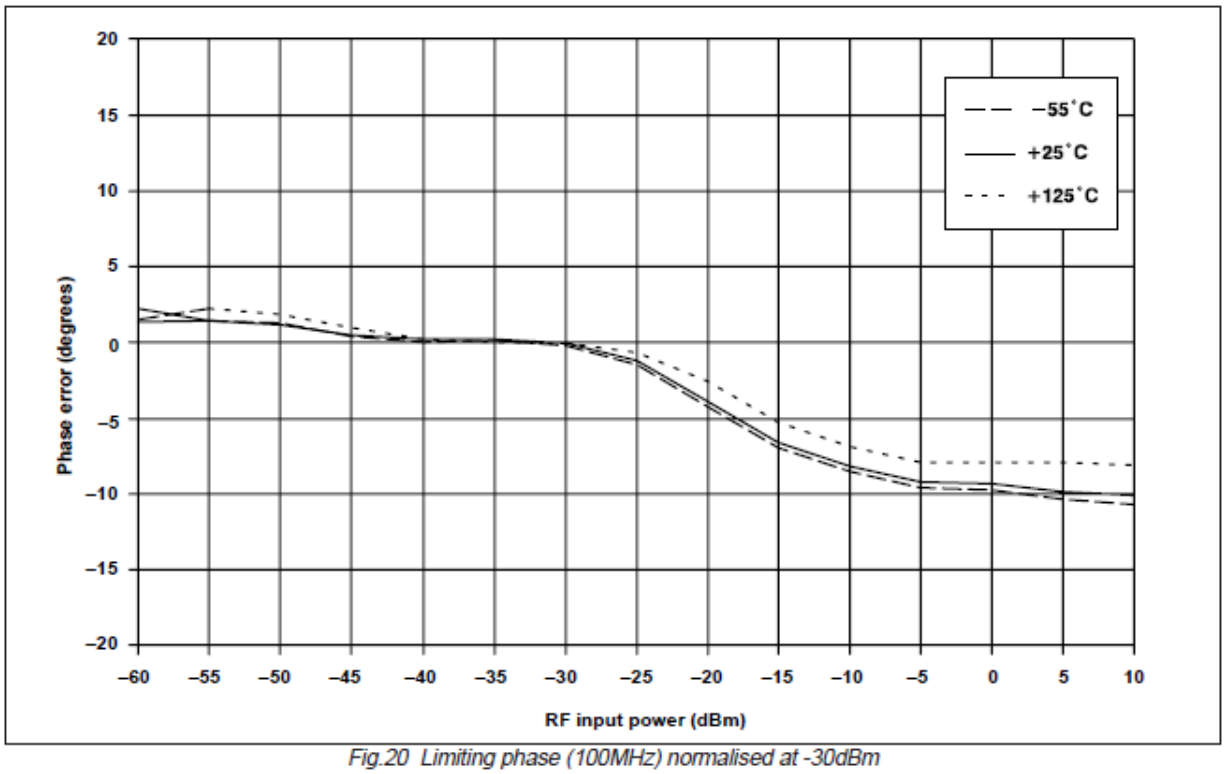

Fig.20 Limiting phase (100MHz) normalised at -30dBm

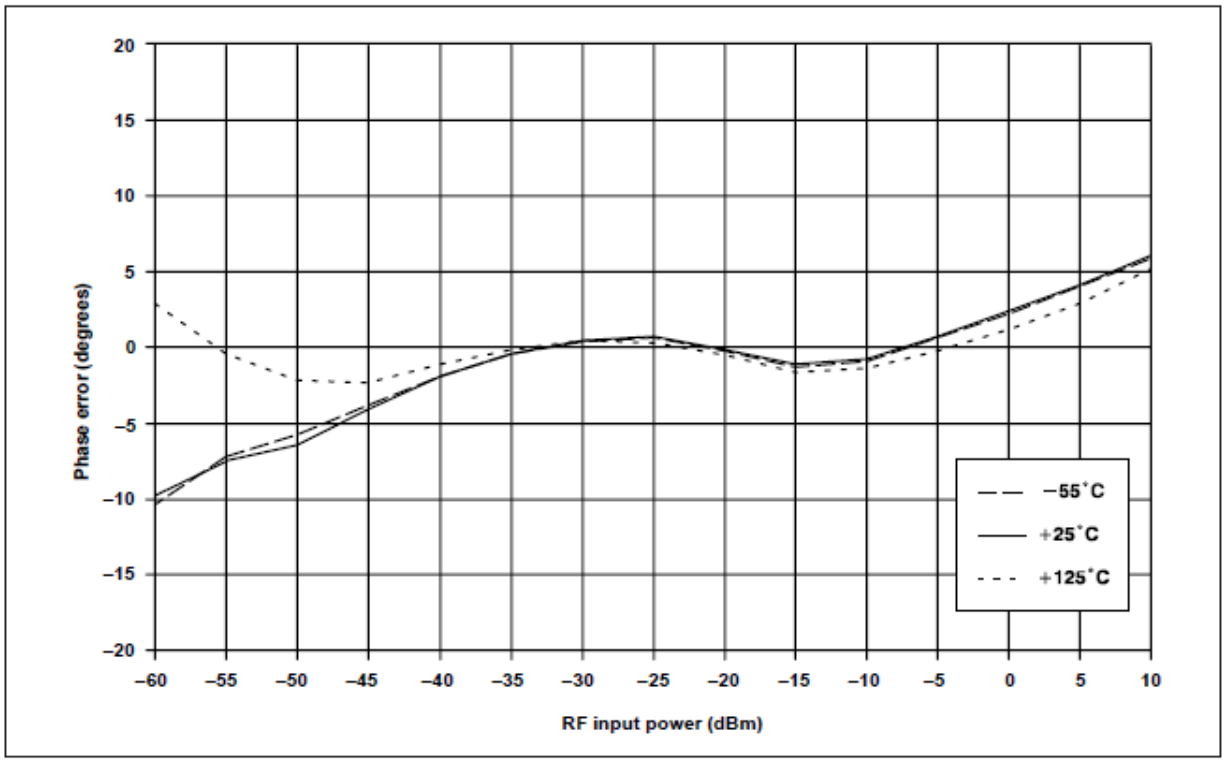

Fig.21 Limiting phase (300MHz) normalised at -30dBm

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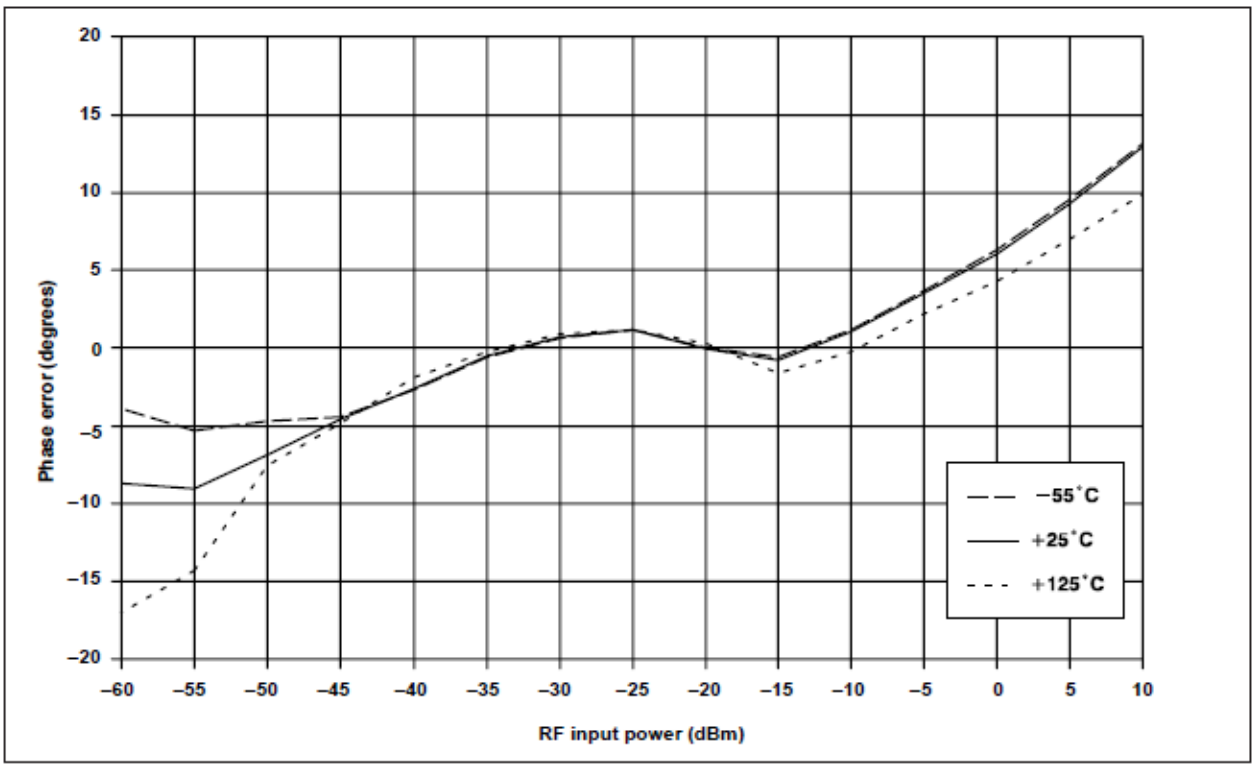

Fig.22 Limiting phase (500MHz) normalised at -30dBm

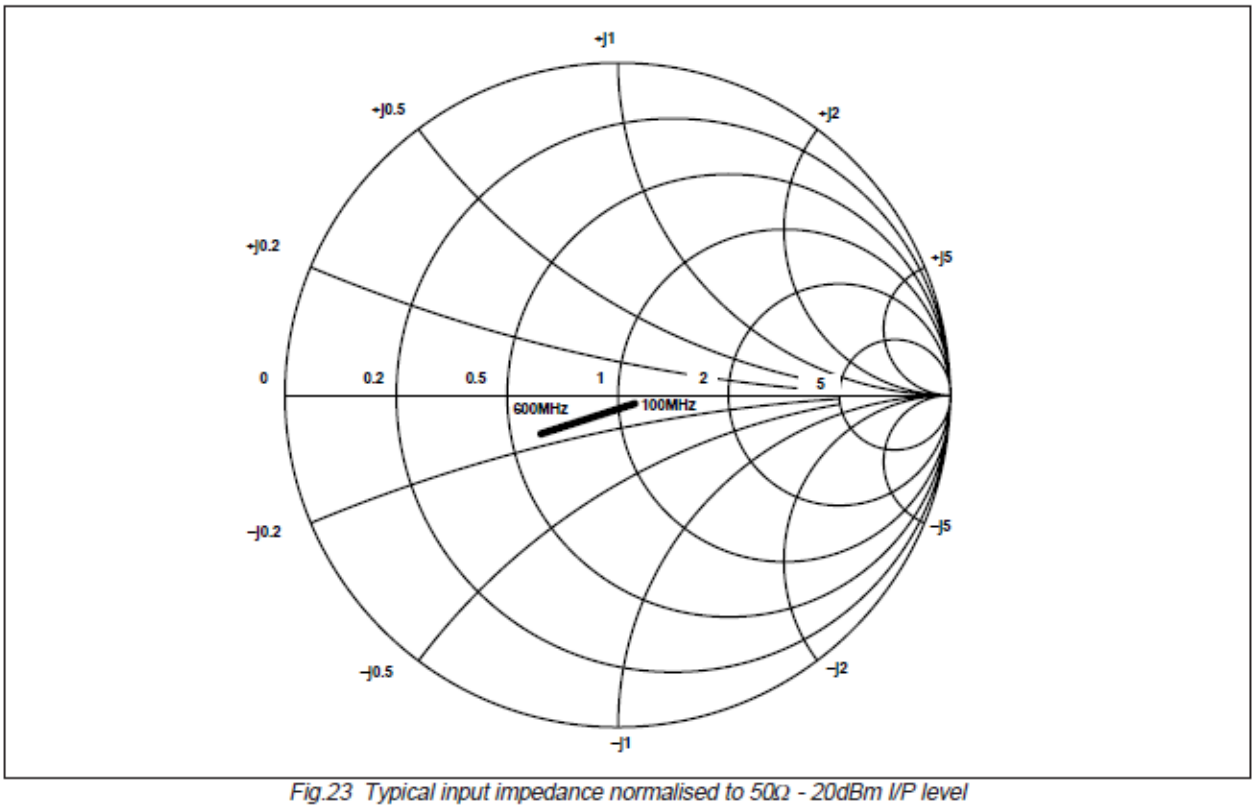

Fig.23 Typical input impedance normalised to 50Ω - 20dBm I/P level

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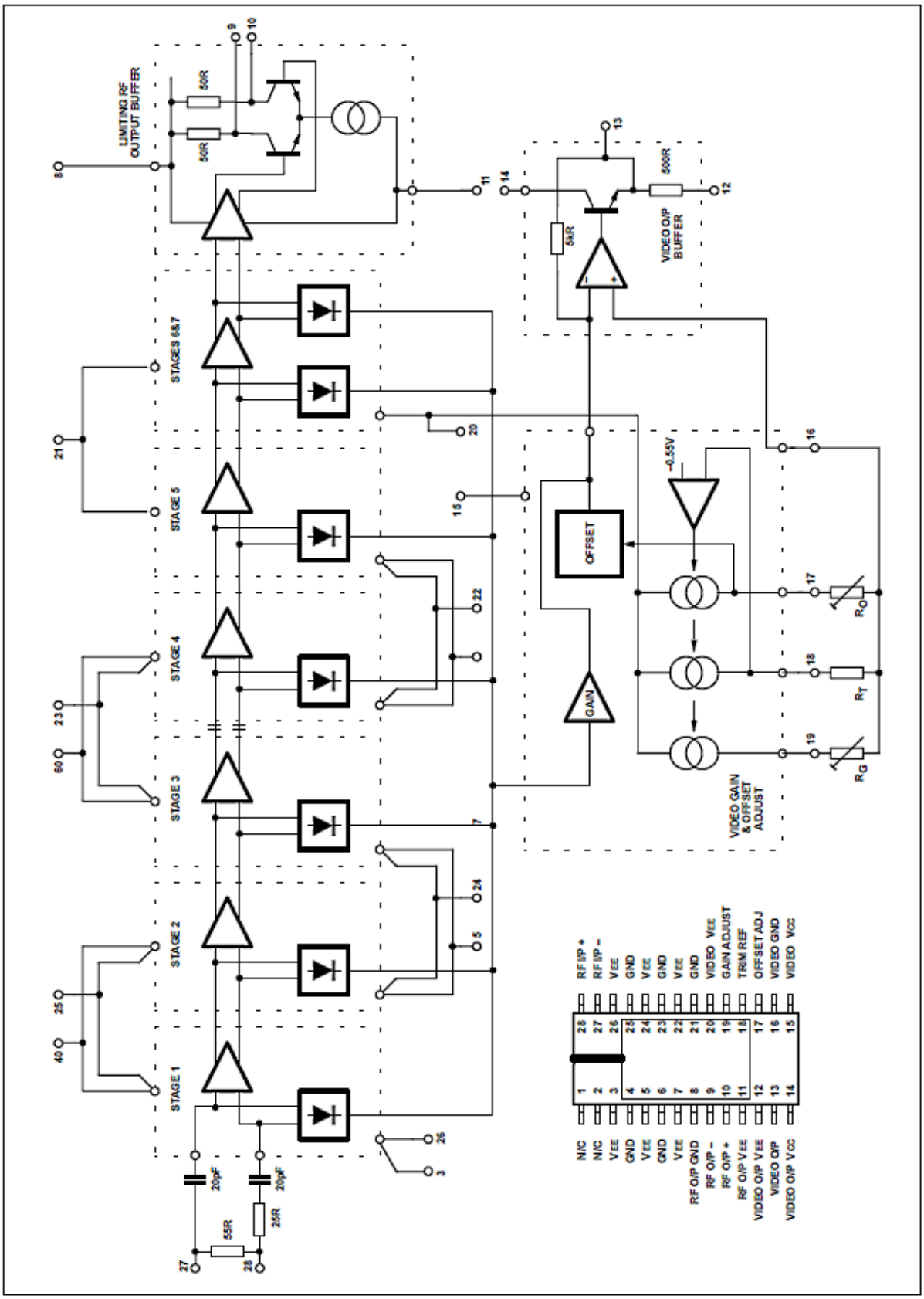

Fig. 24 PS13201 Schematic Diagram

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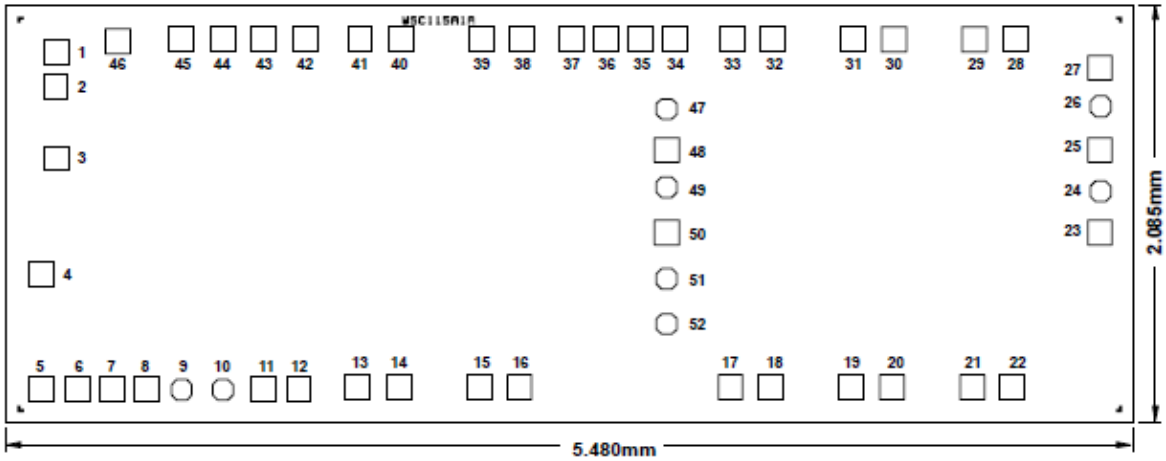

TERMINALS ((X) DENOTES MC PACKAGE PIN NUMBER)							
1	Video O/P (13)	14	V_{EE} 5A (22)	27	Test point	40	V_{EE} 5B (7)
2	Video O/P V_{CC} (14)	15	V_{EE} 4A (22)	28	V_{EE} 1B (3)	41	RF BUF O/P GND (8)
3	Gain V_{CC} (15)	16	GND 4B (23)	29	GND 1B (4)	42	RF BUF O/P GND (8)
4	Video GND (16)	17	GND 3A (23)	30	GND 2B (4)	43	RF O/P – (9)
5	Offset ADJ (17)	18	V_{EE} 3A (24)	31	V_{EE} 2A (5)	44	RF O/P + (10)
6	Trim REF (18)	19	V_{EE} 2A (24)	32	V_{EE} 3A (5)	45	RF BUF O/P V_{EE} (11)
7	Gain ADJ (19)	20	GND 2A (25)	33	GND 3B (6)	46	Video O/P V_{EE} (12)
8	Gain V_{EE} (20)	21	GND 1A (25)	34	Test point	47	Test point
9	Test point	22	V_{EE} 1A (26)	35	Test point	48	Test point
10	Test point	23	Test point	36	Test point	49	Test point
11	V_{EE} 6A (20)	24	RF I/P signal (27)	37	Test point	50	Test point
12	GND 6A (21)	25	Test point	38	GND 4B (6)	51	Test point
13	GND 5A (21)	26	RF I/P return (28)	39	V_{EE} 4B (7)	52	Test point

NOTES
1. All pads with square cross–section =120μm × 120μm
2. All pads with octagonal cross–section =100μm × 100μm
3. Chip is passivated with polyimide

Fig. 25 PS13201 pad map for bare IC dice

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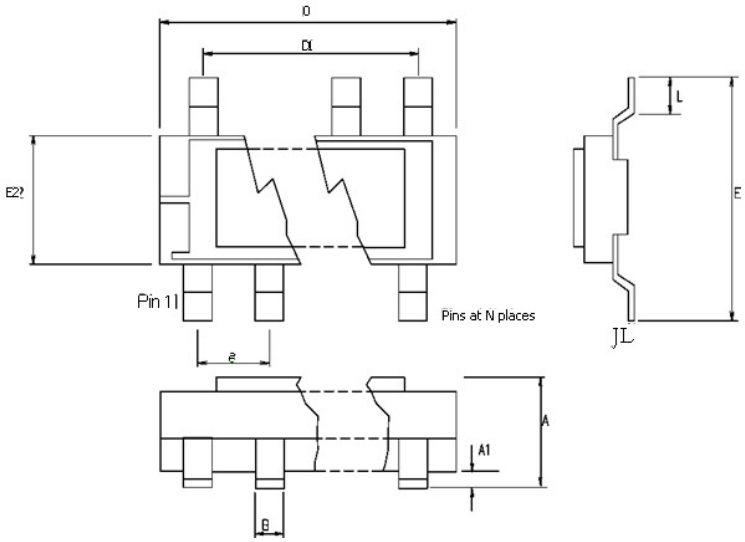
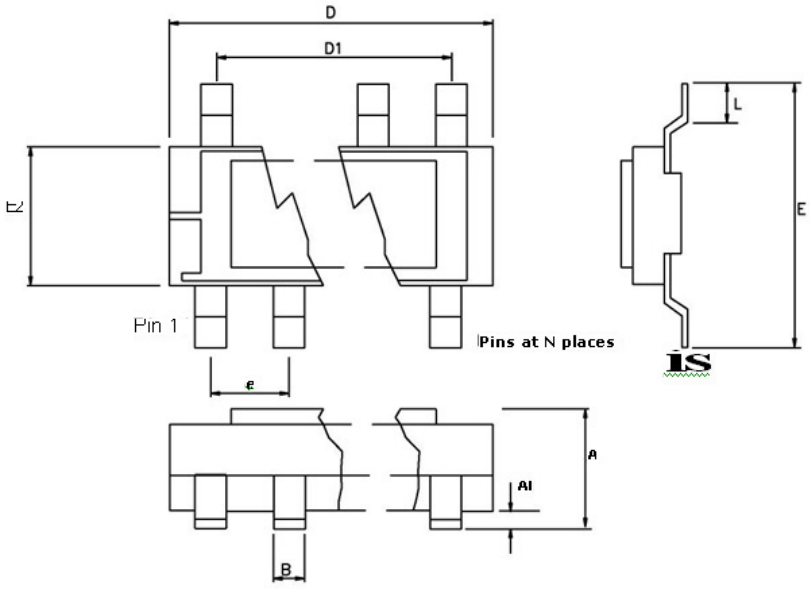


Symbol	Altern. Dimensions in millimetres				Control Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	2.20		2.75		0.087		0.108
A1			0.30				0.012
B	0.37		0.47		0.015		0.019
C	0.17		0.23		0.007		0.009
D	17.70		18.10		0.697		0.713
D1	16.36		16.66		0.644		0.656
E	10.00		10.67		0.394		0.420
E2	7.30		7.60		0.287		0.299
e	1.27 BSC.				0.050 BSC.		
L	0.75		1.08		0.030		0.043
	Pin features						
N	28						
ND	14						
NE	0						
NOTE	RECTANGULAR						

Outline Drawing for 28 Lead S.O. (VAC)



Symbol	Altern. Dimensions in millimetres				Control Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	2.20		2.75		0.087		0.108
A1			0.30				0.012
B	0.37		0.47		0.015		0.019
C	0.17		0.23		0.007		0.009
D	17.70		18.10		0.697		0.713
D1	16.36		16.66		0.644		0.656
E	10.00		10.67		0.394		0.420
E2	7.30		7.60		0.287		0.299
e	1.27 BSC.				0.050 BSC.		
L	0.75		1.08		0.030		0.043
	Pin features						
N	28						
ND	14						
NE	0						
VOTE	RECTANGULAR						

Package Outline for 28 lead SOIC (ceramic) (0.150" Body Width)

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